ASIC/FPGA Design Spring 2025 Assignment 4

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Problem 4

Familiarity with Speed-Related Concepts

In this question, you will become familiar with different speed-related concepts. A module that calculates cube of the input is considered. For each part, after implementation and simulation, calculate **Maximum Frequency**, **Throughput**, and **Latency**. Treat operator delay as a parameter. Compare and analyze synthesis results for each part.

1. Define Maximum Frequency, Throughput, and Latency, and explain their relationship to circuit operating speed.
2. Design a module that computes the cube of an 8 bit input and outputs the result. The structure must be **High Throughput**, meaning all inputs are received and the output is produced in all clocks. Use a `for` loop for implementation.
3. Modify the structure using pipeline to achieve the highest possible operating frequency.
4. Modify the structure to minimize area. Use **resource sharing**.
5. Compare the time/area trade-offs among these parts and discuss the results.

Problem 5

Optimization of FIR Filter for Different Cases

In this question, you will design a **7-tap FIR filter** and optimize it for different implementation scenarios.

1. Draw and implement the structure of an FIR filter with 7 coefficients, using pipelining as much as possible.

2. Draw and implement the structure of an FIR filter with 7 coefficients without pipelining. Assume coefficients are known. The output is produced every clock cycle. Define **Tlast** as the delay of the last multiplication. Discuss its effect. Consider data input as a stream. Show how results are produced and stored in an output stream. Write Verilog code for the module with stream inputs/outputs, and test it with a testbench. Ensure idle cycles output zero.

3. Investigate the case of **symmetric coefficients**. If coefficients are symmetric, modify the filter design to optimize it. Compare it to the non-symmetric case.

4. Discuss the advantages of the symmetric structure compared to the non-symmetric one.

5. Assume coefficients are only 0, 1, or –1. Optimize the structure accordingly.

6. Find the maximum frequency for the structure built in previouse section.

7. Investigate the effect of pipelining on the structure. How does it impact frequency and performance? Verify by simulation.Compare the optimized architectures with and without pipelining.

8. Assume the input arrives every 20 clock cycles. Use **resource sharing** to minimize hardware usage and verify correctness by simulation.

9. Assume the 2 inputs arrives every clock cycle therefore 2 output every clock. Modify the architecture accordingly to maintain correct operation and verify by simulation.