ASIC/FPGA Design Spring 2025 Assignment 1

Professor Shabany

Problem 1

Implementing a simple counter and getting started with Vivado
To complete this section, you need to install the Vivado software (preferably the version matching the lab). For simulation, you can use xSim (Vivado's built-in simulator). Other tools such as Modelsim and QuestaSim are also faster simulators, and it is highly recommended that you get familiar with them as well.

(a) Assume we have a clock signal with a frequency of 50 MHz. We want to design a timer such that it first receives two inputs (minutes and seconds). Then, using this timer, it should count down until the requested time ends. When the countdown finishes, the timer should generate a signal done equal to 1.

(b) Use an active-low reset signal in your design.

(c) Verify the correctness of your code with a simple testbench (checking one case is enough for validation).