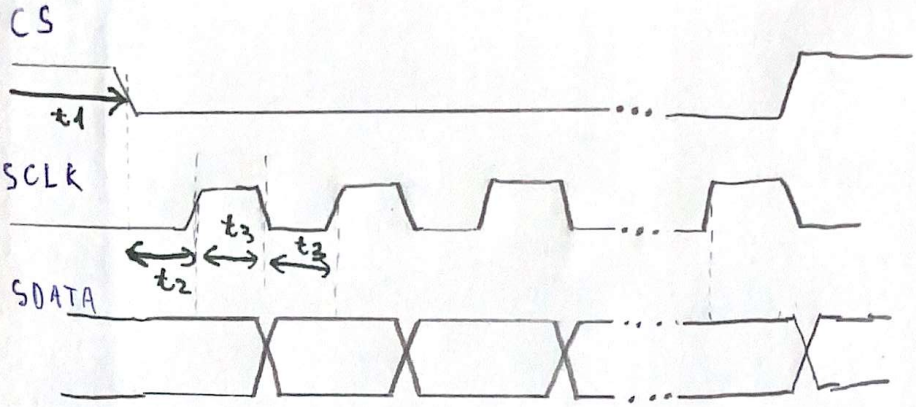


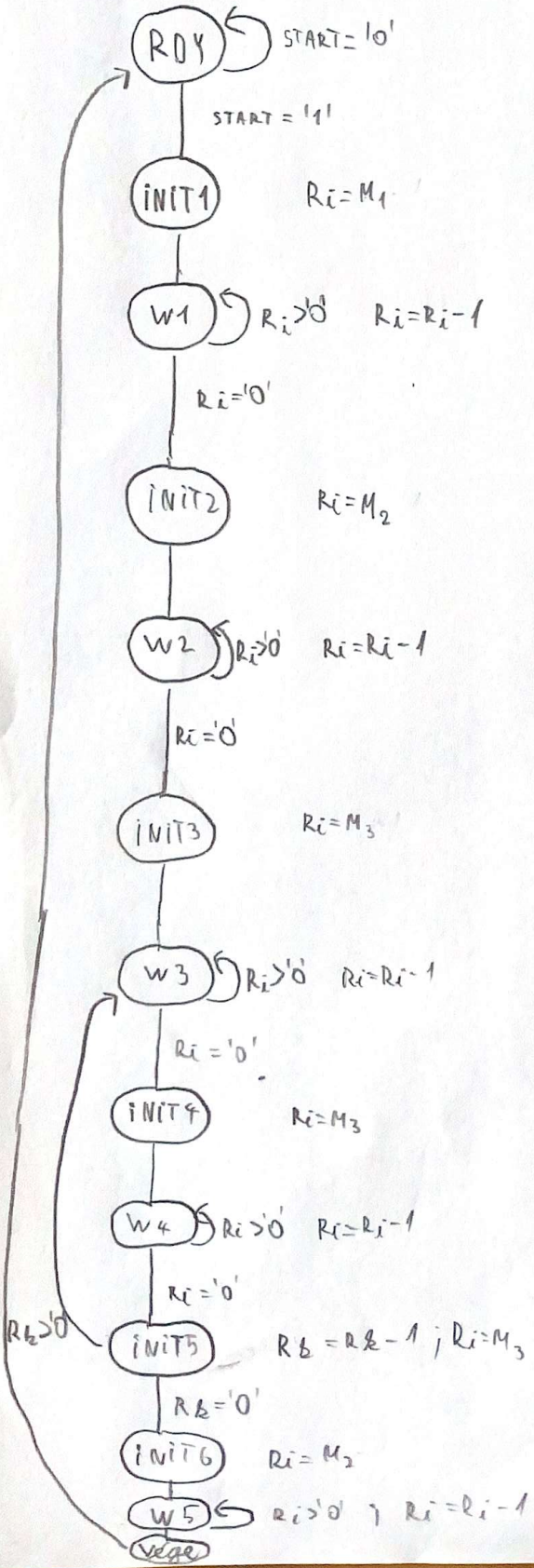
FPGA 100 MHz → 10 ns

ADCS7476 20 MHz → 50 ns

$t_1 = M_1 \cdot 10$ ns

$t_2 = M_2 \cdot 10$ ns → $M_2 = 3$

$t_3 = M_3 \cdot 10$ ns → $M_3 = 3$



	R_i	R_k	R_{CS}	R_{SCLK}	Reg_ki	Reg_ku	R status
RDY	Ri	R_k	1	0	evdet_ku	Reg_ku	0
INIT1	M1	16	1	0	Reg_ki	Reg_ku	0
W1	Ri-1	R_k	1	0	Reg_ki	Reg_ku	0
INIT2	M2	R_k	0	0	Reg_ki	Reg_ku	0
W2	Ri-1	R_k	0	0	Reg_ki	Reg_ku	0
INIT3	M3	R_k	0	0	Reg_ki	Reg_ku	0
W3	Ri-1	R_k	0	1	Reg_ki	Reg_ku	0
INIT4	M3	R_k	0	1	Reg_ki	Reg_ku<<1	0
W4	Ri-1	Rk	0	0	Reg_ki	Reg_ku	0
INIT5	M3	R_k-1	0	0	Reg_ki>>1	Reg_ku	0
INIT6	M2	R_k	0	1	Reg_ki	Reg_ku	0
W5	Ri-1	R_k	0	1	Reg_ki	Reg_ku	0
Vége	Ri	R_k	1	0	Reg_ki	Reg_ku	1