HW/SW Co-Design Lab

Seminar 1

SS 2024

Schedule of the Lab

Introduction:

- Become acquainted with software and tool flows

Lab task:

- Internet: https://www.vodafone-chair.org/teaching+opportunities#courses

Work:

- Autonomous work in groups of 2-3 people
  preferably on your own PC

Delivery:

During WS: until 30th September 2024

- 1. Exported project workspaces including all sources (C, TIE)
- 2. Project report: Word or LaTeX template on website

Hand in via e-mail: viktor.razilov@tu-dresden.de

Evaluation: Grade for 0/0/2 course, ET/IST: Lecture+Lab 7 credits, NES: 4 credits

Do not forget to register for the lab via HISQIS/Selma before examination period starts!

Tasks

1. FIR filter
   - Develop instruction set extensions for Tensilica processor (TIE)
   - Use Fusion, SIMD, FLIX
   - Compare direct form, transposed form
   - ➢ This task need not to take part in the final report.
2. FFT/IFFT
   - Develop instruction set extensions for Tensilica processor (TIE)
   - Use Fusion, SIMD, FLIX, knowledge from task 1
   - Compare DIT, DIF
   - ➢ Main task for the report and valuation.

Seminars

- Today, 23th Apr., 4.DS, POT/13/U:
  - Introduction to Lab
  - First information on Tensilica Instruction Set Extension
  - Demo on Xtensa Xplorer
- Tuesday, 7th May., 4.DS, POT/13/U:
  - Accounts ready to pick-up
  - Discussion/Solution to first task
  - Introduction to second task
- Further questions at any time during semester:
  - Ask questions via e-mail
  - If desired, discussion/consultation some weeks before the end of lab

Submission

Hand in via E-mail until September 30, 2024

Grading:

- Archive with Tensilica workspace including optimized source code
- Project report in English (max. 3 pages w/o source code excerpts)

Assessment criteria:

- 50% practical work, 50% report

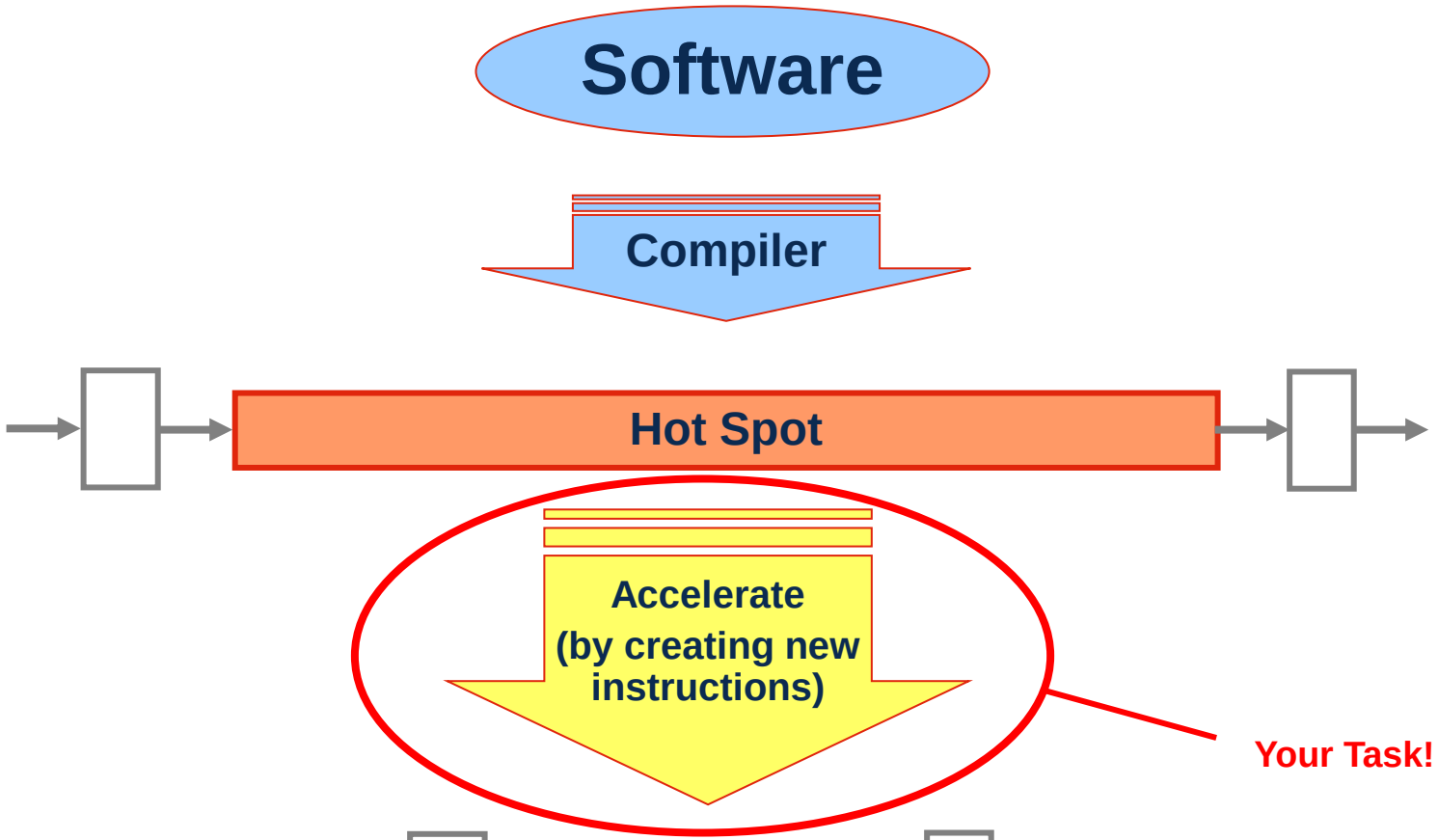
OVERVIEW

Benefits from this Lab

- Practical application of HW/SW Co-Design
- Get familiar with the Tensilica tool flow which is used by many companies today to create customized DSPs
- Grade for 0/0/2 course

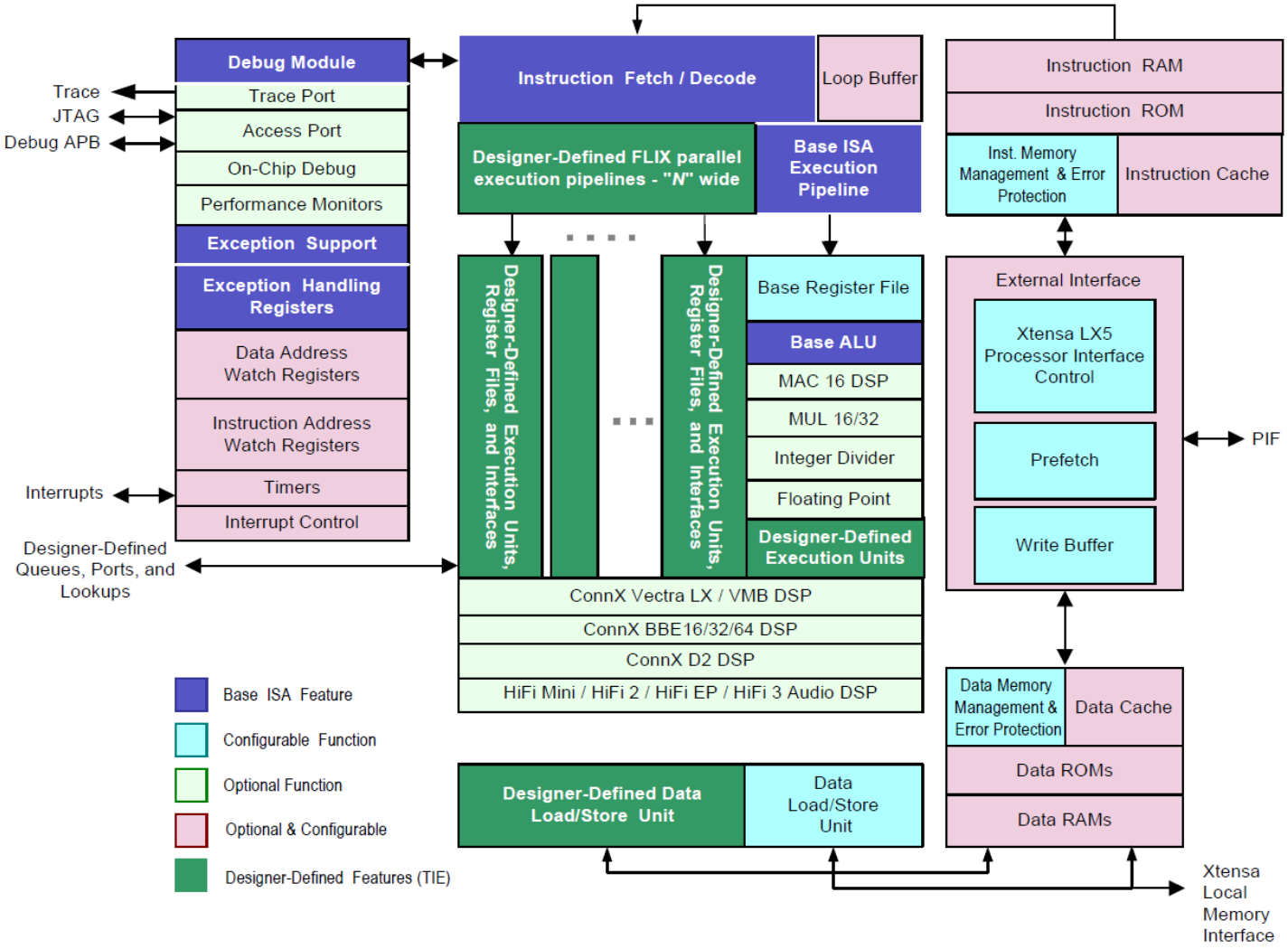
Lab Approach

- RISC

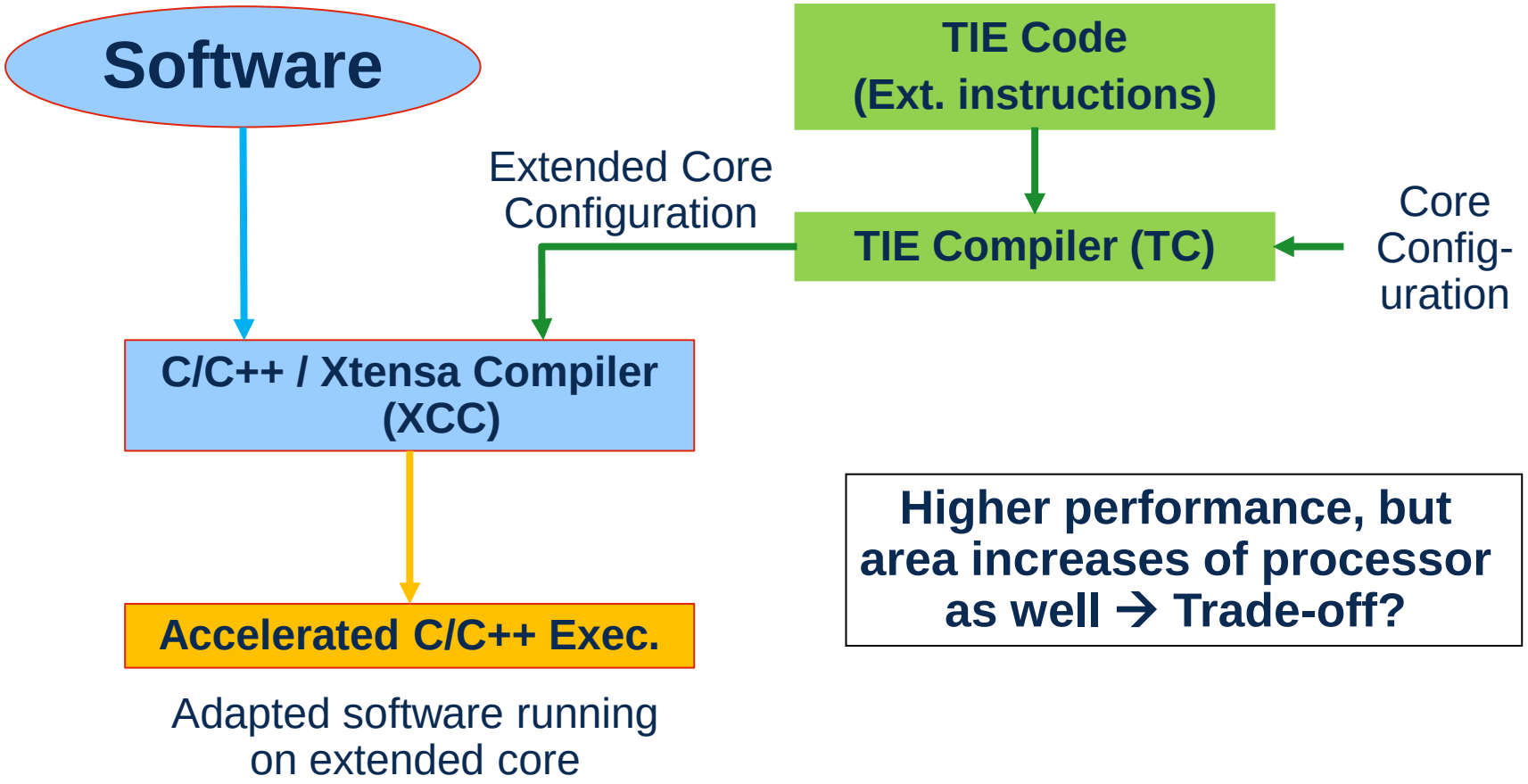


- Enhanced RISC (ASIP)

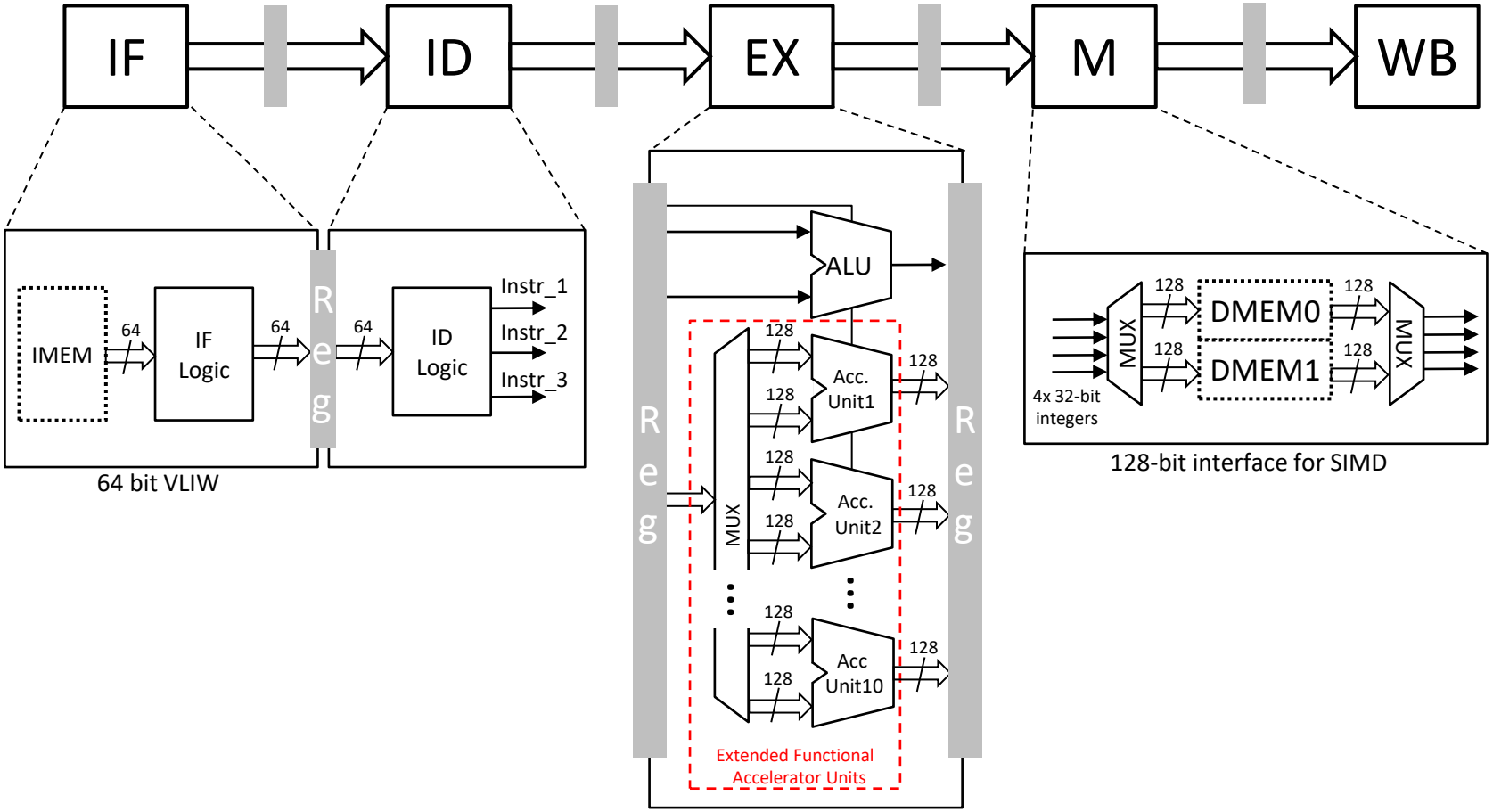
HW architecture: Xtensa LX5



Tensilica Tool Flow



RISC Pipeline



Creating New Instructions

Pure C code:

```
short a, b;
int z1, z2;

z1 = a*b;
z2 = z1 >> 16;
```

TIE code:

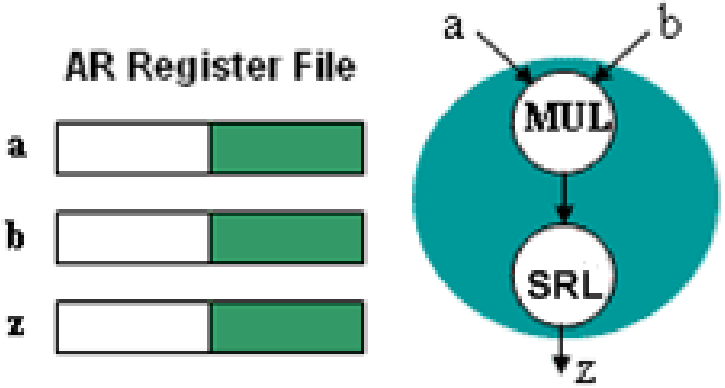
```
operation MUL_SRL_16 {out AR z, in AR a, in AR b} {}
{
        wire [31:0] m = TIEmul(a[15:0],b[15:0],1);
        assign      z = {16'b0, m[31:16]};
}
```

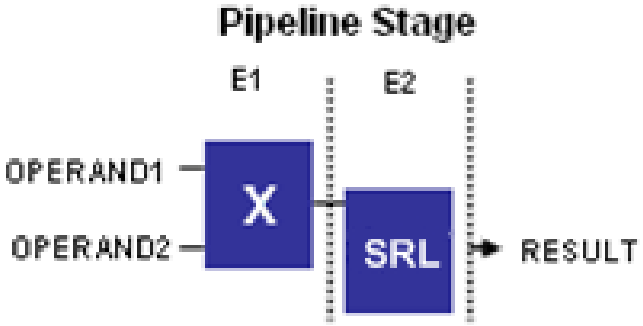
C code with new instructions:

```
#include <xtensa/tie/tie.h>
short a, b;
int z;

z = MUL_SRL_16(a, b);
```

Creating Pipelined Instructions

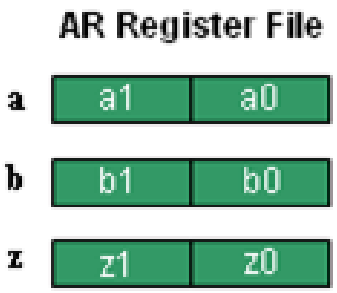

```
operation MUL_SRL_16 {out AR z, in AR a, in AR b} {}
{
        wire [31:0] m = TIEmul(a[15:0],b[15:0],1);
        assign      z = {16'b0, m[31:16]};
}

schedule ms {MUL_SRL_16}
{
        use a 1;
        use b 1;
        def z 2;
}
```

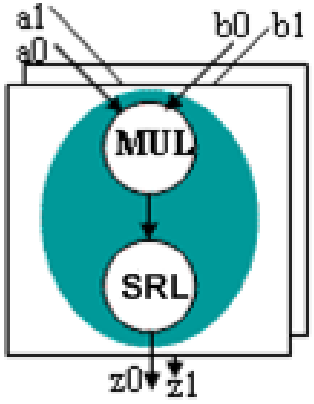




DLP: SIMD Extension


```
operation MUL_SRL_16 {out AR z, in AR a, in AR b} {}
{
        wire [31:0] m1 = TIEmul(a[31:16],b[31:16],1);
        wire [31:0] m0 = TIEmul(a[15:0],  b[15:0],  1);
        assign       z   = {m1[31:16], m0[31:16]};
}
```



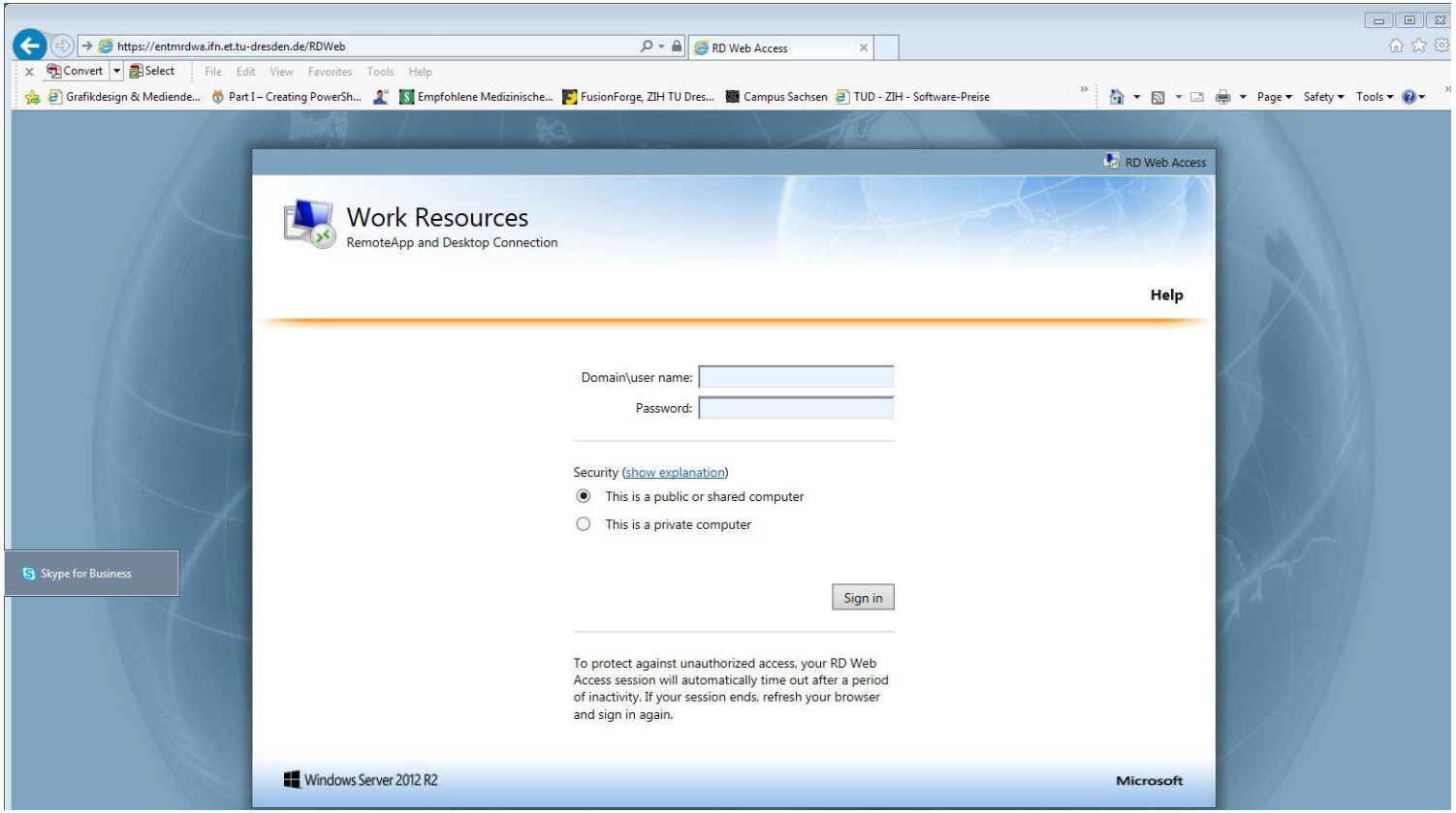


LOGIN PROCEDURE

Login (1)

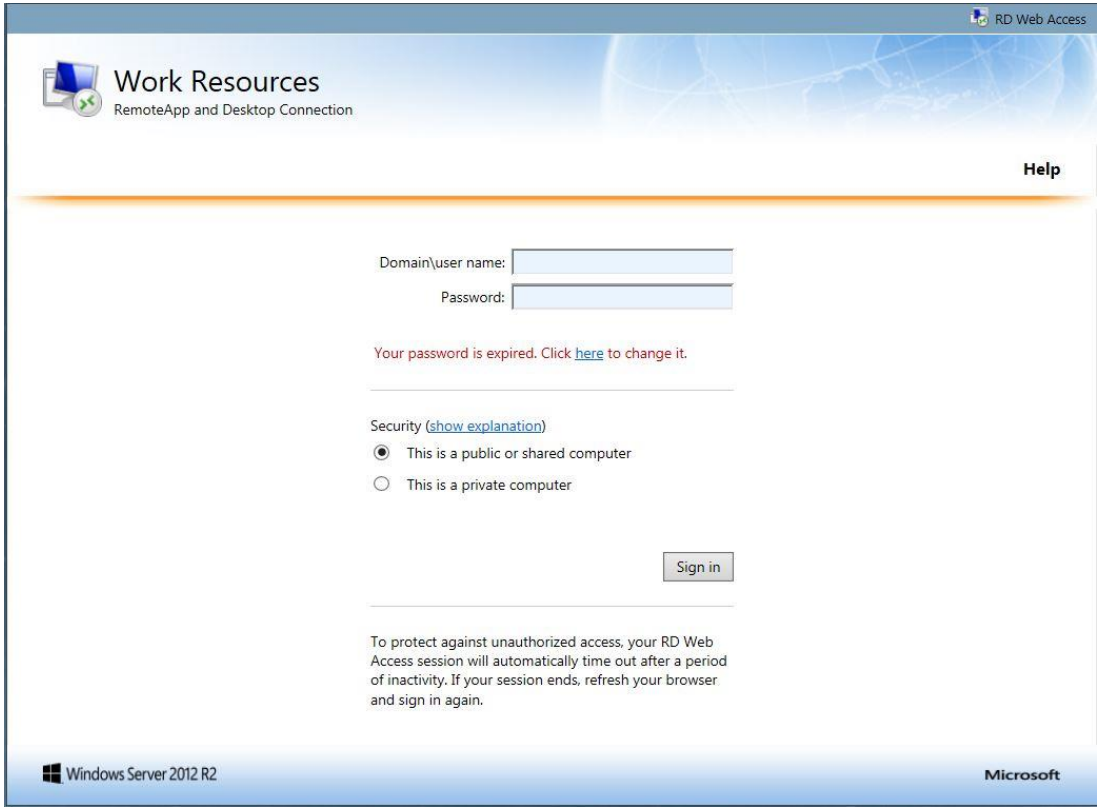
Log in to remote computer with web browser

https://entmrdwa.ifn.et.tu-dresden.de/RDWeb



Login (2)

You will be asked for your credentials. Enter ifn*username* and your password from the account information. After you logged in the first time, you will be requested to change your password (requirements on next slide).



Password requirements

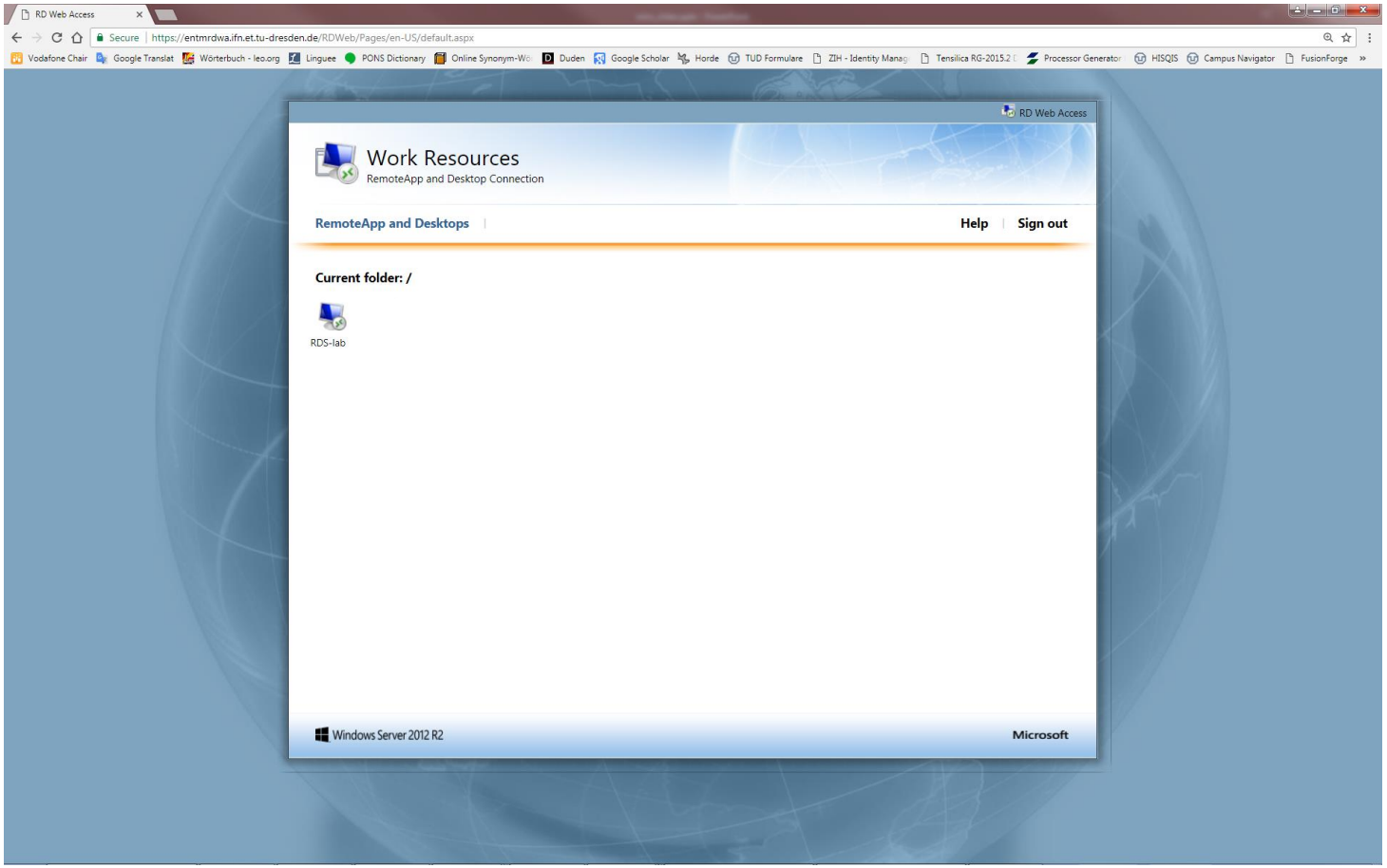
- Must contain at least 20 characters, Must contain at least 1 lowercase letter, Must contain at least 1 uppercase letter, Must contain at least 1 digit.
- Must not repeat any of your previous 11 passwords
- Must differ from your current password by more than the last character

As an alternative, type a password that meets the following requirements:

- Must contain at least 11 characters
- Must contain at least 1 uppercase letter
- Must contain at least 1 lowercase letter
- Must contain at least 1 digit
- Must contain at least 1 special character
- Must not contain your username
- Must not start with a digit
- Must not end with a digit
- Must not contain 3 or more consecutive identical characters
- Must not be from the list of prohibited passwords
- Must not be in the list of breached passwords
- Must not repeat any of your previous 11 passwords
- Must differ from your current password by more than the last character

Login (3)

Once logged in, click on RDS-lab



Login (4)

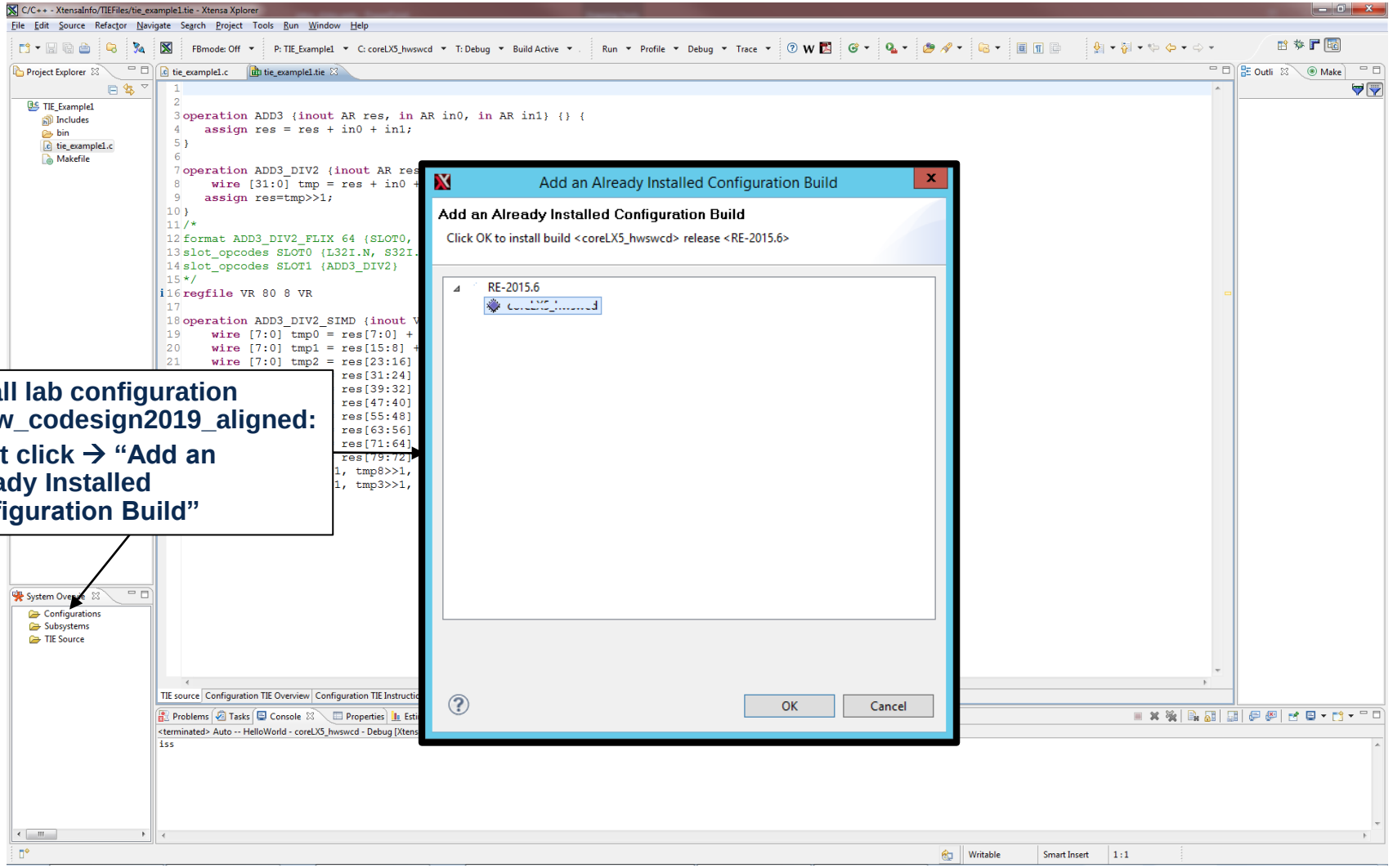
- An *.rdp* file will be downloaded which opens a connection via Remote Desktop Protocol (RDP) to a Windows computer. Your operating system has to provide an RDP client.
- Click the Xplorer icon on the desktop to start Xtensa Xplorer.

Hint:

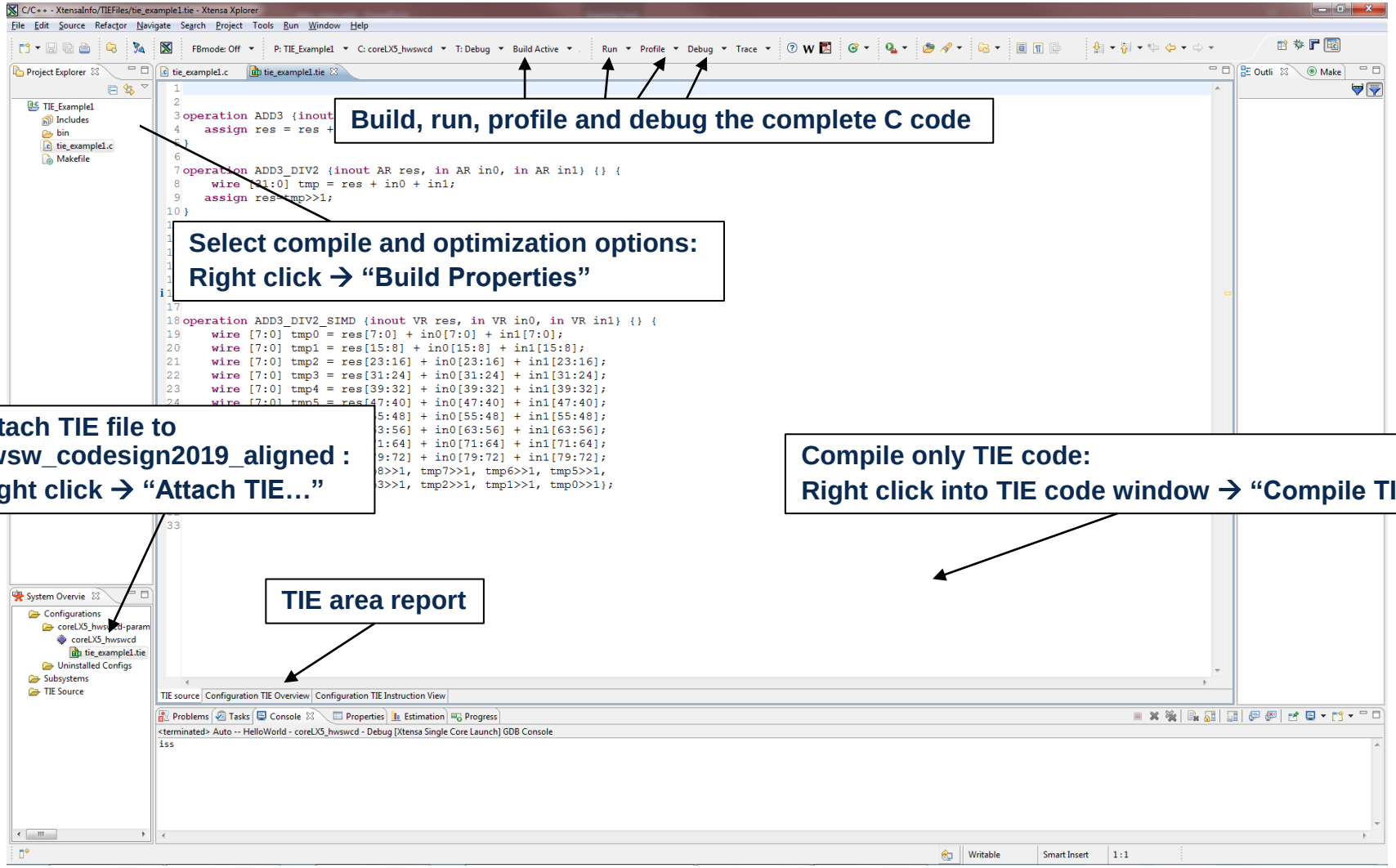
→ Windows automatically provides the RDP client

→ For Linux or Mac users, install an RDP client suitable for your operating system

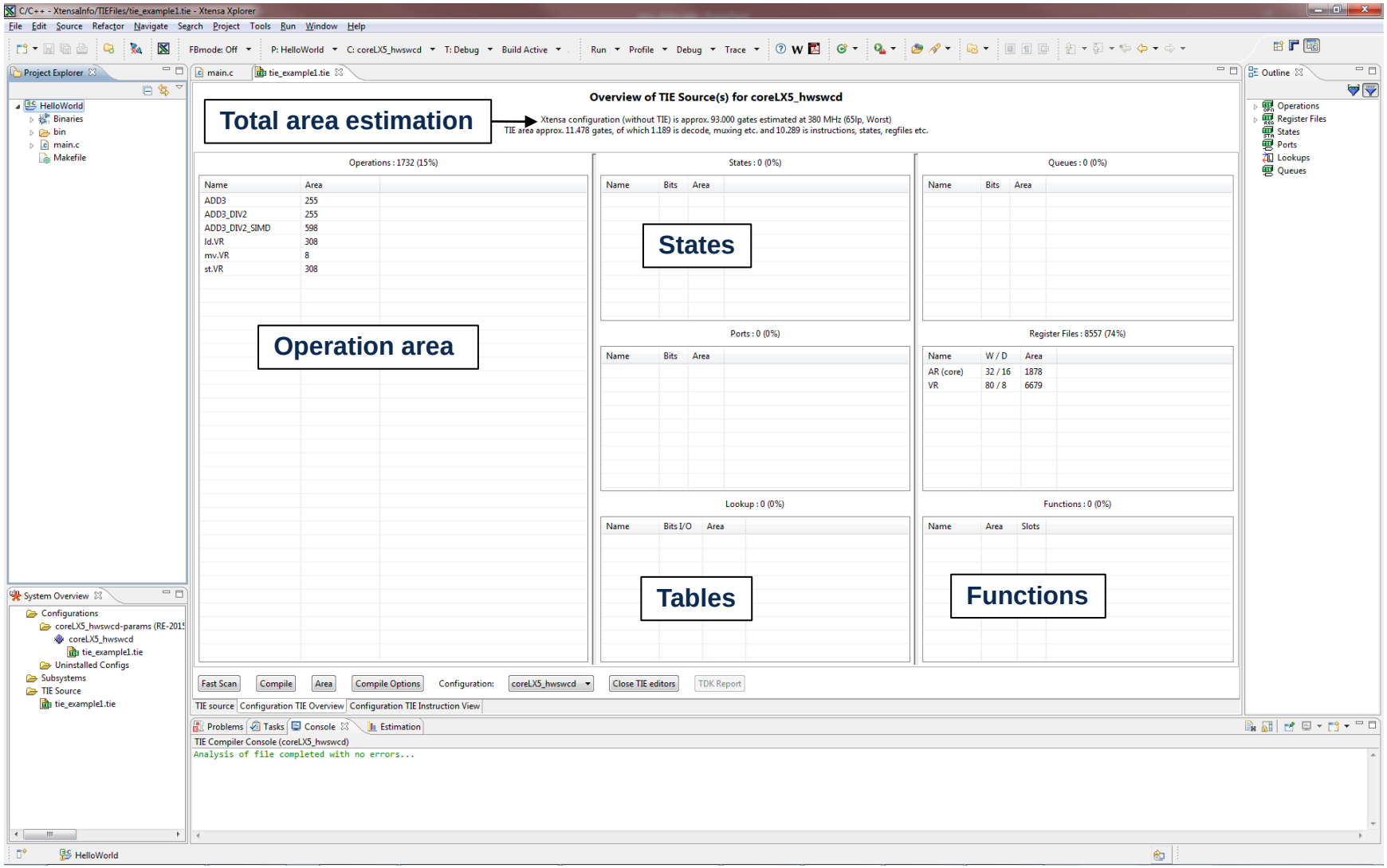
Xtensa Xplorer: Install Configuration



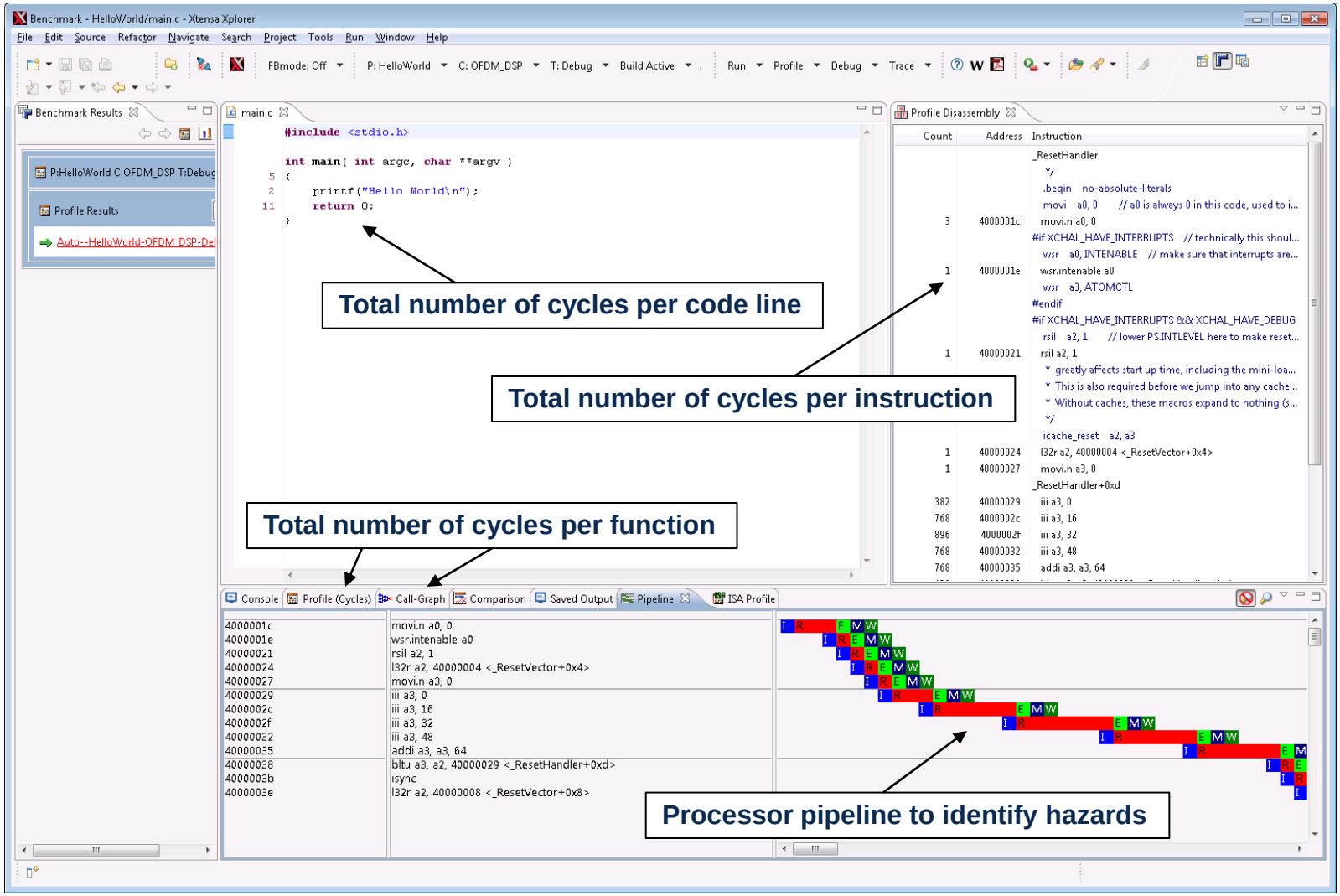
Xtensa Xplorer: C/C++ Perspective



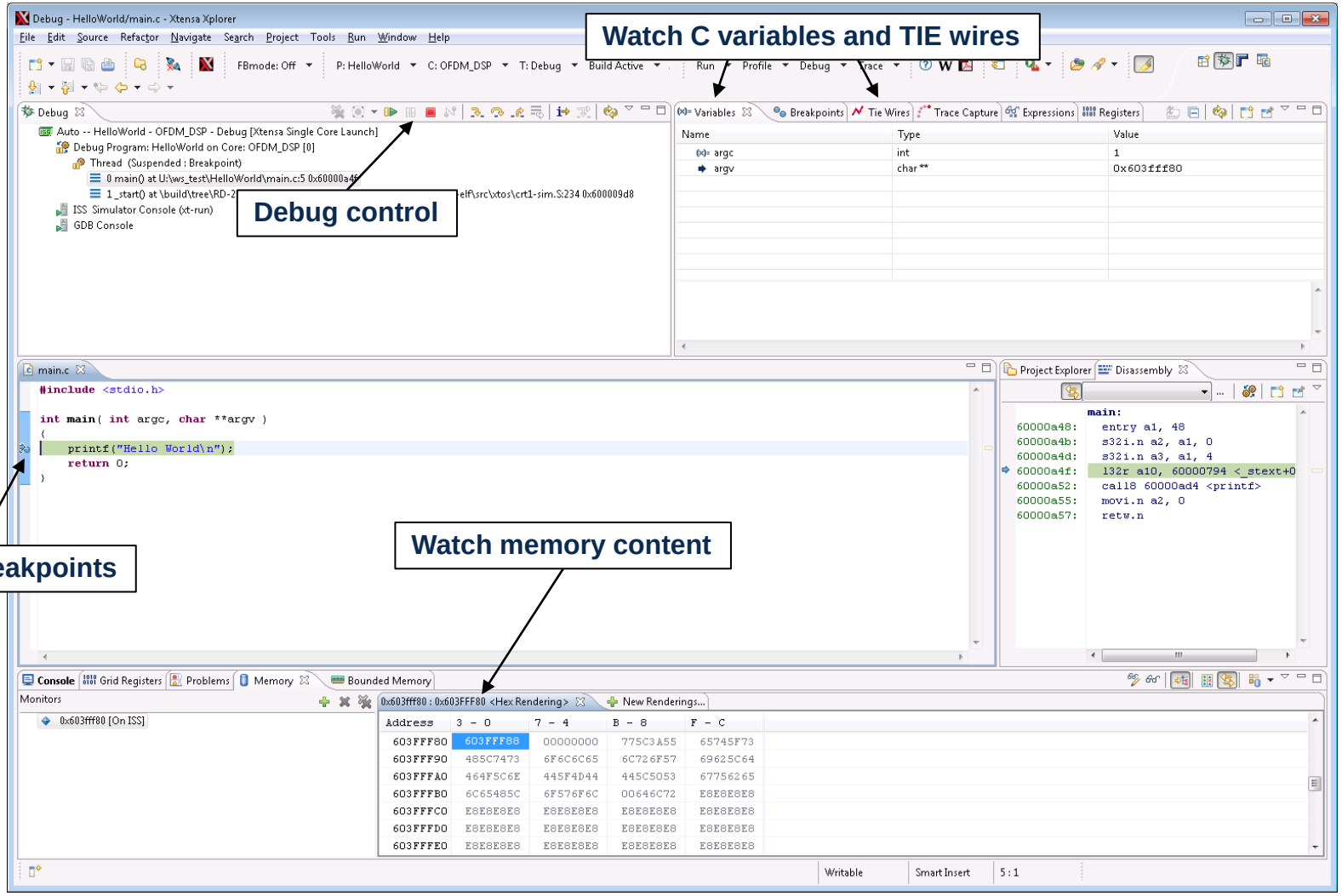
Xtensa Xplorer: TIE area report



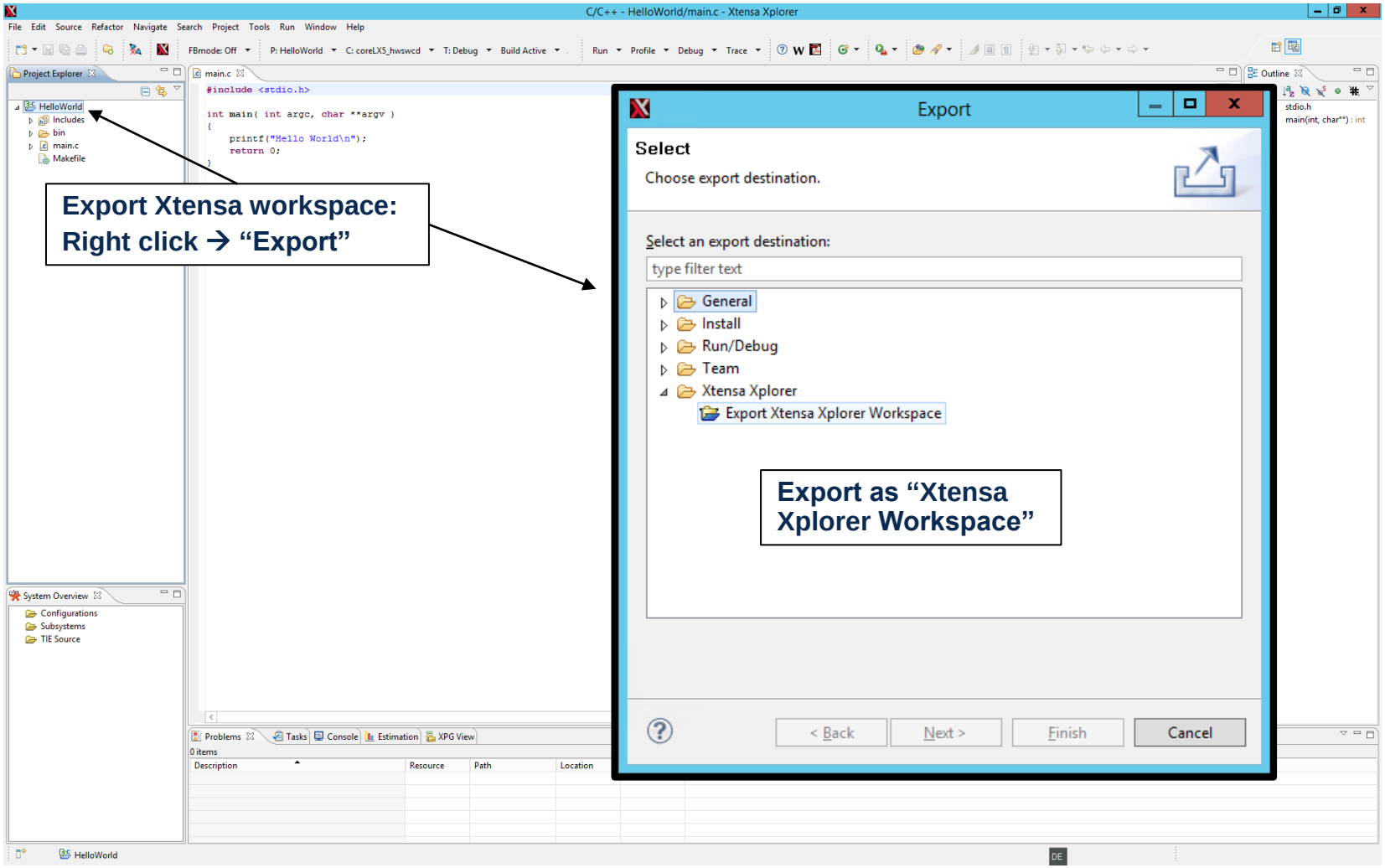
Xtensa Xplorer: Benchmark Perspective



Xtensa Xplorer: Debug Perspective

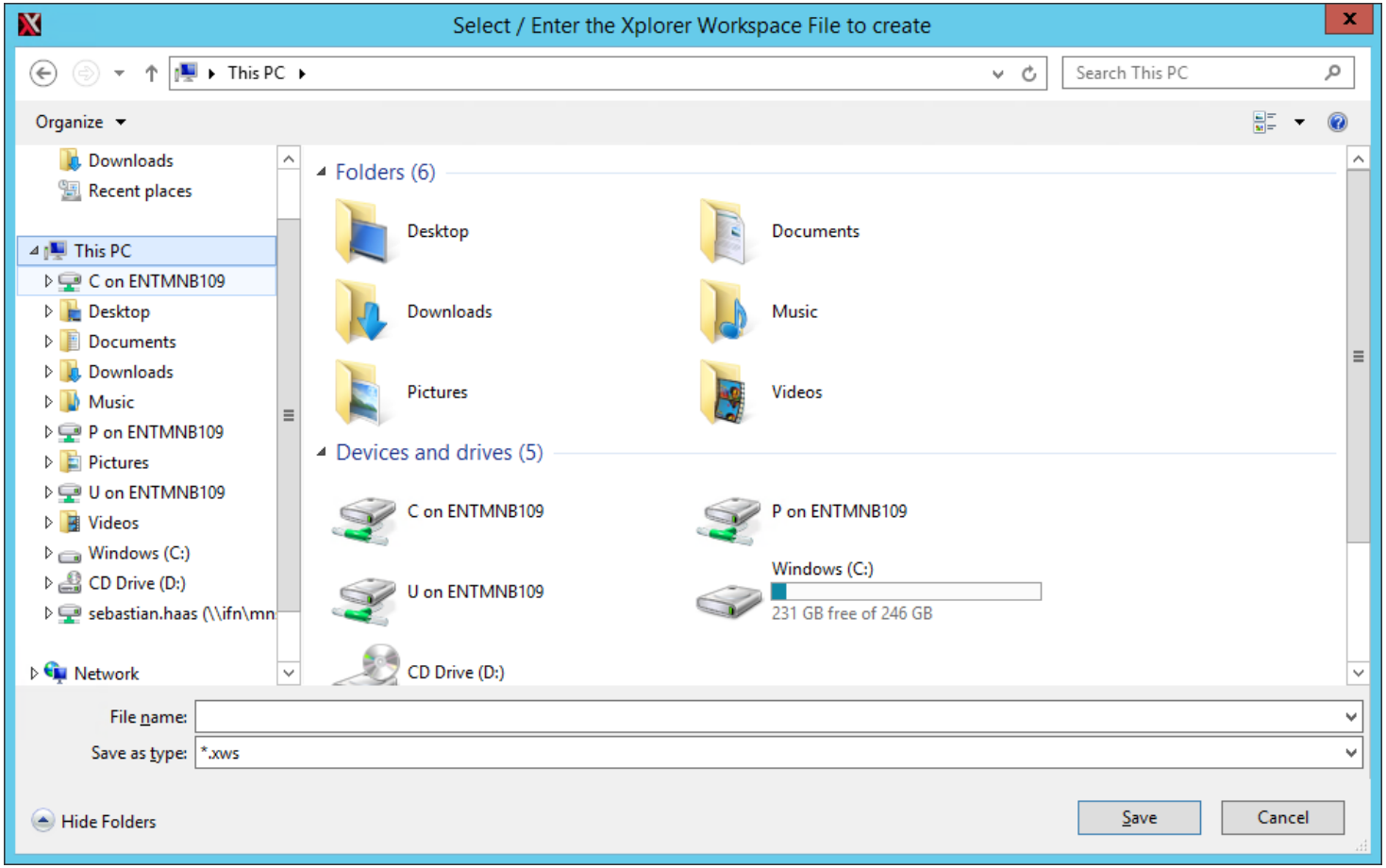


Delivery: Export Xtensa Workspace (1)



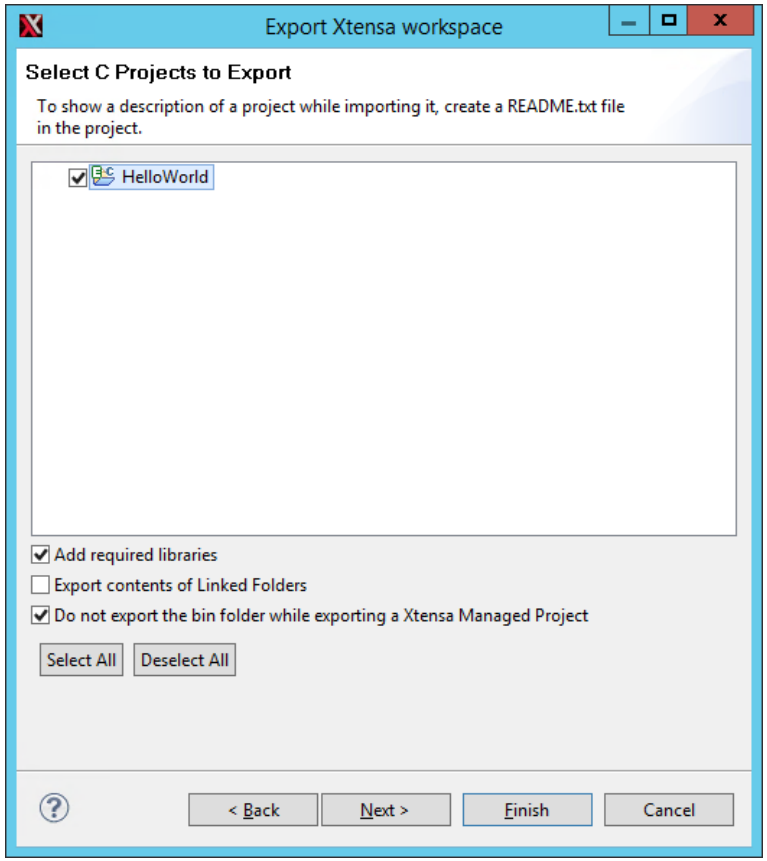
Delivery: Export Xtensa Workspace (2)

Browse and save the *.xws file to your local hard drive. Usually "C on *your_PC_name*"



Delivery: Export Xtensa Workspace (3)

Select your desired project

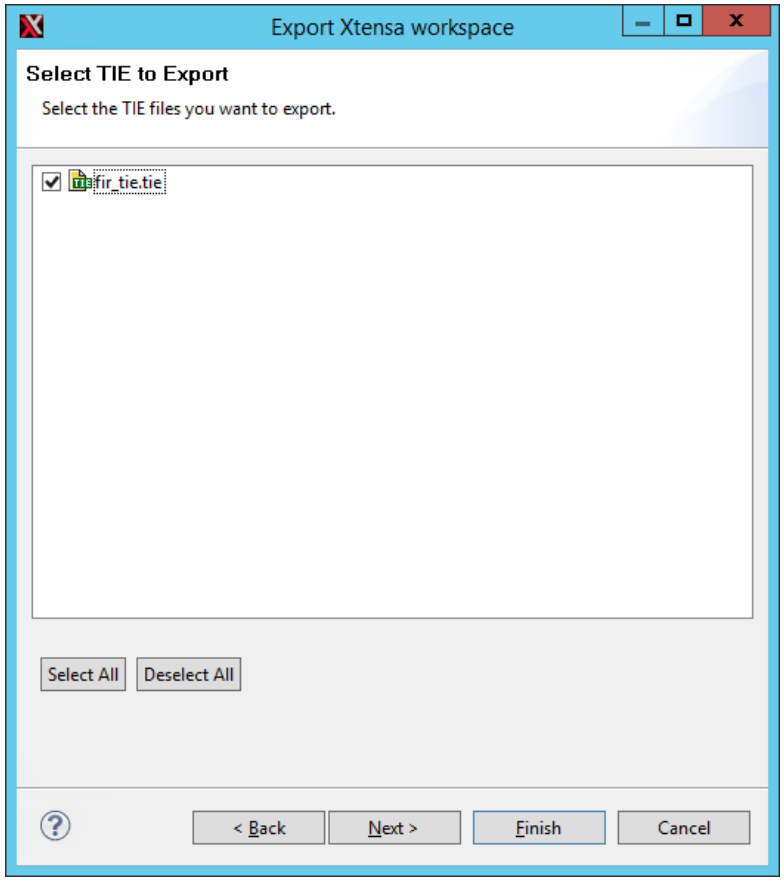


Delivery: Export Xtensa Workspace (4)

Do not export any

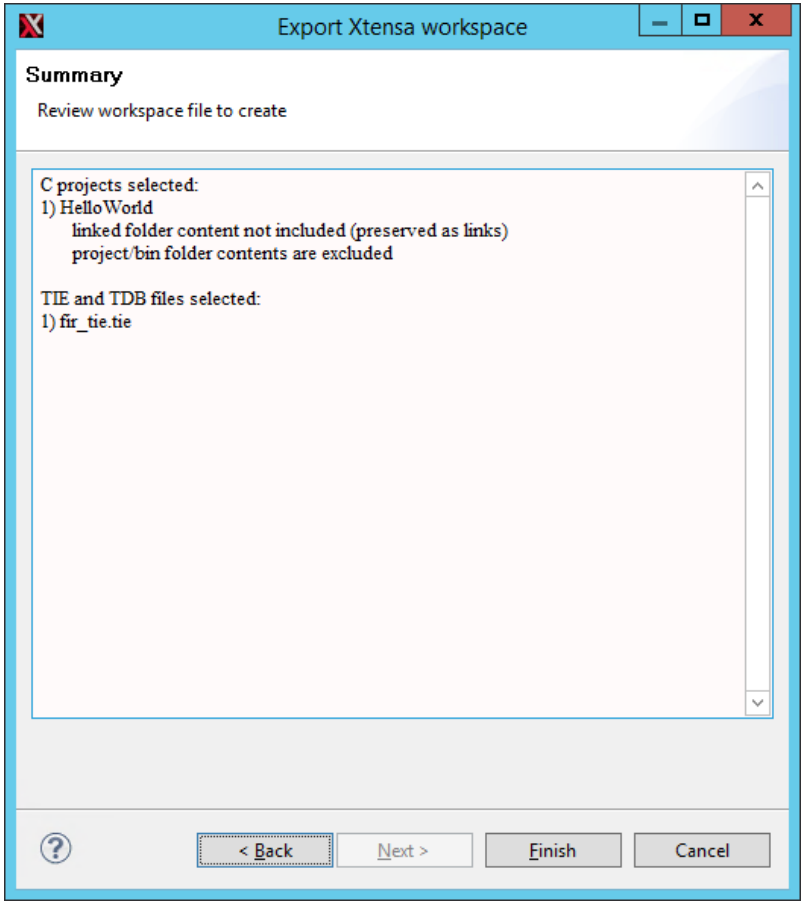
- **Launches**
- **Configurations**
- **Tools**
- **Builds**
- **User-defined formats**

but do export your TIE file(s)



Delivery: Export Xtensa Workspace (5)

Summary → Click on "Finish"



Important Usage Information

- Only a limited number of licenses available
- Please log off via the start menu when not working
  - Do not just close the RDP window
- You may be forcefully logged off when VM is idle for too long (~ 24 hours)
  - All unsaved work will be lost

- Store your data on U:
  - Data might get lost otherwise

TASK 1: FIR FILTER

Task 1: FIR Filter

- FIR filter: $y_n = \sum_{i=0}^{N-1} b_i x_{n-i}$

```
void fir_C(short *in, int *out, int len) {
   int n, i;
   for (n = 0; n < len+7; n++) {
      for (i = 0; i < 8; i++)
         out[n] += in[n+7-i]*coeff[i];
   }
}
```

- Hot-Spots
  - Multiply/Accumulate Operation (MAC)
  - Load input values/coefficients
  - Store output values

- Different approaches:
  1) Performing MAC on one input element with one coefficient
  2) Performing MAC on multiple elements in parallel ➔ SIMD
  3) Separated instructions for Load, MAC and Store

SUMMARY

Your next TODOs:

- Indicate via email the members of your group (1 mail per group) → deadline 30.04.
- Review Task 1: FIR filter
- Wait for your account
  - Account information will be sent via email
- Attend next introduction session on May 7

Contact & Rooms

TECHNISCHE UNIVERSITÄT DRESDEN

vodafone chair

Contact for Questions:

Viktor Razilov
viktor.razilov@tu-dresden.de

Website:

https://www.vodafone-chair.org/teaching+opportunities#courses

Questions?