



HW/SW Co-Design Lab

Seminar 1

SS 2024

Introduction:



Become acquainted with software and tool flows

Lab task:



Internet: <https://www.vodafone-chair.org/teaching+opportunities#courses>

Work:



Autonomous work in groups of 2-3 people
preferably on your own PC

Delivery:



During WS: **until 30th September 2024**

1. Exported project workspaces including all sources (C, TIE)
2. Project report: Word or LaTeX template on website

Hand in via e-mail: viktor.razilov@tu-dresden.de

Evaluation: Grade for 0/0/2 course, ET/IST: Lecture+Lab 7 credits, NES: 4 credits

**Do not forget to register for the lab via
HISQIS/Selma before examination period starts!**

1. FIR filter

- ❑ Develop instruction set extensions for Tensilica processor (TIE)
- ❑ Use Fusion, SIMD, FLIX
- ❑ Compare direct form, transposed form
- This task need not to take part in the final report.

2. FFT/IFFT

- ❑ Develop instruction set extensions for Tensilica processor (TIE)
- ❑ Use Fusion, SIMD, FLIX, knowledge from task 1
- ❑ Compare DIT, DIF
- Main task for the report and valuation.

- Today, 23th Apr., 4.DS, POT/13/U:
 - ❑ Introduction to Lab
 - ❑ First information on Tensilica Instruction Set Extension
 - ❑ Demo on Xtensa Xplorer

- Tuesday, 7th May., 4.DS, POT/13/U:
 - ❑ Accounts ready to pick-up
 - ❑ Discussion/Solution to first task
 - ❑ Introduction to second task

- Further questions at any time during semester:
 - ❑ Ask questions via e-mail
 - ❑ If desired, discussion/consultation some weeks before the end of lab

Hand in via E-mail until September 30, 2024

Grading:

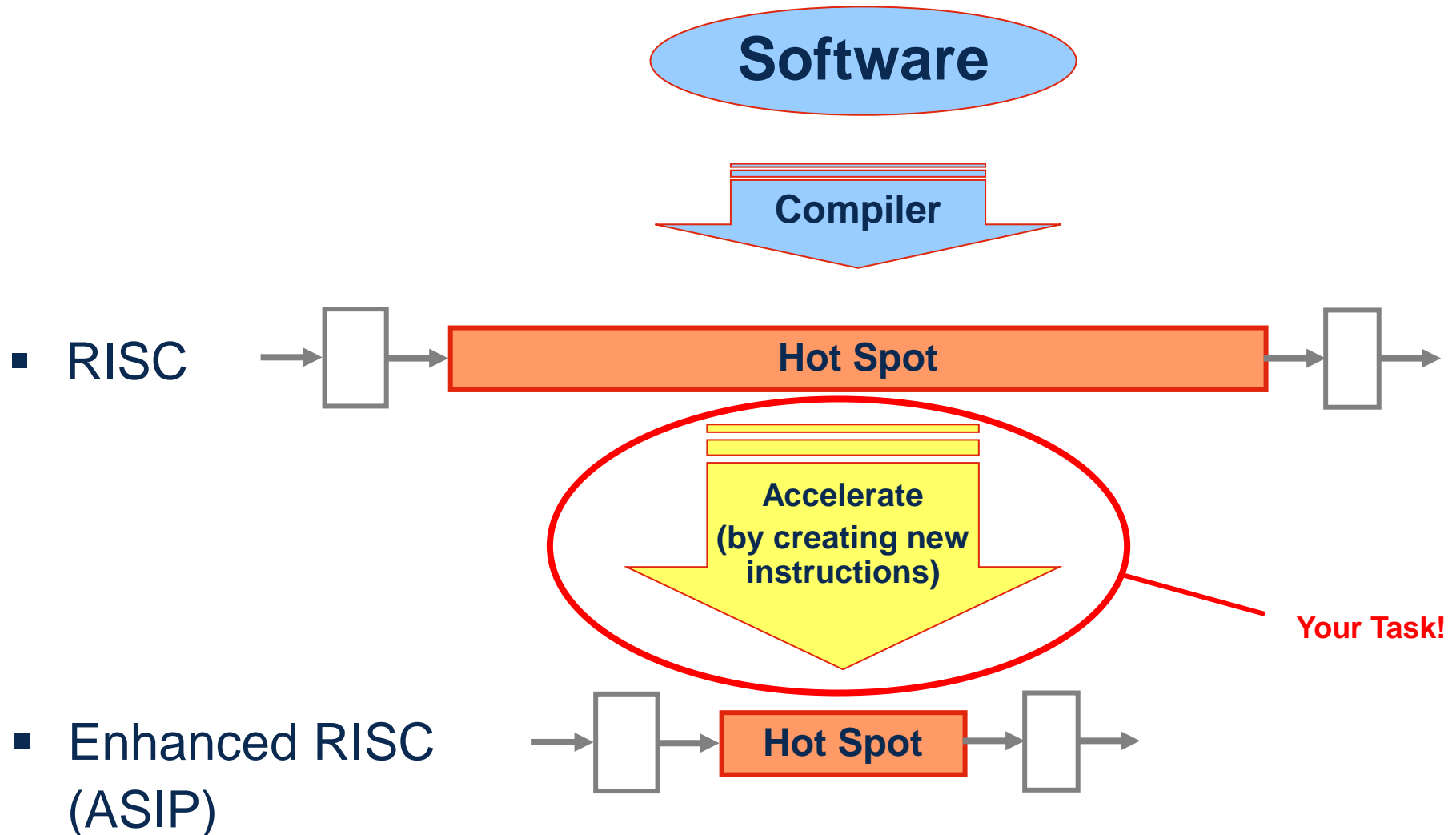
- Archive with Tensilica workspace including optimized source code
- Project report in English (max. 3 pages w/o source code excerpts)

Assessment criteria:

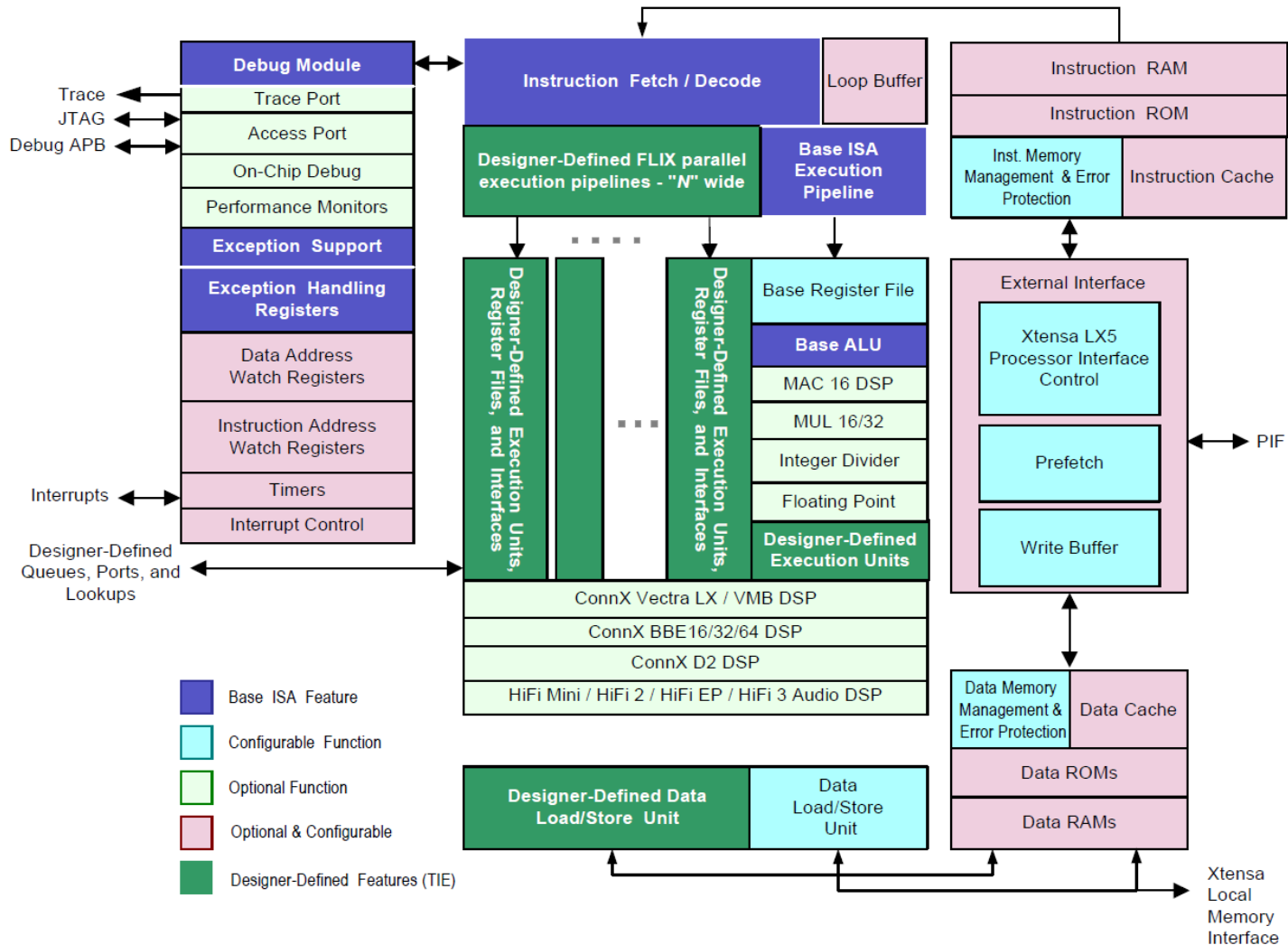
- 50% practical work, 50% report

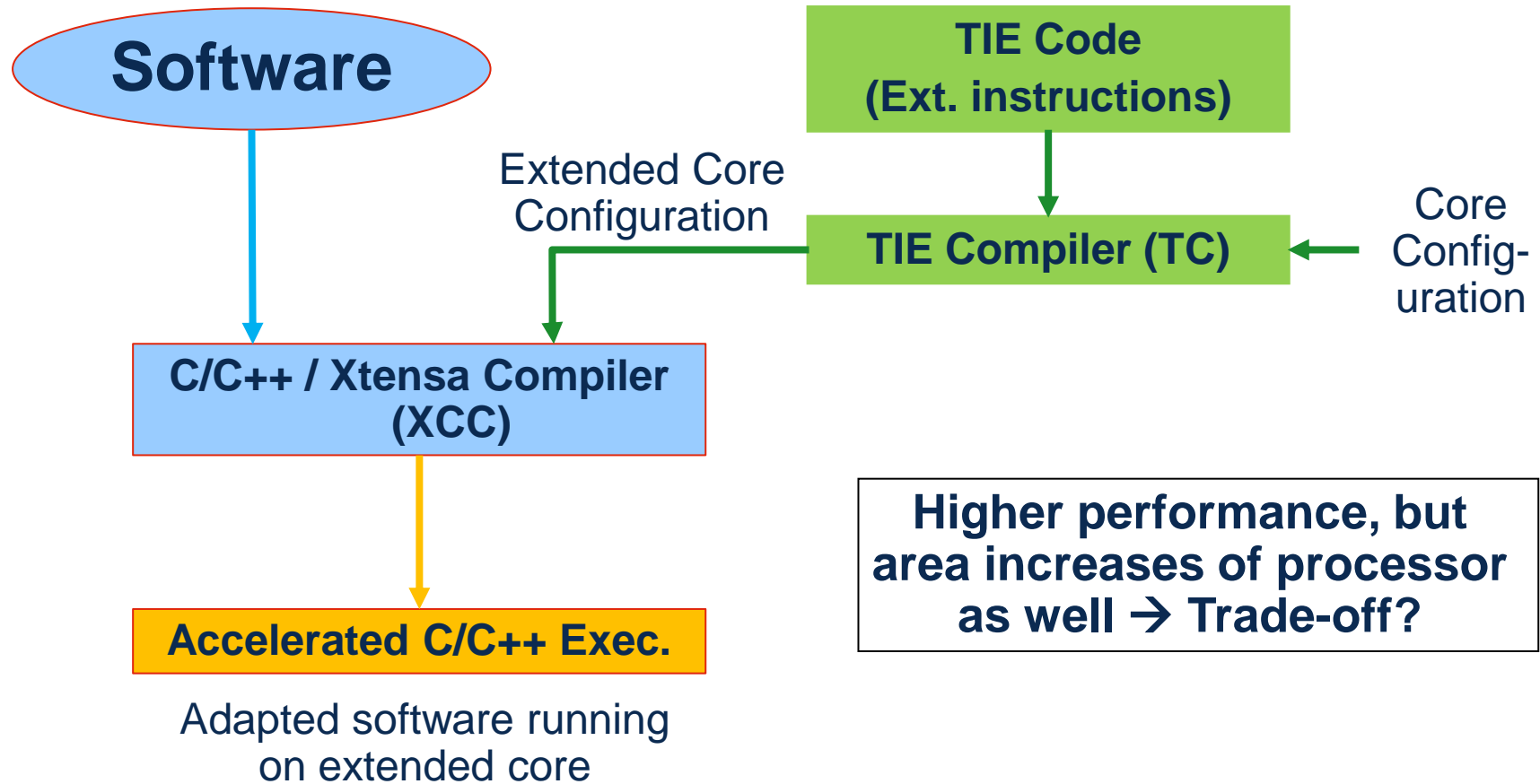
OVERVIEW

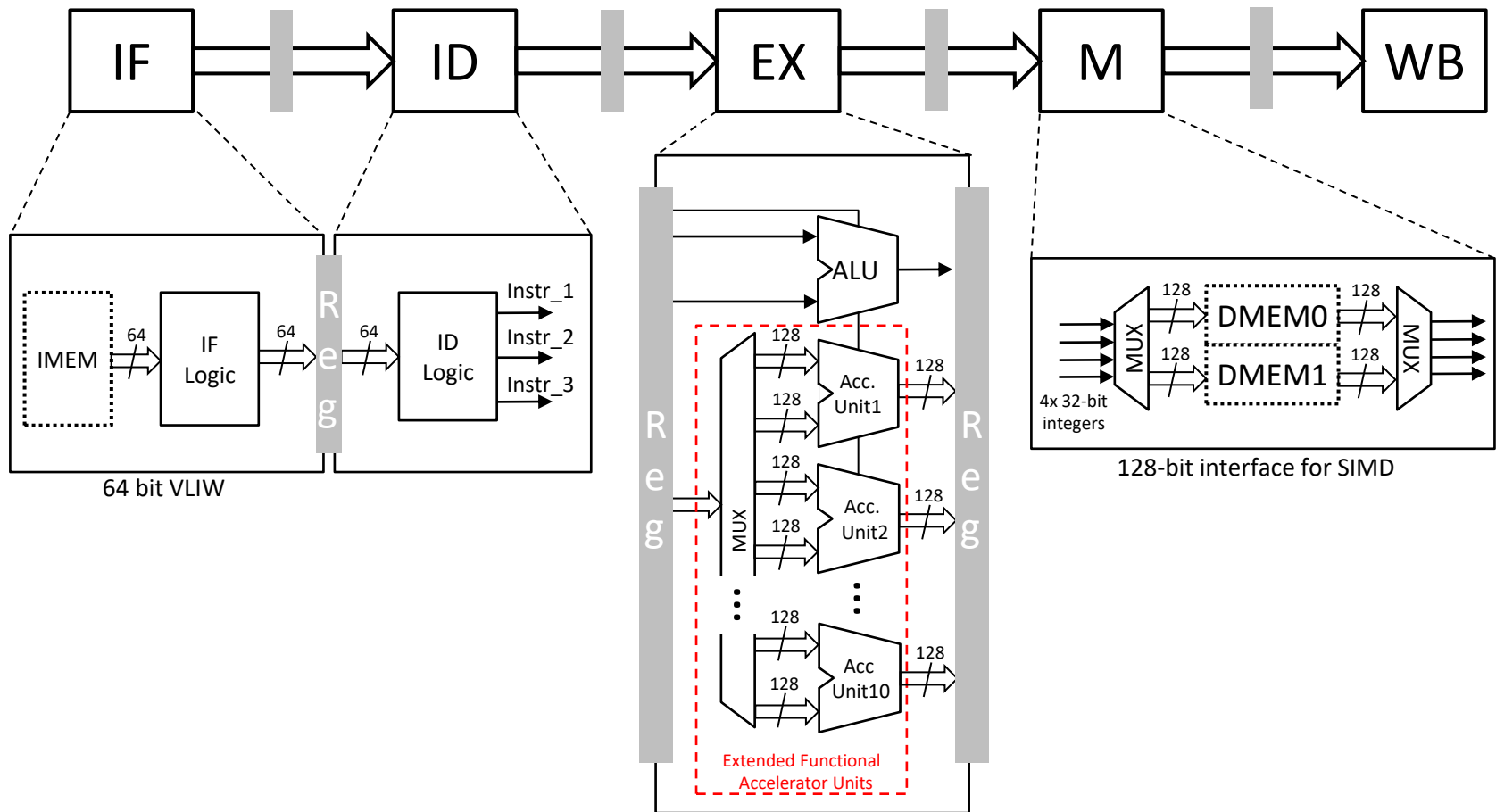
- Practical application of HW/SW Co-Design
- Get familiar with the Tensilica tool flow which is used by many companies today to create customized DSPs
- Grade for 0/0/2 course



HW architecture: Xtensa LX5







Pure C code:



```
short a, b;  
int z1, z2;  
  
z1 = a*b;  
z2 = z1 >> 16;
```

TIE code:



```
operation MUL_SRL_16 {out AR z, in AR a, in AR b} {}  
{  
    wire [31:0] m = TIEmul(a[15:0],b[15:0],1);  
    assign      z = {16'b0, m[31:16]};  
}
```

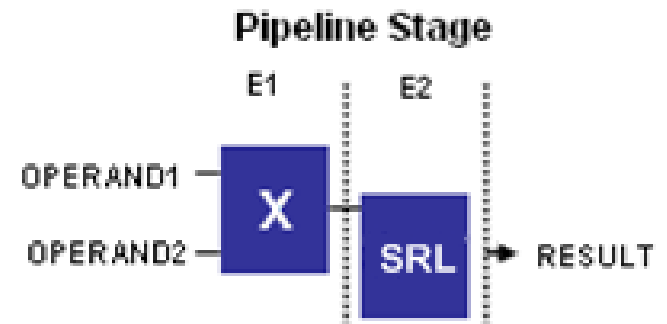
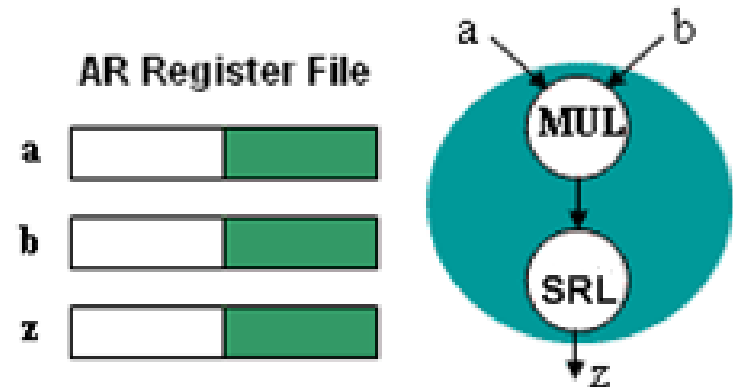
C code with new instructions:

```
#include <xtensa/tie/tie.h>  
short a, b;  
int z;  
  
z = MUL_SRL_16(a, b);
```

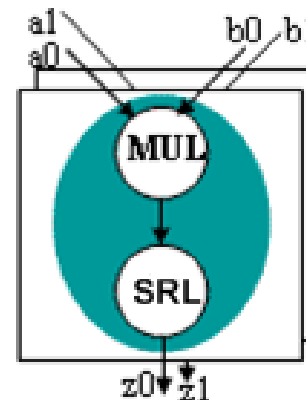
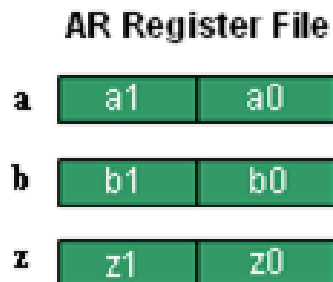
Creating Pipelined Instructions

```
operation MUL_SRL_16 {out AR z, in AR a, in AR b} {}  
{  
    wire [31:0] m = TIEmul(a[15:0],b[15:0],1);  
    assign      z = {16'b0, m[31:16]};  
}
```

```
schedule ms {MUL_SRL_16}  
{  
    use a 1;  
    use b 1;  
    def z 2;  
}
```



```
operation MUL_SRL_16 {out AR z, in AR a, in AR b} {}  
{  
  wire [31:0] m1 = TIEmul(a[31:16],b[31:16],1);  
  wire [31:0] m0 = TIEmul(a[15:0], b[15:0], 1);  
  assign      z  = {m1[31:16], m0[31:16]};  
}
```

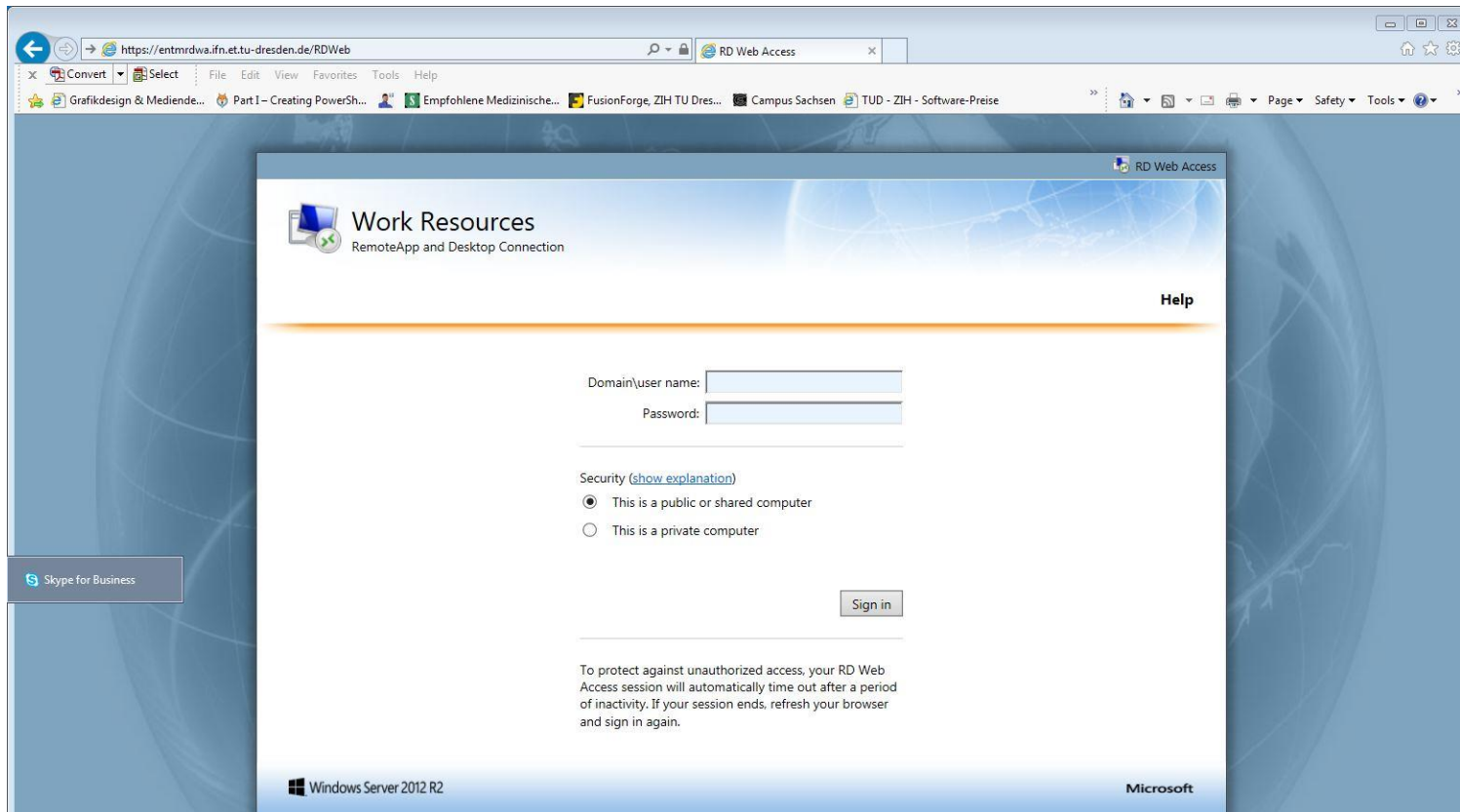


LOGIN PROCEDURE

Login (1)

Log in to remote computer with web browser

<https://entmrdwa.ifn.et.tu-dresden.de/RDWeb>



Work Resources
RemoteApp and Desktop Connection

Help

Domain\user name:

Password:

Security ([show explanation](#))

☒ This is a public or shared computer

☐ This is a private computer

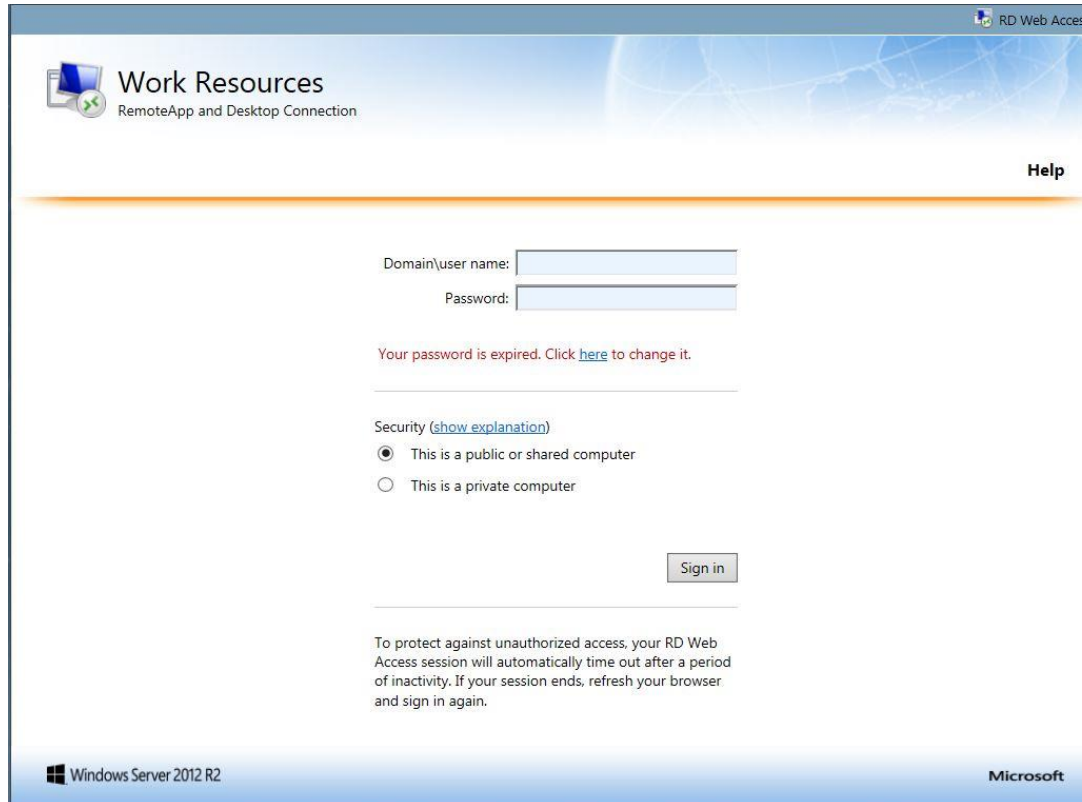
To protect against unauthorized access, your RD Web Access session will automatically time out after a period of inactivity. If your session ends, refresh your browser and sign in again.

Windows Server 2012 R2

Microsoft

Login (2)

You will be asked for your credentials. Enter `ifn\username` and your password from the account information. After you logged in the first time, you will be requested to change your password (requirements on next slide).



RD Web Access

Work Resources
RemoteApp and Desktop Connection

[Help](#)

Domain\user name:

Password:

Your password is expired. Click [here](#) to change it.

Security ([show explanation](#))

☒ This is a public or shared computer

☐ This is a private computer

To protect against unauthorized access, your RD Web Access session will automatically time out after a period of inactivity. If your session ends, refresh your browser and sign in again.

Windows Server 2012 R2

Microsoft

Password requirements

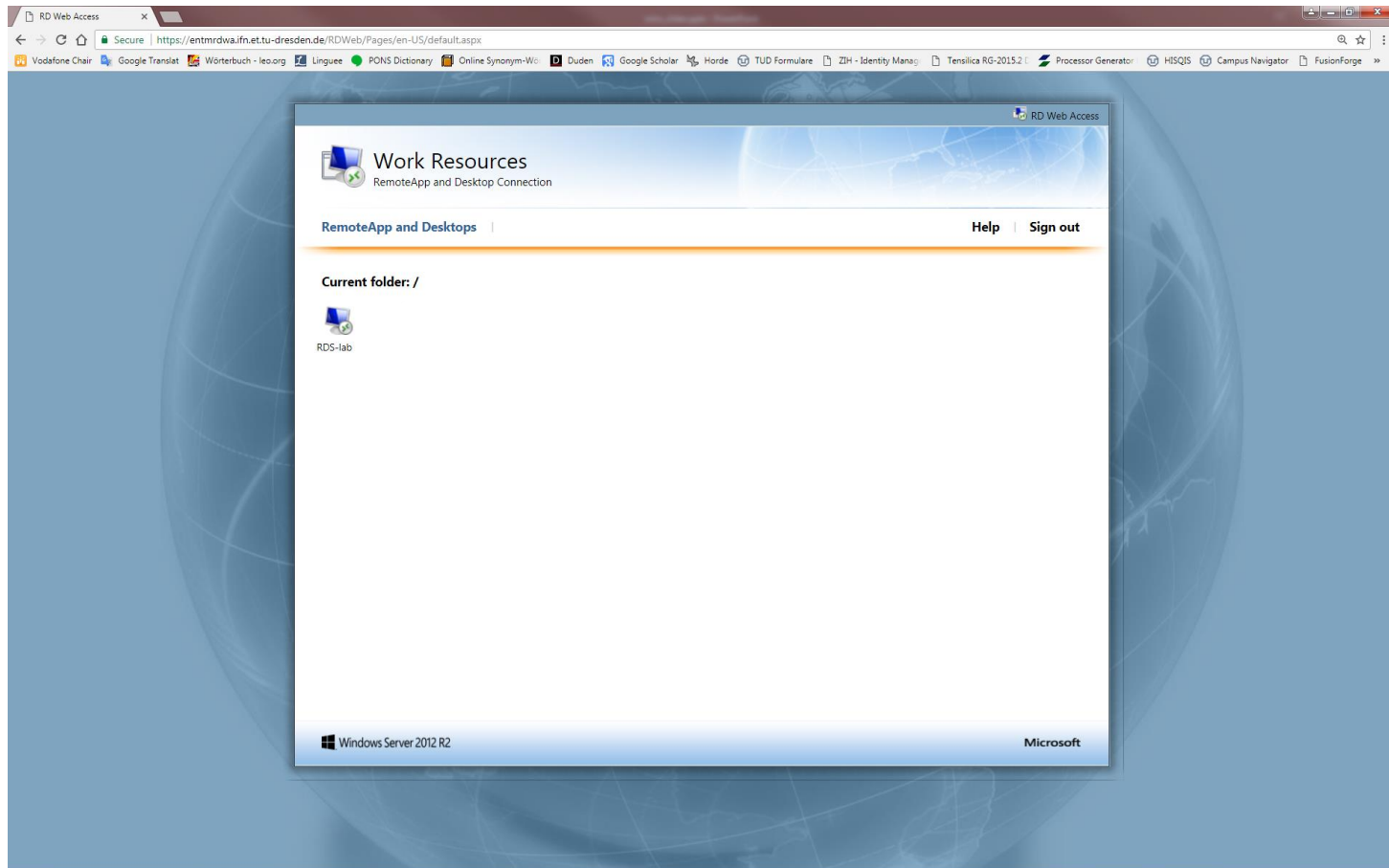
- Must contain at least 20 characters, Must contain at least 1 lowercase letter, Must contain at least 1 uppercase letter, Must contain at least 1 digit.
- Must not repeat any of your previous 11 passwords
- Must differ from your current password by more than the last character

As an alternative, type a password that meets the following requirements:

- Must contain at least 11 characters
- Must contain at least 1 uppercase letter
- Must contain at least 1 lowercase letter
- Must contain at least 1 digit
- Must contain at least 1 special character
- Must not contain your username
- Must not start with a digit
- Must not end with a digit
- Must not contain 3 or more consecutive identical characters
- Must not be from the list of prohibited passwords
- Must not be in the list of breached passwords
- Must not repeat any of your previous 11 passwords
- Must differ from your current password by more than the last character

Login (3)

Once logged in, click on RDS-lab



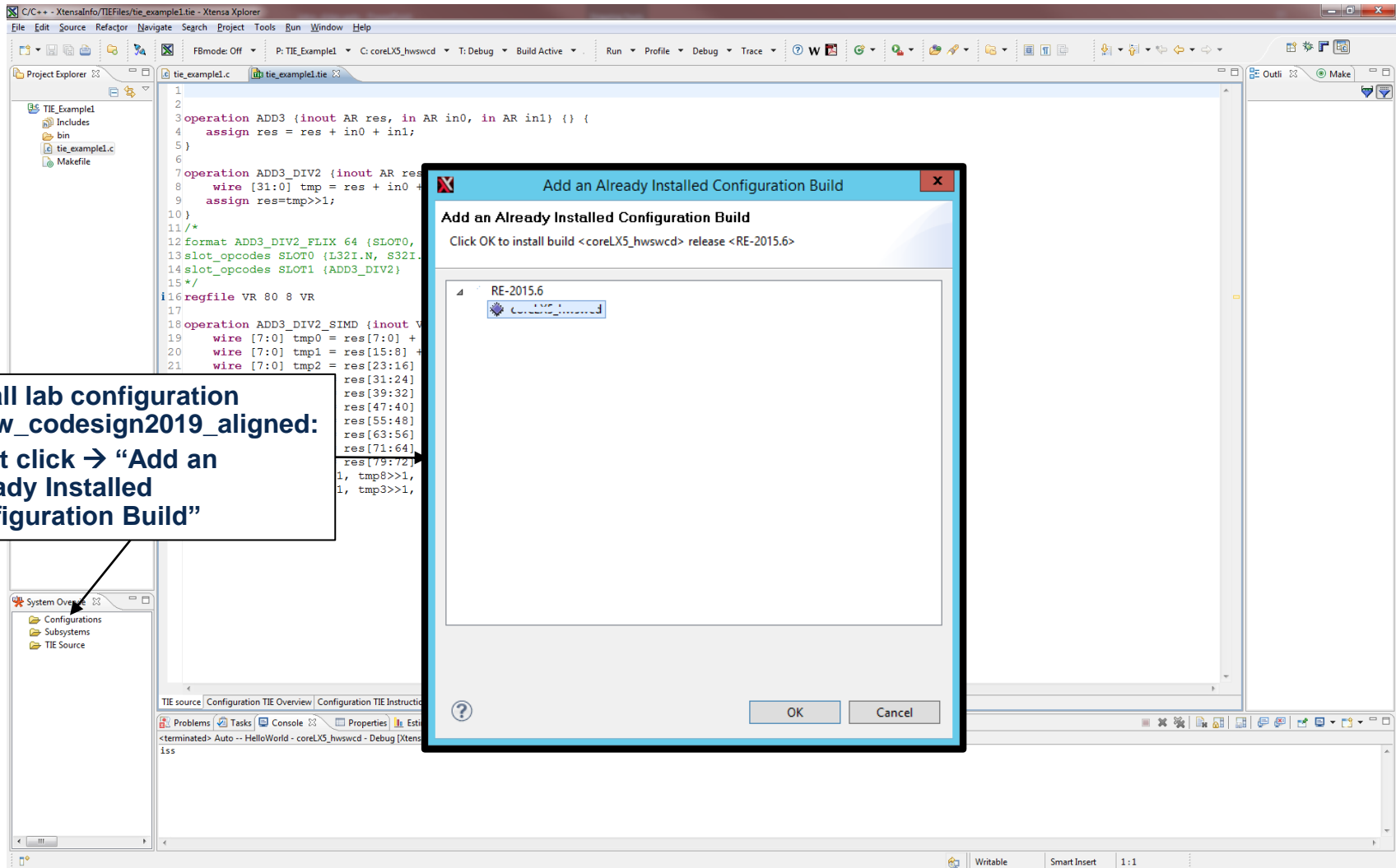
- An *.rdp* file will be downloaded which opens a connection via Remote Desktop Protocol (RDP) to a Windows computer. Your operating system has to provide an RDP client.
- Click the Xplorer icon on the desktop to start Xtensa Xplorer.



Hint:

- Windows automatically provides the RDP client
- For Linux or Mac users, install an RDP client suitable for your operating system

Xtensa Xplorer: Install Configuration



Xtensa Xplorer: C/C++ Perspective

The screenshot shows the Xtensa Xplorer IDE interface. The main editor displays C code for a project named 'TIE_Example1'. The code includes operations like 'ADD3' and 'ADD3_DIV2', and TIE (Tensilica Instructional Extension) code blocks. Annotations with arrows point to various parts of the interface:

- Build, run, profile and debug the complete C code:** Points to the 'Run', 'Profile', 'Debug', and 'Trace' buttons in the top toolbar.
- Select compile and optimization options: Right click → “Build Properties”:** Points to the 'tie_example1.c' file in the Project Explorer on the left.
- Attach TIE file to hwsd_codesign2019_aligned : Right click → “Attach TIE...”:** Points to the 'tie_example1.tie' file in the Project Explorer.
- Compile only TIE code: Right click into TIE code window → “Compile TIE”:** Points to the TIE code block in the main editor.
- TIE area report:** Points to the 'TIE area report' tab in the bottom panel.

The bottom panel shows the 'TIE area report' with tabs for 'TIE source', 'Configuration TIE Overview', and 'Configuration TIE Instruction View'. The 'TIE source' tab is active, showing the TIE code. The bottom status bar indicates 'Writable', 'Smart Insert', and '1:1'.

Xtensa Xplorer: TIE area report

Overview of TIE Source(s) for coreLX5_hwsxcd

Xtensa configuration (without TIE) is approx. 93.000 gates estimated at 380 MHz (65lp, Worst)
TIE area approx. 11.478 gates, of which 1.189 is decode, muxing etc. and 10.289 is instructions, states, regfiles etc.

Total area estimation

Operations : 1732 (15%)

Name	Area
ADD3	255
ADD3_DIV2	255
ADD3_DIV2_SIMD	598
ld.VR	308
mv.VR	8
st.VR	308

Operation area

States : 0 (0%)

Name	Bits	Area
------	------	------

States

Ports : 0 (0%)

Name	Bits	Area
------	------	------

Lookup : 0 (0%)

Name	Bits I/O	Area
------	----------	------

Tables

Queues : 0 (0%)

Name	Bits	Area
------	------	------

Register Files : 8557 (74%)

Name	W / D	Area
AR (core)	32 / 16	1878
VR	80 / 8	6679

Functions

Functions : 0 (0%)

Name	Area	Slots
------	------	-------

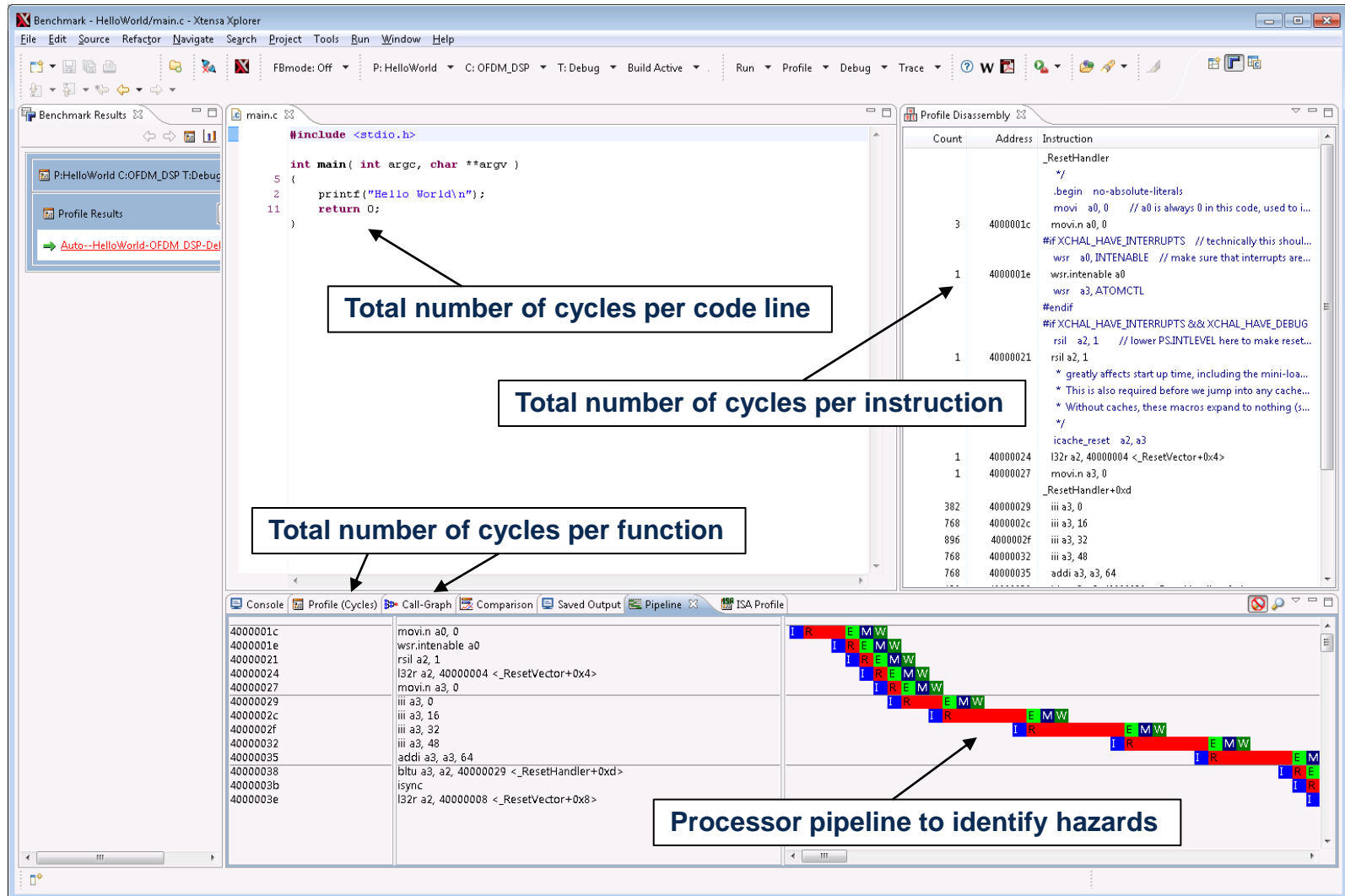
Fast Scan | Compile | Area | Compile Options | Configuration: coreLX5_hwsxcd | Close TIE editors | TDK Report

TIE source | Configuration TIE Overview | Configuration TIE Instruction View

Problems | Tasks | Console | Estimation

TIE Compiler Console (coreLX5_hwsxcd)
Analysis of file completed with no errors...

Xtensa Xplorer: Benchmark Perspective



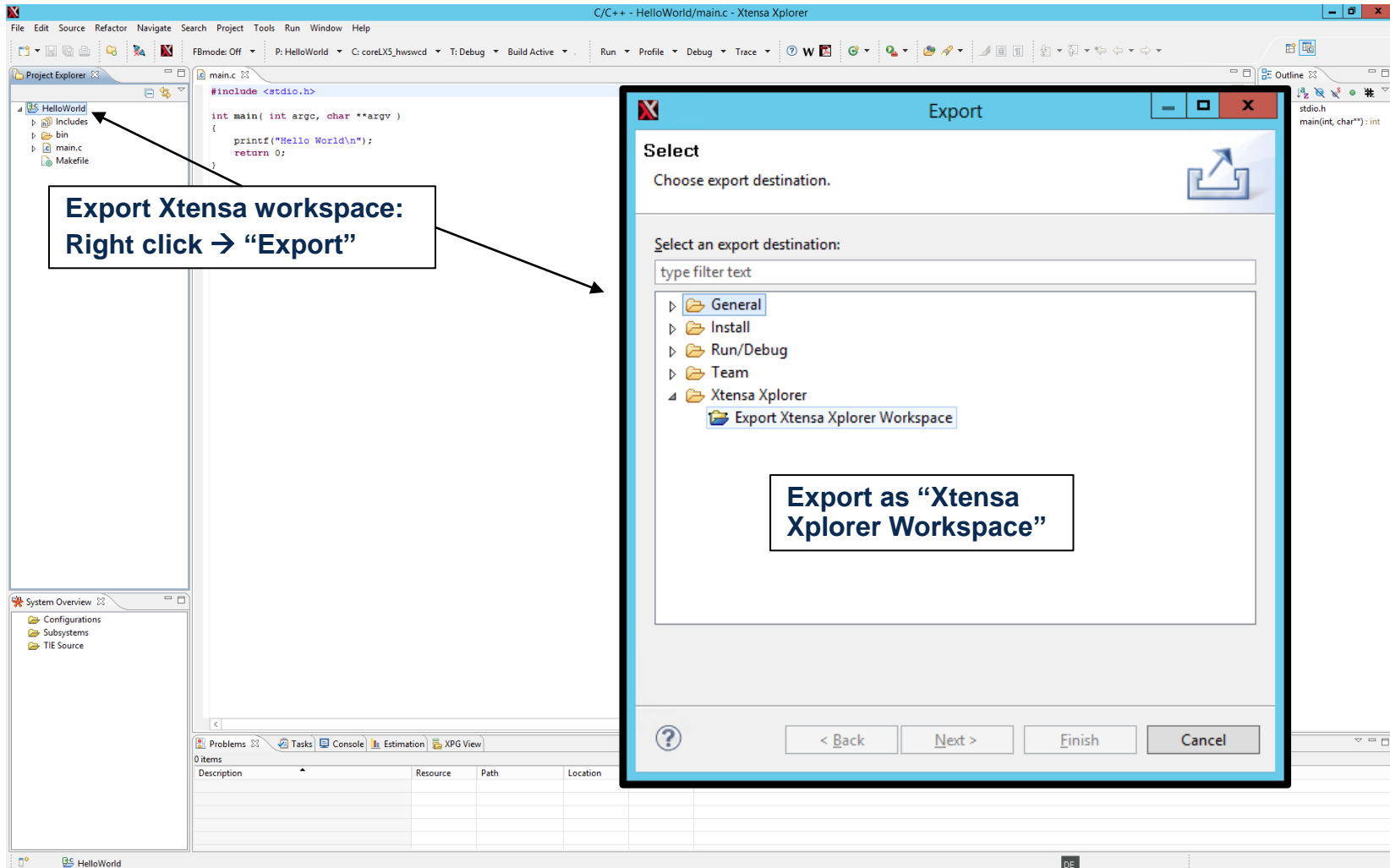
Xtensa Xplorer: Debug Perspective

The screenshot displays the Xtensa Xplorer Debug Perspective with several key components and annotations:

- Top Panel:** Contains the **Debug** tab (showing the program state and thread), **Variables** tab (showing `argc` and `argv`), **Breakpoints**, **Tie Wires**, **Trace Capture**, **Expressions**, and **Registers**. A callout box labeled "Watch C variables and TIE wires" points to the **Variables** and **Tie Wires** tabs.
- Source Editor:** Shows the `main.c` file with a breakpoint set at the `printf` statement. A callout box labeled "Set breakpoints" points to the breakpoint icon in the left margin.
- Disassembly View:** Shows the assembly code for the `main` function, including instructions like `entry a1, 48`, `s32i.n a2, a1, 0`, `s32i.n a3, a1, 4`, `l32r a10, 60000794 <_stext+0`, `call8 60000ad4 <printf>`, `movi.n a2, 0`, and `retw.n`.
- Memory View:** Shows the memory content at address `0x603fff80` in hex rendering. A callout box labeled "Watch memory content" points to the memory view. The memory content is as follows:

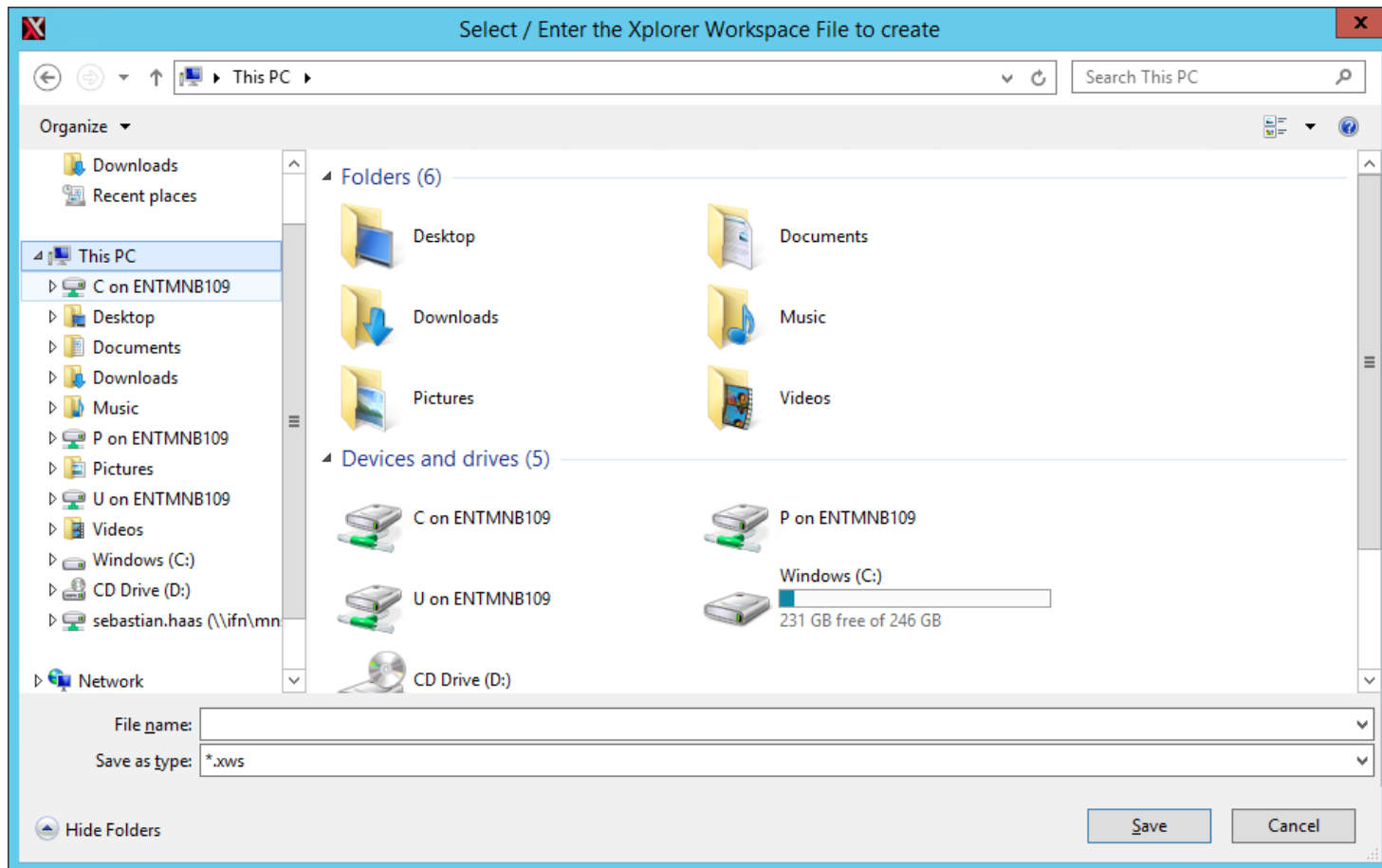
Address	3 - 0	7 - 4	B - 8	F - C
603FFF80	603FFF88	00000000	775C3A55	65745F73
603FFF90	485C7473	6F6C6C65	6C726F57	69625C64
603FFFA0	464F5C6E	445F4D44	445C5053	67756265
603FFFB0	6C65485C	6F576F6C	00646C72	E8E8E8E8
603FFFC0	E8E8E8E8	E8E8E8E8	E8E8E8E8	E8E8E8E8
603FFFD0	E8E8E8E8	E8E8E8E8	E8E8E8E8	E8E8E8E8
603FFFE0	E8E8E8E8	E8E8E8E8	E8E8E8E8	E8E8E8E8
- Console:** Shows the output of the program, including the text "Hello World\n".

Delivery: Export Xtensa Workspace (1)



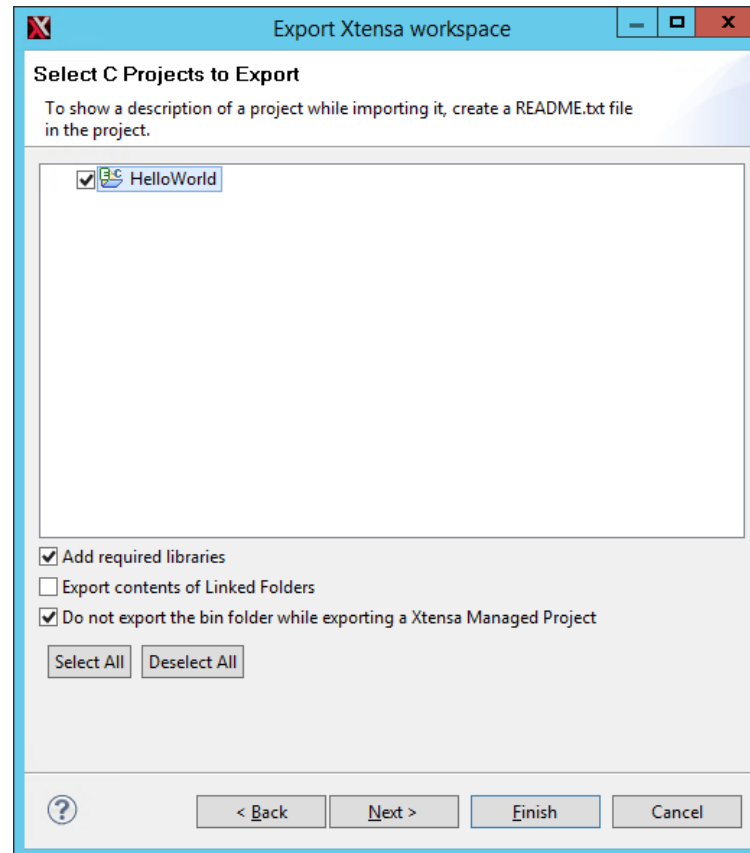
Delivery: Export Xtensa Workspace (2)

Browse and save the *.xws file to your local hard drive. Usually “C on your_PC_name”



Delivery: Export Xtensa Workspace (3)

Select your desired project

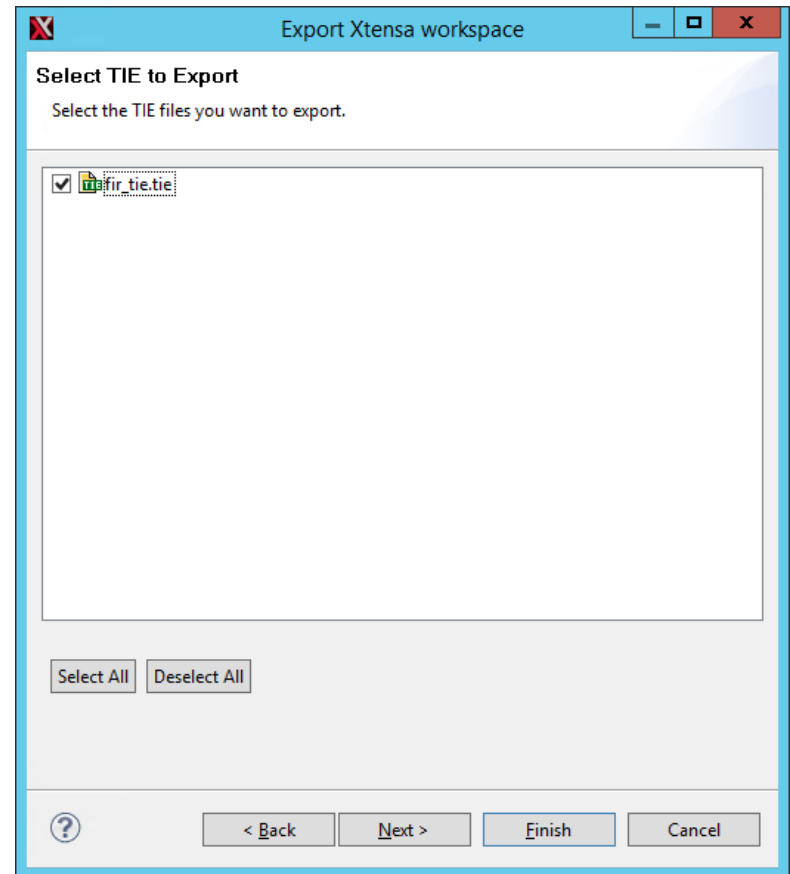


Delivery: Export Xtensa Workspace (4)

Do not export any

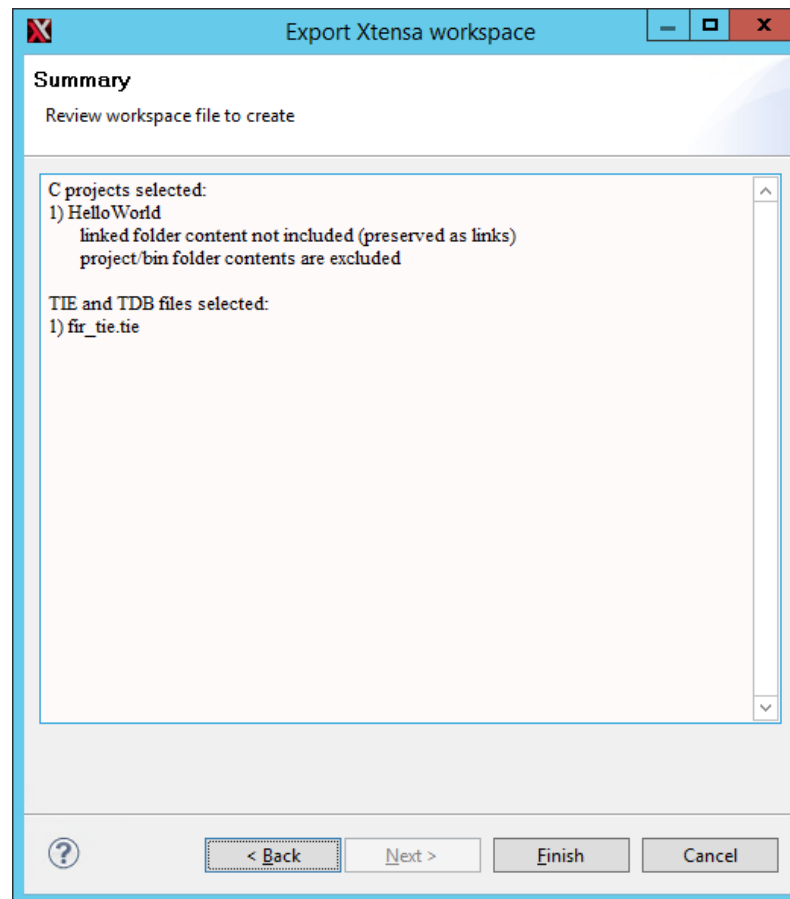
- Launches
- Configurations
- Tools
- Builds
- User-defined formats

but do export your TIE file(s)



Delivery: Export Xtensa Workspace (5)

Summary → Click on “Finish”



- Only a limited number of licenses available
- Please log off via the start menu when not working
 - Do not just close the RDP window
- You may be forcefully logged off when VM is idle for too long (~ 24 hours)
 - All unsaved work will be lost
- Store your data on U:
 - Data might get lost otherwise

TASK 1: FIR FILTER

- FIR filter:
$$y_n = \sum_{i=0}^{N-1} b_i x_{n-i}$$
- Hot-Spots
 - ❑ Multiply/Accumulate Operation (MAC)
 - ❑ Load input values/coefficients
 - ❑ Store output values

- Different approaches:

- 1) Performing MAC on one input element with one coefficient
- 2) Performing MAC on multiple elements in parallel → SIMD
- 3) Separated instructions for Load, MAC and Store

```
void fir_C(short *in, int *out, int len) {  
    int n, i;  
    for (n = 0; n < len+7; n++) {  
        for (i = 0; i < 8; i++)  
            out[n] += in[n+7-i]*coeff[i];  
    }  
}
```

SUMMARY

Your next TODOs:

- Indicate via email the members of your group (1 mail per group) → deadline 30.04.
- Review Task 1: FIR filter
- Wait for your account
 - Account information will be sent via email
- Attend next introduction session on May 7

Contact for Questions:

Viktor Razilov

viktor.razilov@tu-dresden.de

Website:

<https://www.vodafone-chair.org/teaching+opportunities#courses>

Questions?