

**Alma Mater Studiorum  
Università di Bologna**

B.Sc. in Electronic Engineering - Cesena Campus

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# **Boost Converter Project**

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Laboratory Report

Course:

**Power Electronics Laboratory**

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Academic Year 2023/2024

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# 1 Introduction

The objective of this report is to implement a DC-DC boost converter. This device is designed to generate an output voltage  $V_o$  that is greater than or equal to the input voltage  $V_{IN}$ , thus  $V_o \geq V_{IN}$ . The boost converter operates according to the principle of energy accumulation in an inductor and the subsequent transmission of that energy to the output at a higher voltage. The core of the circuit consists of a switch (such as a transistor) connected in series with an inductor and a diode. A capacitor is employed with the aim of stabilizing the output. The operation takes place through two main phases: the energy accumulation phase and the energy transmission phase. During the accumulation phase, the switch is closed, allowing energy to build up in the inductor. Subsequently, the switch opens, stopping the energy accumulation. The energy stored in the inductor is then transferred to the capacitor through the diode, thereby increasing the output voltage relative to the input voltage.

## 2 Design and Sizing

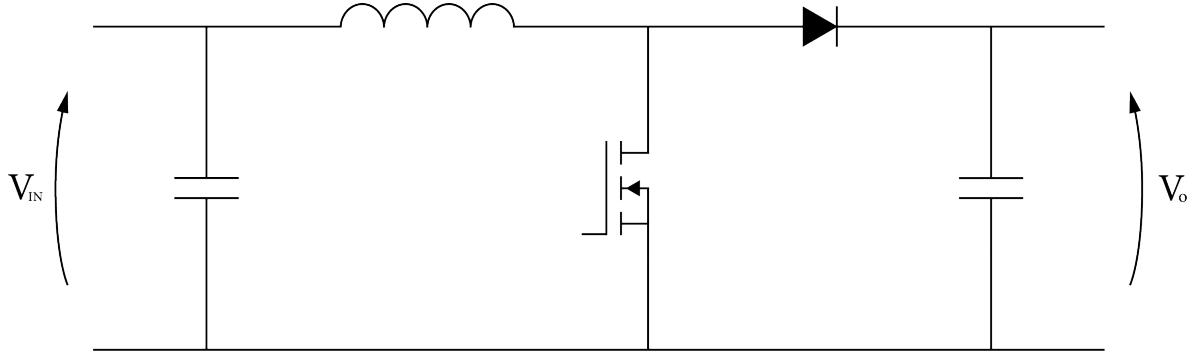


Figure 1: Basic schematic of a boost converter

### 2.1 Design Specifications

The goal is to design a converter based on the following characteristics:

- Input Voltage:  $V_{IN} = 5\text{ V}$ ;
- Output Voltage:  $V_o = 10\text{ V}$ ;
- Output Current:  $200\text{ mA} \leq I_o \leq 600\text{ mA}$ ;
- Switching Frequency:  $f_{sw} = 25\text{ kHz}$ ;
- Output Ripple:  $\frac{\Delta V}{V_o} \leq 1.5\%$ ;
- Input Capacitance:  $C_{IN} = 22\text{ }\mu\text{F}$ ;

Furthermore, it is required that the converter operates in continuous conduction mode (CCM).

### 2.2 Mathematical Analysis

We start by deriving the transfer function in order to find the duty cycle  $D$ . To do this, we analyze the voltage across the inductor during the period  $T_s$ , which must be equal to zero:

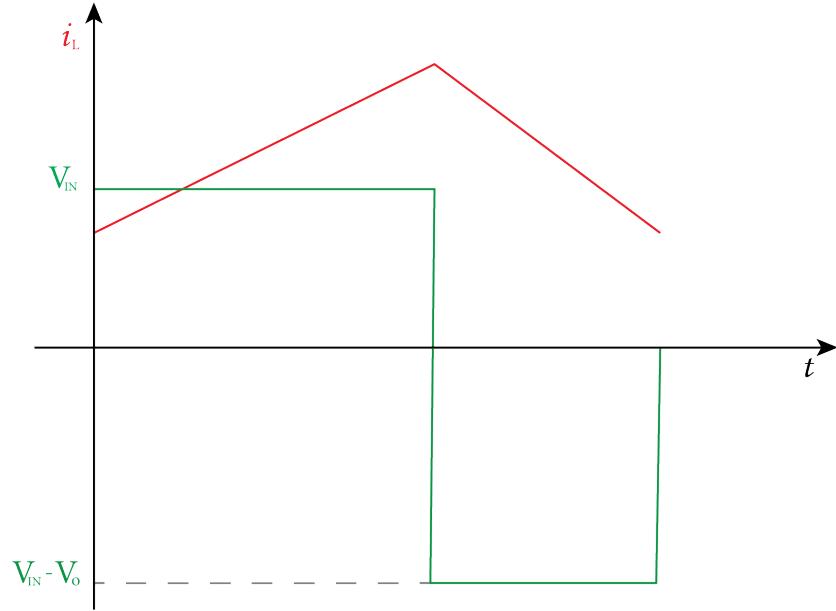


Figure 2: Inductor current and voltage

$$\begin{aligned}
 \int_0^{T_s} v_L(t) dt = 0 &\implies \int_0^{t_{ON}} v_L(t) dt + \int_{t_{ON}}^{T_s} v_L(t) dt = 0 \implies V_{IN} \times t_{ON} + (V_{IN} - V_o) \times (T_s - t_{ON}) = 0 \\
 &\implies V_{IN} \times T_s = V_o \times (T_s - t_{ON}) \implies \frac{V_o}{V_{IN}} = \frac{T_s}{T_s - t_{ON}}
 \end{aligned}$$

recalling that  $D = \frac{t_{ON}}{T_s}$ , we obtain:

$$\frac{V_o}{V_{IN}} = \frac{T_s}{T_s - t_{ON}} = \frac{1}{1 - D}$$

substituting the values yields:

$$\frac{10 \text{ V}}{5 \text{ V}} = \frac{1}{1 - D} \implies (1 - D) = \frac{5 \text{ V}}{10 \text{ V}} \implies D = \frac{1}{2} = 0.5$$

Thus obtaining a  $D$  value of 50%. Subsequently, we proceed by calculating the average inductor current in boundary mode to study the circuit and then proceed with the sizing.

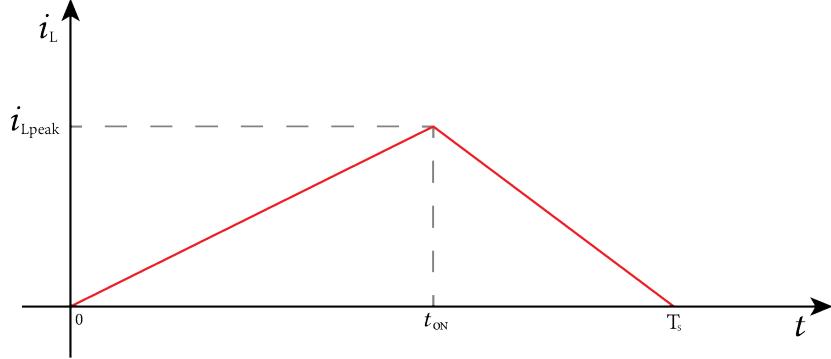


Figure 3: Inductor current in boundary mode

$$I_{LB} = \frac{1}{T_s} \times \int_0^{T_s} i_L(t) dt = \frac{1}{T_s} \times \frac{T_s \times i_{Lpeak}}{2} \implies I_{LB} = \frac{i_{Lpeak}}{2}$$

calculating  $i_{Lpeak}$ :

$$i_{Lpeak} = \frac{1}{L} \times \int_0^{t_{ON}} v_L(t) dt = \frac{1}{L} \times V_{IN} \times t_{ON} \implies i_{Lpeak} = \frac{V_{in} \times T_s \times D}{L}$$

substituting  $i_{Lpeak}$  into  $I_{LB}$  yields:

$$I_{LB} = \frac{V_{IN} \times T_s}{2L} \times D$$

Since we are given the  $I_o$  value, it is convenient to study the output current in boundary mode. To do this, we use the following relationship:  $I_{OB} = I_{LB} \times (1 - D)$  which derives from  $P_{IN} = P_o \implies \frac{I_{IN}}{I_o} = \frac{1}{1-D}$ . Substituting  $I_{LB}$  yields:

$$I_{OB} = \frac{V_{IN} \times T_s}{2L} \times D \times (1 - D)$$

we proceed to derive  $L$ , remembering to substitute  $I_{OB}$  with the smallest  $I_o$  value to consider the worst-case scenario:

$$L = \frac{V_{IN} \times T_s}{2I_{OB}} \times D \times (1 - D)$$

after calculating  $T_s = \frac{1}{f_{sw}} = 40 \mu s$ , we substitute the values and derive  $L$ :

$$L = \frac{5 \text{ V} \times 40 \mu \text{s}}{2 \times 200 \text{ mA}} \times 0.5 \times (1 - 0.5) \implies L = 125 \mu \text{H}$$

In this case, the duty cycle is a single value, as I have only one  $V_{IN}$  and one  $V_o$ , so I substitute it into the formula without worrying about which value to choose. If, however, I had two different duty cycle values, a  $D_{min}$  and a  $D_{max}$ , I would have had to take the worst-case scenario based on the graph of  $I_{OB}$  versus  $D$ , which in this case is with constant  $V_{IN}$ . Therefore, I would have chosen a  $D$  with a value closer to 0.5, since the goal is to have an  $I_{OB}$  that lies above the curve, as this determines operation in continuous conduction mode (CCM). Conversely, if the circuit were intended to operate in discontinuous conduction mode (DCM), a  $D$  value should be chosen to keep  $I_{OB}$  below the curve even in the worst-case scenario.

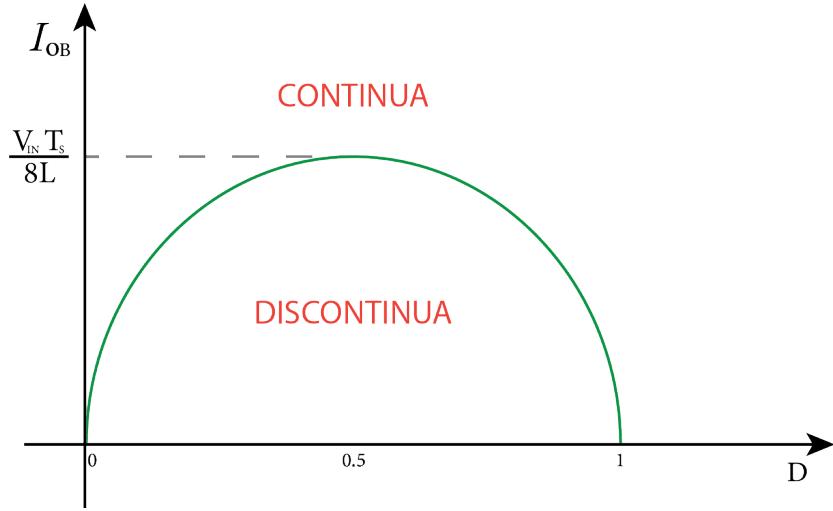


Figure 4: Boundary output current as a function of the duty cycle

Given that components have tolerances, to ensure operation in continuous conduction mode (CCM), we choose an  $L$  value that is about 20 – 25% larger, so  $L = 150 \mu \text{H}$ . In this case, the inductor with p/n: 1415440C was chosen.

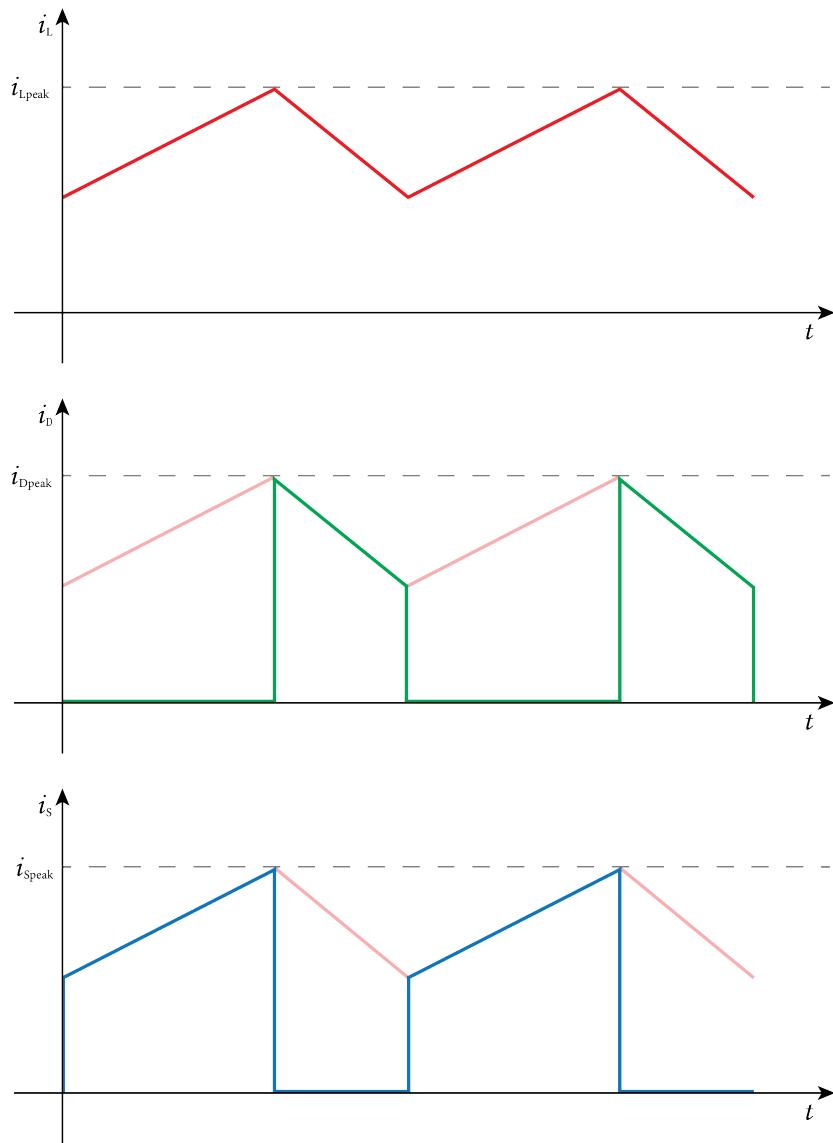


Figure 5: Current through the diode, MOSFET, and inductor

We then proceed to determine  $I_{Lavg}$  (maximum average inductor current) in order to understand the currents involved:

$$I_{Lavg} = \frac{I_{omax}}{1 - D} = \frac{0.6 \text{ A}}{1 - 0.5} \implies I_{Lavg} = 1.2 \text{ A}$$

From this, the maximum average current across the diode and the transistor,  $I_{Davg}$  and  $I_{Savg}$  respectively, can be derived:

$$I_{Davg} = I_{Lavg} \times (1 - D) = 1.2 \text{ A} \times (1 - 0.5) \implies I_{Davg} = 0.6 \text{ A}$$

$$I_{Savg} = I_{Lavg} \times D = 1.2 \text{ A} \times 0.5 \implies I_{Savg} = 0.6 \text{ A}$$

we proceed by calculating  $I_{Lpeak}$ , which is the peak inductor current in continuous conduction mode (note that  $i_{Lpeak} = \Delta i_L$ ):

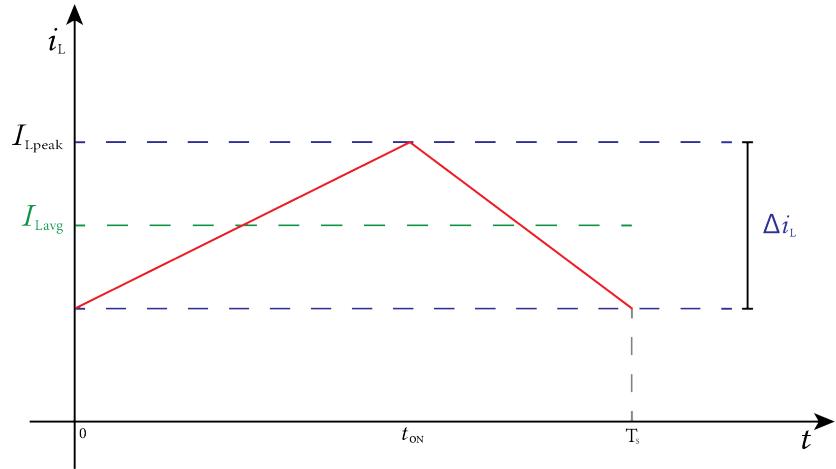


Figure 6: Maximum and peak inductor current

$$I_{Lpeak} = \frac{1}{2} \times \Delta i_L + I_{Lavg} = \frac{V_{in} \times T_s \times D}{2L} + I_{Lavg} = \frac{5 \text{ V} \times 40 \mu\text{s} \times 0.5}{2 \times 150 \mu\text{H}} + 1.2 \text{ A} \implies I_{Lpeak} = 1.53 \text{ A}$$

It is important to emphasize that \$L = 150 \mu\text{H}\$ was used in the formula, as this is the actual value that will be utilized, making the calculated \$I\_{Lpeak}\$ value more realistic. To calculate the output capacitor's capacitance, the load resistance value is needed. In this case, having an acceptable current range, two resistance values will be obtained, a minimum and a maximum:

$$R_{min} = \frac{V_o}{I_{omax}} = \frac{10 \text{ V}}{0.6 \text{ A}} \implies R_{min} = 16.67 \Omega$$

$$R_{max} = \frac{V_o}{I_{omin}} = \frac{10 \text{ V}}{0.2 \text{ A}} \implies R_{max} = 50 \Omega$$

Now we move on to sizing the capacitance by analyzing the current across the diode:

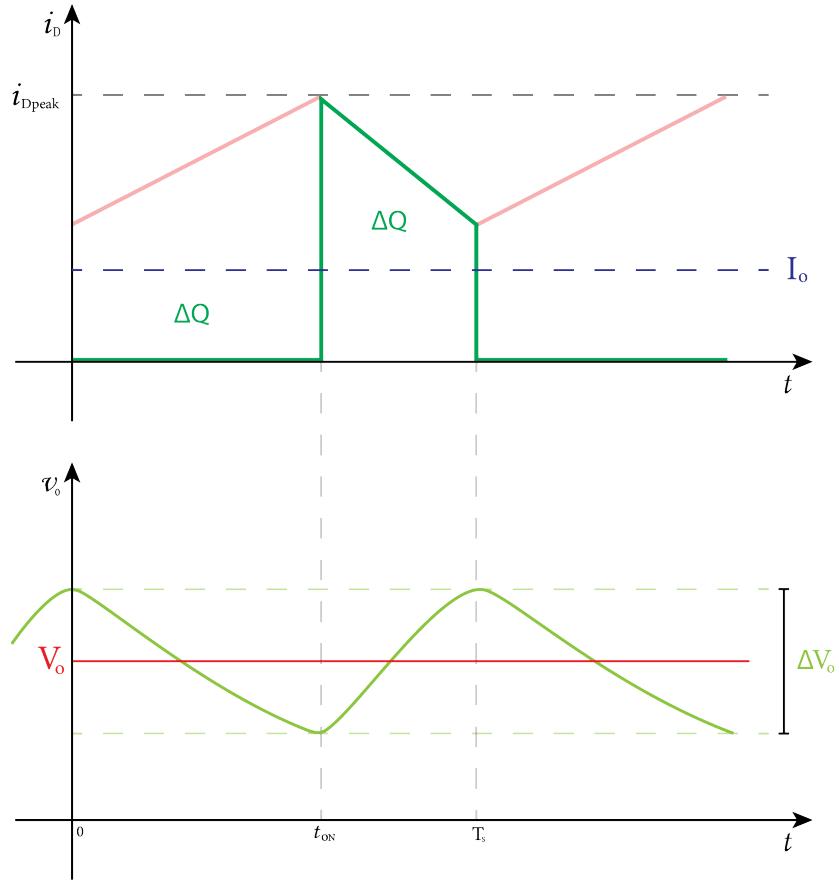


Figure 7: Capacitor

$$\Delta V_o = \frac{\Delta Q}{C} = \frac{D \times T_s \times V_o}{R_{min} \times C} \implies C = \frac{D \times T_s}{R_{min} \times \frac{\Delta V_o}{V_o}} = \frac{0.5 \times 40 \mu s}{16.67 \Omega \times 0.015} \implies C = 80 \mu F$$

$R_{min}$  was chosen as it represents the worst-case scenario with the highest output current. In this case too, a capacitor with approximately 20 – 25% more capacitance is chosen, so  $C = 100 \mu F$ .

### 2.3 Final Results

The previously calculated data are reported below:

- Duty Cycle:  $D = 50\%$
- Load Resistances:  $R_{min} = 16.67 \Omega$ ,  $R_{max} = 50 \Omega$
- Inductor:  $L = 150 \mu H$ ,  $I_{Lavg} = 1.2 A$
- Capacitor:  $C = 100 \mu F$ ,  $V_C = 50 V$
- Diode:  $V_{RRM} = 60 V$ ,  $I_{Davg} = 0.6 A$
- MOSFET:  $V_{DS} = 60 V$ ,  $I_{Savg} = 0.6 A$

The voltage values for the MOSFET, the diode, and the capacitor were chosen based on the availability of components in the laboratory. It is good practice to choose a voltage rating that is approximately double the actual voltage across the component (in this case, more than double) in order to have a good margin and avoid failures or malfunctions. Similarly, regarding the calculated currents, components with current limits significantly higher than those calculated will be chosen to maintain reliability.

### 3 Simulation

#### 3.1 Introduction

LTspice is a widely used electronic circuit simulator. It is an electronic circuit simulation software that allows for the design, simulation, and analysis of circuits before their physical implementation. The program provides a complete platform for testing the performance of analog and digital circuits, including integrated circuits, filters, power regulators, and more. LTspice enables circuits to be designed and optimized without the need to physically build a prototype. This saves time and resources during the development phase. Furthermore, it allows for the analysis of circuit behavior under various electrical conditions. Users can examine voltages, currents, power, and other crucial parameters to understand the circuit's operation. For complex circuits or integrated devices, it offers an efficient way to verify correct functioning before large-scale production. The use of LTspice reduces the costs associated with the physical construction of prototypes. Additionally, it allows for the identification and resolution of problems before production, reducing resource waste.

#### 3.2 Simulation Objective

The objective is to simulate a Boost Converter using LTspice in order to verify its correct operation and validate the values previously calculated during the sizing process. During the simulation, the behavior of the Boost Converter is analyzed, evaluating the output voltage, output current, and the circuit's efficiency.

#### 3.3 Simulation Procedure

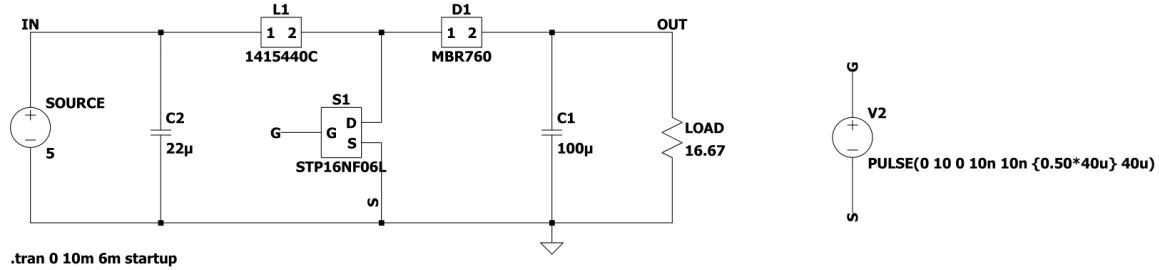


Figure 8: LTspice boost converter circuit

Firstly, we proceed with the realization of the circuit illustrated in Figure 1. For this purpose, components are imported from external libraries to ensure reliable simulation. Component models are chosen that exhibit characteristics very similar to those of the real component, considering parasitics and non-idealities. The components were selected based on availability and the calculations performed in Section 2.2. It is worth noting that some components, such as capacitors, do not have dedicated models. In such cases, the default component present in the LTspice library is used, manually integrating the parameters related to parasitics by consulting the datasheet beforehand. Specifically, parameters such as Voltage Rating, RMS Current Rating, and ESR are inserted, for both the  $100\mu F$  capacitor and the  $22\mu F$  capacitor. It should be noted that the  $22\mu F$  capacitor was added as it helps stabilize the input current and remove any noise. Another aspect to consider is the MOSFET driving. To do this, devices called gate drivers are used, which ensure correct and fast turn-on and turn-off of the MOSFET. In this case, however, not having a gate driver available, a square wave generator was configured, assuming the  $V_{on}$  is 10 V and that the rise and fall times are 10 ns, a scenario still possible in a physical circuit. For the frequency and duty cycle parameters, the values calculated previously are set.

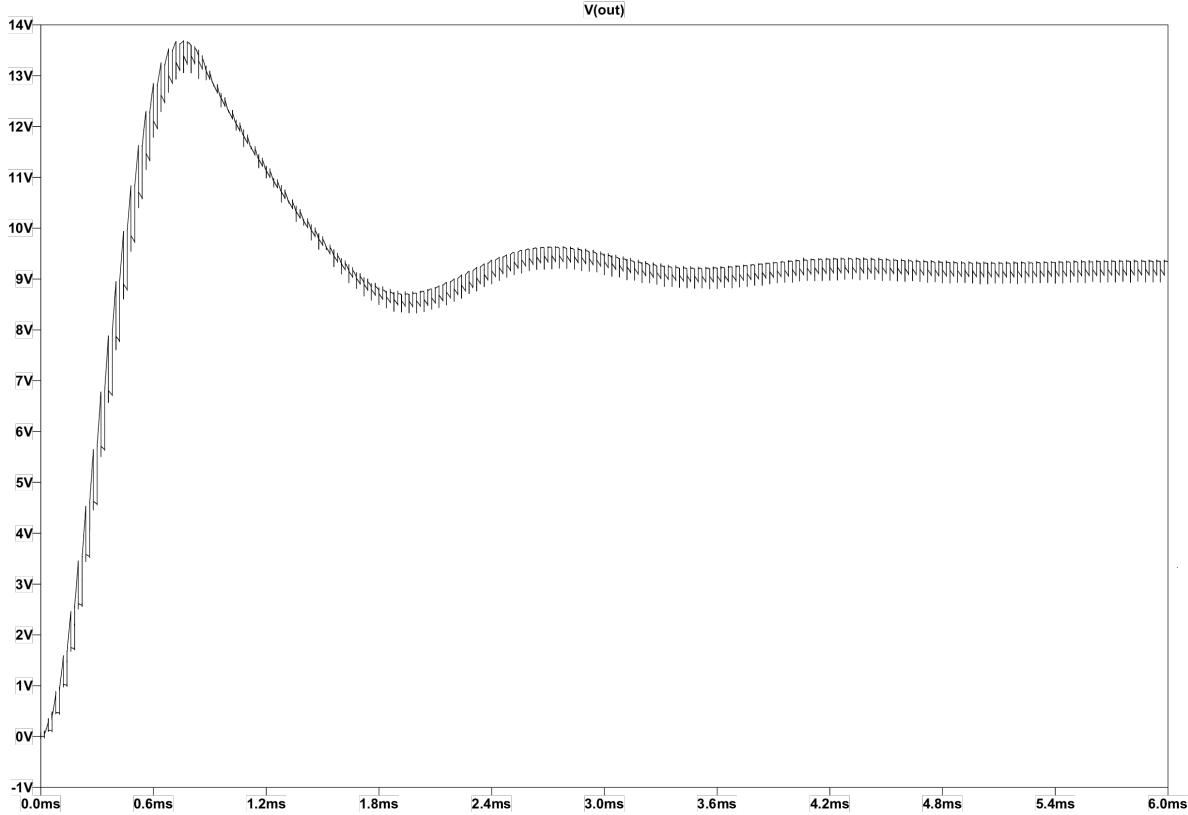


Figure 9: Initial transient

Once the circuit is realized, the simulation itself can proceed. If the simulation is started from time zero, an initial spike in the output voltage can be observed. This phenomenon is attributable to the initial conditions of the components, such as capacitors and inductors, which initially lack stored energy and thus tend to draw a significant amount of current. A possible solution to this problem is to implement a soft start mode, and possibly also a soft shut down procedure, to limit the initial voltage peak. To avoid including the transient in the measurements and consequently minimize possible errors, the simulation was configured so that the program starts recording data after approximately 6 ms, thus analyzing the circuit in steady-state. Furthermore, to automate the measurement process, directives were provided to the program to automatically calculate certain parameters.

### 3.4 Results and Analysis

The circuit analysis is performed for the two limiting cases, corresponding to  $R_{min} = 16.67 \Omega$  and  $R_{max} = 50 \Omega$ . We verify the congruence between the calculated parameters and those actually measured in the simulation. First, we confirm the presence of  $V_o = 10 \text{ V}$ . Subsequently, we verify the consistency between the calculated average currents and voltages and those obtained from the simulation. For this purpose, LTSpice directives are used, as previously indicated. Specifically, the following commands are utilized:

- vo: AVG(v(out))
- io: AVG(i(load))
- pout: AVG(v(out)\*i(load))
- pin: AVG(-v(in)\*i(source))
- eff: pout/pin
- id: AVG(ix(d1:1))

- il: AVG(ix(l1:1))
- is: AVG(ix(s1:d))

The values calculated by the software based on the provided directives can be found in the .log file generated by the simulation.

Table 1: Case 1 with  $R_{min} = 16.67 \Omega$

Quantity	Value	Unit
$v_{out}$	9.233 23	V
$i_{load}$	0.553 85	A
$p_{out}$	5.1145	W
$p_{in}$	5.546 35	W
$e_{ff}$	0.922 138	
$i_d$	0.553 632	A
$i_l$	1.109 27	A
$i_s$	0.555 639	A

Table 2: Case 2 with  $R_{max} = 50 \Omega$

Quantity	Value	Unit
$v_{out}$	9.497 61	V
$i_{load}$	0.189 952	A
$p_{out}$	1.804 14	W
$p_{in}$	1.913 24	W
$e_{ff}$	0.942 972	
$i_d$	0.190 302	A
$i_l$	0.382 649	A
$i_s$	0.192 347	A

The power involved in the circuit was also calculated, and consequently, the efficiency, which varies depending on the load, was determined. It is observed that with a 50% duty cycle, exactly  $V_o = 10 V$  is not achieved. This is attributable to the diode's voltage drop, which depends on the current flowing through the diode itself.

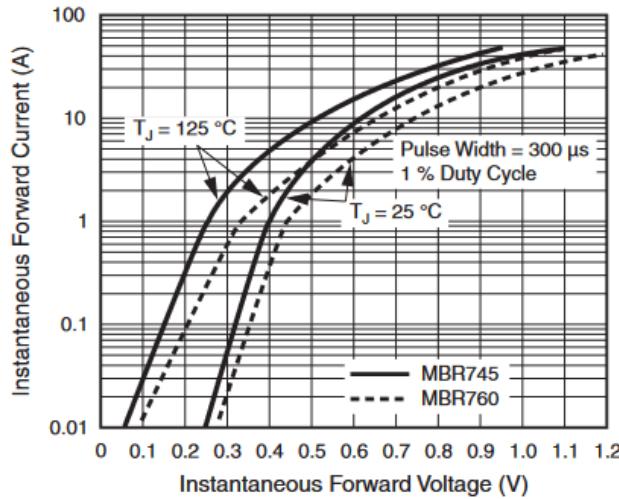


Figure 10:  $V_f$  as a function of  $I_f$

It can be noted that the voltage drop across the diode is also influenced by temperature; however, this aspect is neglected in this analysis as a thermal simulation software was not considered. Having established this, we proceed with adjusting the duty cycle in order to achieve  $V_o = 10\text{ V}$  in both cases.

Table 3: Case 1 with a 54% duty cycle

Quantity	Value	Unit
$v_{\text{out}}$	10.002	V
$i_{\text{load}}$	0.600 001	A
$p_{\text{out}}$	6.002 14	W
$p_{\text{in}}$	6.533 61	W
$e_{\text{ff}}$	0.918 655	
$i_d$	0.599 977	A
$i_l$	1.306 72	A
$i_s$	0.706 745	A

Table 4: Case 2 with a 52.5% duty cycle

Quantity	Value	Unit
$v_{\text{out}}$	10.0042	V
$i_{\text{load}}$	0.200 084	A
$p_{\text{out}}$	2.001 72	W
$p_{\text{in}}$	2.134 02	W
$e_{\text{ff}}$	0.938 007	
$i_d$	0.201 615	A
$i_l$	0.426 803	A
$i_s$	0.225 188	A

It is noted that Case 1 constitutes the most critical scenario, as it exhibits the highest average currents, which approximately coincide with the calculated ones. Specifically, the diode current matches the calculated value, while the inductor and transistor currents are slightly higher. This is attributable to approximations in the mathematical formulas and the unavoidable discrepancies in the simulation. It is observed that an increase in the output current leads to a decrease in efficiency. After adjusting the duty cycle, we verify whether the circuit operates in Continuous Conduction Mode (CCM) in both cases. To this end, the inductor current, which must remain above zero, is monitored:

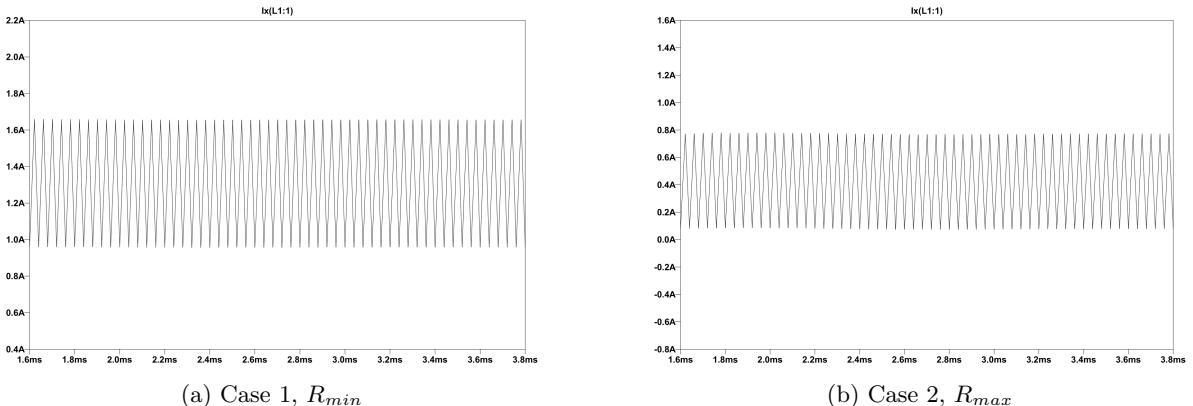


Figure 11: Inductor Current

As highlighted by the simulation analysis, the converter operates in CCM in both limiting cases, thus indicating a correct inductor sizing. Once this is verified, we proceed to confirm that the ripple requirements are effectively met by carefully examining  $V_o$ .

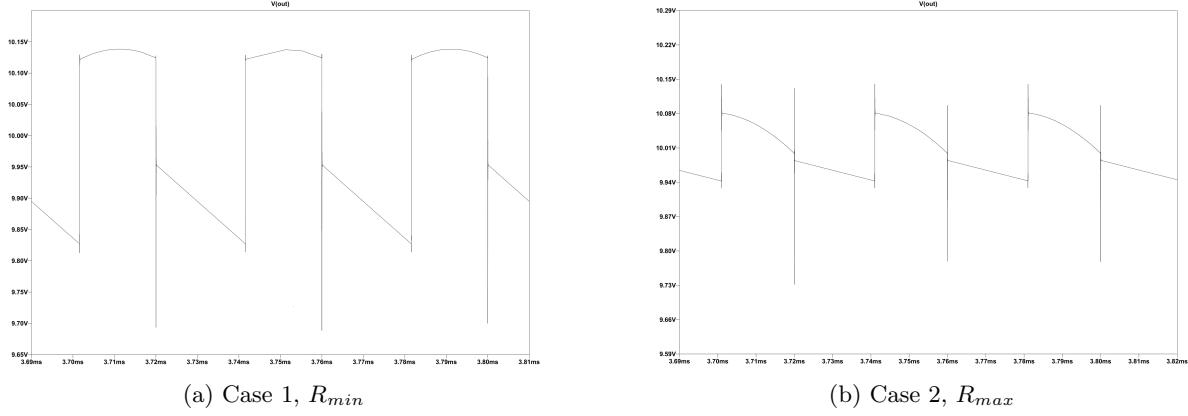


Figure 12: Ripple

Monitoring the output, a variation in the ripple is observed in the two limiting cases. In Case 1, the ripple is about 3%, while in Case 2, the ripple is about 1.5%. It is important to emphasize that spikes were not considered in this analysis. In Case 1, the design specifications are not met. This is due to the capacitor having an ESR (Equivalent Series Resistance) that affects the ripple. Therefore, the intention is to select a capacitor with a very low ESR. Since large-capacitance capacitors tend to have a relatively high ESR, a technique to reduce it involves coupling a smaller capacitor in parallel with this large-capacitance capacitor. This results in the ESRs being in parallel, and consequently, a reduction in the equivalent ESR. The different ripple amplitude based on the load is described by the following formula:

$$\frac{\Delta V_o}{V_o} = \frac{D \times T_s}{R \times C}$$

The relationship is inversely proportional: the higher the load resistance, the smaller the output ripple amplitude. This phenomenon is due to the reduction in the peak current through the inductor when the load resistance increases. In other words, a higher load resistance leads to a more gradual change in the current through the inductor, contributing to a reduction in the output ripple amplitude.

## 4 Snubber

### 4.1 Introduction

In the context of DC-DC converter design, system efficiency and safety are crucial aspects. One of the key elements for optimizing the performance of such converters is the use of appropriate protection and control circuits. Among these, snubbers play a significantly relevant role, particularly in the scenario of converters like the boost. Snubbers are circuits designed to limit voltage and current transients, thereby minimizing undesirable effects such as overvoltages, overtemperatures, and possible component damage. The objective is to reduce the electrical stress to which circuit components are subjected during the switching phase. Among the various snubber configurations, the resistor-capacitor circuit, known as the "RC snubber", has proven to be particularly effective.

### 4.2 Sizing Procedure

The sizing of the RC snubber circuit was performed through simulation, as it was not possible to conduct measurements in the laboratory. Initially, the ringing frequency ( $f_R$ ), which is the frequency of unwanted oscillations during switching transitions, was determined using LTspice. In this case, the result is  $f_R = 122\text{MHz}$ . Subsequently, a capacitor  $C_{P0}$  was introduced between the switching node and ground, in order to determine the value that halves the ringing frequency. Through iterations, a value of  $C_{P0} = 0.5\text{nF}$  was identified, thereby obtaining  $f_R = 61\text{MHz}$ . Proceeding, it was possible to calculate the value of the parasitic capacitance present in the circuit  $C_{P2}$  using the formula  $C_{P2} =$

$\frac{C_{P0}}{3} = \frac{0.5 \text{ nF}}{3} \approx 0.166 \text{ nF}$ . From this, the value of the parasitic inductance  $L_P$  was calculated using the equation:

$$f_R = \frac{1}{2\pi \times \sqrt{L_P \times C_{P2}}} \implies L_P = \frac{1}{(2\pi \times f_R)^2 \times C_{P2}}$$

$$L_P = \frac{1}{(2\pi \times 61 \text{ MHz})^2 \times 0.166 \text{ nF}} = 41 \text{ nH}$$

After this, it was possible to calculate the resistance value of the RC circuit using the following formula:

$$Z = \sqrt{\frac{L_P}{C_{P2}}} = \sqrt{\frac{41 \text{ nH}}{0.166 \text{ nF}}} = 15.71 \Omega \approx 16 \Omega$$

Regarding the snubber capacitance  $C_{SNB}$ , a value between 1 and 8 times that of  $C_{P2}$  was chosen. The higher the capacitance, the greater the attenuation of unwanted oscillations (ringing) during switching transitions; however, this results in higher power dissipation. A good compromise is to choose  $C_{SNB} = 4 \times C_{P2} = 4 \times 0.166 \text{ nF} \approx 0.66 \text{ nF}$ . Therefore, the calculated values are:

- $R_{SNB} = 16 \Omega$
- $C_{SNB} = 0.66 \text{ nF}$

### 4.3 Simulation of the Circuit with Snubber

The circuit, appropriately modified with the addition of the RC snubber suppressor circuit, is shown below.

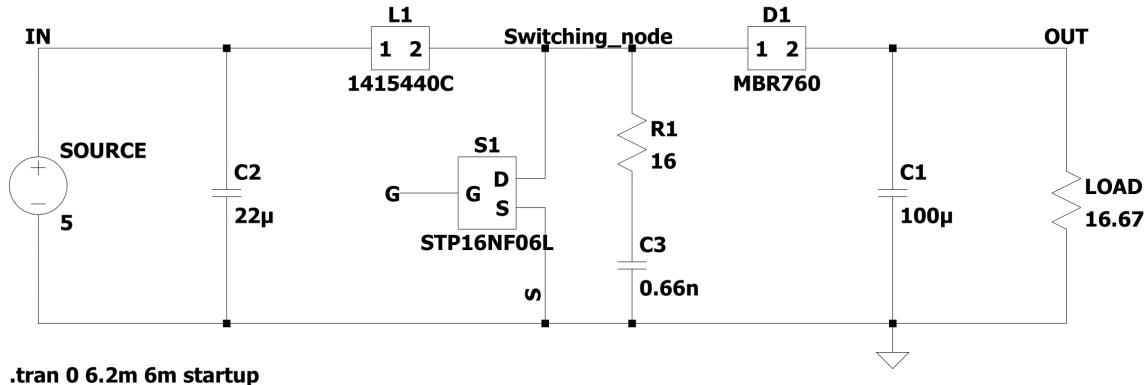


Figure 13: Circuit with snubber

The case analyzed considers  $R_{load} = 16.67 \Omega$ , but the same principle applies to  $R_{load} = 50 \Omega$ , yielding analogous benefits. The graphs below highlight the improvements made to the signals at both the switching node and the output, before and after the inclusion of the snubber circuit.

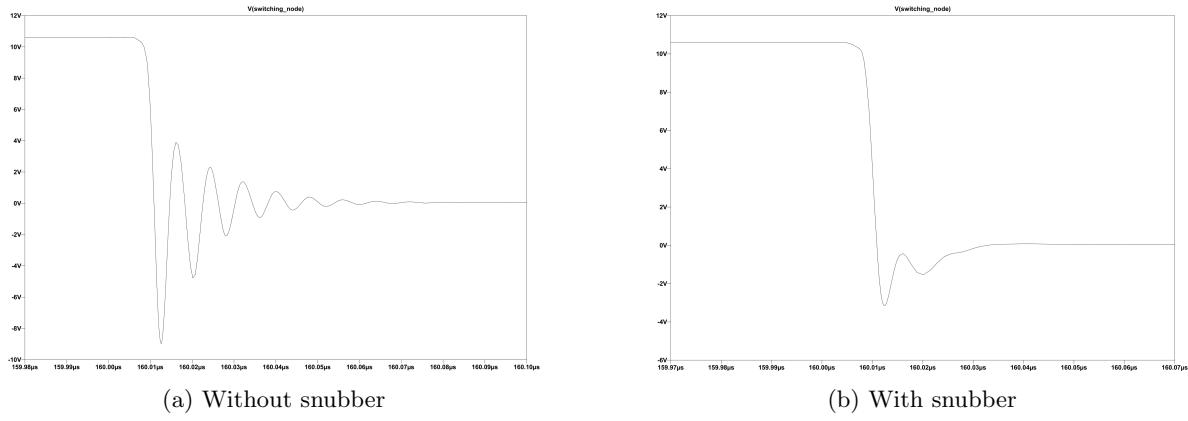


Figure 14: Switching node

The analysis of the graphs reveals a notable reduction in the amplitude and duration of unwanted oscillations at the switching node after the introduction of the snubber circuit. Furthermore, a significant decrease in the overall number of oscillations is observed. These improvements indicate increased circuit robustness and enhanced overall performance.

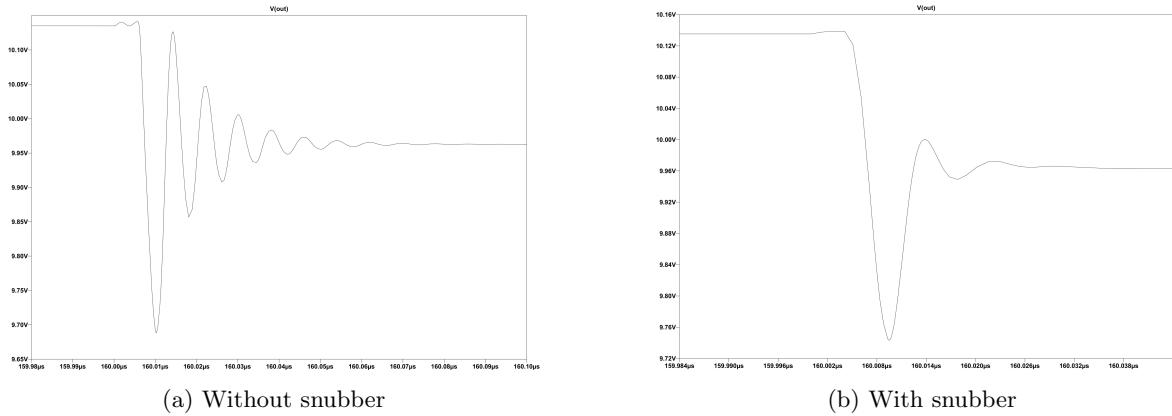


Figure 15: Output

In the evaluation of the output, it is observed that the snubber had a limited impact on the ripple amplitude. However, it significantly influenced the duration, making it considerably shorter, and the overall number of oscillations, which was significantly reduced. This suggests that the introduction of the snubber circuit led to an improvement in the stability of the output signal, reducing the persistence of unwanted oscillations over time.

#### 4.4 Conclusion

In conclusion, the implementation of the RC snubber circuit for the boost converter proved effective in enhancing the overall robustness of the system. Through careful component sizing and accurate simulation with LTspice, promising results were obtained, confirming the validity of the proposed solution. The improvements made to the circuit contributed significantly to the reduction of unwanted oscillations and the minimization of stress on critical components. Analysis of the results obtained during the simulation confirmed the system's stability and the RC snubber circuit's ability to mitigate negative effects, ensuring a more reliable and robust operation of the boost converter. Furthermore, it is important to emphasize that the sizing of the RC snubber circuit is a delicate process and requires careful consideration of the system parameters. Balancing the circuit's damping characteristics and the boost converter's specifications is crucial for achieving the best results. In the future, further optimizations could be explored to refine the system's performance, taking into account variations in loads and operating conditions.

## 5 Circuit Implementation

### 5.1 Introduction

The phase of practical implementation of a circuit assumes a fundamental role in the design and simulation process. The transition from sizing and simulation to realization on a breadboard opens the door to more detailed considerations, focused on the real interaction of components and the management of inevitable parasitics that can influence circuit performance. In this section, we will explore how the circuit was concretely realized on the breadboard, highlighting the implementation details and analyzing the considerations related to parasitics.

### 5.2 Circuit Realization on Breadboard

We now proceed with the assembly of the circuit on a breadboard, an essential tool in electronics for prototyping experimental circuits. Its utility lies in the ease with which it allows electronic components to be connected and tested without the need for permanent soldering. Furthermore, it facilitates modification and updating of the circuit, enabling rapid iteration in the development process. However, it is important to consider some disadvantages associated with breadboard use, including unstable connections, interference and parasitic capacitance, current and power limitations, as well as operating frequency limits. Additionally, attention must be paid to the circuit's size and footprint. During the assembly of the boost converter circuit, it is advisable to position the components as close as possible to avoid high parasitic interference. Once this is done, we proceed with connecting all the instruments to operate the circuit.

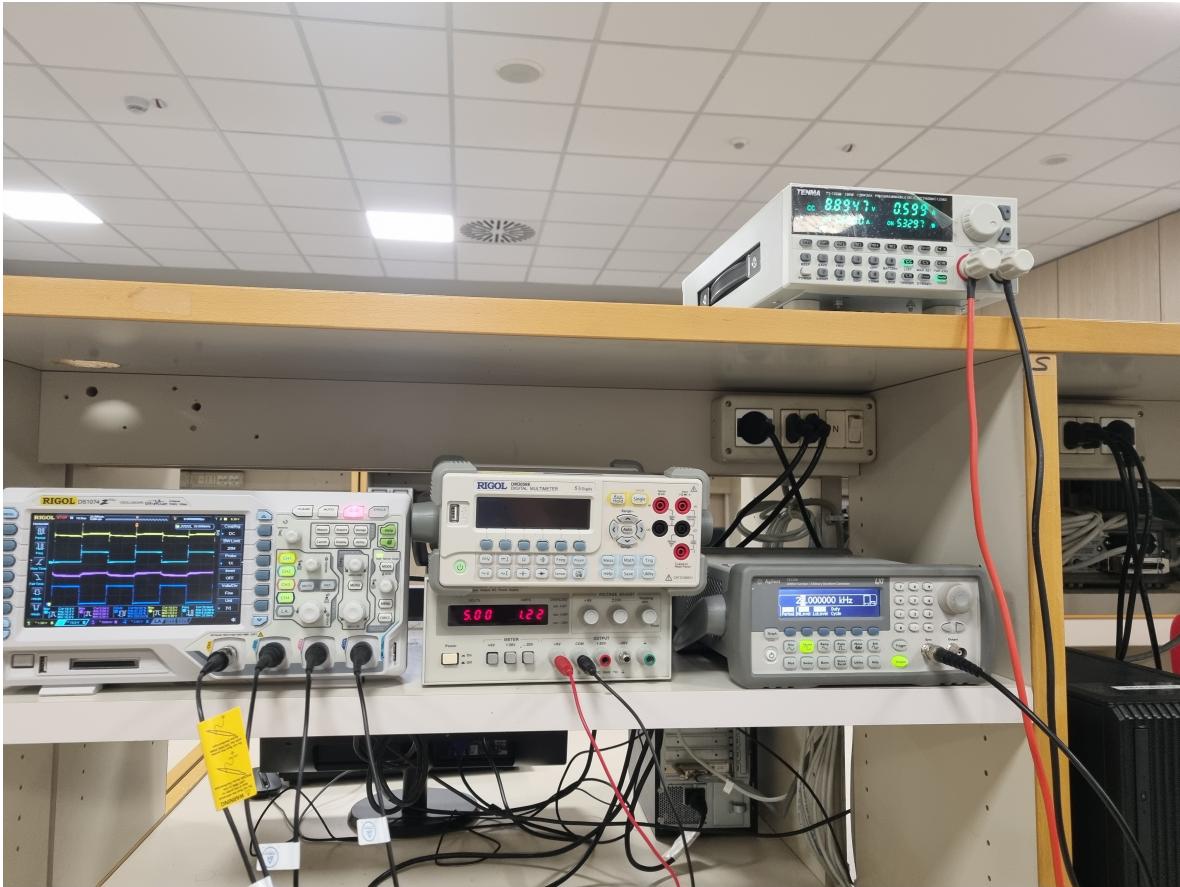


Figure 16: Instrumentation used

The image above shows the instruments used to analyze and test the circuit. The following instruments were employed to verify the circuit's correct operation:

1. **Bench Power Supply:** Used to provide power to the circuit, the power supply can deliver an adjustable voltage. In this specific case, the input voltage  $V_{IN}$  was set to 5 V.
2. **Function Generator:** Employed to generate the square wave used to drive the MOSFET's gate. The function generator offers the ability to adjust the switching frequency  $f_{sw}$  and the duty cycle. In the current configuration, the switching frequency was set to 25 kHz, while the duty cycle was adjusted to obtain an output voltage  $V_o$  equal to 10 V.
3. **Electronic Load:** Used to simulate an adjustable load, the electronic load allows the circuit's behavior to be analyzed under various output conditions.
4. **Oscilloscope:** Employed to monitor and analyze the signals within the circuit. Specifically, the converter output is observed on channel CH1, the switching node on CH2, the input voltage on CH3, and the square wave driving the MOSFET gate on CH4. The oscilloscope provides a detailed visualization of the signals, allowing for an accurate evaluation of the circuit's performance.

The coordinated use of these instruments allows for an in-depth analysis of the circuit and verifies its correct operation under different operating conditions. The signals displayed on the oscilloscope are presented in the following figure, offering a complete overview of the circuit's dynamic characteristics.

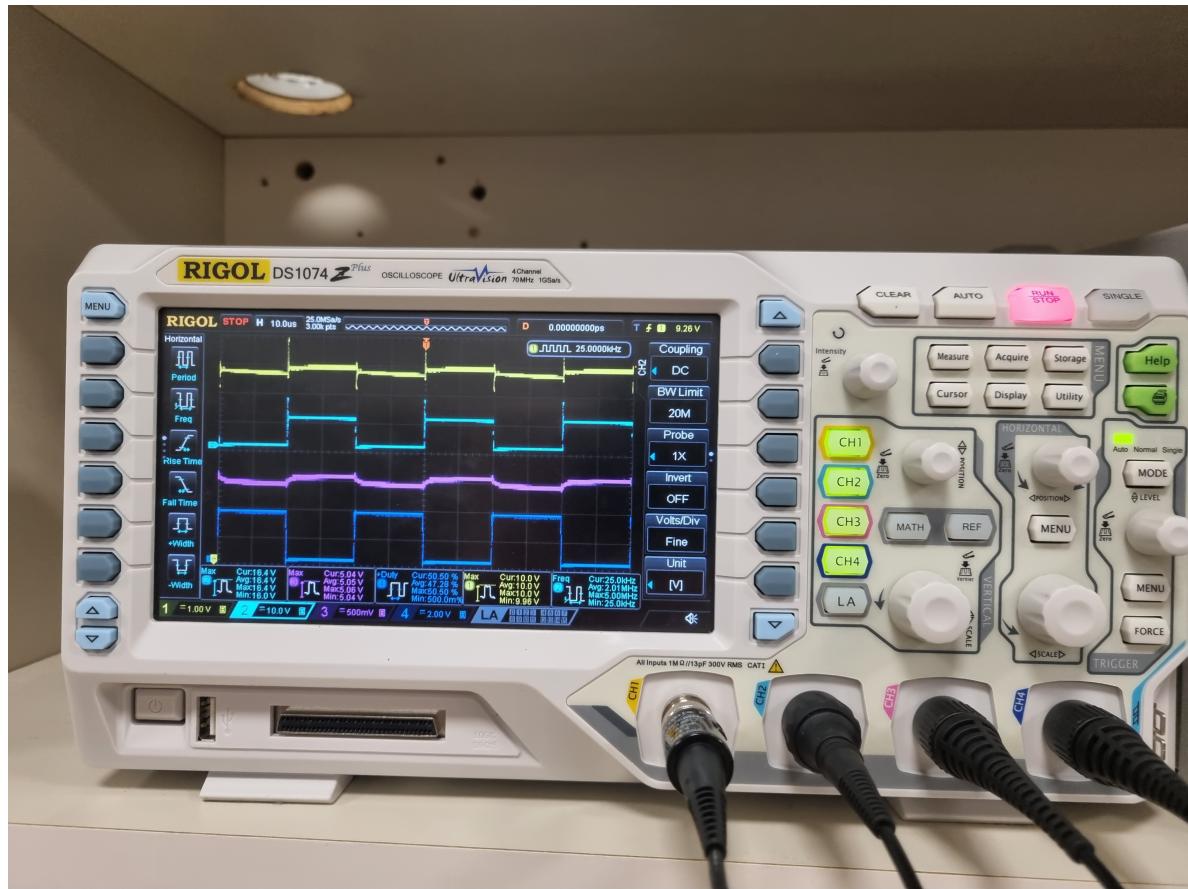


Figure 17: Signals present on the oscilloscope

The assembled circuit on the breadboard, complete with wiring and probes, is shown below. The input is positioned on the left, while the output is on the right. Note that an oscilloscope probe without a ground clip is present at the switching node. This choice is motivated by the switching node's sensitivity to interference. By using a spring tip on the probe, the parasitic inductance created by the cable is limited, resulting in a more accurate measurement without significantly affecting the circuit's behavior.

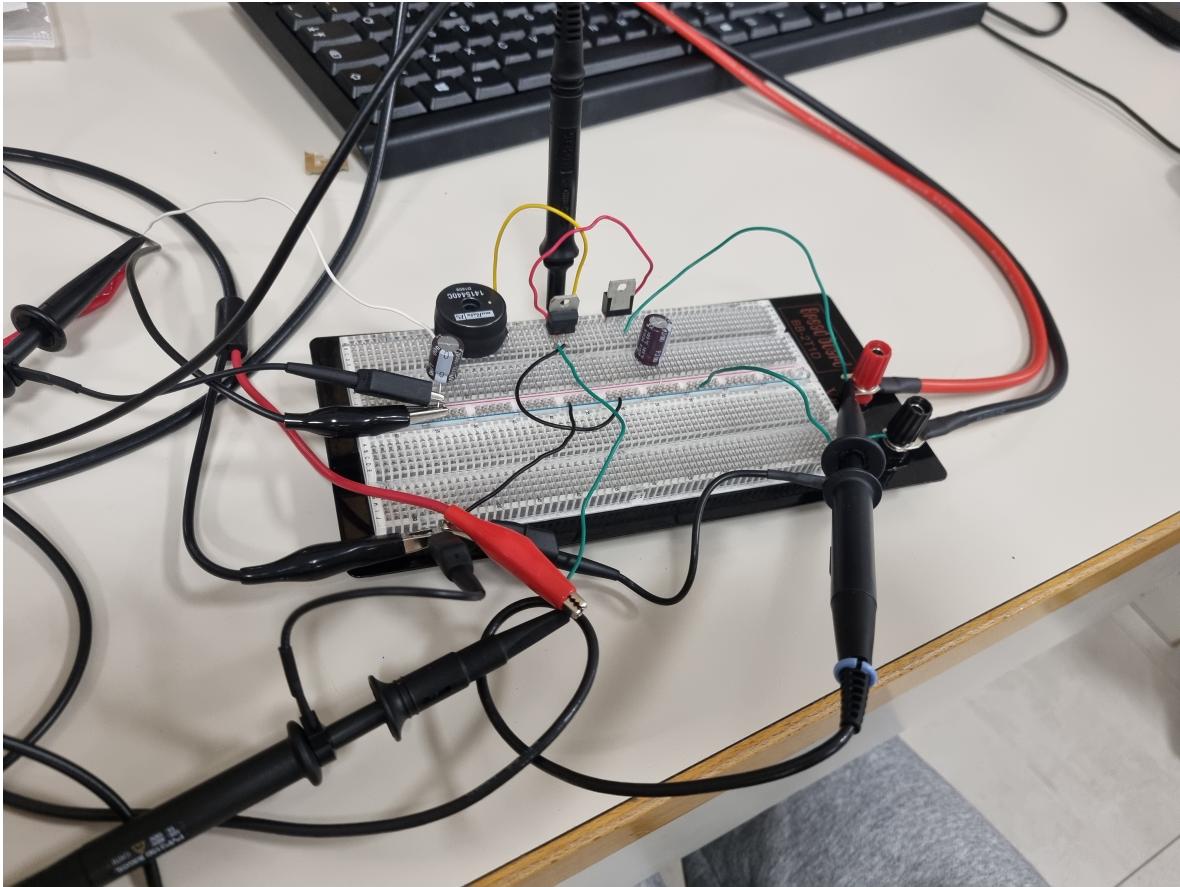


Figure 18: Circuit on breadboard

### 5.3 Operational Analysis

Due to the unavailability of a current probe, it was not possible to directly monitor the current through the inductor. However, a detailed analysis of the circuit's correct operation was conducted by varying the load, with a particular focus on the power involved and the overall efficiency. The following figures report the results of the analysis with two distinct configurations:

Iout	0.15 A	Vin	5 V	Vout	9.94 V	Iin	0.34 A	Pin	1.70 W	Pout	1.491 W	Eff	87.70%	Duty	50%
Iout	0.2 A	Vin	5 V	Vout	9.49 V	Iin	0.43 A	Pin	2.15 W	Pout	1.898 W	Eff	88.27%	Duty	50%
Iout	0.3 A	Vin	5 V	Vout	9.22 V	Iin	0.62 A	Pin	3.10 W	Pout	2.766 W	Eff	89.20%	Duty	50%
Iout	0.4 A	Vin	5 V	Vout	9.32 V	Iin	0.83 A	Pin	4.15 W	Pout	3.728 W	Eff	89.80%	Duty	50%
Iout	0.5 A	Vin	5 V	Vout	9.16 V	Iin	1.03 A	Pin	5.15 W	Pout	4.580 W	Eff	88.90%	Duty	50%
Iout	0.6 A	Vin	5 V	Vout	9.08 V	Iin	1.24 A	Pin	6.20 W	Pout	5.448 W	Eff	87.87%	Duty	50%
Iout	0.7 A	Vin	5 V	Vout	9.07 V	Iin	1.44 A	Pin	7.20 W	Pout	6.349 W	Eff	88.10%	Duty	50%
Iout	0.8 A	Vin	5 V	Vout	8.90 V	Iin	1.64 A	Pin	8.20 W	Pout	7.120 W	Eff	86.82%	Duty	50%
Iout	0.9 A	Vin	5 V	Vout	8.72 V	Iin	1.84 A	Pin	9.20 W	Pout	7.848 W	Eff	85.30%	Duty	50%

Figure 19: Analysis with duty cycle fixed at 50%

Iout	0.15 A	Vin	5 V	Vout	10 V	lin	0.35 A	Pin	1.75 W	Pout	1.5 W	Eff	85.70%	Duty	50.40%
Iout	0.2 A	Vin	5 V	Vout	10 V	lin	0.44 A	Pin	2.20 W	Pout	2 W	Eff	90.90%	Duty	52.20%
Iout	0.3 A	Vin	5 V	Vout	10 V	lin	0.66 A	Pin	3.31 W	Pout	3 W	Eff	90.63%	Duty	52.60%
Iout	0.4 A	Vin	5 V	Vout	10 V	lin	0.89 A	Pin	4.45 W	Pout	4 W	Eff	89.80%	Duty	53.50%
Iout	0.5 A	Vin	5 V	Vout	10 V	lin	1.13 A	Pin	5.65 W	Pout	5 W	Eff	88.40%	Duty	54.50%
Iout	0.6 A	Vin	5 V	Vout	10 V	lin	1.36 A	Pin	6.80 W	Pout	6 W	Eff	88.24%	Duty	54.60%
Iout	0.7 A	Vin	5 V	Vout	10 V	lin	1.61 A	Pin	8.05 W	Pout	7 W	Eff	86.95%	Duty	55.30%
Iout	0.8 A	Vin	5 V	Vout	10 V	lin	1.88 A	Pin	9.40 W	Pout	8 W	Eff	85.10%	Duty	56.40%
Iout	0.9 A	Vin	5 V	Vout	10 V	lin	2.18 A	Pin	10.9 W	Pout	9 W	Eff	82.50%	Duty	57.70%

Figure 20: Analysis with adapted duty cycle

More specifically, the following parameters were analyzed:

- $I_{out}$  : Output current
- $V_{in}$  : Input voltage
- $V_{out}$  : Output voltage
- $I_{in}$  : Input current
- $P_{in} = V_{in} \times I_{in}$  : Input power
- $P_{out} = V_{out} \times I_{out}$  : Output power
- $E_{ff} = \frac{P_{out}}{P_{in}}$  : Converter efficiency
- $Duty$  : Duty cycle utilized

In addition to the two limiting cases, extreme cases falling outside the specifications were also analyzed to evaluate the circuit's behavior and monitor efficiency. Figure 19 shows the circuit's behavior with the duty cycle fixed at 50%. As previously mentioned, 10 V is not reached at the output; instead, the voltage depends on the diode's voltage drop. In this configuration, considering the experimental nature of the circuit on a breadboard, \*\*parasitics\*\* such as resistances, inductances, and capacitances that influence the output must be taken into account. Figure 20 shows the results obtained by adapting the duty cycle to achieve 10 V at the output. By analyzing the power involved, efficiency can be estimated. It is noted that the efficiency is maximum with an output current of 0.2 A, while the minimum efficiency is recorded at 0.9 A. The power graph provides further details on this behavior.

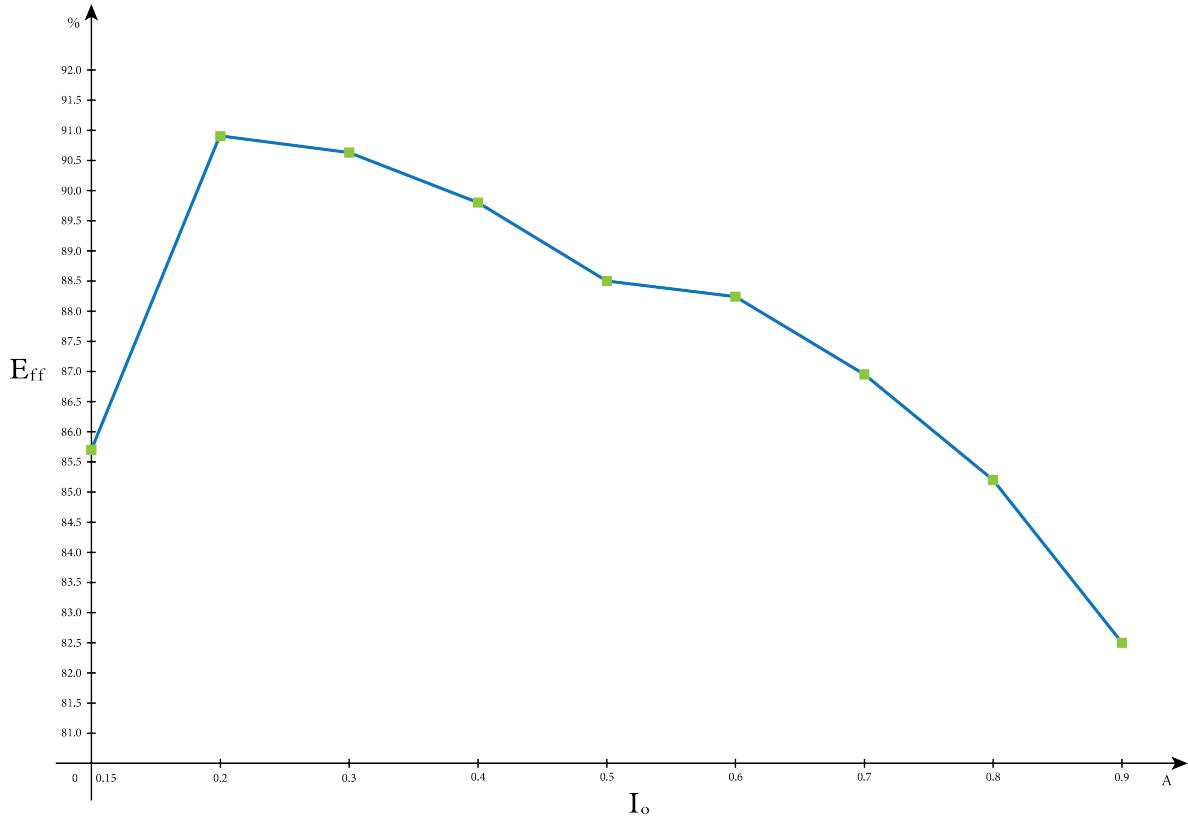


Figure 21: Relationship between efficiency and output current

Graph 21 displays the relationship between efficiency ( $E_{ff}$ ) and output current ( $I_{out}$ ). This representation highlights a trend characterized by a peak of maximum efficiency corresponding to  $I_{out} = 0.2$  A, followed by a decrease as the current increases. A decrease in efficiency is also noted for currents below 0.2 A. A noticeable increase in losses is observed as the current grows; these losses can stem from various sources, including internal resistances, Joule heating effects in electrical components, or other factors that can generate heat. At high power levels, greater effort may be required to maintain stable output voltage or current. This might necessitate the boost converter operating with a more extended duty cycle, increasing losses and decreasing overall efficiency. This is an important aspect to consider in design and practical use, especially when the goal is to achieve optimal energy efficiency. Furthermore, an analysis of the output ripple in the two limiting cases was conducted using the cursors present on the oscilloscope, as shown in Figure 22.

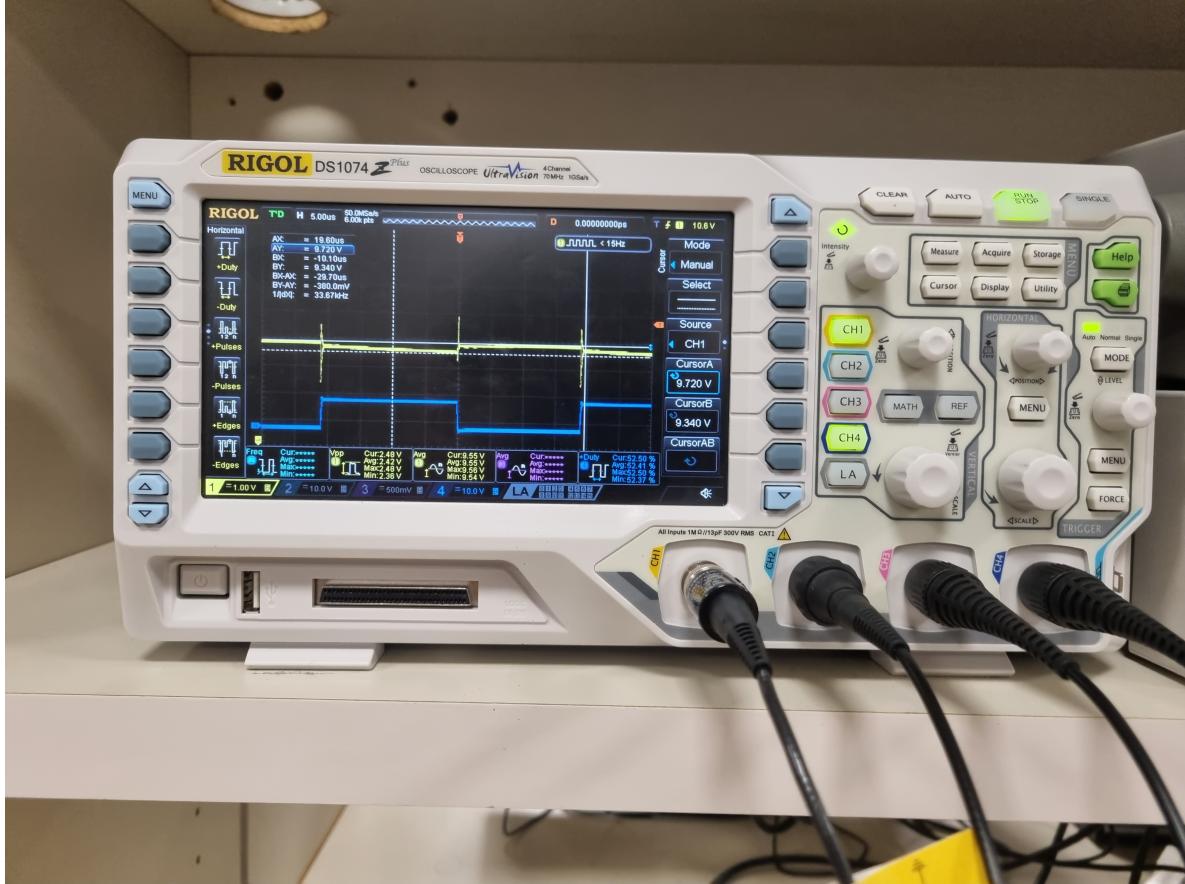


Figure 22: Output ripple

By iterating this operation across different operating conditions, the following results were obtained, reported in the table:

Table 5: Ripple

$I_{out}$	Duty	Ripple
0.6 A	50 %	2.8 %
0.2 A	50 %	2.1 %
0.6 A	54.6 %	3.8 %
0.2 A	52.2 %	2.4 %

It is noted that, once again, the ripple requirements are not completely satisfied. This is attributable to the capacitor's Equivalent Series Resistance (ESR) combined with the parasitic resistance introduced by the breadboard, which both contribute to the presence of the ripple.

## 6 Conclusion

In conclusion, this work has provided a comprehensive overview of the boost converter, covering crucial aspects such as sizing, simulation, and practical implementation. Through careful design and simulation, we were able to determine the key circuit parameters to ensure the correct operation of the boost converter. The implementation phase confirmed the effectiveness of the design choices, highlighting the importance of a proper physical realization to achieve optimal performance. The simulations proved useful in correcting any errors made during the design phase and demonstrated that the designed circuit meets the specified requirements, guaranteeing acceptable efficiency. Furthermore, the practical phase

helped to underscore the real-world challenges and practical aspects of the implementation process. This study provides a solid foundation for further research and development in the field of DC-DC converters, with the aim of further optimizing performance and addressing integration challenges. The boost converter is confirmed as a versatile and fundamental solution in numerous applications and industrial sectors. In the future, further optimizations could be explored to adapt the circuit to the specific needs of certain application contexts. Potential future work includes the detailed design of a dedicated PCB to mitigate parasitics and ensure acceptable thermal response, and it would also be interesting to study the implementation of various gate drivers and verify their impact on the total efficiency.