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B.Sc. in Electronic Engineering - Cesena Campus

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# **Two-Stage Converter Project**

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Laboratory Report

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**Power Electronics Laboratory**

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# 1 Introduction

The objective of this simulation is the realization of an electronic circuit capable of converting an alternating current (AC) signal into a stabilized direct current (DC) signal. Within the context of this requirement, we propose the creation of a system consisting of two distinct stages: a diode rectifier followed by a buck converter. The development methodology, in addition to focusing on creating a functional circuit, involves the implementation of targeted simulations and separate analyses of the individual stages to thoroughly understand their operating dynamics, identify any critical issues, and subsequently integrate everything into a harmonic solution. The first stage, the diode rectifier, plays a crucial role in the process of transforming the AC signal into DC. This process is essential for powering electronic devices that require a constant voltage, ensuring a stable and reliable energy supply. The selection of diodes and the configuration of the rectifier bridge will be subject to careful consideration to maximize the efficiency of this phase. The goal is to obtain a clean and stable DC current, ready to power the subsequent stage of the system. The second stage, the buck converter, takes on the task of reducing the DC voltage level obtained from the diode rectifier to a specific desired value. This type of converter, also known as a step-down converter, operates by modulating the duty cycle, thereby reducing the output voltage while maintaining high energy efficiency. The design of this stage requires the correct selection of components, including inductors and power transistors, to ensure accurate regulation of the output voltage. The interconnection of these two stages represents an integrated and optimized solution for power conversion, allowing a stable and regulated DC voltage to be obtained from an input AC signal. Such a system meets the needs of numerous electronic devices, helping to ensure reliable and efficient operation in various application contexts. A key element of this design phase is the simulation, which will allow for the verification and optimization of the performance of each stage separately. The use of simulation software, such as LTSpice, will enable a detailed analysis of the behavior of individual components under different operating conditions, facilitating the identification of any errors or inefficiencies. Subsequently, an integrated analysis will be performed, bringing together the various stages of the circuit to ensure a smooth transition between them and identify any undesired interactions. This sequential approach, based on separate simulations and analyses, aims to guarantee an accurate and reliable design, providing a comprehensive overview of the system's operation before its physical implementation. During the course of this design, crucial aspects relating to the specific component choices, operating characteristics, and the effects on the overall circuit efficiency will be explored in depth.

# 2 Procedure

## 2.1 Specifications

The project specifications play a crucial role in determining the design and operation of the power conversion system. Through the analysis of these parameters, it will be possible to understand the specific requirements of the circuit and ensure the fulfillment of the requested conditions.

- Input Voltage: The system must be able to accept an AC input voltage of 110V with a frequency of 60Hz, with an allowed tolerance of  $\pm 10\%$ .
- Output Voltage: The primary objective of the circuit is to convert the AC input voltage into a stable and regulated DC output voltage. The output voltage must be set to 48V with a power of 400W.
- Output Ripple: The presence of low output ripple is essential to ensure a stable and disturbance-free voltage output. The output ripple value is limited to 1%, indicating the need for a high level of precision in voltage regulation to minimize any variations.
- Buck Converter Operating Mode: The buck converter must operate in Continuous Conduction Mode (CCM), meaning it must maintain continuous current conduction through the inductor during the entire switching cycle. This approach ensures accurate regulation of the output voltage and helps maintain high energy efficiency in the system.

- System Efficiency: A key objective is to achieve optimal system efficiency, minimizing losses during power conversion. The design of each stage, from the diode rectifier to the buck converter, must be optimized to guarantee the highest possible yield, allowing the circuit to operate efficiently and sustainably.

The project specifications outline a detailed framework of the requirements and performance demanded of the power conversion system. The design must address each aspect in a targeted manner, ensuring a precise and reliable response to the demands of the application context. The specifications serve as a fundamental guide, orienting design choices and contributing to the achievement of a functional and efficient system.

## 2.2 Approach

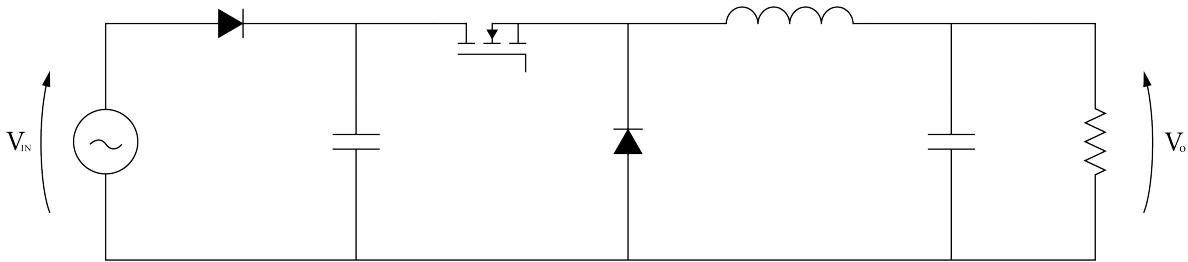


Figura 1: Basic Concept

Figure 1 shows the basic schematic of the circuit, which will be subject to further improvements to optimize its efficiency. For the correct sizing of the circuit, some preliminary considerations must be conducted. Initially, it is observed that the circuit consists of two stages: the rectifier circuit and the step-down (Buck) circuit. We then proceed with the sizing of each stage separately. Based on the provided data, an output power of  $P_{out} = 400 \text{ W}$  is required. Since in the ideal Buck converter  $P_{in} = P_{out}$ , it follows that the input power to the rectifier must also be  $P_{out} = 400 \text{ W}$ . A crucial aspect is represented by the input voltage  $V_{in}$ , which is indicated as  $110 \text{ V} \pm 10\%$ . However, it should be noted that this value represents the RMS voltage, so it is necessary to calculate its peak value to ensure accurate sizing. We obtain  $V_{in} = 110 \text{ V} \times \sqrt{2} \approx 155.56 \text{ V} \pm 10\%$ . Considering the two extreme cases ( $\pm 10\%$ ), we obtain  $V_{in_{max}} = 155.56 \text{ V} + (155.56 \text{ V} \times 10\%) \approx 171.12 \text{ V}$  and  $V_{in_{min}} = 155.56 \text{ V} - (155.56 \text{ V} \times 10\%) \approx 140 \text{ V}$ . Once these aspects have been considered, it will be possible to proceed with the sizing of the individual stages of the circuit.

## 3 Half-Wave Rectifier

### 3.1 Introduction

Half-wave rectifiers constitute a fundamental component in power electronics, finding crucial applications in power supply circuits and electronic devices. These devices perform an essential function: they transform the input energy, in the form of a sinusoidal alternating voltage, into a unidirectional flow of direct current. This results in the elimination of the negative part of the waveform, leaving only the positive half-wave. The rectification process represents the first stage in the transformation of electrical energy from the grid into a more usable form. The rectification operation is fundamental for powering loads such as electronic devices, power supply circuits, and energy conversion systems. The operation of a half-wave rectifier is relatively simple. When the input voltage exceeds a specific threshold, the diode (the main component of the rectifier) turns on, allowing current to pass through the circuit. During the positive half-wave of the input signal, current flows smoothly through the diode, contributing to the creation of a DC voltage at the output terminals. The main characteristics of a half-wave rectifier include its constructive simplicity and low circuit complexity. However, it is important to note that the half-wave rectifier has limitations, such as lower efficiency compared to other more advanced types of rectifiers. In particular, during the negative half-wave of the input signal, the diode is reverse-biased, causing a lack of conduction and the consequent absence of output

voltage. Half-wave rectifiers are often used in situations where the loss of half of the energy during the rectification process is acceptable, such as in powering loads that are not sensitive to voltage variations or in the feedback circuits of some switching power supplies. The output of a half-wave rectifier, having provided a sine wave input, is shown below:

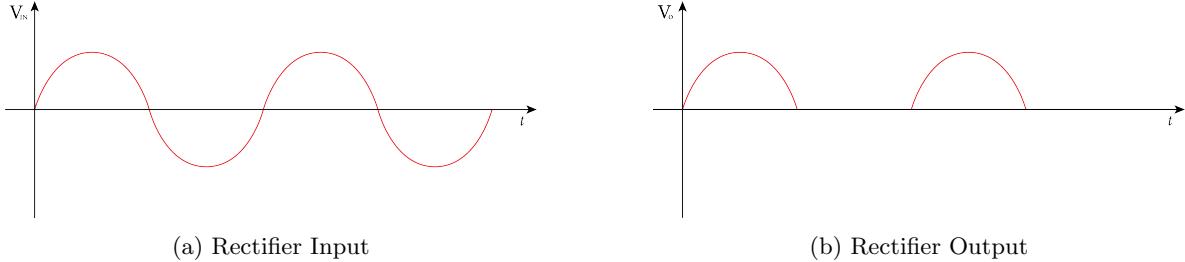


Figura 2: Half-Wave Rectifier Operation

As highlighted in Figure 2 (b), the output waveform is non-linear. In order to mitigate the variations of the voltage  $V_o$ , a capacitor is introduced between the output and the ground (GND). By increasing the output capacitor's capacitance, it is possible to reduce the ripple amplitude. However, this approach leads to an increase in the size, cost, and parasitic effects associated with the component. Consequently, it is essential to proceed with the sizing of the capacitor in a way that effectively balances the requirements for ripple reduction with considerations relating to physical size, cost, and parasitic effects.

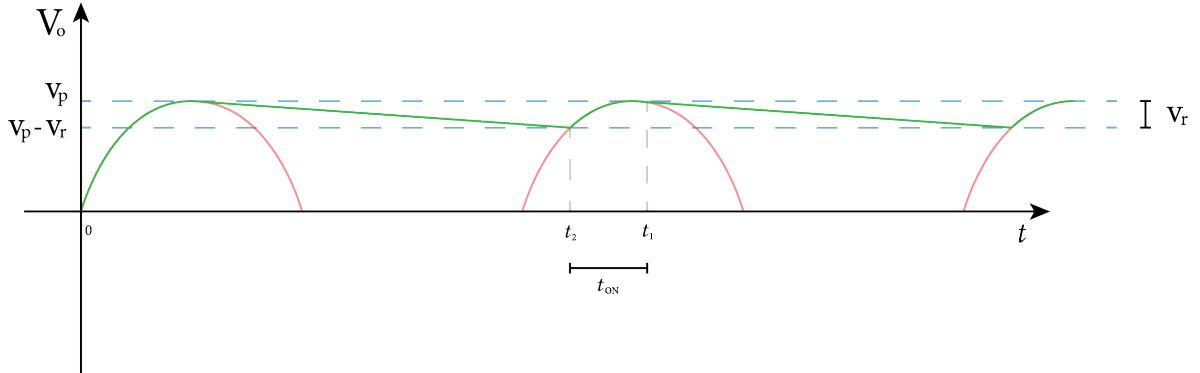


Figura 3: Rectifier Output with Capacitor

### 3.2 Sizing

To size the rectifier, it is necessary to define the desired output ripple. In this case, a ripple of  $\frac{V_f}{V_p} = 5\%$  was chosen, with the objective of keeping the output capacitance within acceptable limits. We consider the worst-case input voltage, which is  $V_{in,min} = 140 \text{ V}$ . Applying the 5% ripple to obtain the worst-case scenario, we get  $V_{in,min} = 140 - (140 \text{ V} \times 5\%) = 133 \text{ V}$ . Furthermore, the voltage drop across the diode must be taken into account. The VS-ETH3007THN3 diode was chosen, which will be discussed later. Analyzing the datasheet, we note the graph that describes the relationship between  $V_f$  and  $I_f$ :

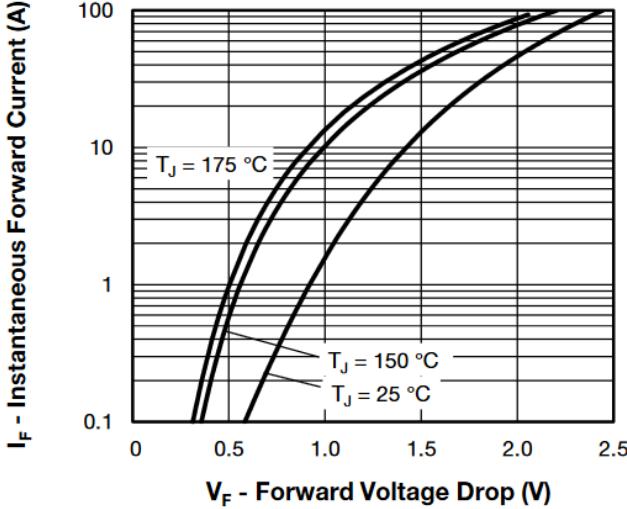


Figura 4:  $V_f$  as a function of  $I_f$  of the VS-ETH3007 diode

It is emphasized that temperature is a parameter that can significantly influence these characteristics. However, in the current context, the consideration of this variable has been omitted. Therefore, we obtain  $V_{in_{min}} = V_{in_{min}} - V_f = 133 \text{ V} - 2.2 \text{ V} = 130.8 \text{ V}$ . At this point, we proceed to calculate the output current and the load resistance, which corresponds to the buck converter:

$$I_o = \frac{P_o}{V_{in_{min}}} = \frac{400 \text{ W}}{130.8 \text{ V}} = 3.05 \text{ A}$$

$$R_o = \frac{V_{in_{min}}}{I_o} = \frac{130.8 \text{ V}}{3.05 \text{ A}} = 42.88 \Omega$$

To calculate the output capacitance, we use the following formula:

$$V_c(t) = V_p \times \exp\left(-\frac{t}{RC}\right) \implies V_p - V_r = V_p \times \exp\left(-\frac{t_2}{RC}\right)$$

$$\frac{t_2}{RC} \ll 1 \implies \exp\left(-\frac{t_2}{RC}\right) \approx 1 - \frac{t_2}{RC}$$

Consequently, we obtain  $V_r = V_p \times \frac{t_2}{RC}$ . Assuming that  $t_2 \approx T$ , the expression can be simplified to  $V_r = \frac{V_p}{f \times RC}$ . We proceed by deriving C:

$$C = \frac{1}{f \times R_o \times \frac{V_r}{V_p}} = \frac{1}{60 \text{ Hz} \times 42.88 \Omega \times 0.05} = 7.7 \text{ mF}$$

We choose a capacitance that is between 20% and 25% in excess of the calculated one. This approach takes into account component tolerances, ensuring a safety margin to guarantee the correct operation of the circuit. Therefore, we obtain  $C \approx 9 \text{ mF}$ . The capacitor must be able to withstand a voltage across its terminals that is approximately double  $V_{in_{max}}$ , again to have a margin, so  $V_c = 350 \text{ V}$ . We proceed by calculating  $V_r$  considering that  $V_p = V_p - V_f = 140 \text{ V} - 2.2 \text{ V} = 137.8 \text{ V}$ .

$$\frac{V_r}{V_p} = 0.05 \implies V_r = \Delta V = 0.05 \times V_p = 0.05 \times 137.8 \text{ V} = 6.89 \text{ V}$$

Having done this, we calculate the diode's  $t_{on}$ , knowing that  $\omega \Delta t$  is the diode's conduction angle:

$$V_p - V_r = V_p - (V_p \times \cos \omega_o - V_p \times \cos \omega \Delta t) \implies V_p - V_r = V_p \times \cos \omega \Delta t$$

Assuming  $\Delta t \ll 1$ , it follows that:

$$\cos \omega \Delta t = 1 - \frac{1}{2} \times \omega^2 \Delta t^2$$

Substituting, we can derive  $\Delta t$  as:

$$\Delta t = t_{on} = \frac{1}{\omega} \times \sqrt{2 \frac{V_r}{V_p}} = \frac{1}{2\pi \times f} \times \sqrt{2 \frac{V_r}{V_p}} = \frac{1}{2\pi \times 60 \text{ Hz}} \times \sqrt{2 \times 0.05} = 839 \mu\text{s}$$

At this point, it is possible to proceed with the calculation of the currents in the circuit.

$$i_{C_{av}} = C \times \frac{\Delta V}{\Delta t} = 7.7 \text{ mF} \times \frac{6.89 \text{ V}}{839 \mu\text{s}} = 63.23 \text{ A}$$

By KCL (Kirchhoff's Current Law), we have  $i_{D_{av}} = i_{C_{av}} + i_{R_{av}}$  with  $i_{R_{av}} = I_o$ , therefore  $i_{D_{av}} = 63.23 \text{ A} + 3.05 \text{ A} = 66.28 \text{ A}$ .  $i_{D_{av}}$  is the average current during the diode conduction period; we now proceed to calculate the average current over the entire period:

$$I_D = f \times (i_{D_{av}} \times t_{on}) = 60 \text{ Hz} \times 66.28 \text{ A} \times 839 \mu\text{s} = 3.33 \text{ A}$$

The peak current on the diode will be:

$$i_{D_{peak}} = 2 \times i_{D_{av}} = 2 \times 66.28 \text{ A} = 132.56 \text{ A}$$

At the output, i.e., at the input of the buck circuit, the voltage exhibits a variation ranging between a minimum value of 130.8 V and a maximum value of 171.12 V.

### 3.3 Simulation

Before proceeding with the simulation, it is necessary to select the components based on the calculated values, in order to create a circuit that is as realistic as possible, taking parasitic effects into account. Regarding the capacitor, due to its large size, an electrolytic capacitor was chosen; specifically, the ALS30A472NP400 model was selected, characterized by a capacitance of  $C = 4700 \mu\text{F}$  and a nominal voltage of 400 V. In order to achieve the desired capacitance of 9 mF, two such capacitors were configured in parallel. This choice is motivated by the desire to limit the equivalent series resistance (ESR), which, being resistive in nature, will be halved by the parallel arrangement. As for the diode, as anticipated, the selection fell on the VS-ETH3007THN3 model, characterized by an average forward current  $I_{f_{av}}$  of 30 A and a maximum repetitive reverse voltage  $V_{rrm}$  equal to 650 V. It should be remembered that the diode will see a reverse voltage across its terminals of about 342 V in the worst case, because when the diode is off, the input has a maximum voltage of -171.12 V and the output has a voltage of +171.12 V due to the capacitor; summing the absolute values gives 342 V. Therefore, it is essential to select a diode with a breakdown voltage greater than the calculated value. Once the components have been chosen, the circuit simulation proceeds. The first step is to import the components: for the capacitor, all characteristics and parasitics are inserted manually, while for the diode, a Vishay Tool is used, which provides all the information, including SPICE models, relating to the chosen component.

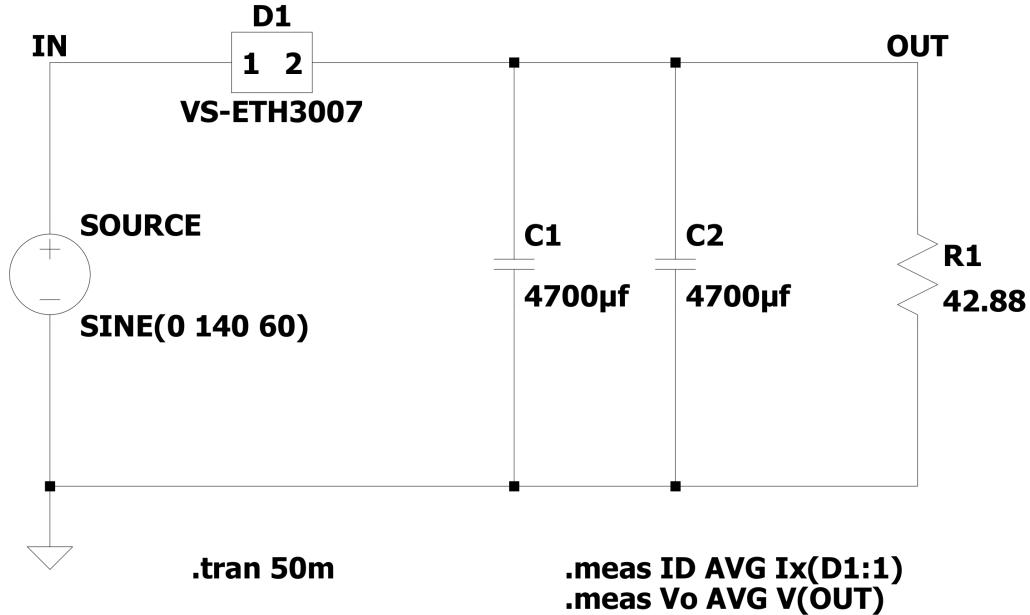


Figura 5: Half-Wave Rectifier Schematic

Figure 5 shows the circuit implemented in LTSpice using real component models to make the simulation more realistic. Reading the .log file produced by SPICE in the case of an input of 140 V, the following results are obtained:

- id:  $\text{AVG}(ix(d1:1))=3.22013$
- vo:  $\text{AVG}(v(out))=135.331$

While in the case of an input of 171.12 V, the following values are recorded:

- id:  $\text{AVG}(ix(d1:1))=3.93975$
- vo:  $\text{AVG}(v(out))=165.685$

The values obtained from the LTSpice simulation, although similar to those calculated previously, may present slight discrepancies due to the presence of parasitic components and the approximations made by the real component models used in the simulation. These differences are common in real-circuit simulations, where accuracy can be influenced by variables such as parasitic capacitances, inductances, and other non-ideal component characteristics. In any case, the simulation provides a more accurate representation of the real circuit conditions.

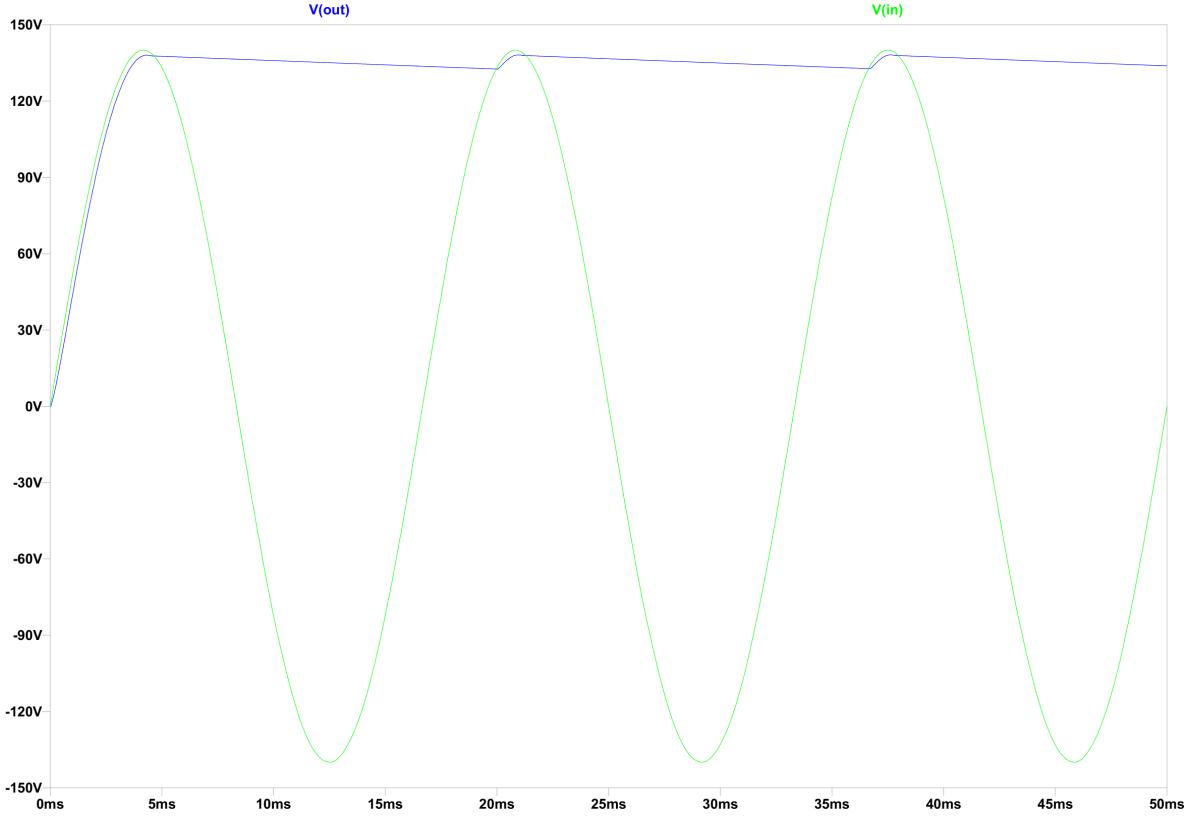


Figura 6: Rectifier Input-Output Relationship

In Figure 7 it can be noted that as the  $V_{in}$  increases, the ripple increases accordingly. Furthermore, it should be noted that the ripple does not perfectly comply with the established 5%. This is attributable to the presence of the capacitor's equivalent series resistance (ESR), which, despite its small magnitude, contributes significantly to the deviation from the specified ripple percentage.

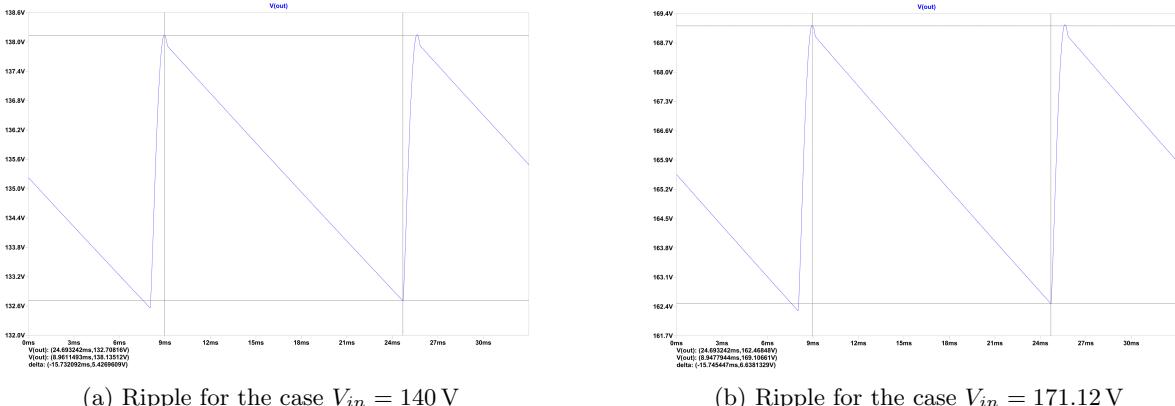


Figura 7: Output Ripple

## 4 Full-Wave Rectifier

### 4.1 Introduction

Full-wave rectifiers constitute an advanced category of devices within power electronics, also suitable for converting alternating voltage into direct voltage. These components play a crucial role in energy supply for many applications, thanks to their ability to utilize both half-waves of the input signal. This

distinctive characteristic contributes to increasing the efficiency of the rectification process, reducing the energy losses encountered in half-wave rectifiers. Unlike half-wave rectifiers, full-wave rectifiers utilize both the positive and negative half-waves of the input signal. This results in greater efficiency. The key component enabling this operation is the diode bridge, a specific arrangement of four diodes designed to handle both signal polarities. The operation of a full-wave rectifier is based on the use of the bridge: during the positive half-wave of the input signal, two diodes conduct current, allowing flow through the circuit. During the negative half-wave, the other two diodes begin conduction, once again allowing current to pass. Despite the advantages, full-wave rectifiers can present some challenges, such as the necessity of a complete diode bridge and the resulting increase in voltage drop. However, their superior performance in terms of efficiency and reliability often justifies the use of this advanced topology.

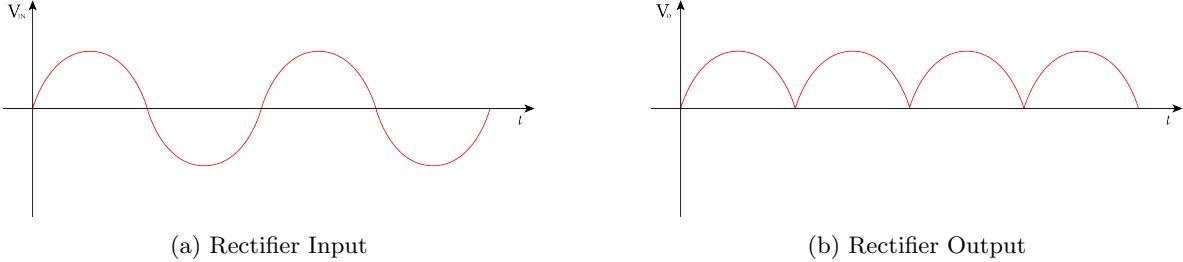


Figura 8: Full-Wave Rectifier Operation

Also in this case, the use of a capacitor is indispensable to linearize the output, with the advantage, however, of having a reduced capacitance since the period is doubled.

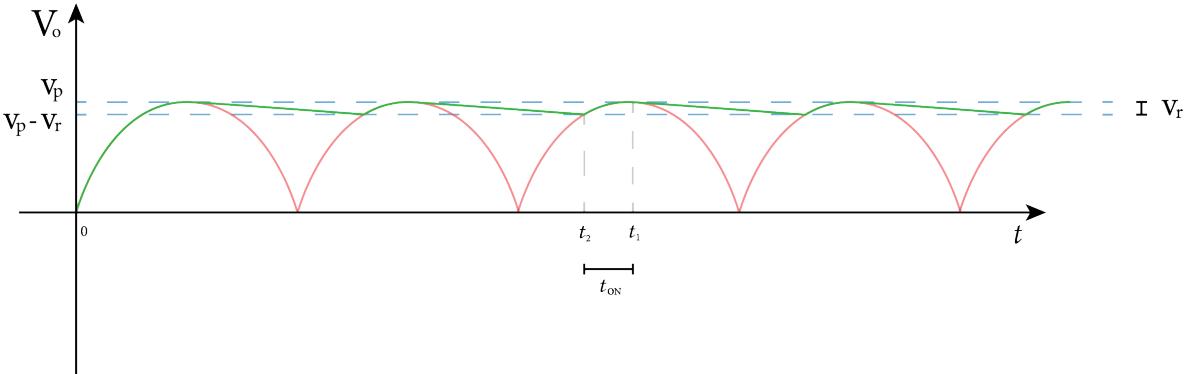


Figura 9: Rectifier Output with Capacitor

As highlighted by the image, for the same output capacitance, it is observed that  $V_r$  assumes a lower value, consequently leading to a smaller voltage ripple. Additionally, a decrease in  $t_{on}$  is noted.

## 4.2 Sizing

For the sizing, the GBUE2560 diode bridge was chosen, which will be described later. It should be noted that, even in this case, it is important to consider the voltage drop, which is lower compared to the previously chosen single diode. Generally, when using a diode bridge, the voltage drop is often higher than with a single diode, as it involves a series of diodes. However, in this specific configuration, a component optimized for the specific application was chosen, characterized by a significantly reduced voltage drop.

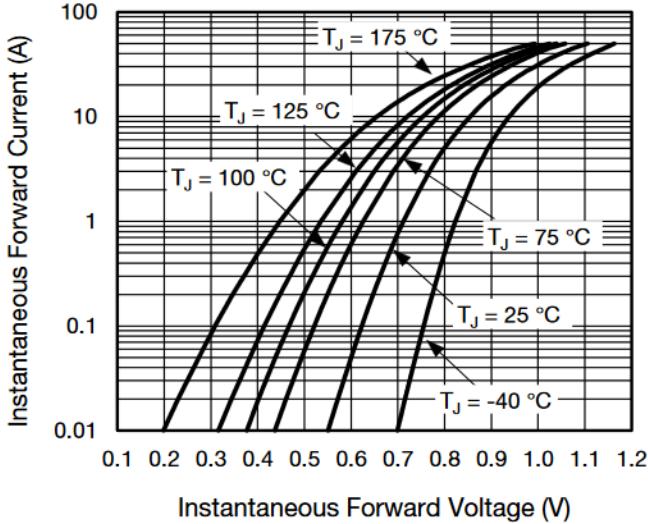


Figura 10:  $V_f$  as a function of  $I_f$  of the GBUE2560 diode bridge

Consulting the datasheet, it is evident that, for the same current and temperature, the GBUE2560 diode has a lower forward voltage ( $V_f$ ) compared to the VS-ETH3007 diode. This characteristic implies an increase in the overall efficiency of the circuit, as a lower voltage drop across the diode translates into less power dissipation in the form of heat. Therefore, the choice of the GBUE2560 contributes to improving the system's efficiency. We proceed to calculate  $V_{in_{min}} = V_{in_{min}} - V_f = 133\text{ V} - 1.1\text{ V} = 131.9\text{ V}$  and consequently calculate the output current and the load resistance:

$$I_o = \frac{P_o}{V_{in_{min}}} = \frac{400\text{ W}}{131.9\text{ V}} = 3.03\text{ A}$$

$$R_o = \frac{V_{in_{min}}}{I_o} = \frac{131.9\text{ V}}{3.03\text{ A}} = 43.53\Omega$$

In this case, it is verified that the period  $T$  is halved, resulting in a doubling of the frequency  $f = f \times 2 = 60\text{ Hz} \times 2 = 120\text{ Hz}$ . Substituting these values into the previously mentioned formula for capacitor sizing, we obtain:

$$C = \frac{1}{f \times R_o \times \frac{V_r}{V_p}} = \frac{1}{120\text{ Hz} \times 43.53\Omega \times 0.05} = 3.82\text{ mF}$$

Again, a capacitance greater by about 20%-25% is chosen, thus obtaining  $C \approx 4.7\text{ mF}$ . The voltage across the capacitor, similar to the previous situation, will be approximately double  $V_{in_{max}}$ .

We proceed to calculate  $t_{on}$ :

$$\Delta t = t_{on} = \frac{1}{2\pi \times f} \times \sqrt{2 \frac{V_r}{V_p}} = \frac{1}{2\pi \times 120\text{ Hz}} \times \sqrt{2 \times 0.05} = 420\text{ }\mu\text{s}$$

We calculate  $V_r$  considering  $V_p = V_p - V_f = 140\text{ V} - 1.1\text{ V} = 138.9\text{ V}$ .

$$\frac{V_r}{V_p} = 0.05 \implies V_r = \Delta V = 0.05 \times V_p = 0.05 \times 138.9\text{ V} = 6.95\text{ V}$$

The current in the capacitor is:

$$i_{C_{av}} = C \times \frac{\Delta V}{\Delta t} = 3.82\text{ mF} \times \frac{6.95\text{ V}}{420\text{ }\mu\text{s}} = 63.21\text{ A}$$

The average diode current over  $t_{on}$  is:

$$i_{D_{av}} = 63.21\text{ A} + 3.03\text{ A} = 66.24\text{ A}$$

The average current over the entire period can be expressed as:

$$I_D = f \times (i_{D_{av}} \times t_{on}) = 120 \text{ Hz} \times 66.24 \text{ A} \times 420 \mu\text{s} = 3.33 \text{ A}$$

The peak current on the diode is calculated as:

$$i_{D_{peak}} = 2 \times i_{D_{av}} = 2 \times 66.24 \text{ A} = 132.48 \text{ A}$$

A decrease in capacitance, a reduction in the conduction time, and a slight increase in currents are observed. This behavior can be attributed to the change in the switching frequency, resulting from the modification of the operating period. The decrease in the capacitor's capacitance, while contributing to a faster transient response, results in a lower conduction period, influencing the amount of charge stored. This reduction in conduction time implies an increase in currents. By using a full-wave rectifier at the output, the voltage will have a variation ranging between 131.9 V and 171.12 V.

### 4.3 Simulation

Also in this case, we proceed to choose components consistent with the values calculated previously. Regarding the capacitor, as previously indicated, we opted again for the use of a parallel mounting in order to leverage the benefits previously illustrated. The chosen capacitor is the ALS80A242KF400 model, characterized by a capacitance of  $C = 2400 \mu\text{F}$  and a maximum voltage of 400 V. The parallel configuration of two of these capacitors provides a total capacitance of  $C = 4800 \mu\text{F}$ , resulting from the limitations of commercial standard values, although slightly higher than the estimated one. However, this variation is acceptable as a slightly higher capacitance is preferable in these applications. In this phase, instead of opting for the selection and formation of a diode bridge via a schematic, we chose to use a pre-packaged diode bridge, as it offers optimal performance. Specifically, the GBUE2560 model was chosen, a diode capable of handling  $I_{f_{av}} = 25 \text{ A}$  and  $V_{rrm} = 600 \text{ V}$ . Also in this selection, attention was paid to choosing a diode bridge with a high breakdown voltage, for the reasons previously illustrated. With the chosen components, we proceed to the simulation phase, during which the components are imported, the circuit is configured, and finally, the simulation is launched to analyze the system's behavior.

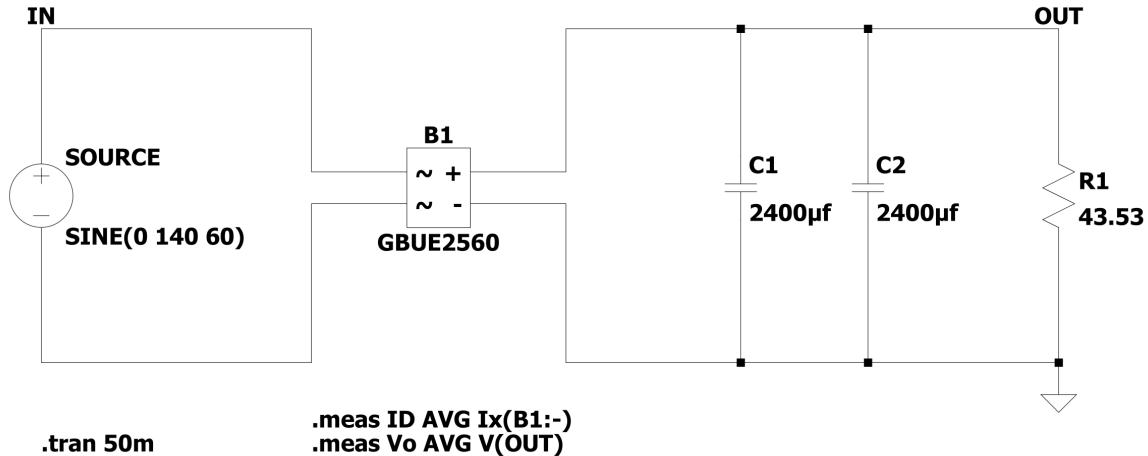


Figura 11: Full-Wave Rectifier Schematic

In Figure 11 shown above, it is evident that the diode bridge is contained within a single package, where the tilde symbol (~) denotes the AC current inputs. At the output, a DC current is observed with a positive component (+) and a negative component (-). The values obtained from the LTSpice simulation, in the case of an input of 140 V and 171.12 V, are reported below. For 140 V input:

- id: AVG(ix(b1:-))=3.23722
- vo: AVG(v(out))=135.664

For 171.12 V input:

- id:  $\text{AVG}(ix(b1:-))=3.96364$
- vo:  $\text{AVG}(v(\text{out}))=166.162$

These results reflect the operating characteristics of the circuit in the two different input scenarios. As previously discussed, the slight discrepancies in the values obtained from the LTSpice simulation compared to theoretical calculations may derive from the presence of parasitic components in the circuit and the approximations introduced by the real component models used in the simulation. These factors can influence the accuracy of the results, but the simulation still provides a more accurate representation of the real circuit conditions, also considering non-ideal effects and the practical characteristics of the components.

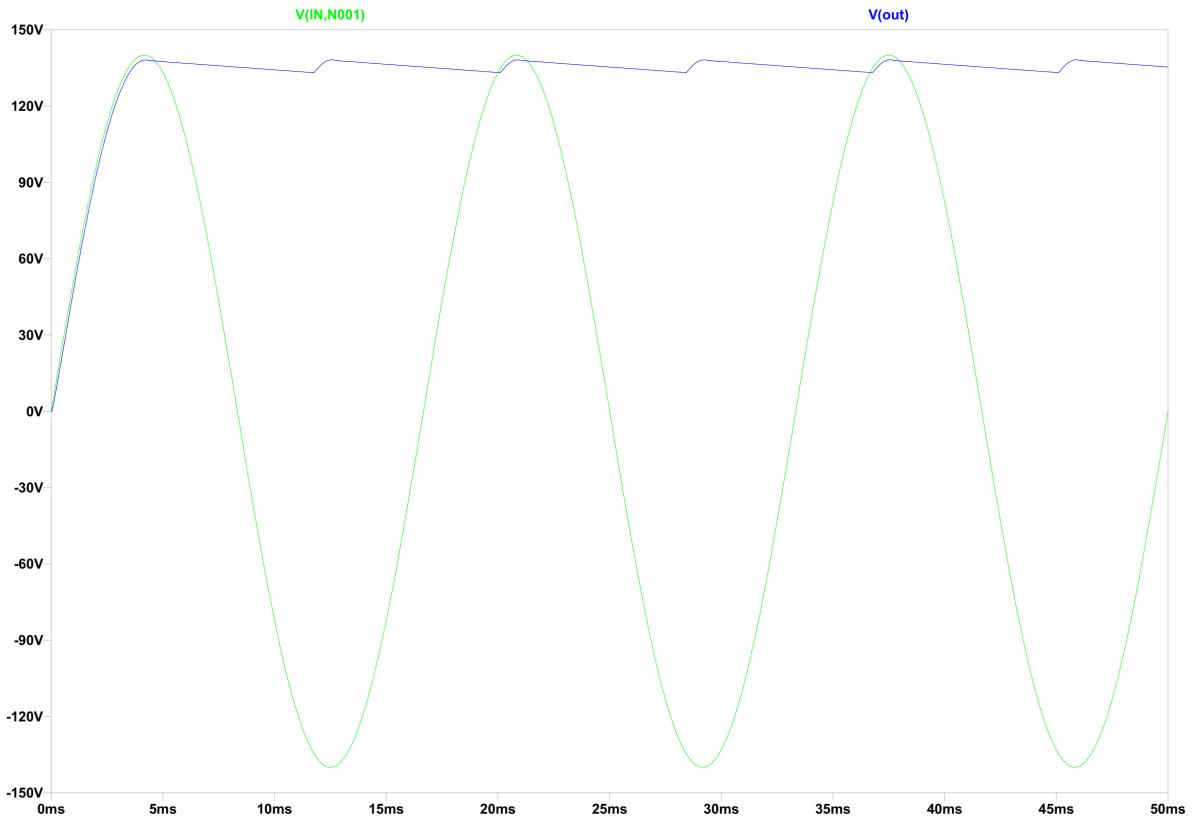


Figura 12: Rectifier Input-Output Relationship

In the image provided, it is evident how the negative half-wave is also utilized, unlike the half-wave rectifier. Consequently, by keeping the ripple level constant, it was possible to reduce the required capacitor capacitance.

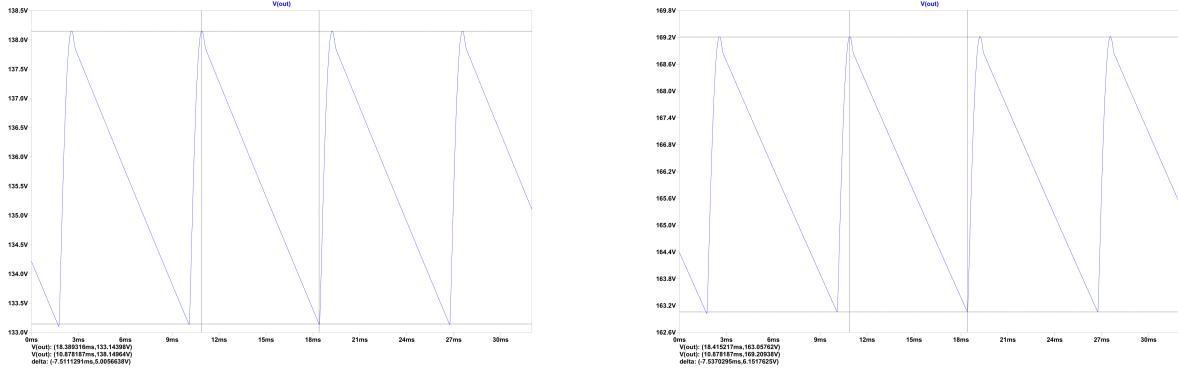


Figura 13: Output Ripple

Also in this case, the ripple is slightly higher than the established 5%. This is due to the resistive parasitics associated with the capacitor.

## 5 Buck Converter

### 5.1 Introduction

A buck converter, also known as a step-down converter, is a type of DC-DC converter used to convert a DC input voltage to a lower voltage level at the output. This device is widely used in electronic power applications to supply regulated voltages to various types of devices. The operation of a buck converter is based on switching principles. During its duty cycle, the buck converter alternates between a conduction state and an off state. When the switching transistor (usually a MOSFET) is conducting, the input voltage is supplied to the inductor, storing magnetic energy. When the transistor is off, the energy stored in the inductor is transferred to the load through output diodes. The main characteristic of a buck converter is its ability to reduce the output voltage compared to the input voltage, while maintaining high efficiency. This makes buck converters ideal for applications where it is necessary to provide a constant and regulated voltage, but with a lower value than the power source. They can be found in a wide range of electronic devices, such as computer power supplies, mobile phone chargers, and many other battery-powered devices. Furthermore, buck converters are often used in switching power supply systems, helping to improve energy efficiency and reduce energy losses compared to traditional linear solutions. Their versatility and efficiency make them a fundamental element in the design of modern electronic power supply systems.

### 5.2 Sizing

Adhering to the project requirements, the desired output is 48 V with a ripple of  $\frac{\Delta V_o}{V_o^2} = 1\%$ . Furthermore, the converter is intended to operate in Continuous Conduction Mode (CCM), where the output inductor is always conducting during the entire switching period. This implies that the current through the inductor never reaches zero during the duty cycle. This operating mode is commonly adopted in buck and boost converters. It should be noted that there are also other conduction modes, such as discontinuous and boundary mode. In this case, the boundary mode will be considered for sizing. It is important to emphasize that the input voltage to the buck,  $V_d$ , will vary between  $131.9 \text{ V} \leq V_d \leq 171.12 \text{ V}$ , considering that it is placed after the full-wave rectifier. To obtain the transfer function, we analyze the integral of the voltage across the inductor, which is known to be zero:

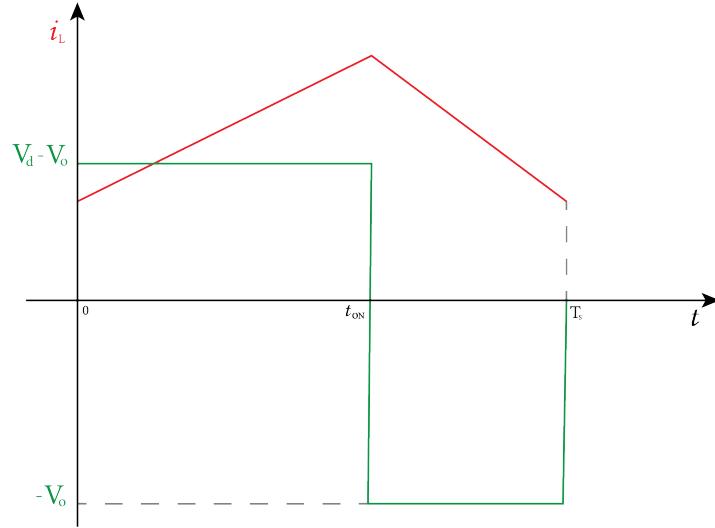


Figura 14: Inductor Voltage and Current

$$\int_0^{T_s} v_L(t) dt = 0 \implies \int_0^{t_{on}} v_L(t) dt + \int_{t_{on}}^{T_s} v_L(t) dt = 0 \implies (V_d - V_o) \times t_{on} - V_o \times (T_s - t_{on}) = 0$$

From which we derive that:

$$V_d \times t_{on} = V_o \times T_s \implies \frac{V_o}{V_d} = \frac{T_{on}}{T_s} = D$$

Since the input power is equal to the output power, we have:

$$P_d = P_o \implies V_d \times I_d = V_o \times I_o$$

$$\frac{V_o}{V_d} = \frac{I_d}{I_o} = D$$

Consequently, since  $V_d$  can vary, two cases are distinguished:

$$D_{min} = \frac{V_o}{V_{d_{max}}} = \frac{48 \text{ V}}{171.12 \text{ V}} = 0.28 \quad D_{max} = \frac{V_o}{V_{d_{min}}} = \frac{48 \text{ V}}{131.9 \text{ V}} = 0.36$$

A switching frequency  $f_s$  of 100 kHz was chosen to determine the MOSFET switching frequency. This intermediate choice considers the trade-off between losses, passive component sizes, and costs. It is important to emphasize that very high frequencies increase losses, while low frequencies lead to bulkier, more expensive passive components and are susceptible to more parasitics. Furthermore, working at high frequencies requires the use of specific drivers and MOSFETs, such as GaN technology MOSFETs. With this choice, a switching period  $T_s = \frac{1}{f_s} = \frac{1}{100 \text{ kHz}} = 10 \mu\text{s}$  is obtained. To ensure that the converter operates in CCM, it is essential that the inductor current is constantly greater than the boundary current  $I_L > I_{LB}$ . We now proceed to calculate  $I_{LB}$ :

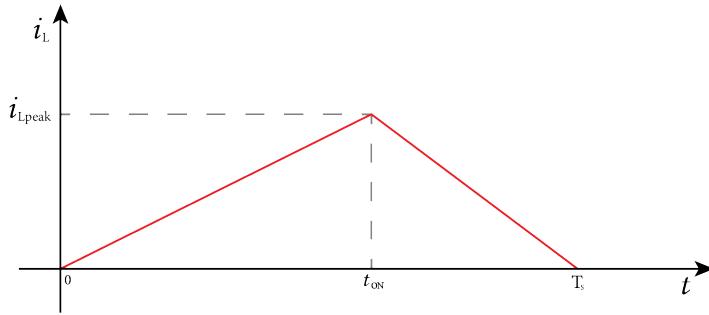


Figura 15: Inductor Current in Boundary Mode

$$I_{LB} = \frac{1}{T_s} \times \int_0^{T_s} i_L(t) dt = \frac{1}{T_s} \times \frac{T_s \times i_{Lpeak}}{2} \implies I_{LB} = \frac{i_{Lpeak}}{2}$$

$$i_{Lpeak} = \frac{1}{L} \times \int_0^{t_{on}} v_L(t) dt = \frac{1}{L} \times (V_d - V_o) \times t_{on} \implies i_{Lpeak} = \frac{(V_d - V_o) \times T_s \times D}{L}$$

Substituting  $i_{Lpeak}$  into  $I_{LB}$  gives:

$$I_{LB} = \frac{(V_d - V_o) \times D \times T_s}{2L}$$

However, considering  $V_o$  constant,  $I_{LB}$  can be reformulated in terms of  $V_o$ :

$$I_{LB} = \frac{V_o \times T_s}{2L} \times (1 - D)$$

Since  $I_L = I_o$ , we have:

$$I_o > I_{LB} = \frac{V_o \times T_s}{2L} \times (1 - D)$$

Knowing that the output power from the converter must be  $P_o = 400 \text{ W}$ , the output current and the load resistance can be derived:

$$P_o = V_o \times I_o \implies I_o = \frac{P_o}{V_o} = \frac{400 \text{ W}}{48 \text{ V}} = 8.33 \text{ A}$$

$$R_L = \frac{V_o}{I_o} = \frac{48 \text{ V}}{8.33 \text{ A}} = 5.76 \Omega$$

Furthermore, it is appropriate to note that to calculate the inductance ( $L$ ), the appropriate Duty Cycle must be determined. For this purpose, we consult the graph illustrated in Figure 16.

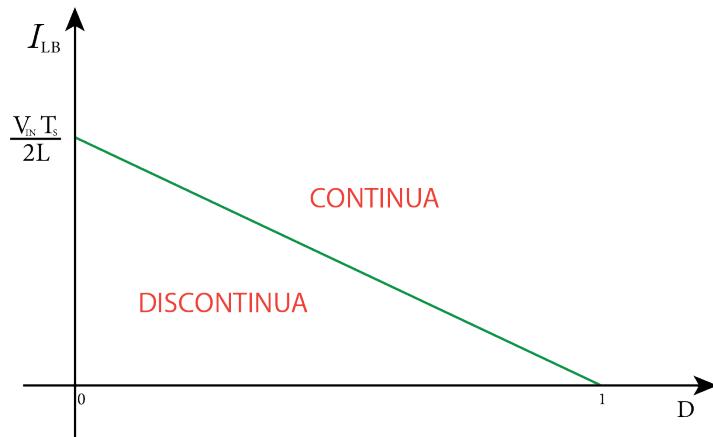


Figura 16: Boundary Output Current as a Function of Duty Cycle

It is observed that  $D_{min}$  represents the worst case. Therefore, we can proceed with the calculation of the inductance:

$$L > \frac{V_o \times T_s}{2 \times I_o} \times (1 - D_{min}) \implies L > \frac{48 \text{ V} \times 10 \mu\text{s}}{2 \times 8.33 \text{ A}} \times (1 - 0.28) \implies L > 20 \mu\text{H}$$

It is good practice to choose an inductance value that is greater than the one found, in order to ensure that the circuit operates in continuous mode even in the worst case. Furthermore, considering component tolerances, a slightly higher value is preferred. An inductance of  $27 \mu\text{H}$  is chosen; being a standard value, it is easily available. The average current across the inductor ( $I_L$ ) corresponds to the output current ( $I_o$ ), and is equal to  $8.33 \text{ A}$ . To calculate the capacitance  $C$ , we observe the current across the inductor. Both areas  $\Delta Q$  are equal, determining the variation of  $\Delta V_o$ , i.e., the ripple, in fact  $\Delta Q = \frac{\Delta V_o}{C}$ . The base of the triangle represented by  $\Delta Q$  is always  $\frac{T_s}{2}$ . With this information, we can proceed with the calculations:

$$\Delta Q = \frac{T_s}{2} \times \frac{\Delta i_L}{2} \times \frac{1}{2} = \frac{T_s \times \Delta i_L}{8}$$

$\Delta i_L$  can be derived as:

$$\Delta i_L = \frac{1}{L} \times \int_0^{T_{on}} v_L(t) dt = \frac{1}{L} \times (V_d - V_o) \times D \times T_s = \frac{V_o \times T_s}{L} \times (1 - D)$$

Substituting everything, we obtain:

$$\frac{\Delta V_o}{V_o} = \frac{(1 - D)}{f_s^2 \times 8LC}$$

Solving for C gives:

$$C = \frac{(1 - D_{min})}{f_s^2 \times 8L \times \frac{\Delta V}{V_o}} = \frac{(1 - 0.28)}{(100 \text{ kHz})^2 \times 8 \times 27 \mu\text{H} \times 0.01} = 33.3 \mu\text{F}$$

Also in this case, a standard capacitance value greater than the obtained result is preferred,  $C = 56 \mu\text{F}$ . Furthermore, the voltage to which the capacitor is subjected, which in this case is  $V_o = 48 \text{ V}$ , must be taken into consideration; consequently, a capacitor capable of withstanding approximately double the voltage is chosen.

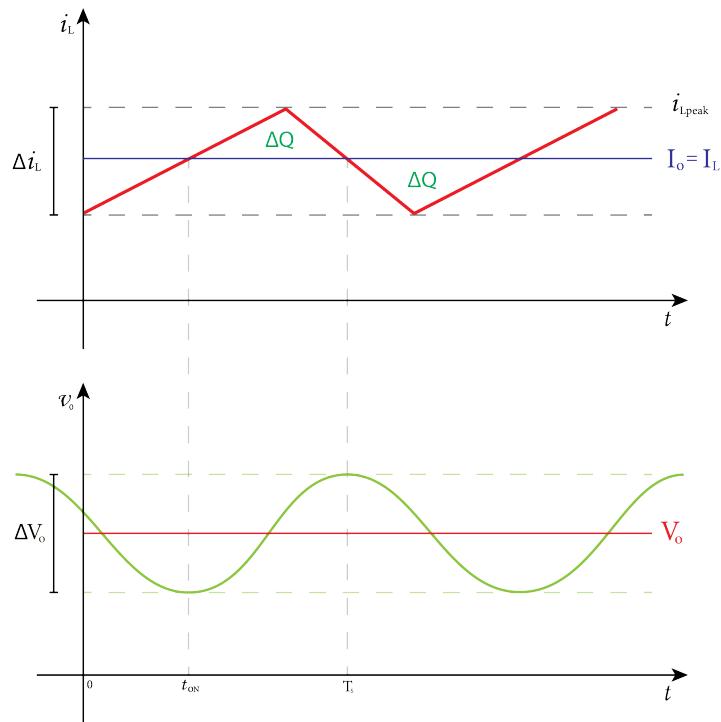


Figura 17: Capacitor

To calculate the peak current  $i_{Lpeak}$ , it is necessary to find  $\Delta i_L$ :

$$\Delta i_L = \frac{V_o \times T_s \times (1 - D_{min})}{L} = \frac{48 \text{ V} \times 10 \mu\text{s} \times (1 - 0.28)}{27 \mu\text{H}} = 12.8 \text{ A}$$

$D_{min}$  is chosen because it represents the worst-case scenario, where the current through the inductor reaches its maximum value. Consequently,  $i_{Lpeak}$  will be:

$$i_{Lpeak} = I_o + \frac{1}{2} \Delta i_L = 8.33 \text{ A} + \frac{1}{2} \times 12.8 \text{ A} = 14.73 \text{ A}$$

As before, an inductor is preferred that can operate with an average current of about double the calculated one, paying attention to choosing an adequate peak current value.

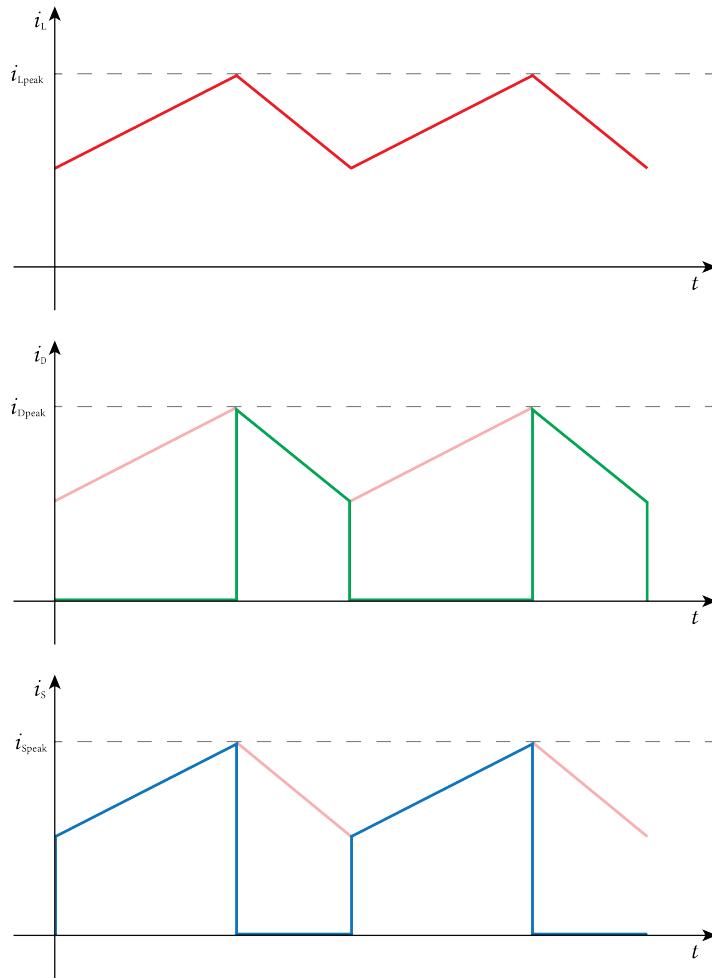


Figura 18: Current on Diode, MOSFET, and Inductor

With reference to Figure 17, it is observed that the peak current of the diode, the MOSFET, and the inductor coincide, assuming the value of 16.97 A. Subsequently, we proceed with the determination of the diode parameters. The breakdown voltage must be greater than  $V_d$ , which in the worst case is 171.12 V. However, to ensure greater robustness, a breakdown voltage of approximately double  $V_d$  is chosen. We then proceed with the calculation of the average current across the diode:

$$I_{D_{av}} = I_o \times (1 - D_{min}) = 8.33 \text{ A} \times (1 - 0.28) = 5.99 \text{ A}$$

We proceed with the evaluation of the average current across the MOSFET, which corresponds to the current delivered by the source:

$$D = \frac{I_d}{I_o} \implies I_d = I_{D_{av}} = I_o \times D_{max} = 8.33 \text{ A} \times 0.36 = 2.99 \text{ A}$$

The MOSFET will be subjected to a maximum voltage equal to  $V_{d_{max}}$ . As previously illustrated, for both the diode and the MOSFET, current and voltage values higher than the calculated ones are chosen in order to guarantee an adequate safety margin.

### 5.3 Simulation

The components chosen for this section are:

- MOSFET: STP34NM60N capable of sustaining a voltage of  $V_{DS} = 600 \text{ V}$  and a continuous current of  $I_D = 31.5 \text{ A}$

- Diode: VS-ETU1506-M3 which has a not too high  $V_f$  and is capable of sustaining a continuous current of  $I_D = 15 \text{ A}$
- Capacitor: EEU-FS2A560L with  $56 \mu\text{F}$   $100 \text{ VDC}$
- Inductor: 2306-V-RC capable of sustaining currents of  $15.6 \text{ A}$

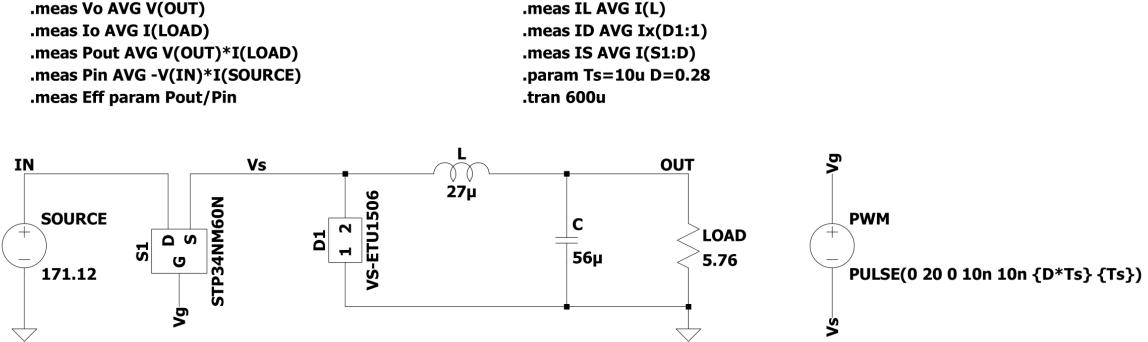


Figura 19: Buck converter schematic

In Figure 19, the presence of a PWM generator is evident, which represents a driver with the function of generating a square wave used to drive the MOSFET. In an attempt to make it realistic, the rise and fall times ( $t_{rise}$  and  $t_{fall}$ ) were configured to  $10 \text{ ns}$ . Furthermore, the period was fixed at  $T_s = 10 \mu\text{s}$ , corresponding to a frequency of  $100 \text{ kHz}$ , and the duty cycle is regulated based on the input voltage. A resistor was inserted at the output to simulate a load, whose value was calculated as  $R_L = \frac{V_o}{I_o} = \frac{48 \text{ V}}{8.33 \text{ A}} = 5.76 \Omega$ . Moreover, as highlighted in the figure, various models were integrated to make the simulation more realistic. Following this, the graph relating to  $V_d$ ,  $V_o$ ,  $I_L$ , and the switching node is presented.

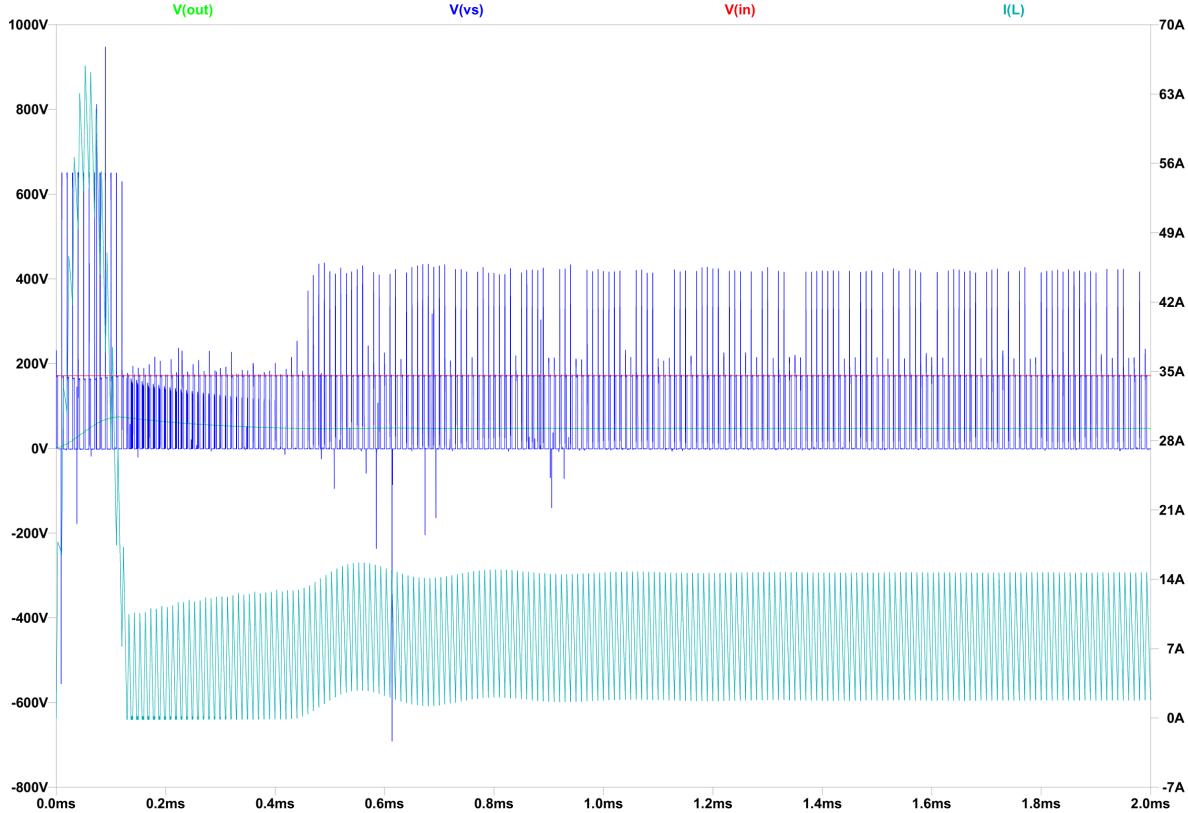


Figura 20:  $V_d$ ,  $V_o$ ,  $I_L$ , and switching node

The manifestation of an initial transient is observable, stemming from the initial conditions of the components, such as capacitors and inductors, which, in the initial phase, are devoid of stored energy and, consequently, tend to absorb a significant amount of current. A plausible approach to mitigate this problem consists in implementing a gradual start-up mode, known as "soft start", and a gradual shutdown procedure, called "soft shutdown". These modes aim to limit the initial and final voltage peaks. In order to exclude the transient from the measurements to minimize potential errors, the simulation was configured such that the program only starts recording data once the circuit has reached a steady state. Furthermore, to automate the measurement process, the program was instructed to automatically calculate certain parameters. A further relevant aspect concerns the spikes present in the switching node, which can cause various problems and compromise the reliability of the circuit. As highlighted in the simulation, especially in the initial phase, peaks reaching 650 V are observed. Therefore, in order to mitigate these effects, components, such as MOSFETs, capable of withstanding voltages and currents higher than those calculated were selected. Subsequently, a circuit known as a "snubber" will be examined, whose purpose is to limit these undesirable effects.

## 5.4 Simulation Results

To conduct a circuit analysis and verify its correct functioning, as previously mentioned, SPICE directives are used, which provide essential support. This approach allows for precise value estimation, delegating the execution of calculations to the program. Below are the commands used:

- vo: AVG(v(out))
- io: AVG(i(load))
- pout: AVG(v(out)\*i(load))
- pin: AVG(-v(in)\*i(source))
- eff: pout/pin

- id: AVG(ix(d1:1))
- il: AVG(i(l))
- is: AVG(ix(s1:d))

LTS spice will produce a .log file containing the calculated values. This document represents a detailed trace of the elaborations carried out during the circuit analysis, providing an exhaustive record of the obtained results. The presence of this file is crucial for an accurate and informed verification of the simulations performed, constituting an indispensable resource for the correct evaluation of the analyzed circuit's performance.

Tabella 1: Results with  $V_{d_{max}}$  and  $D = 0.28$

Quantity	Value	Unit
$v_{out}$	47.0748	V
$i_{load}$	8.17271	A
$p_{out}$	384.786	W
$p_{in}$	436.599	W
$e_{ff}$	0.881327	
$i_d$	6.32082	A
$i_l$	8.93709	A
$i_s$	2.55142	A

In addition to the calculations related to voltage and current values, the circuit's power and efficiency were also determined. It is evident that the expected values do not precisely correspond to those obtained, which can be attributed to losses and parasitic factors associated with the various components. The use of SPICE models allowed for more realistic values to be obtained, unlike what would have happened with ideal components, which would have produced results coinciding with theoretical calculations. In this specific case, the analysis was conducted considering an input of  $V_{d_{max}}$  and a duty cycle  $D = 0.28$ . A similar analysis was performed for the case of an input  $V_{d_{min}}$  and a duty cycle  $D = 0.36$ , producing analogous results.

Tabella 2: Results with  $V_{d_{min}}$  and  $D = 0.36$

Quantity	Value	Unit
$v_{out}$	47.6152	V
$i_{load}$	8.26653	A
$p_{out}$	393.645	W
$p_{in}$	432.405	W
$e_{ff}$	0.910363	
$i_d$	5.58685	A
$i_l$	8.80173	A
$i_s$	3.25116	A

It is observed that in the case with  $V_{d_{min}}$  and  $D = 0.36$ , the circuit efficiency shows a slight increase. To mitigate the problem arising from losses, the duty cycle was adjusted to obtain the desired output values. In the case of  $V_{d_{max}}$ , an increase of 0.55% in the duty cycle, bringing it to  $D = 0.2855$ , yielded results very close to those desired. Similarly, in the case of  $V_{d_{min}}$ , a 0.3% increase was necessary, bringing the duty cycle to  $D = 0.363$ , to obtain acceptable values. The obtained results are reported below:

Tabella 3: Results with  $V(d_{max})$  and  $D = 0.2855$

Quantity	Value	Unit
$v_{out}$	48.076	V
$i_{load}$	8.346 53	A
$p_{out}$	401.329	W
$p_{in}$	457.385	W
$e_{ff}$	0.877 444	
$i_d$	6.565 04	A
$i_l$	9.158 45	A
$i_s$	2.672 89	A

Tabella 4: Results with  $V(d_{min})$  and  $D = 0.363$

Quantity	Value	Unit
$v_{out}$	48.0298	V
$i_{load}$	8.338 51	A
$p_{out}$	400.528	W
$p_{in}$	438.828	W
$e_{ff}$	0.912 721	
$i_d$	5.459 56	A
$i_l$	8.8511	A
$i_s$	3.299 46	A

A further parameter to verify is whether the circuit is operating in Continuous Conduction Mode or not. To perform this check, the current across the inductor must be monitored, which should never reach zero:

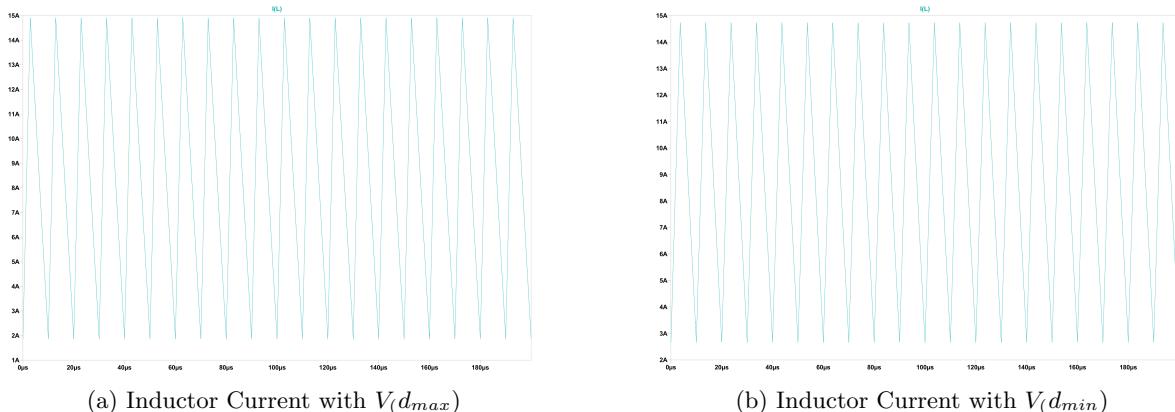


Figura 21: Inductor Current

Figure 21 highlights that with both  $V_{d_{max}}$  and  $V_{d_{min}}$ , the circuit operates in continuous mode, indicating that the inductor has been correctly sized. As a final step, we proceed to verify that the ripple reflects the design parameters. For this purpose, the output oscillations, which must maintain values within a determined range, are observed.

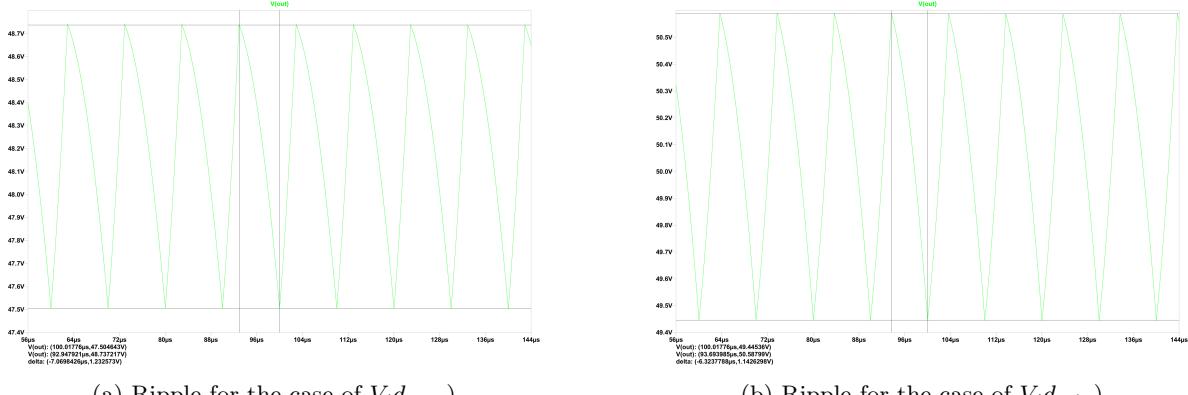


Figura 22: Ripple

In both cases, a ripple of about 1 V is observed, slightly higher than the 1% required by the specifications. This increase is attributable to the presence of the Equivalent Series Resistance (ESR) of the capacitor, which influences the ripple value.

## 6 Snubber

### 6.1 Introduction

The introduction to snubbers in buck converters represents a crucial aspect in the field of power conversion circuit design. Snubbers are protection and optimization devices implemented with the aim of mitigating undesirable effects, such as voltage spikes and oscillations, that can occur during the operation of these converters. The implementation of a snubber in a buck converter aims to limit the overvoltages that can be generated during the switching of power devices, such as MOSFETs. These voltage spikes can arise from the rapid change in current through the switching elements, leading to undesired phenomena that can compromise the integrity of the circuit. In the course of this analysis, an RC snubber type will be introduced, where the combination of a resistor and a capacitor will be employed with the objective of attenuating oscillations and limiting transients. The choice of an RC snubber was found to be effective and simple to implement.

### 6.2 Sizing

The sizing of the RC snubber circuit is performed through simulation, adjusting the parameters based on the simulation results themselves. We proceed by determining the ringing frequency ( $f_R$ ) present at the switching node, which is the frequency of the oscillations caused by the parasitics. It is important to emphasize that the smaller the parasitics, the higher the  $f_R$  will be. From the simulation, it emerged that  $f_R = 400 \text{ MHz}$ . The goal is now to find a capacitance  $C_{P0}$  that, placed between the switching node and ground, manages to halve  $f_R$ . Since there are no preliminary calculations to estimate  $C_{P0}$ , a trial-and-error approach is used. With a capacitance of  $C_{P0} = 56 \text{ pF}$ , the resulting  $f_R = 200 \text{ MHz}$ . Using the formula  $C_{P2} = \frac{C_{P0}}{3}$ , the value of the parasitic capacitance present in the circuit is calculated:  $C_{P2} = \frac{56 \text{ pF}}{3} \approx 18.66 \text{ pF}$ . Subsequently, it is possible to calculate the value of the parasitic inductance  $L_P$ :

$$f_R = \frac{1}{2\pi \times \sqrt{L_P \times C_{P2}}} \implies L_P = \frac{1}{(2\pi \times f_R)^2 \times C_{P2}}$$

$$L_P = \frac{1}{(2\pi \times 200 \text{ MHz})^2 \times 18.66 \text{ pF}} = 33.9 \text{ nH}$$

Following this procedure, the value of the resistance for the RC circuit was calculated using the following expression:

$$Z = \sqrt{\frac{L_P}{C_{P2}}} = \sqrt{\frac{33.9 \text{ nH}}{18.66 \text{ pF}}} = 42.62 \Omega$$

Since  $42.62 \Omega$  does not correspond to a standard resistance value, a higher standard value is chosen, approximating it to  $R = 47 \Omega$ . To determine the snubber circuit capacitance  $C_{SNB}$ , a value between 1 and 8 times that of  $C_{P2}$  is chosen. Increasing the capacitance leads to a more pronounced attenuation of unwanted oscillations during switching transitions, but this increase also translates into greater power dissipation. To achieve an optimal balance,  $C_{SNB} = 4 \times C_{P2} = 4 \times 18.66 \text{ pF} = 74.64 \text{ pF}$  was chosen. The closest standard capacitance value is  $C_{SNB} = 75 \text{ pF}$ .

### 6.3 Simulation

For the simulation, the C322C750JCG5TA capacitor was selected, with a capacitance of  $C = 75 \text{ pF}$  capable of sustaining a voltage of 500 V.

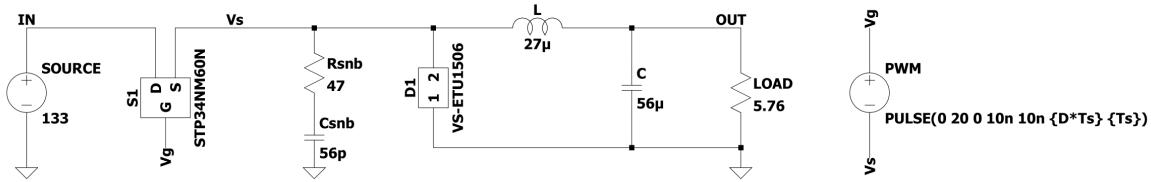


Figura 23: Circuit with Snubber

By observing the switching node, the improvements resulting from the addition of the snubber can be noted. Below are the graphs of the ringing for the case where the input is  $V_{d_{min}}$ . It is important to emphasize that the same benefits are observed also in the case of  $V_{d_{max}}$ .

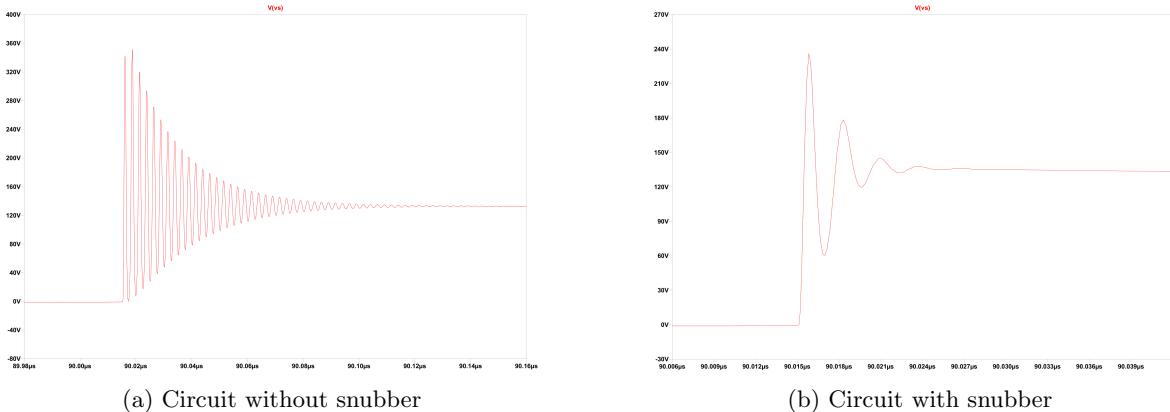


Figura 24: Switching Node

From Figure 24, a significant difference in the ringing phenomena is evident between the case with a snubber and the case without one. In the first scenario (without snubber), the presence of peaks reaching up to 360 V is observed, with a ringing duration of approximately 120 ns. By adding the RC circuit (with snubber), the peaks are reduced to approximately 240 V with a ringing duration of 10 ns. This improvement represents a considerable advantage, contributing to preserving the integrity of the components and offering greater reliability to the circuit.

## 7 Driver and Feedback

### 7.1 Introduction

The driver and feedback play a fundamental role within the buck converter, as they are responsible for the precise and dynamic management of switching transitions, as well as the stabilization of the output voltage in response to variations in load and supply conditions. The driver takes on a crucial role in managing the switching process of the power elements. Its design aims to optimize the system's efficiency by minimizing switching losses and ensuring accurate control of current flow through the circuit. Feedback, on the other hand, represents a key element in maintaining the stability and precision of the output voltage. It involves the constant monitoring of the output voltage and returning this information to the control circuit to regulate the pulse width (duty cycle) in order to maintain the desired output voltage.

### 7.2 Implementation

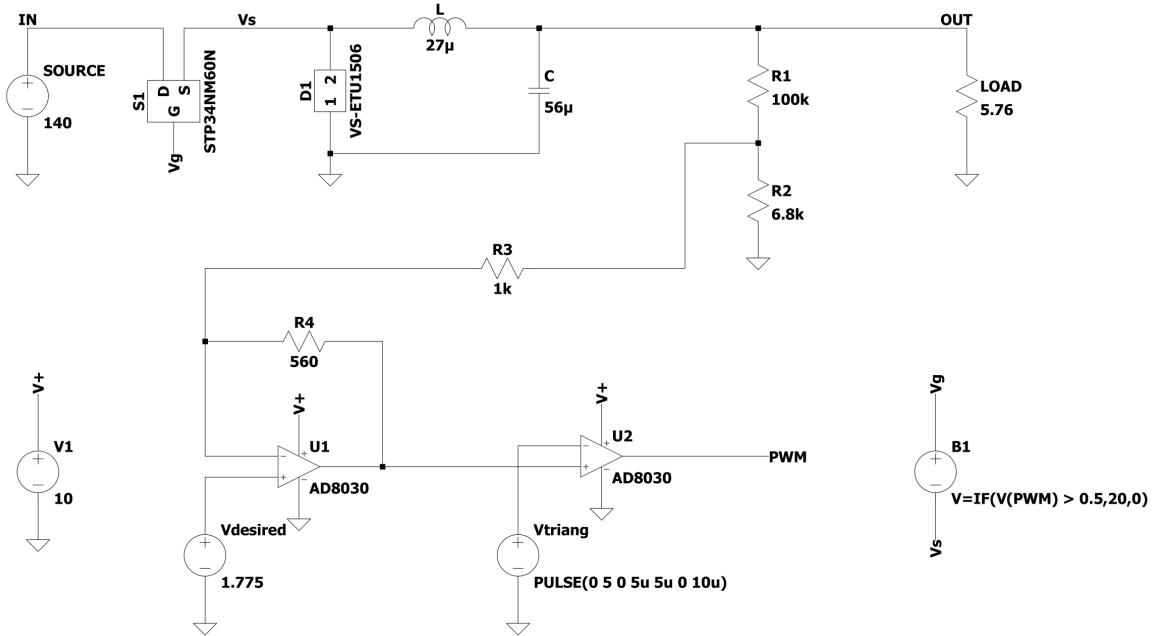


Figura 25: Driver and Feedback Implementation

As can be seen in the image above, external components have been added to the buck in order to ensure correct driving. In particular, the implementation of an output voltage divider is noted, aimed at reducing the voltage level and making it compatible with the feedback and driver logic. It is important to emphasize that the control section operates at low power, therefore it is necessary to adapt the involved voltages. Once the output signal is adapted, it is introduced into an operational amplifier, specifically an AD8030ARZ, designed to operate at high speeds and with low energy consumption. In this initial phase, the output signal is compared with a suitably scaled fixed signal, which represents the desired output voltage ( $V_o = 48 \text{ V}$  in this case). Resistors R3 and R4 are intended to make the system more stable. Subsequently, the resulting signal is subjected to a second operational amplifier, where it is compared with a triangular wave (a sawtooth wave can also be used). The frequency of this wave determines the MOSFET's switching frequency. When the amplitude of the triangular wave exceeds that of the compared signal, the output has a low value; conversely, when the amplitude is lower than the compared signal, a high value is observed at the output. In order to attenuate possible perturbations at the buck converter output, a duty cycle modulation approach is adopted, which dynamically adapts to the operating conditions. Since it is not practical to directly drive the MOSFET through the amplifier's output, a driver consisting of an ideal voltage generator, controlled by a function, is used. The function used follows the logic: " $V = \text{IF}(V(\text{PWM}) > 0.5, 20, 0)$ ". In practical terms, the driver

emulates the PWM waveform generated by the amplifier, adapting it to the MOSFET's specifications. This implies providing an adequate voltage and high current, optimizing the device's switching times.

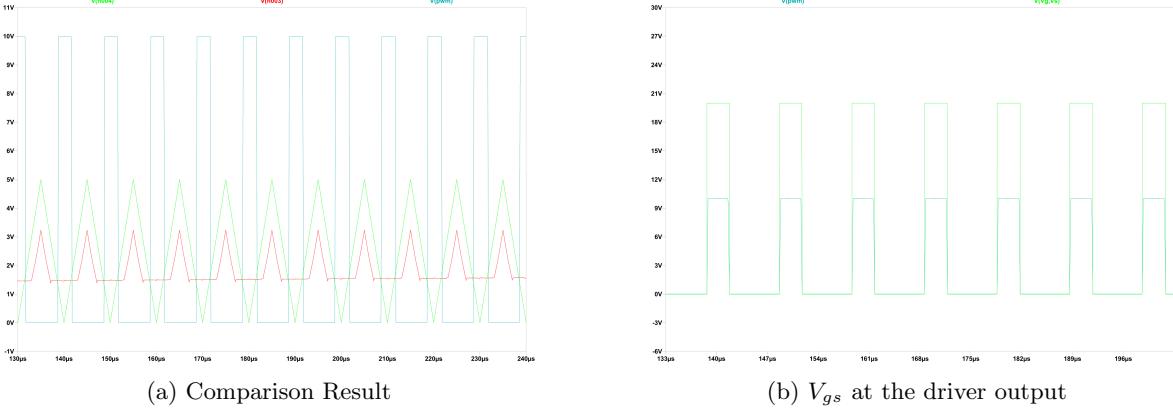


Figura 26: PWM Analysis

## 8 Final Simulation

### 8.1 Introduction

The integration of a rectifier circuit with a subsequent buck converter represents a consolidated design strategy in the field of electronic power systems. The rectifier circuit constitutes the first stage of this configuration. Its main function is to provide a DC voltage, ready to be regulated and adapted to the specific needs of the system. The continuation of this process is represented by the buck converter, the second stage of the circuit. This component, through its ability to step down the input voltage, aims to optimize the energy efficiency of the system and provide a regulated output voltage. The integration of these two stages allows for a complete and coherent solution for the conversion, regulation, and supply of energy in electronic systems. Within this configuration, the DC voltage produced by the rectifier is supplied to the buck converter, which, through its dynamic regulation, adapts the output voltage according to the specific requirements of the load. This integration between the rectifier and the buck converter offers significant advantages in terms of efficiency, stability, and flexibility, contributing to ensuring an optimal power supply for the system as a whole. In order to fully leverage the benefits of this configuration, a simulation of the complete circuit will now be performed. The simulation will provide a detailed overview of the overall system performance and allow for the evaluation of its reliability and efficiency under different operating conditions.

## 8.2 Simulation and Results

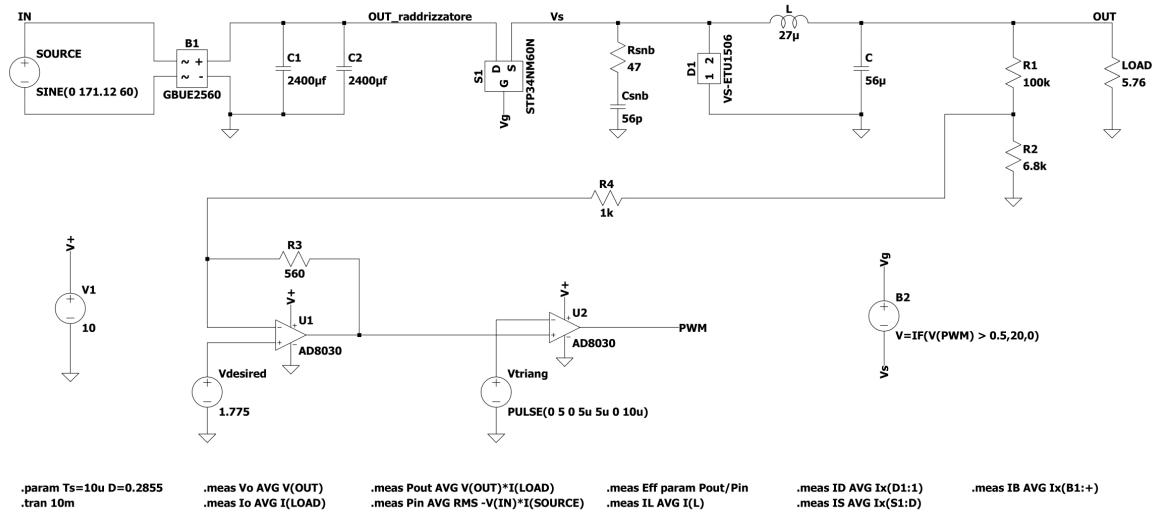


Figura 27: Two-stage converter schematic

Figure 27 illustrates the complete circuit schematic. Proceeding from left to right, the following elements are encountered: a sinusoidal generator of 110 VRMS with a  $\pm 10\%$  variation, a full-wave rectifier with related capacitors, a buck converter with integrated snubber, and finally, the load connected to the output.

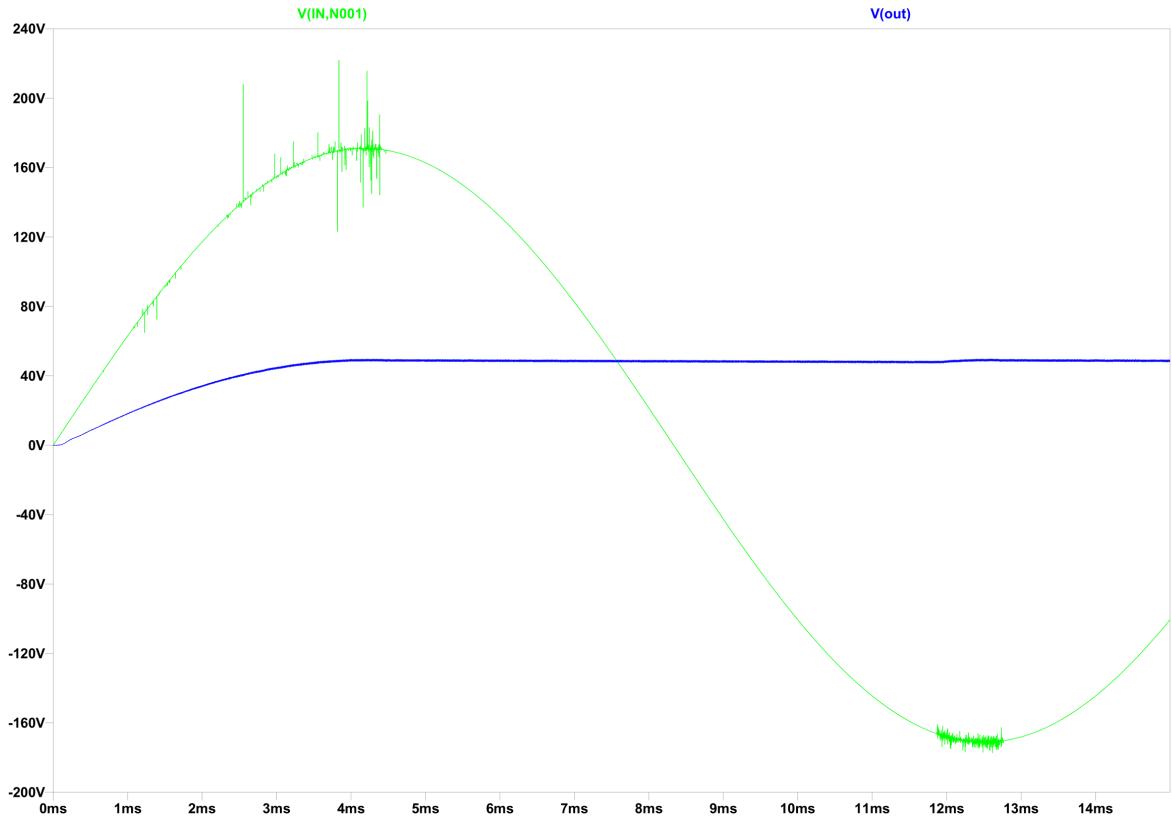


Figura 28: Initial Transient

Starting the simulation, the manifestation of an initial transient can be observed, characterized by the presence of disturbances. These disturbances are attributable to the charging of passive components, as previously discussed, and also affect the AC input voltage. In order to exclude the transient from the acquired values, the simulation is started when the circuit has already reached a steady state. Also in this case, SPICE directives useful for circuit analysis are present. The results obtained are reported below:

Tabella 5: Case  $V_{in} = 140 \text{ V}$

Quantity	Value	Unit
$v_{out}$	48.3879	V
$i_{load}$	8.400 67	A
$i_d$	5.283 07	A
$i_l$	8.387 61	A
$i_s$	3.104 54	A

Tabella 6: Case  $V_{in} = 171.12 \text{ V}$

Quantity	Value	Unit
$v_{out}$	47.0088	V
$i_{load}$	8.161 24	A
$i_d$	5.766 68	A
$i_l$	8.153 39	A
$i_s$	2.386 73	A

Observing the data reported above, it can be seen that the currents and voltages required by the project are respected. By performing a fine adjustment of the buck's duty cycle, a precise output of 48 V can be obtained. Analyzing the inductor current, it is observed that the buck operates in continuous mode in both cases, as previously established.

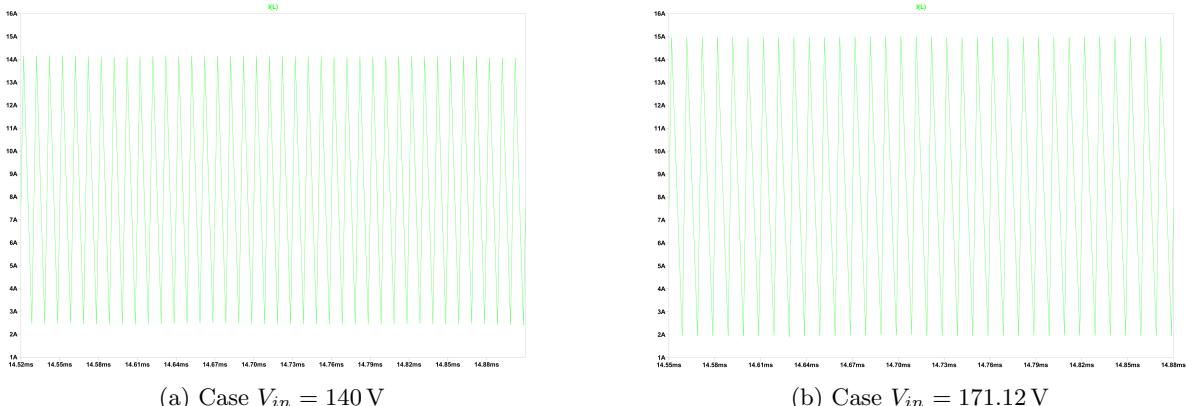


Figura 29: Inductor Current

In the analysis of the output ripple, a value of about 1 V is observed for both cases, which is slightly higher than the 1%, but still considered acceptable. This discrepancy can be attributed to the losses caused by parasitic elements present in the circuit.

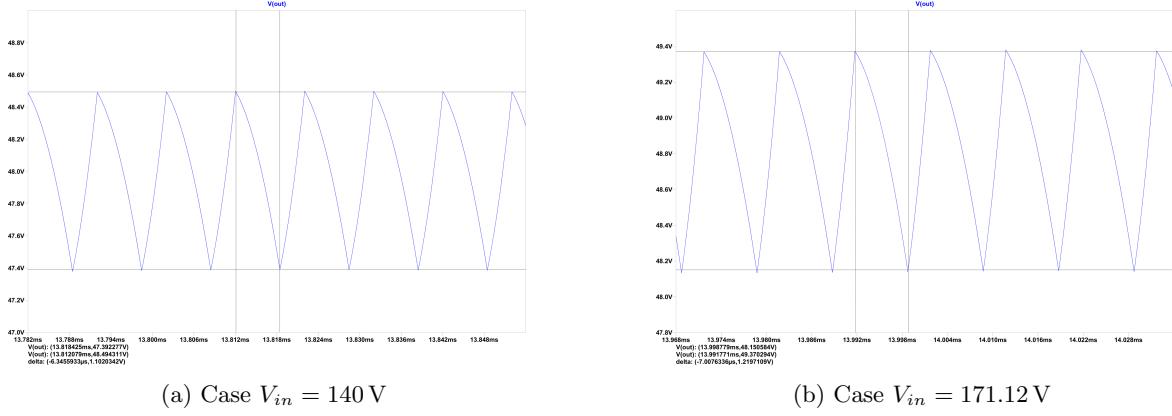


Figura 30: Output Ripple

## 9 Conclusion

In conclusion, this research has addressed in a detailed and in-depth manner the analysis and design of a two-stage circuit, integrating a half-wave rectifier, a full-wave rectifier, a buck converter, and a snubber to optimize the overall performance of the system. In the course of the procedure, clear specifications and a rigorous methodology were established, which guided the entire design process. The accurate sizing of the individual components, supported by detailed simulations, allowed for the evaluation of the effectiveness of each circuit stage in terms of energy efficiency and general performance. The analysis of the half-wave and full-wave rectifiers highlighted the crucial differences between the two configurations, enabling the selection of the solution best suited to the specific needs of the system. The buck converter was successfully designed and optimized, integrating a snubber to improve the management of switching transitions and reduce undesired effects. The final simulations provided a comprehensive overview of the overall circuit performance, confirming the effectiveness of the design choices adopted. The obtained results demonstrated the circuit's ability to meet the required performance specifications, while ensuring optimal energy efficiency. In summary, this research has provided a significant contribution to the understanding and optimization of the analyzed two-stage circuit, offering a complete framework of the design choices and the results obtained. The knowledge acquired can constitute a solid basis for future developments and applications in the field of power electronics.