ATS2823B Datasheet

Version: 1.4

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Revision History

Date	Revision	Description
2015-07-02	1.0	First Release
2015-09-09	1.1	Correct spelling mistakes
2015-10-16	1.2	Update Bluetooth edition and pin description list; Add battery charger parameter list
2016-05-23	1.3	Update pinlist
2016-08-08	1.4	Update register descriptions

1 Introduction

Features

- 104MHz MIPS32 Processor and 180MHz CEVA DSP
- Internal ROM and SPI Flash memory
- Internal RAM for data and program
- Built-in high performance stereo 24 bit input DAC & ADC
- Supports Digital microphones, single-ended Analog microphones and full difference microphone
- Built-in stereo PA for headphone
- Bluetooth V4.2 compatible with Bluetooth V4.1/ V4.1 LE/V4.0/V3.0/ V2.1 + EDR systems
- Bluetooth fast AGC control to improve receiving dynamic range
- Supports AFH to dynamically detect channel quality to improve Bluetooth transmission quality
- Support SD/MMC/eMMC card interface
- Serial Interfaces: UART, SPI
- Infrared Remote controller supported
- Integrated PMU supports multiple low energy states
- Integrated Linear battery charger up to 600mA charging current
- QFN-40 (5mm*5mm, Pitch 0.4mm)

Actions® ATS2823B™ QFN40

Bluetooth Audio Solution

Low Power Solution for
Portable & Wireless Audio Applications
Headphone and Earphone

MIPS + DSP Dual-core Single-chip
Bluetooth V4.2

Revision V1.2

Applications

- Stereo headsets and headphones
- Other Bluetooth audio applications

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1.1 Overview

Actions' ATS2823B is a highly integrated single-chip Bluetooth Audio solution. Targeting at Bluetooth headsets and earphones market, ATS2823B satisfies the market requirements with high performance, low cost and low power consumptions.

ATS2823B adopts MIPS + DSP dual core architecture. Large capacity RAM is embedded to meet different Bluetooth applications. ATS2823B supports decoding Bluetooth A2DP audio and loading sound effects simultaneously, supports Bluetooth handfree calls with dual MIC AEC and noise reduction.

ATS2823B integrates Bluetooth controller support V4.2 and compliant with V4.1/V4.1 LE/V4.0/V3.1/V2.1 Bluetooth specification, and supports dual mode (BR/EDR + Low Energy Controllers). The links in BR/EDR and LE can be active simultaneously.

ATS2823B take special methods at power optimization, especially for various applications scenarios, including sniff, Bluetooth idle, Bluetooth playing and call modes. Embedded PMU supports power optimization and provide long battery life. The competitive advantages of ATS2823B are high music and call qualities with low power and BOM, which lays the foundation for our goal at high-end market. Above all, ATS2823B provides a true "ALL-IN-ONE" solution, making it the ideal choice for highly integrated and optimized Bluetooth audio products.

1.2 Application Diagram

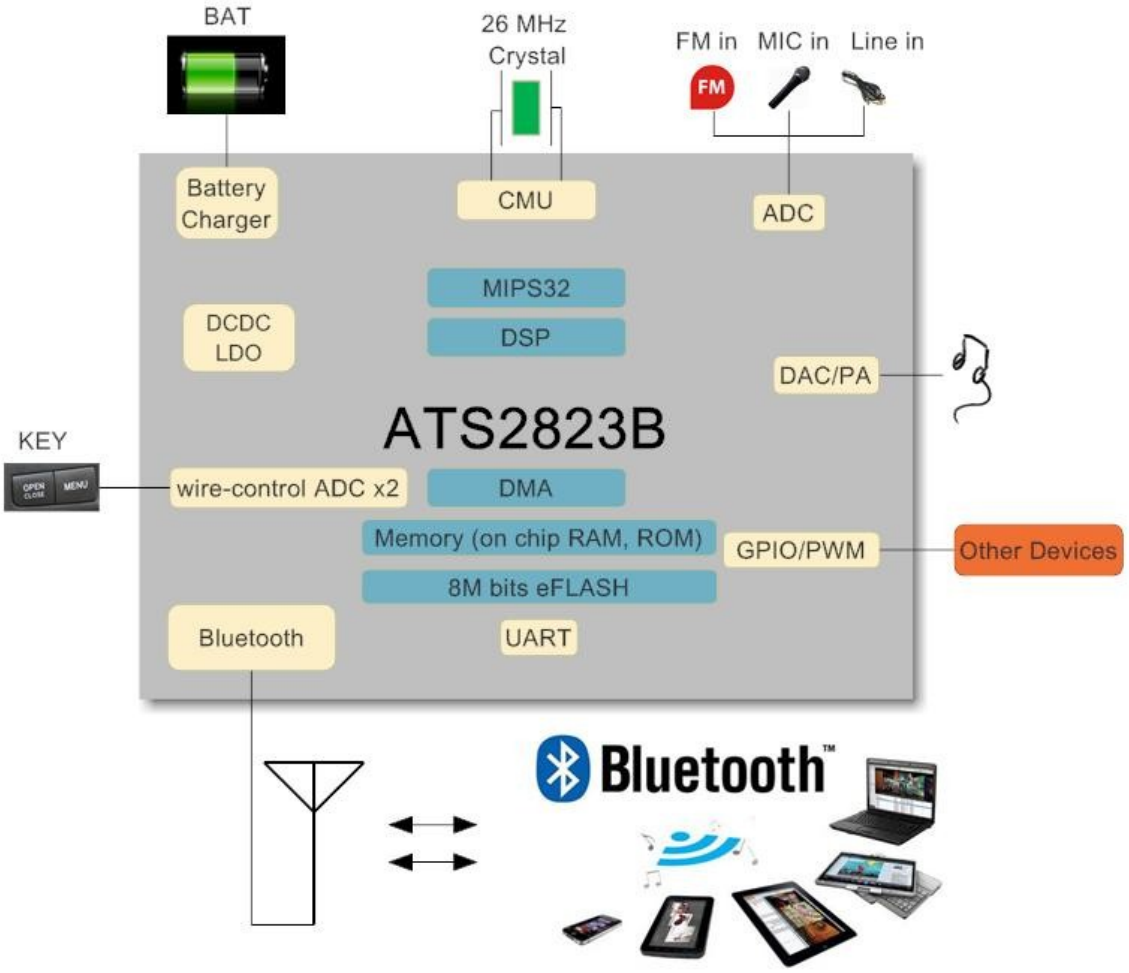

Figure 1-1 ATS2823B Application Diagram

1.3 Detail Features

System

- 104MHz MIPS32 processor Core
- 180MHz CEVA DSP core
- Internal RAM for data and program storage
- Internal 8M bit SPI Flash
- Support 26MHz OSC with on-chip PLL
- Operating voltage: I/O 3.1V, Core 1.2V
- Fully configurable PEQ, up to 14 segments
- Actions' super voice technology for voice connections
- Support for echo cancellation and noise reduction
- Support for wind noise reduction
- Support for packet loss concealment
- Support for multiple sound effect, such as TEQ, MDRC, bass enhancement, virtual surround effects
- Support for voice prompt

Audio

- Built-in stereo 24 bit input sigma-delta DAC, SNR > 98dB, THD <- 87dB
- DAC supports sample rate 8k/12k/11.025k/ 16k/22.05k/24k/32k/44.1/48kHz
- Built-in stereo 20mW PA for headphone. PA output supports traditional mode and direct drive mode (for earphone)
- Built-in stereo 24 bit input sigma-delta ADCs, SNR>90dB, THD<-82dB.
- ADC supports sample rate 8k/12k/11.025k/ 16k/22.05k/24k/32k/44.1k/48kHz
- Supports stereo single-ended input analog or mono full difference input microphone
- Supports Digital microphones and Analog microphones

Physical Interfaces

- Support SD/MMC/eMMC card interface
- A variety of serial controllers supporting SPI, UART

• Package

- QFN-40 (5mm*5mm, Pitch 0.4mm)

Bluetooth

- Support Bluetooth V4.2
- Compatible with Bluetooth V4.1/V4.1 LE/V4.0/V3.0/V2.1 + EDR systems
- Compatible with AVRCP Profile V1.6
- Compatible with A2DP Profile V1.3
- Compatible with HFP Profile V1.7
- Compatible with HSP Profile V1.2
- Supports all packet types in basic rate and enhanced data rate
- Supports SCO/Esco link
- Supports Secure Simple Pairing
- Supports Low Power Mode (Sniff / Sniff Sub-rating / Hold / Park)
- Bluetooth Dual Mode support: Simultaneous LE and BR / EDR
- Supports multiple Low Energy states
- Fast AGC control to improve receiving dynamic range
- Supports AFH to dynamically detect channel quality to improve transmission quality
- Integrated Class1, Class2, and Class 3 PA
- Supports Power / Enhanced Power Control
- Integrated 32K oscillator for power management

Power Management

- Supports Li-Ion battery and 5V power supply
- Energy saving with dynamic power management
- Integrated Linear battery charger
- Integrated DC-DC buck converters, which can be switch to LDO mode
- Linear regulators output VCC, AVCC, BTVCC
- Standby Leakage Current: <1μA (Whole System)
- Low Power Consumption: Typical Sniff Current: 800μA @ Vbat = 3.8V; ACL: < 19mA @ Vbat = 3.8V; SCO: < 21mA@Vbat=3.8V

1.4 Pin Assignment and Descriptions

1.4.1 Pin Assignment

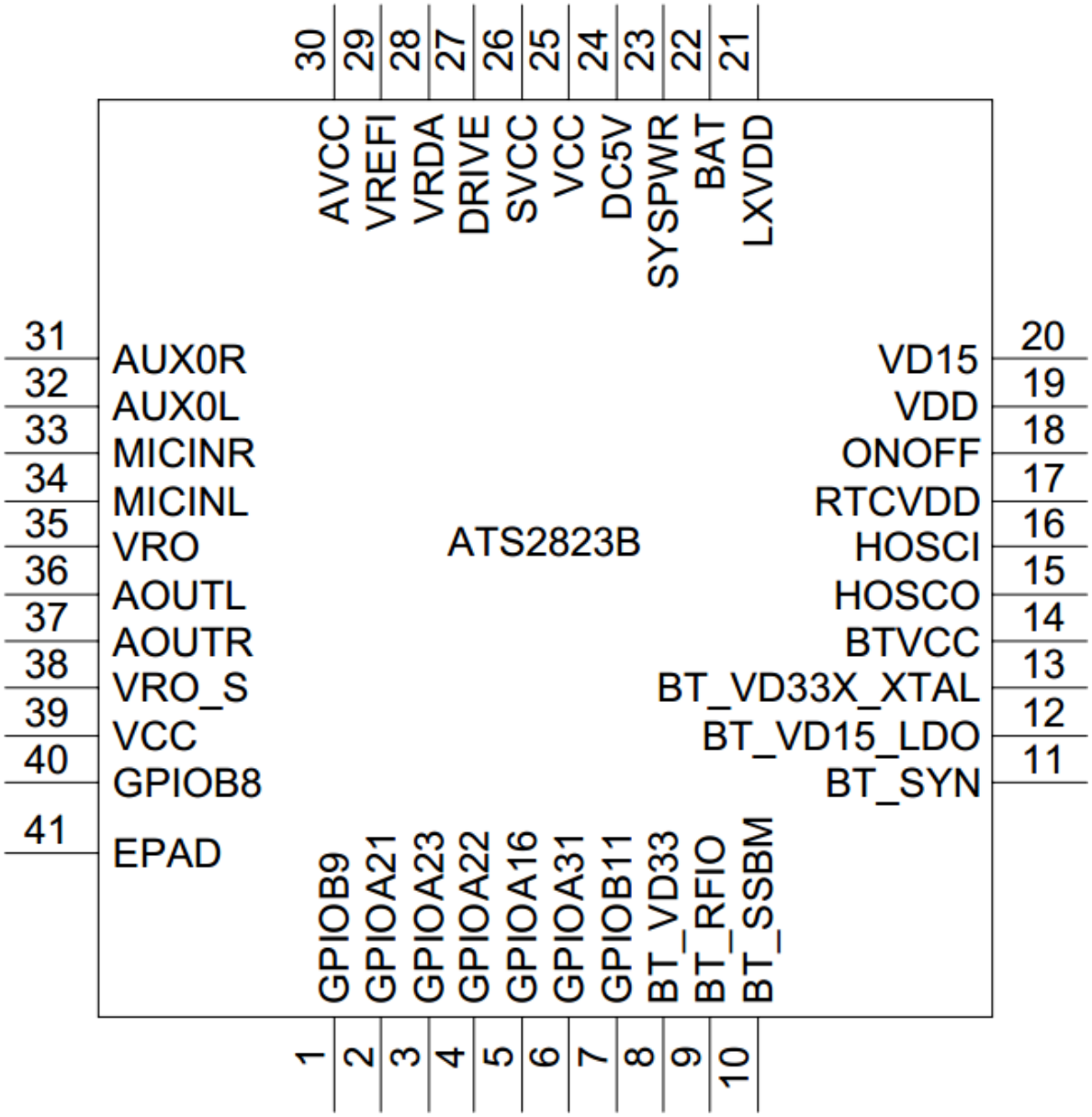

Figure 1-2 ATS2823B (QFN40) Pin Assignment

1.4.2 Pin Description

Table 1-1 ATS2823B Pin Description

Pin No.	Pin Name	Default Function	Function Mux	IO Type	PAD Drive Level	GPIO Initial state	Description
1	GPIOB9	DEJ_TDI	DEJ_TDI/LCD_SEG30/PWM2/TK3	DIO	1,2,3,4,5,6,7,8(2/4/6/8/10/12/14/16mA)	H	Bit9 of General purpose I/O port B
2	GPIOA21	SD_DAT1	SD_DAT1/EM_D9/LCD_D9/LCD_SEG11/UART_RX1/PWM0/TEMPADC/TK0/MEJ_TRST	DIO	1,2,3,4,5,6,7,8(2/4/6/8/10/12/14/16mA)	Z	Bit21 of General purpose I/O port A
3	GPIOA23	SD_DAT3	SD_DAT3/EM_D11/LCD_D11/LCD_SEG13/PWM2/UART_TX1/SD_DAT0/LRADC3/TK7/MEJ_TDO	DIO	1,2,3,4,5,6,7,8(2/4/6/8/10/12/14/16mA)	Z	Bit23 of General purpose I/O port A
4	GPIOA22	SD_DAT2	SD_DAT2/EM_D10/LCD_D10/LCD_SEG12/SIRQ0/IR_RX/PWM1/UART_TX1/LRADC2/SHIELD/MEJ_TCK	DIO	1,2,3,4,5,6,7,8(2/4/6/8/10/12/14/16mA)	Z	Bit22 of General purpose I/O port A
5	GPIOA16	POWER_ON_TRAP	POWER_ON_TRAP/SD_CMD/UART_RX1/LCD_SEG14/MEJ_TMS	DIO	1,2,3,4,5,6,7,8(2/4/6/8/10/12/14/16mA)	Z	Bit16 of General purpose I/O port A
6	GPIOA31	SPI_MOSI	SPI_MOSI/SPI_MISO/LCD_SEG20	DIO	1,2,3,4,5,6,7,8(2/4/6/8/10/12/14/16mA)	Z	Bit31 of General purpose I/O port A
7	GPIOB11	SPI_IO2	SPI_IO2/TWI_SCL/PWM3/SIRQ0/IR_RX/SD_CLK0/MEJ_TDI	DIO	1,2,3,4,5,6,7,8(2/4/6/8/10/12/14/16mA)	Z	Bit11 of General purpose I/O port B
8	BT_VD33			PWR			3.3v voltage
9	BT_RFIO			RF			Bluetooth antenna IO
10	BT_SSBM			PWR			1.2v voltage
11	BT_SYN			PWR			1.2v voltage
12	BT_VD15_LDO			PWR			1.5v voltage
13	BT_VD33X_XTAL			PWR			3.3v voltage
14	BTVCC			PWR			VCC
15	HOSCO			AO			26MHz clock output
16	HOSCI			AI			26MHz clock input

17	RTCVDD			PWR			RTC power
18	ONOFF			PWR			ON/OFF reset signal
19	VDD			PWR			Digital Core power
20	VD15			PWR			1.5v voltage
21	LXVDD			PWR			LXVDD
22	BAT			PWR			Battery Voltage input.
23	SYSPWR			PWR			System power input
24	DC5V			PWR			5.0V Voltage
26	SVCC			PWR			Power for standby
27	DRIVE			AIO			PMOS Drive pin
28	VRDA			PWR			AUDIO power
29	VREFI			PWR			Reference Voltage input
30	AVCC			PWR			Power supply of Analog
31	AUX0R	AUX0R	AUX0R/SpecialIO3	AI/DIO	SIO:5mA	Z	Right channal of AUX0 input
32	AUX0L	AUX0L	AUX0L/SpecialIO2	AI/DIO	SIO:5mA	Z	Left channal of AUX0 input
33	MICINR	MICINR	MICINR/MICINLN/DMICDAT/SpecialIO1	AI/AI/DI/DIO	SIO:5mA	Z	Right channal of Microphone input
34	MICINL	MICINL	MICINL/MICINLP/DMICCLK/SpecialIO0	AI/AI/DO/DIO	SIO:5mA	Z	Left channal of Microphone input
35	VRO	VRO	VRO/SpecialIO7/AOUTLN	AIO/DIO/DIO	1,2,3,4,5,6,7,8(2/4/6/8/10/12/14/16mA)	Z	Direct drive
36	AOUTL	AOUTL	AOUTL/AOUTLP/SpecialIO6	AO/DIO/DIO	1,2,3,4,5,6,7,8(2/4/6/8/10/12/14/16mA)	Z	Left channal of AUDIO Analog output
37	AOUTR	AOUTR	AOUTR/AOUTRP/SpecialIO8	AO/DIO/DIO	1,2,3,4,5,6,7,8(2/4/6/8/10/12/14/16mA)	Z	Right channal of AUDIO Analog output
38	VRO_S	VRO_S	VRO_S/SpecialIO9/AOUTRN	AI/DO/DI	1,2,3,4,5,6,7,8(2/4/6/8/10/12	Z	Direct Drive circuit

				O	/14/16mA)		reference voltage
39	VCC			PWR			Digital power pin
40	GPIOB8	DEJ_TCK	DEJ_TCK/LCD_SEG29/PWM1/TK2	DIO	1,2,3,4,5,6,7,8(2/4/6/8/10/12/14/16mA)	H	Bit8 of General purpose I/O port B
41	EPAD			GND			Exposed pad as ground

Note: H: high level; L:low level; Z: high resistance

2 Bluetooth

- Support Bluetooth V4.2
- Compatible with Bluetooth V4.1/V4.1 LE/V3.0/V2.1 +EDR systems
- Supports all packet types in basic rate and enhanced data rate
- Supports SCO/Esco link
- Supports Secure Simple Pairing
- Supports Low Power Mode (Sniff / Sniff Sub-rating / Hold / Park)
- Bluetooth Dual Mode support: Simultaneous LE and BR / EDR
- Supports multiple Low Energy states
- Fast AGC control to improve receiving dynamic range
- Supports AFH to dynamically detect channel quality to improve transmission quality
- Integrated Class1, Class2, and Class 3 PA
- Supports Power / Enhanced Power Control
- Integrated 32K oscillator for power management

Performance

- Bluetooth transmitting power: -20dBm~10dBm
- Bluetooth receiving sensitivity: -93dBm

3 Processor Core

- 104MHz MIPS32 processor Core
- 32-bit Address and Data Paths
- MIPS32-Compatible Instruction Set
- MIPS32 Enhanced Architecture (Release 2) Features
- MIPS16e™ Code Compression
- Enhanced JTAG (EJTAG) Controller

4 DSP Core

Audio Configuration Features set

- High code compactness
- All instructions can be conditional:
  - Conditional execution
  - Reduces cycle count and code size on control and overhead code
- Computational units:
  - One 32-bit x 32-bit Multiply-and-Accumulate (MAC) using 72-bit product
  - One 32-bit x 16-bit MAC using 72-bit product
  - One 32-bit x 32-bit MAC unit with automatic scaling
  - One 32-bit x 16-bit MAC unit with automatic scaling
  - One 36-bit arithmetic unit
  - One 36-bit logical unit
  - One 36-bit bit-manipulation unit, including a full barrel shifter and an exponent unit
  - Four 36-bit accumulators
  - Fully programmable product post-shifter for product scaling
- 32-bit Scalar (SC) unit for integer operations

- Unaligned memory access for load and store operations

5 Memory Controller

- Full synchronous design with operation clock rate up to 104MHz.
- It is accessible for all the RAM blocks through DMA0/1/2/3/4/5
- It is accessible for all the RAM blocks through DSP's data bus and program bus.
- It is accessible for all the RAM and ROM block through MIPS' data bus and program bus.
- The hardware code replace mechanism can fix up to 4 instructions at the same time.
- The page miss control mechanism can support 22 different pages at the same time.

6 DMA Controller

6.1 Features

- DMA transmission is independent with the CPU and DSP.
- Support memory-to-memory, memory-to-peripheral, and peripheral-to-memory transmission.
- 6-channel DMA
  - 5-channel ordinary DMA, including DMA0, DMA1, DMA2, DMA3, and DMA4, supports for transmission in burst 8 mode.
  - 1-channel special DMA (DMA5), supports for transmission in single mode.
  - Only one of the six DMA channels can transfer data at the same time.
- DMA0/DMA1/DMA2/DMA3/DMA4 transmission can be triggered on the occurrence of selected events as following:
  - SPI TX DRQ
  - SPI RX DRQ
  - UART TX DRQ
  - UART RX DRQ
  - ADC DRQ
  - SD/MMC DRQ
  - DAC DRQ
- DMA5 transmission can only be triggered by UART RX DRQ.
- Each channel can send two interrupts to the CPU on completion of certain operational events as following:
  - DMA5HFIP
  - DMA4HFIP
  - DMA3HFIP
  - DMA2HFIP
  - DMA1HFIP
  - DMA0HFIP
  - DMA5TCIP
  - DMA4TCIP
  - DMA3TCIP
  - DMA2TCIP
  - DMA1TCIP
  - DMA0TCIP
- Transmission width includes 8-bit, 16-bit, 24-bit, 32-bit, and 64-bit, which is determined by DMA transmission type as following:

- 8-bit: SPI, UART, ADC and DAC
- 16-bit: ADC and DAC
- 24-bit: ADC and DAC
- 32-bit: memory, SPI and SD/MMC
- 64-bit: memory

6.2 Memory and Peripheral Access Description

6.2.1 Access Peripheral FIFO

The peripherals that can be accessed by DMA are shown as following:

Table 6-1 Accessible Peripherals FIFO for DMA

FIFO Type	FIFO Width
SPI TX FIFO	32
SPI RX FIFO	32
UART TX FIFO	8
UART RX FIFO	8
SD/MMC FIFO	32
DAC TX FIFO0	24
DAC TX FIFO1	24
ADC FIFO	24

6.2.2 DMA channel priority

The DMA can access the memory block, once the DMA obtains a highest priority and the DMA channel occupies the DMA bus according to the following internal priority table of DMA channels. The possible combinations of priority of each DMA channel are listed below:

Table 6-2 Priority of Each DMA Channel

Priority / Channel Combinations	Priority0 (highest)	Priority1	Priorit2	Priority3	Priority4	Priority5 (lowest)
0	DMA5	DMA0	DMA1	DMA2	DMA3	DMA4
1	DMA0	DMA5	DMA1	DMA2	DMA3	DMA4
2	DMA0	DMA1	DMA5	DMA2	DMA3	DMA4
3	DMA0	DMA1	DMA2	DMA5	DMA3	DMA4
4	DMA0	DMA1	DMA2	DMA3	DMA5	DMA4
5	DMA0	DMA1	DMA2	DMA4	DMA4	DMA5

6.3 DMA Register List

Table 6-3 DMA Control Group Base Address

Name	Physical Base Address	KSEG1 Base Address
DMAController	0xC00C0000	0xC00C0000

Table 6-4 DMA Controller Register List

Offset	Register Name	Description
0x00000000	DMAPriority	DMA priority register
0x00000004	DMAIP	DMA interrupt pending register
0x00000008	DMAIE	DMA interrupt enable register
0x00000010	DMA0CTL	DMA0 control register
0x00000014	DMA0SADDR0	DMA0 source address register 0
0x00000018	DMA0SADDR1	DMA0 source address register 1

0x0000001C	DMA0DADDR0	DMA0 destination address register 0
0x00000020	DMA0DADDR1	DMA0 destination address register 1
0x00000024	DMA0FrameLen	DMA0 frame length register
0x00000028	DMA1CTL	DMA1 control register
0x0000002C	DMA1SADDR0	DMA1 source address register 0
0x00000030	DMA1SADDR1	DMA1 source address register 1
0x00000034	DMA1DADDR0	DMA1 destination address register 0
0x00000038	DMA1DADDR1	DMA1 destination address register 1
0x0000003C	DMA1FrameLen	DMA1 frame length register
0x00000040	DMA2CTL	DMA2 control register
0x00000044	DMA2SADDR0	DMA2 source address register 0
0x00000048	DMA2SADDR1	DMA2 source address register 1
0x0000004C	DMA2DADDR0	DMA2 destination address register 0
0x00000050	DMA2DADDR1	DMA2 destination address register 1
0x00000054	DMA2FrameLen	DMA2 frame length register
0x00000058	DMA3CTL	DMA3 control register
0x0000005C	DMA3SADDR0	DMA3 source address register 0
0x00000060	DMA3SADDR1	DMA3 source address register 1
0x00000064	DMA3DADDR0	DMA3 destination address register 0
0x00000068	DMA3DADDR1	DMA3 destination address register 1
0x0000006C	DMA3FrameLen	DMA3 frame length register
0x00000070	DMA4CTL	DMA4 control register
0x00000074	DMA4SADDR0	DMA4 source address register 0
0x00000078	DMA4SADDR1	DMA4 source address register 1
0x0000007C	DMA4DADDR0	DMA4 destination address register 0
0x00000080	DMA4DADDR1	DMA4 destination address register 1
0x00000084	DMA4FrameLen	DMA4 frame length register
0x00000088	DMA5CTL	DMA5 control register
0x0000008C	DMA5DADDR	DMA5 destination address register
0x00000090	DMA5FrameLen	DMA5 frame length register
0x00000094	DMA5CONT	DMA5 counter register

6.4 DMA Register Description

6.4.1 DMAPriority

DMAPriority (DMA Priority Register, offset = 0x00000000)

Bits	Name	Description	Access	Reset
31:3	-	Reserved	-	-
2:0	PRIORITYTAB	DMA Priority table : 5'd0:DMA5>DMA0>DMA1>DMA2>DMA3>DMA4 5'd1:DMA0>DMA5>DMA1>DMA2>DMA3>DMA4 5'd2:DMA0>DMA1>DMA5>DMA2>DMA3>DMA4 5'd3:DMA0>DMA1>DMA2>DMA5>DMA3>DMA4 5'd4:DMA0>DMA1>DMA2>DMA3>DMA5>DMA4 5'd5:DMA0>DMA1>DMA2>DMA3>DMA4>DMA5 Others:DMA5>DMA0>DMA1>DMA2>DMA3>DMA4	RW	0x0

6.4.2 DMAIP

DMAIP (DMA Interrupt Pending Register, offset = 0x00000004)

Bits	Name	Description	Access	Reset
31:14	-	Reserved	-	-
13	DMA5HFIP	DMA5 Half Transmission IRQ Pending This bit can be written '1' to clear. (1)	RW	0x0
12	DMA4HFIP	DMA4 Half Transmission IRQ Pending This bit can be written '1' to clear. (1)	RW	0x0
11	DMA3HFIP	DMA3 Half Transmission IRQ Pending This bit can be written '1' to clear. (1)	RW	0x0
10	DMA2HFIP	DMA2 Half Transmission IRQ Pending This bit can be written '1' to clear. (1)	RW	0x0
9	DMA1HFIP	DMA1 Half Transmission IRQ Pending This bit can be written '1' to clear. (1)	RW	0x0
8	DMA0HFIP	DMA0 Half Transmission IRQ Pending This bit can be written '1' to clear. (1)	RW	0x0
7:6	-	Reserved	-	-
5	DMA5TCIP	DMA5 Transmission Complete IRQ Pending This bit can be written '1' to clear.	RW	0x0
4	DMA4TCIP	DMA4 Transmission Complete IRQ Pending This bit can be written '1' to clear.	RW	0x0
3	DMA3TCIP	DMA3 Transmission Complete IRQ Pending This bit can be written '1' to clear.	RW	0x0
2	DMA2TCIP	DMA2 Transmission Complete IRQ Pending This bit can be written '1' to clear.	RW	0x0
1	DMA1TCIP	DMA1 Transmission Complete IRQ Pending This bit can be written '1' to clear.	RW	0x0
0	DMA0TCIP	DMA0 Transmission Complete IRQ Pending This bit can be written '1' to clear.	RW	0x0

6.4.3 DMAIE

DMAIE (DMA Interrupt Enable Register, offset = 0x00000008)

Bits	Name	Description	Access	Reset
31:14	-	Reserved	-	-
13	DMA5HFIE	DMA5 Half Transmission Complete IRQ enable: 0: Disable Half Transmission Complete interrupt; 1: Enable Half Transmission Complete interrupt.	RW	0x0
12	DMA4HFIE	DMA4 Half Transmission Complete IRQ enable: 0: Disable Half Transmission Complete interrupt; 1: Enable Half Transmission Complete interrupt.	RW	0x0
11	DMA3HFIE	DMA3 Half Transmission Complete IRQ enable: 0: Disable Half Transmission Complete interrupt; 1: Enable Half Transmission Complete interrupt.	RW	0x0
10	DMA2HFIE	DMA2 Half Transmission Complete IRQ enable: 0: Disable Half Transmission Complete interrupt; 1: Enable Half Transmission Complete interrupt.	RW	0x0
9	DMA1HFIE	DMA1 Half Transmission Complete IRQ enable: 0: Disable Half Transmission Complete interrupt; 1: Enable Half Transmission Complete interrupt.	RW	0x0
8	DMA0HFIE	DMA0 Half Transmission Complete IRQ enable: 0: Disable Half Transmission Complete interrupt; 1: Enable Half Transmission Complete interrupt.	RW	0x0
6:7	-	Reserved	-	-
5	DMA5TCIE	DMA5 Transmission Complete IRQ Enable:	RW	0x0

		0: disable DMA5 Transmission Complete interrupt 1: enable DMA5 Transmission Complete interrupt		
4	DMA4TCIE	DMA4 Transmission Complete IRQ Enable: 0: disable DMA4 Transmission Complete interrupt 1: enable DMA4 Transmission Complete interrupt	RW	0x0
3	DMA3TCIE	DMA3 Transmission Complete IRQ Enable: 0: disable DMA3 Transmission Complete interrupt 1: enable DMA3 Transmission Complete interrupt	RW	0x0
2	DMA2TCIE	DMA2 Transmission Complete IRQ Enable: 0: disable DMA2 Transmission Complete interrupt 1: enable DMA2 Transmission Complete interrupt	RW	0x0
1	DMA1TCIE	DMA1 Transmission Complete IRQ Enable: 0: disable DMA1 Transmission Complete interrupt 1: enable DMA1 Transmission Complete interrupt	RW	0x0
0	DMA0TCIE	DMA0 Transmission Complete IRQ Enable: 0: disable DMA0 Transmission Complete interrupt 1: enable DMA0 Transmission Complete interrupt	RW	0x0

6.4.4 DMA0CTL

DMA0CTL (DMA0 control Register, offset = 0x00000010)

Bits	Name	Description	Access	Reset
31:17	-	Reserved	-	-
16	AUDIOTYPE	The method of audio data stored of DMA-ADC, DMA-DAC transmission: 0: interleaved stored in the memory 1: separated stored in the memory	RW	0x0
15:14	DATAWIDTH	The data width to write to DAC or read from ADC FIFO: 00: 8bit 01: 16bit 10: 24bit 11: reserved The data width to write to SPI TX FIFO or read from SPI RX FIFO: 00: 8bit 01: reserved 10: reserved 11: 32bit	RW	0x0
13:12	-	Reserved	-	-
11:8	DSTTYPE	Destination type: 4'b0000: memory 4'b0011: UART0 TX FIFO 4'b0110: SD/MMC FIFO 4'b1001: UART1 TX FIFO 4'b1011: DAC TX FIFO0 4'b1100: DAC TX FIFO1 Others: Reserved	RW	0x0
7:4	SRCTYPE	Source type: 4'b0000: memory 4'b0011: UART0 RX FIFO 4'b0110: SD/MMC FIFO 4'b1001: UART1 RX FIFO 4'b1011: ADC FIFO	RW	0x0

		Others: Reserved		
3:2	-	Reserved	-	-
1	reload	Reload the DMA controller registers and start DMA transmission after current DMA transmission is complete: 0: disable reload mode 1: enable reload mode	RW	0x0
0	DMA0START	DMA0 start bit: A low-to-high conversion of this bit will lead to load source address, destination address, destination step size, source step size, transfer type, burst length, DRQ type, and data width to the DMA controller. This bit will be automatically cleared by the DMA0 controller if the DMA0 transmission is complete or DMA0 transmission error occurs. This bit can be written '0' to abort DMA0 transmission.	RW	0x0

6.4.5 DMA0SADDR0

DMA0SADDR0 (DMA0 Source Address Register 0, offset = 0x00000014)

Bits	Name	Description	Access	Reset
31:18	-	Reserved	-	-
17:0	DMA0SADDR0	The source address 0 of DMA0 transmission. The bit[0] is no effect if data width is 16-bit. The bit[1:0] is no effect if data width is 24-bit or 32-bit.	RW	0x0

6.4.6 DMA0SADDR1

DMA0SADDR1 (DMA0 Source Address Register 1, offset = 0x00000018)

Bits	Name	Description	Access	Reset
31:18	-	Reserved	-	-
17:0	DMA0SADDR1	The source address 1 of DMA0 transmission. The bit[0] is no effect if data width is 16-bit. The bit[1:0] is no effect if data width is 24-bit or 32-bit.	RW	0x0

6.4.7 DMA0DADDR0

DMA0DADDR0 (DMA0 Destination Address Register 0, offset = 0x0000001C)

Bits	Name	Description	Access	Reset
31:18	-	Reserved	-	-
17:0	DMA0DADDR0	The destination address 0 of DMA0 transmission. The bit[0] is no effect if data width is 16-bit. The bit[1:0] is no effect if data width is 24-bit or 32-bit.	RW	0x0

6.4.8 DMA0DADDR1

DMA0DADDR1 (DMA0 Destination Address Register 1, offset = 0x00000020)

Bits	Name	Description	Access	Reset
31:18	-	Reserved	-	-
17:0	DMA0DADDR1	The destination address 1 of DMA0 transmission. The bit[0] is no effect if data width is 16-bit. The bit[1:0] is no effect if data width is 24-bit or 32-bit.	RW	0x0

6.4.9 DMA0FrameLen

DMA0FrameLen (DMA0 Frame Length Register 1, offset = 0x00000024)

Bits	Name	Description	Access	Reset
31:18	-	Reserved	-	-
17:0	DMA0FrameLen	The frame length of DMA0 transmission. If DSTTYPE is DAC TX FIFO, the value of DMA0FrameLen is equal to the times that DMA writes FIFO. If SRCTYPE is ADC FIFO, the value of DMA0FrameLen is equal to the times that DMA reads FIFO. If other DSTTYPE or SRCTYPE, the value of DMA0FrameLen is equal to the number of bytes transferred by DMA.	RW	0x0

6.4.10 DMA1CTL

DMA1CTL (DMA1 control Register, offset = 0x00000028)

Bits	Name	Description	Access	Reset
31:17	-	Reserved	-	-
16	AUDIOTYPE	The method of audio data stored of DMA-ADC/ DMA-DAC transmission: 0: interleaved stored in the memory 1: separated stored in the memory	RW	0x0
15:14	DATAWIDTH	The data width to write DAC FIFO or read from ADC FIFO: 00: 8bit 01: 16bit 10: 24 bit 11: reserved The data width to write SPI TX FIFO or read from SPI RX FIFO: 00: 8bit 01: reserved 10: reserved 11: 32bit	RW	0x0
13:12	-	Reserved	-	-
11:8	DSTTYPE	Destination type: 4'b0000: memory 4'b0010: reserved 4'b0011: UART0 TX FIFO 4'b0110: SD/MMC FIFO 4'b1001: UART1 TX FIFO 4'b1011: DAC TX FIFO0 4'b1100: DAC TX FIFO1 Others: Reserved	RW	0x0
7:4	SRCTYPE	Source type: 4'b0000: memory 4'b0010: reserved 4'b0011: UART0 RX FIFO 4'b0110: SD/MMC FIFO 4'b1001: UART1 RX FIFO 4'b1011: ADC FIFO Others: Reserved	RW	0x0
3:2	-	Reserved	-	-
1	RELOAD	Reload the DMA controller registers and start DMA	RW	0x0

		transmission after current DMA transmission is complete: 0: disable reload mode 1: enable reload mode		
0	DMA1START	DMA1 start bit: A low-to-high conversion of this bit will lead to load source address, destination address, destination step size, source step size, transfer type, burst length, DRQ type, and data width to the DMA controller. This bit will be automatically cleared by the DMA1 controller if the DMA1 transmission is complete or DMA1 transmission error occurs. This bit can be written '0' to abort DMA1 transmission.	RW	0x0

6.4.11 DMA1SADDR0

DMA1SADDR0 (DMA1 Source Address Register 0, offset = 0x0000002C)

Bits	Name	Description	Access	Reset
31:18	-	Reserved	-	-
17:0	DMA1SADDR0	The source address 0 of DMA1 transmission. The bit[0] is no effect if data width is 16-bit. The bit[1:0] is no effect if data width is 24-bit or 32-bit.	RW	0x0

6.4.12 DMA1SADDR1

DMA1SADDR1 (DMA1 Source Address Register 1, offset = 0x00000030)

Bits	Name	Description	Access	Reset
31:18	-	Reserved	-	-
17:0	DMA1SADDR1	The source address 1 of DMA1 transmission. The bit[0] is no effect if data width is 16-bit. The bit[1:0] is no effect if data width is 24-bit or 32-bit.	RW	0x0

6.4.13 DMA1DADDR0

DMA1DADDR0 (DMA1 Destination Address Register 0, offset = 0x00000034)

Bits	Name	Description	Access	Reset
31:18	-	Reserved	-	-
17:0	DMA1DADDR0	The destination address 0 of DMA1 transmission. The bit[0] is no effect if data width is 16-bit. The bit[1:0] is no effect if data width is 24-bit or 32-bit.	RW	0x0

6.4.14 DMA1DADDR1

DMA1DADDR1 (DMA1 Destination Address Register 1, offset = 0x00000038)

Bits	Name	Description	Access	Reset
31:18	-	Reserved	-	-
17:0	DMA1DADDR1	The destination address 1 of DMA1 transmission. The bit[0] is no effect if data width is 16-bit. The bit[1:0] is no effect if data width is 24-bit or 32-bit.	RW	0x0

6.4.15 DMA1FrameLen

DMA1FrameLen (DMA1 Frame Length Register 1, offset = 0x0000003c)

Bits	Name	Description	Access	Reset
31:18	-	Reserved	-	-
17:0	DMA1FrameLen	The frame length of DMA1 transmission. If DSTTYPE is DAC TX FIFO, the value of DMA1FrameLen is equal to the times that DMA writes FIFO. If SRCTYPE is ADC FIFO or, the value of DMA1FrameLen is equal to the times that DMA reads FIFO. If other DSTTYPE or SRCTYPE, the value of DM1FrameLen is equal to the number of bytes transferred by DMA.	RW	0x0

6.4.16 DMA2CTL

DMA2CTL (DMA2 control Register, offset = 0x00000040)

Bits	Name	Description	Access	Reset
31:17	-	Reserved	-	-
16	AUDIOTYPE	The method of audio data stored of DMA-ADC/ DMA-DAC transmission: 0: interleaved stored in the memory 1: separated stored in the memory	RW	0x0
15:14	DATAWIDTH	The data width to write DAC FIFO or read from ADC FIFO: 00: 8bit 01: 16bit 10: 24bit 11: reserved The data width to write SPI TX FIFO or read from SPI RX FIFO: 00: 8bit 01: reserved 10: reserved 11: 32bit	RW	0x0
13:12	-	Reserved	-	-
11:8	DSTTYPE	Destination type: 4'b0000: memory 4'b0001: reserved 4'b0010: reserved 4'b0011: UART0 TX FIFO 4'b0110: SD/MMC FIFO 4'b1001: UART1 TX FIFO 4'b1011: DAC TX FIFO0 4'b1100: DAC TX FIFO1 Others: Reserved	RW	0x0
7:4	SRCTYPE	Source type: 4'b0000: memory 4'b0010: reserved 4'b0011: UART0 RX FIFO 4'b0110: SD/MMC FIFO 4'b1001: UART1 RX FIFO 4'b1011: ADC FIFO Others: Reserved	RW	0x0
3:2	-	Reserved	-	-
1	RELOAD	Reload the DMA controller registers and start DMA transmission after current DMA transmission is complete: 0: disable reload mode	RW	0x0

		1: enable reload mode		
0	DMA2START	DMA2 start bit: A low-to-high conversion of this bit will lead to load source address, destination address, destination step size, source step size, transfer type, burst length, DRQ type, and data width to the DMA controller. This bit will be automatically cleared by the DMA2 controller if the DMA2 transmission is complete or DMA2 transmission error occurs. This bit can be written '0' to abort DMA2 transmission.	RW	0x0

6.4.17 DMA2SADDR0

DMA2SADDR0 (DMA2 Source Address Register 0, offset = 0x00000044)

Bits	Name	Description	Access	Reset
31:18	-	Reserved	-	-
17:0	DMA2SADDR0	The source address 0 of DMA2 transmission. The bit[0] is no effect if data width is 16-bit. The bit[1:0] is no effect if data width is 24-bit or 32-bit.	RW	0x0

6.4.18 DMA2SADDR1

DMA2SADDR1 (DMA2 Source Address Register 1, offset = 0x00000048)

Bits	Name	Description	Access	Reset
31:18	-	Reserved	-	-
17:0	DMA2SADDR1	The source address 1 of DMA2 transmission. The bit[0] is no effect if data width is 16-bit. The bit[1:0] is no effect if data width is 24-bit or 32-bit.	RW	0x0

6.4.19 DMA2DADDR0

DMA2DADDR0 (DMA2 Destination Address Register 0, offset = 0x0000004C)

Bits	Name	Description	Access	Reset
31:18	-	Reserved	-	-
17:0	DMA2DADDR0	The destination address 0 of DMA2 transmission. The bit[0] is no effect if data width is 16-bit. The bit[1:0] is no effect if data width is 24-bit or 32-bit.	RW	0x0

6.4.20 DMA2DADDR1

DMA2DADDR1 (DMA2 Destination Address Register 1, offset = 0x00000050)

Bits	Name	Description	Access	Reset
31:18	-	Reserved	-	-
17:0	DMA2DADDR1	The destination address 1 of DMA2 transmission. The bit[0] is no effect if data width is 16-bit. The bit[1:0] is no effect if data width is 24-bit or 32-bit.	RW	0x0

6.4.21 DMA2FrameLen

DMA2FrameLen (DMA2 Frame Length Register 1, offset = 0x00000054)

Bits	Name	Description	Access	Reset
31:18	-	Reserved	-	-

17:0	DMA2FrameLen	The frame length of DMA2 transmission. If DSTTYPE is DAC TX FIFO, the value of DMA2FrameLen is equal to the times that DMA writes FIFO. If SRCTYPE is ADC FIFO or, the value of DMA2FrameLen is equal to the times that DMA reads FIFO. If other DSTTYPE or SRCTYPE, the value of DMA2FrameLen is equal to the number of bytes transferred by DMA.	RW	0x0

6.4.22 DMA3CTL

DMA3CTL (DMA3 control Register, offset = 0x00000058)

Bits	Name	Description	Access	Reset
31:17	-	Reserved	-	-
16	AUDIOTYPE	The method of audio data stored of DMA-ADC/ DMA-DAC transmission: 0: interleaved stored in the memory 1: separated stored in the memory	RW	0x0
15:14	DATAWIDTH	The data width to write DAC FIFO or read from ADC FIFO: 00: 8bit 01: 16bit 10: 24bit 11: reserved The data width to write SPI TX FIFO or read from SPI RX FIFO: 00: 8bit 01: reserved 10: reserved 11: 32bit	RW	0x0
13:12	-	Reserved	-	-
11:8	DSTTYPE	Destination type: 4'b0000: memory 4'b0010: reserved 4'b0011: UART0 TX FIFO 4'b0110: SD/MMC FIFO 4'b1001: UART1 TX FIFO 4'b1011: DAC TX FIFO0 4'b1100: DAC TX FIFO1 Others: Reserved	RW	0x0
7:4	SRCTYPE	Source type: 4'b0000: memory 4'b0010: reserved 4'b0011: UART0 RX FIFO 4'b0110: SD/MMC FIFO 4'b1001: UART1 RX FIFO 4'b1011: ADC FIFO Others: Reserved	RW	0x0
3:2	-	Reserved	-	-
1	reload	Reload the DMA controller registers and start DMA transmission after current DMA transmission is complete: 0: disable reload mode 1: enable reload mode	RW	0x0
0	DMA3START	DMA3 start bit: A low-to-high conversion of this bit will lead to load source	RW	0x0

		address, destination address, destination step size, source step size, transfer type, burst length, DRQ type, and data width to the DMA controller. This bit will be automatically cleared by the DMA3 controller if the DMA3 transmission is complete or DMA3 transmission error occurs. This bit can be written '0' to abort DMA3 transmission.		

6.4.23 DMA3SADDR0

DMA3SADDR0 (DMA3 Source Address Register 0, offset = 0x0000005c)

Bits	Name	Description	Access	Reset
31:18	-	Reserved	-	-
17:0	DMA3SADDR0	The source address 0 of DMA3 transmission. The bit[0] is no effect if data width is 16-bit. The bit[1:0] is no effect if data width is 24-bit or 32-bit.	RW	0x0

6.4.24 DMA3SADDR1

DMA3SADDR1 (DMA3 Source Address Register 1, offset = 0x00000060)

Bits	Name	Description	Access	Reset
31:18	-	Reserved	-	-
17:0	DMA3SADDR1	The source address 1 of DMA3 transmission. The DMA3SADDR1[0] is no effect if data size is 16 bit, 24 bit or 32 bit. The DMA3SADDR1[1] is no effect if data size is 24 bit or 32 bit.	RW	0x0

6.4.25 DMA3DADDR0

DMA3DADDR0 (DMA3 Destination Address Register 0, offset = 0x00000064)

Bits	Name	Description	Access	Reset
31:18	-	Reserved	-	-
17:0	DMA3DADDR0	The destination address 0 of DMA3 transmission. The bit[0] is no effect if data width is 16-bit. The bit[1:0] is no effect if data width is 24-bit or 32-bit.	RW	0x0

6.4.26 DMA3DADDR1

DMA3DADDR1 (DMA3 Destination Address Register 1, offset = 0x00000068)

Bits	Name	Description	Access	Reset
31:18	-	Reserved	-	-
17:0	DMA3DADDR1	The destination address 1 of DMA3 transmission. The bit[0] is no effect if data width is 16-bit. The bit[1:0] is no effect if data width is 24-bit or 32-bit.	RW	0x0

6.4.27 DMA3FrameLen

DMA3FrameLen (DMA3 Frame Length Register 1, offset = 0x0000006c)

Bits	Name	Description	Access	Reset
31:18	-	Reserved	-	-
17:0	DMA3FrameLen	The frame length of DMA3 transmission.	RW	0x0

		If DSTTYPE is DAC FIFO, the value of DMA3FrameLen is equal to the times that DMA writes FIFO. If SRCTYPE is ADC FIFO, the value of DMA3FrameLen is equal to the times that DMA reads FIFO. If other DSTTYPE or SRCTYPE, the value of DMA3FrameLen is equal to the number of bytes transferred by DMA.		

6.4.28 DMA4CTL

DMA4CTL (DMA4 control Register, offset = 0x00000070)

Bits	Name	Description	Access	Reset
31:17	-	Reserved	-	-
16	AUDIOTYPE	The method of audio data stored of DMA-ADC/ DMA-DAC transmission: 0: interleaved stored in the memory 1: separated stored in the memory	RW	0x0
15:14	DATAWIDTH	The data width to write DAC or read from ADC FIFO: 00: 8bit 01: 16bit 10: 24bit 11: reserved The data width to write SPI TX FIFO or read from SPI RX FIFO: 00: 8bit 01: reserved 10: reserved 11: 32bit	RW	0x0
13:12	-	Reserved	-	-
11:8	DSTTYPE	Destination type: 4'b0000: memory 4'b0011: UART0 TX FIFO 4'b0110: SD/MMC FIFO 4'b1001: UART1 TX FIFO 4'b1011: DAC TX FIFO0 4'b1100: DAC TX FIFO1 Others: Reserved	RW	0x0
7:4	SRCTYPE	Source type: 4'b0000: memory 4'b0011: UART0 RX FIFO 4'b0110: SD/MMC FIFO 4'b1001: UART1 RX FIFO 4'b1011:ADC FIFO Others: Reserved	RW	0x0
3:2	-	Reserved	-	-
1	reload	Reload the DMA controller registers and start DMA transmission after current DMA transmission is complete: 0: disable reload mode 1: enable reload mode	RW	0x0
0	DMA4START	DMA4 start bit: A low-to-high conversion of this bit will lead to load source address, destination address, destination step size, source step size, transfer type, burst length, DRQ type, and data width to the DMA controller. This bit will be automatically	RW	0x0

		cleared by the DMA4 controller if the DMA4 transmission is complete or DMA4 transmission error occurs. This bit can be written '0' to abort DMA4 transmission.		

6.4.29 DMA4SADDR0

DMA4SADDR0 (DMA4 Source Address Register 0, offset = 0x00000074)

Bits	Name	Description	Access	Reset
31:18	-	Reserved	-	-
17:0	DMA4SADDR0	The source address 0 of DMA4 transmission. The bit[0] is no effect if data width is 16-bit. The bit[1:0] is no effect if data width is 24-bit or 32-bit.	RW	0x0

6.4.30 DMA4SADDR1

DMA4SADDR1 (DMA4 Source Address Register 1, offset = 0x00000078)

Bits	Name	Description	Access	Reset
31:18	-	Reserved	-	-
17:0	DMA4SADDR1	The source address 1 of DMA4 transmission. The DMA4SADDR1[0] is no effect if data size is 16 bit, 24 bit or 32 bit. The DMA4SADDR1[1] is no effect if data size is 24 bit or 32 bit.	RW	0x0

6.4.31 DMA4DADDR0

DMA4DADDR0 (DMA4 Destination Address Register 0, offset = 0x0000007C)

Bits	Name	Description	Access	Reset
31:18	-	Reserved	-	-
17:0	DMA4DADDR0	The destination address 0 of DMA4 transmission. The bit[0] is no effect if data width is 16-bit. The bit[1:0] is no effect if data width is 24-bit or 32-bit.	RW	0x0

6.4.32 DMA4DADDR1

DMA4DADDR1 (DMA4 Destination Address Register 1, offset = 0x00000080)

Bits	Name	Description	Access	Reset
31:18	-	Reserved	-	-
17:0	DMA4DADDR1	The destination address 1 of DMA4 transmission. The bit[0] is no effect if data width is 16-bit. The bit[1:0] is no effect if data width is 24-bit or 32-bit.	RW	0x0

6.4.33 DMA4FrameLen

DMA4FrameLen (DMA4 Frame Length Register 1, offset = 0x00000084)

Bits	Name	Description	Access	Reset
31:18	-	Reserved	-	-
17:0	DMA4FrameLen	The frame length of DMA4 transmission. If DSTTYPE is DAC TX FIFO, the value of DMA4FrameLen is equal to the times that DMA writes FIFO. If SRCTYPE is ADC FIFO or, the value of DMA4FrameLen is	RW	0x0

		equal to the times that DMA reads FIFO. If other DSTTYPE or SRCTYPE, the value of DMA4FrameLen is equal to the number of bytes transferred by DMA.		

6.4.34 DMA5CTL

DMA5CTL (DMA5 control Register, offset = 0x00000088)

Bits	Name	Description	Access	Reset
31:5	-	Reserved	-	-
4	SRCTYPE	Source type: 1'b0: UART0 RX FIFO 1'b1: UART1 RX FIFO	RW	0x0
3:2	-	Reserved	-	-
1	reload	Reload the DMA controller registers and start DMA transmission after current DMA transmission is complete: 0: disable reload mode 1: enable reload mode	RW	0x0
0	DMA5START	Special DMA start bit: A low-to-high conversion of this bit will lead to load source address, destination address, destination step size, source step size, transfer type, burst length, DRQ type, and data width to the DMA controller. This bit will be automatically cleared by the DMA controller if the DMA transmission is complete or DMA transmission error occurs. This bit can be written '0' to abort DMA transmission.	RW	0x0

6.4.35 DMA5DADDR

DMA5DADDR (DMA5 Destination Address Register, offset = 0x0000008C)

Bits	Name	Description	Access	Reset
31:18	-	Reserved	-	-
17:0	DMA5DADDR	The destination address of Special DMA transmission.	RW	0x0

6.4.36 DMA5FrameLen

DMA5FrameLen (DMA5 Frame Length Register 1, offset = 0x00000090)

Bits	Name	Description	Access	Reset
31:18	-	Reserved	-	-
17:0	DMA5FrameLen	The value of DMA5FrameLen is equal to the number of bytes transferred by Special DMA.	RW	0x0

6.4.37 DMA5CONT

DMA5CONT (DMA5 counter register, offset = 0x00000094)

Bits	Name	Description	Access	Reset
31:18	-	Reserved	-	-
17:0	DMA5CONT	The counter is equal to the number of bytes written to memory by special DMA currently. The counter is cleared automatically by hardware when special DMA transmission is complete.	R	0x0

7 PMU

7.1 Features

The ATS2823B integrates a comprehensive power supply system, including the following features:

- Supports Li-Ion battery / 5V power supply and Integrate Linear battery charger
- Integrated DC-DC buck converters output 1.5V, which can be switch to LDO mode.
- Linear regulators output VCC, BTVCC, AVCC

7.2 Module Description

7.2.1 DC-DC Converter

The DC-DC converter integrated in ATS2823B efficiently scales battery voltage to the required supply voltage. It can work in Pulse Frequency Modulation (PFM) or Pulse Width Modulation (PWM) automatically for different load current.

7.2.2 Linear Regulators

The ATS2823B integrates multiple linear regulators; they generate VCC, VDD, AVCC, BTVCC and VD15.

7.2.2.1 Regulators Accurate and Maximum Output Current

The output voltages are precisely within ±2%, providing large currents with a significantly small dropout voltage within ±5%. Table below shows data of maximum output current.

Table 7-1 Regulators Maximum Output Current

Block Name	Output Voltage	Load Capacity
VCC	2.7~3.4V	300 mA
VDD	0.8~1.5V	100 mA
VD15	1.0~1.7V	170 mA
BTVCC	2.8~3.5V	100 mA
AVCC	VCC-0.15V	50 mA@98%

7.2.2.2 Regulators Power Down

If the system is to operate from an external power supply, then the internal linear regulators are powered down automatically.

7.2.3 Li-Ion Cell Charger

Some products in the ATS2823B family integrate charging for Li-Ion battery from a 5-V source connected to the DC5V pin. The battery charger is essentially a linear regulator that has current and voltage limits. Charge current is software-programmable within REG[CHG_CURRENT]. You can enable charger by setting REG[CHGEN]=1.

One can programmatically monitor the battery voltage using the BATADC. The charger has its own voltage limiting that operates independently of the BATADC. But monitoring the battery voltage and VBUS voltage during the charge might be helpful for reporting the charge progress.

The battery charger is capable of generating a large amount of heat within the ATS2823B, especially at currents above 400 mA. The dissipated power can be estimated as: (5V – battery voltage) * current. At max current (500 mA) and a 3-V battery, the charger can dissipate 1 W.
The TEMPADC can be used to monitor battery temperatures.
The SENSADC is used to monitor the charger and diode's temperature.

7.2.4 Reference Voltage

7.2.5 A/D Converters

There are 4 low resolutions 7 bit A/Ds for system monitor, the input voltage range of which is 0.7V to 2.2V at TEMPADC pin, 1.4V to 4.4V at VBAT pin, 2.1V to 6.6V at DC5V pin and 0.7V to 2.2V at temp sensor circuit, 0V to SVCC at LRADC2 / LRADC3 pin.

1LSB= 3.1/(2^7) = 24.22mV

When the input voltage is V, the related ADC data n = V/(3.1/2^7).
Then the data n is 0x00 related from 0V to 0.02422V, the data n is 0x01 related from 0.02422Vto 0.4844V.

7.3 Register List

Table 7-2 PMU block base address

Name	Physical Base Address	KSEG1 Base Address
PMU	0xC0020000	0xC0020000

Table 7-3 PMU Block Configuration Registers List

Offset	Register Name	Description	Voltage Domain
0x00	VOUT_CTL	VCC/VDD/AVCC voltage set Register	VDD
0x08	VD15_DCDC_CTL	VDD DCDC Modulation/frequency/MAX current set Register	RTCVDD
0x0C	CHG_CTL	Charge enable and current set Register	VDD
0x10	CHG_DET	Charge status detect Register	VDD
0x14	PMUADC_CTL	PMU ADC frequency and enable Register	RTCVDD
0x18	BATADC_DATA	BATADC data Register	VDD
0x1C	TEMPADC_DATA	TEMPADC data Register	VDD
0x20	DC5VADC_DATA	DC5V ADC data Register	VDD
0x24	SENSADC_DATA	Sensor ADC DATA Register	VDD
0x2C	LRADC2_DATA	LRADC2 data Register	AVDD
0x30	LRADC3_DATA	LRADC3 data Register	AVDD
0x38	BDG_CTL	Bandgap enable and voltage set Register	RTCVDD
0x3C	LDO_CTL	LDO SET Register	RTCVDD
0x40	SYSTEM_SET	System set Register	RTCVDD
0x44	POWER_CTL	POWER on/off control Register	RTCVDD
0x48	TIMER_CTL	S3/S3BT MODE auto Play/standby time set	RTCVDD
0x4C	WKEN_CTL	Wake up source select Register	RTCVDD
0x50	WAKE_PD	Wake up source pending	RTCVDD
0x54	ONOFF_KEY	On/off KEY control Register	RTCVDD
0x5C	NFC_CTL	NFC field detect control	RTCVDD
0x64	SPD_CTL	Standby mode power pull down	RTCVDD

7.4 Register Description

7.4.1 VOUT_CTL

Voltage set register (VDD) Default: 0x60048

Offset: 0x00

Bit (s)	Name	Description	Access	Reset
31:19	-	Reserved	-	-
18	AVDD_PD	AVDD no capacitor LDO pull down 0: no pull down 1: 1mA pull down	RW	1
17:16	AVDD_VOL	00 1.0V 01 1.1V 10 1.2V 11 1.3V	RW	0x2
15	-	Reserved	-	-
13:12	AVCC_DROP	AVCC LDO margin tuning, voltage drop from VCC 00 0.15V 01 0.20V 10 0.25V 11 0.30V	RW	00
11:10	-	Reserved	-	-
9	VCCOC_SET	VCC LDO Current limit: 0: 400mA 1: 500mA	RW	0
8	VDDOC_SET	VDD LDO Current limit: 0: 200mA 1: 300mA	RW	0
7	-	Reserved	-	-
6:4	VCC_SET	VCC voltage level select 000: 2.7V 001: 2.8V 010: 2.9V 011: 3.0V 100: 3.1V 101: 3.2V 110: 3.3V 111: 3.4V	RW	0x4
3:0	VDD_SET	VDD (Regulator) voltage coarse control 0000: 0.80V 0001: 0.85V 0010: 0.90V 0011: 0.95V 0100: 1.00V 0101: 1.05V 0110: 1.10V 0111: 1.15V 1000: 1.20V 1001: 1.25V 1010: 1.30V 1011: 1.35V 1100: 1.40V 1101: 1.45V	RW	0x8

		1111: 1.50V		

7.4.2 VD15_DCDC_CTL

VD15 DCDC set register (RTCVDD) Default: 0x942625

Offset: 0x08

Bit (s)	Name	Description	Access	Reset
29:17	-	Reserved	-	-
16:15	ANTI_ADUIO	Provide pull down current selection 00: disable 01: 4mA 10: 8mA 11: 12mA	RW	0
14:13	-	Reserved	-	-
12:11	VD15_MODE_S1	Under S1 state, VD15 using DCDC or LDO mode switch bit: 00: fixed to LDO 01: fixed to DCDC 10: switch automatically through UVLO signal 11: switch automatically through DC5VOV signal	RW	0
9:8	-	Reserved	-	-
3:1	DCDC_FS	DC-DC frequency control 000: 889KHz (8 / 9) 001: 1MHz 010: 1.4MHz 011: 2MHz 100: 2.6MHz 101: 3MHz 110: 4MHz 111: 4MHZ Adjustable DC-DC frequency for difference load current.	RW	0x2
0	-	Reserved	-	-

7.4.3 CHG_CTL

Charging control register (VDD) Default: 0x18013A

Offset = 0x0C

Bit (s)	Name	Description	Access	Reset
31:21	-	Reserved	-	-
19	DC5VOV_EN	DC5V overvoltage detection enable bit 0:disable/ reset 1:enable	RW	1
16	-	Reserved	-	-
15	CHGEN	Enable Charge Circuit 0:disable 1:enable	RW	0
14	ENTKLE	Trickle charging enable: 0: disable trickle charge. 1: enable trickle charge.	RW	0
13:11	CHG_CURRENT	Charger constant charging Current Configure	RW	0

		000:25mA 001:50mA 010:100mA 011:200mA 100:300mA 101:400mA 110:500mA 111:600mA		
10	ENBATDT	Battery detection enable bit: 0:disable 1:enable	RW	0
9:7	ENFASTCHG	Constant charging voltage setting: 000: 4.2V 001: 4.23V 010: 4.26V 011: 4.29V 100: 4.32V 101: 4.35V 110: 4.38V 111: 4.41V	RW	0x2
6:5	STOPV	End-of-charging voltage 00: 4.16V 01 :4.18V 10: 4.32V 11: 4.34V	RW	1
4	ENSAMP	DC5V constant loop enable bit: 0:disable 1:enable	RW	1
3:2	STDY_SET	Set DC5V steady voltage 00 3.81 01 4.0 10 4.25 11 4.4	RW	0x2
1	ENCHGATDT	Auto detection of end-of-charging enable bit 0:disable 1:enable	RW	1
0	DTSEL	End-of-charging detection time selection: 0: once per 12min 1: once per 20s	RW	0

7.4.4 CHG_DET

Charging detect register (VDD)

Offset = 0x10

Bit (s)	Name	Description	Access	Reset
31:8	-	Reserved	-	-
7	UVLO	DC5V insertion detection conditions: 0: no DC5V is inserted 1: DC5V >= BAT+0.1V or BAT+0.02V	R	x
6:5	CHGPHASE	Charging state flag bit 00: reserved 01: trickle charging phase 10: CC charging phase	R	x

		11: CV charging phase		
4	CHG_STA0	Whether Ichg>5%Ichg_reg flag 0: Ichg<5%Ichg_reg 1: Ichg>5%Ichg_reg	R	x
3	CHG_STA1	Whether Ichg>20%Ichg_reg flag 0: Ichg<20%Ichg_reg 1: Ichg>20%Ichg_reg	R	x
2	CHGEND	End-of-charging flag 0: in charging 1: end-of-charging	R	x
1	BATEXT	BAT exsistants flag 0: no battery 1: battery is on	R	x
0	DTOVER	Battery detection over flag 0: under detection 1: detection is over	R	x

7.4.5 PMUADC_CTL

PMUADC Control Register Default: 0xD7

Offset = 0x14

Bit (s)	Name	Description	Access	Reset
31:8	-	Reserved	-	-
7	BATADC_FS	BAT/DC5V/TEMP/SENSOR ADCs Frequency Source Select: 0: 125HZ 1: 250HZ	RW	1
6	LRADC_FS	LRADC234 Frequency Source Select: 0: 125HZ 1: 250HZ	RW	1
5	LRADC234_EN	7bit LRADC2/3/4 A/D enable. 0: Disable 1: Enable	RW	0
4	-	Reserved	-	-
3	SENSORADC_EN	TEMP sensor A/D enable 0: Disable, TEMP sensor circuit and output disable 1: Enable, TEMP sensor circuit and output enable	RW	0
2	DC5VADC_EN	DC5V A/D enable 0: Disable 1: Enable	RW	1
1	TEMPADC_EN	TEMP A/D enable 0: Disable 1: Enable	RW	1
0	BATADC_EN	Battery A/D enable 0: Disable 1: Enable	RW	1

7.4.6 BATADC_DATA

BATADC DATA Register (VDD)

Offset = 0x18

Bit (s)	Name	Description	Access	Reset

15:7	-	Reserved	-	-
6:0	BATADC	7bit Voltage ADC, used to detect Battery voltage. Input voltage range is: Li-ion: 1.4-4.4V	R	x

7.4.7 TEMPADC_DATA

TEMPADC DATA Register (VDD)

Offset = 0x1C

Bit (s)	Name	Description	Access	Reset
15:7	-	Reserved	-	-
6:0	TEMPADC	7bit Voltage ADC, used to detect TEMPADC voltage. Input voltage range is: 0.7-2.2V	R	x

7.4.8 DC5VADC_DATA

DC5V ADC DATA Register (VDD)

Offset = 0x20

Bit (s)	Name	Description	Access	Reset
15:7	-	Reserved	-	-
6:0	DC5VADC	7bit Voltage ADC, used to detect DC5V voltage. Input voltage range is: 2.1-6.6V	R	x

7.4.9 SENSADC_DATA

Sensor ADC DATA Register (VDD)

Offset = 0x24

Bit (s)	Name	Description	Access	Reset
15:7	-	Reserved	-	-
6:0	SENSADC	7bit Voltage ADC, used to detect TEMPSENSOR voltage.	R	x

7.4.10 LRADC2_DATA

LRADC2 DATA Register (VDD)

Offset = 0x2C

Bit (s)	Name	Description	Access	Reset
31:7	-	Reserved	-	-
6:0	LRADC2	7bit LRADC2 data output LRADC2 input voltage range is from 0 to AVCC.	R	x

7.4.11 LRADC3_DATA

LRADC3 DATA Register (VDD)

Offset = 0x30

Bit (s)	Name	Description	Access	Reset
31:7	-	Reserved	-	-
6:0	LRADC3	7bit LRADC3 data output. LRADC3 input voltage range is from 0 to AVCC.	R	x

7.4.12 BDG_CTL

Bandgap Control Register (RTCVDD) Default: 0x2D

Offset = 0x38

Bit (s)	Name	Description	Access	Reset
31:7	-	Reserved	-	-
6	BDG_FILTER	BANDGAP filter Control REG 0: BANDGAP has no filter resistor 1: BANDGAP has filter resistor Notes: Make sure this bit is set to 1 before using DAC/ADC, OR IT WILL CAUSE BIG NOISE!	RW	0
5	BDG_PDR	BANDGAP pull down resistor control 0: NO pull down resistor 1: have pull down resistor	RW	1

7.4.13 LDO_CTL

LDO set register (RTCVDD) Default: 0x002AA888

Offset: 0x3C

Bit (s)	Name	Description	Access	Reset
31:19	-	Reserved	-	-
18	VD15OC_SET	VD15 LDO Current limit: 0: 270mA 1: 370mA	RW	0
17:14	VD15_SET	VD15 DC-DC / Regulator voltage coarse control 0000: 1.00V 0001: 1.05V 0010: 1.10V 0011: 1.15V 0100: 1.20V 0101: 1.25V 0110: 1.30V 0111: 1.35V 1000: 1.40V 1001: 1.45V 1010: 1.50V 1011: 1.55V 1100: 1.60V 1101: 1.65V 1111: 1.70V	RW	0xA
13	BTVDD_PD	BTVDD no capacitor LDO pull down 0: no pull down 1: 1mA pull down	RW	1
12	BTVDD_EN	BTVDD enable bit 0: disable 1: enable	RW	0
11:8	BTVDD_VOL	BTVDD voltage coarse control 0000: 0.80V 0001: 0.85V 0010: 0.90V 0011: 0.95V 0100: 1.00V 0101: 1.05V	RW	0x8

		0110: 1.10V 0111: 1.15V 1000: 1.20V 1001: 1.25V 1010: 1.30V 1011: 1.35V 1100: 1.40V 1101: 1.45V 1111: 1.50V		
4	BTVCCOC_SET	BTVCC LDO Current limit: 0: 200mA 1: 300mA	RW	0
3:1	BTVCC_VOL	BTVCC voltage level select 000: 2.8V 001: 2.9V 010: 3.0V 011: 3.1V 100: 3.2V 101: 3.3V 110: 3.4V 111: 3.5V	RW	0x4
0	BTVCC_EN	BTVCC power enable: 0: disable 1: enable	RW	0

7.4.14 SYSTEM_SET

System set Register (RTCVDD) Default: 0x3BF

Offset = 0x40

Bit (s)	Name	Description	Access	Reset
31:8	-	Reserved	-	-
7	LB_EN	LB (Low battery) enter standby enable: 0: disable 1: enable	RW	1
6:5	LB_VOL	LB (Low battery) voltage setting 00: 2.7V 01: 3.0V 1x: 3.3V	RW	1
4	OC_EN	VCC/VDD/BTVCC/VD15 LDO overcurrent protection enable bit 0: disable 1: enable	RW	1
3	LVPRO_EN	VCC/VDD/BTVCC/VD15 undervoltage protection enable 0: disable 1: enable	RW	1

7.4.15 POWER_CTL

Power source as VCC/VDD/BTVCC/SVCC on/off Control Register (RTCVDD) Default: 0x1

Offset = 0x44

Bit (s)	Name	Description	Access	Reset
31:3	-	Reserved	-	-

2	EN_S3	EN_S3 enable bit 0:disable 1:enable	RW	0
1	EN_S3BT	EN_S3BT enable bit 0:disable 1:enable	RW	0
0	EN_S1	EN_S1 enable bit 0:disable 1:enable	RW	1

7.4.16 TIMER_CTL

System timer set Register (RTCVDD) Default: 0x200000

Offset = 0x48

Bit (s)	Name	Description	Access	Reset
31:22	-	Reserved	-	-
21	S3_TIMER_EN	S3timer_EN bit 0:Disable 1:Enable	RW	1
20	S3TIMER	S3timer 0: 300ms 1: 1s	RW	0
19:16	-	Reserved	-	-
15	S3BT_ON_EN	S3BT ON timer Enable bit 0:Disable 1:Enable	RW	0
14:8	S3BT_ON_TIMER	S3BT power on by alarm timer 7 bits corresponds to 0~127 mins	RW	0
7:0	-	Reserved	-	-

7.4.17 WKEN_CTL

WAKE up source enable Register (RTCVDD) Default: 0x6FB

Offset = 0x4C

Bit (s)	Name	Description	Access	Reset
31:11	-	Reserved	-	-
10	BATWK_EN	Battery insert wakeup enable bit 0: disable 1: enable	RW	1
9	REMOTE_WKEN	Drive-by-wire wakeup enable bit 0: disable 1: enable	RW	1
8	HDSW_BLOCK	Toggle switch shields long/short press on play key to wakeup enable release bit 0: Toggle switch turn to OFF will shield long/shot press on the play key to wake up 1: Toggle switch do not shield long/short press on the play key to wake up	RW	0
7	HDSWOFF_EN	Under S3BT state, toggle switch ON/OFF enable 0:disable 1:enable	RW	1
5	BT_WK_EN	Bluetooth wakeup enable	RW	1

		0:Disable 1:Enable		
4	NFC_WK_EN	NFC wakeup enable 0:Disable 1: enable	RW	1
3	RESET_WKEN	RESET wakeup enable 0:disable 1:enable	RW	1
2	SHORT_WKEN	On off short press wakeup enable 0:disable 1:enable	RW	0
1	LONG_WKEN	On off long press wakeup enable 0:disable 1:enable	RW	1
0	HDSW_WKEN	HDSW toggle switch wakeup enable 0:disable 1:enable	RW	1

Note: needs to update code before writing this register.

7.4.18 WAKE_PD

WAKE up source enable Register (RTCVDD) Default: 0x0

Offset = 0x50

Bit (s)	Name	Description	Access	Reset
31:9	-	Reserved	-	-
8	BATIN_PD	Battery insert wakeup pending bit 0: no battery insert wakeup 1: battery insert wakeup happened	RW	0
7	REMOTE_PD	Drive-by-wire wakeup pending bit 0: no Drive-by-wire wakeup 1: Drive-by-wire happened	RW	0
6	LONG_PLAY	Long press on play key pending bit 0: no long press on play key 1: long press on play key happened	RW	0
5	S3BT_TON_PD	S3BT_ON timer wakeup indication pending bit 0: no S3BT_ON_TIMER wakeup 1: S3BT_ON_TIMER wakeup	RW	0
4	HDSWOFF_PD	Toggle switch OFF pending bit 0: no toggle switch operation 1: toggle switch OFF operation	RW	0
3	HDSWON_PD	Toggle switch ON pending bit 0: no toggle switch operation 1: toggle switch ON operation	RW	0
2	ONOFF_PD	ONOFF wakeup pending bit 0: no ONOFF wakeup happened 1: ONOFF wakeup happened	RW	0
1	NFC_PD	NFC Pending 0: Interrupt source is not active. 1: Interrupt source is active. Write 1 to this bit to clear this pending bit. This bit must be cleared by software before trigger a new interrupt pending.	RW	0
0	BT_PD	Bluetooth Pending	RW	0

		0: Interrupt source is not active. 1: Interrupt source is active. Write 1 to this bit to clear this pending bit. This bit must be cleared by software before trigger a new interrupt pending.		

7.4.19 ONOFF_KEY

ONOFF key control & detect register (RTCVDD) Default: 0x80D8

Offset = 0x54

Bit (s)	Name	Description	Access	Reset
31:11	-	Reserved	-	-
10	RESTART_SET	RESET key function setting 0: reset VDD region registers 1: restart	RW	0
9:7	ONOFF_PRESS_TIME	ONOFF key press time setting: 000: 50ms < t < 0.125s, recognized as short press; t >=0.125s, recognized as long press; 001: 50ms < t < 0.25s, recognized as short press; t >=0.25s, recognized as long press; 010: 50ms < t < 0.5s, recognized as short press; t >=0.5s, recognized as long press; 011: 50ms < t < 1s, recognized as short press; t >=1s, recognized as long press; 100: 50ms < t < 1.5s, recognized as short press; t >=2s, recognized as long press; 101: 50ms < t < 2s, recognized as short press; t >=2s, recognized as long press; 110: 50ms < t < 3s, recognized as short press; t >=3s, recognized as long press; 111: 50ms < t < 4s, recognized as short press; t >=4s, recognized as long press;	RW	1
6	ONOFF_RST_EN	ONOFF long press reset function enable 0:disable 1:enable	RW	1
5:4	ONOFF_RST_T_SEL	ONOFF long press send Reset time selection 00:6s 01:8s 10:10s 11:12s	RW	1
2	HDSWOFF_2_3	ONOFF level 0: not on this level 1: on 2/3 level (digital realization)	R	0
1	HDSWON_1_3	ONOFF level 0: not this level 1: at 1/3 level (digital realization)	R	0
0	ONOFF_PRESS_0	ONOFF key whether pressed down 0:ONOFF not pressed 1:ONOFF is pressed (digital realization)	R	0

7.4.20 NFC_CTL

NFC field detect control Register (RTCVDD) Default: 0x1C

Offset = 0x5C

Bit (s)	Name	Description	Access	Reset
31:9	-	Reserved	-	-
8	BT_WAKE_DET	BT_WAKE_HOST signal level flag: 0: signal is low 1: signal is high	R	0
7	NFC_DET	NFC_FD level flag	R	X
6	NFCPU_CTL	Pull up resistor selection: 0: disable 1: 50K	RW	0
5:1	-	Reserved	-	-
0	NFCTM_SET	Trigger mode set: 0: when higher than 2/3RTCVDD, trigger interrupt sending and wakeup 1: when lower than 2/3RTCVDD, trigger interrupt sending and wakeup	RW	0

7.4.21 SPD_CTL

Standby power pull down control (RTCVDD) Default: 0x13D

Offset: 0x64

Bit (s)	Name	Description	Access	Reset
31:9	-	Reserved	-	-
8:7	DC5V_SYS_VOL	Adjusting DC5V generated SYSPOWER voltage 00: 3.3V 01: 4.2V 10: 4.3V 11: 4.4V	RW	0x2

8 System Control

8.1 RMU

8.1.1 Features

The RMU Controller of ATS2823B has following features:

- The RMU (Reset Management Unit) can reset all the peripherals.
- The MCU can enter power-saving mode by setting the registers of RMU .

8.1.2 Register List (Digital part)

Table 8-1 RMU digital part base address

Name	Physical Base Address	KSEG1 Base Address
RMU_DIGITAL	0xC0000000	0xC0000000

Table 8-2 RMU digital part register list

Offset	Register Name	Description
0x00000000	MRCR	Module Reset Control Register

8.1.3 Register Description

8.1.3.1 MRCR

MRCR (Module Reset Control Register, offset = 0x00000000)

Bit (s)	Name	Description	Access	Reset
31:18	-	Reserved	-	-
17	UART1RESET	UART1 Controller & IR Reset 0: reset 1: normal	RW	0
16:13	-	Reserved	-	-
12	PWM_LIGHT_RESET	PWM back light Reset 0: reset 1: normal	RW	0
11	AUDIOIORESET	DAC & ADC Reset 0: reset 1: normal	RW	0
10:5	-	Reserved	-	-
4	UART0RESET	UART0 & H5 Controller Reset 0: reset 1: normal	RW	0
3	SDRESET	SD/MMC Card Controller Reset 0: reset 1: normal	RW	0
2	DSP_PART	All but OCEM DSP reset 0: reset DSP except OCEM 1: normal	RW	1

		Note: Debug use only, do not set to 0.		
1	DSP_ALL	All DSP reset 0: reset all DSP 1: depends on DSP_PART	RW	0
0	DMA012345RESET	DMA012345 Reset 0: reset 1: normal The reset bit of DMA012345 controller is active while it is driven by MCU clock.	RW	0

*Note: * The reset signal of SPI BOOT controller and interrupt controller is connected to the wire of CPU reset. It can be reset while the power on reset, watch dog reset or the reset pin of CPU is set low.*
** RTC, LRADC, timer0/1 have no reset control in this register.*

8.2 CMU Analog

8.2.1 Features

- Support only one oscillator inputs: 26MHz
- Supply 3 PLLs and special clocks of all modules. The 3 PLLs is PLL_24M, CORE PLL, Audio PLL
- CORE PLL can select from two clock source: CK_24M and HOSC

8.2.2 Register List

Table 8-3 CMU Analog Controller Registers Address

Name	Physical Base Address	KSEG1 Base Address
CMU_ANALOG_REGISTER	0xC0000100	0xC0000100

Table 8-4 CMU Analog Controller Registers

Offset	Register Name	Description
0x00	HOSC_CTL	HOSC control register
0x08	_24MPLL_CTL	24M PLL Control Register
0x0C	CORE_PLL_CTL	CORE_PLL Control Register

8.2.3 Register Description

8.2.3.1 HOSC_CTL

HOSC control register.
Offset = 0x00 (RTCVDD domain)

Bit (s)	Name	Description	Access	Reset
31:16	-	Reserved	-	-
15:13	HOSCI_BC_SEL	HOSCI PAD base capacitor select: 000: 0p 001: 3p 010: 6p 011: 9p 100: 6p 101: 9p 110: 12p	RW	101

		111: 15p		
12:8	HOSCI_TC_SEL	HOSCI PAD trim cap select, range from 0pF to 3.1pF Trim cap = 0.1pF * HOSCI_TC_SEL	RW	0x00
7:5	HOSCO_BC_SEL	HOSCO PAD base capacitor select: 000: 0p 001: 3p 010: 6p 011: 9p 100: 6p 101: 9p 110: 12p 111: 15p	RW	101
4:0	HOSCO_TC_SEL	HOSCO PAD trim cap select, range from 0pF to 3.1pF Trim cap = 0.1pF * HOSCO_TC_SEL	RW	0x00

8.2.3.2 _24MPLL_CTL

24MPLL Control Register
Offset = 0x08 (VDD domain)

Bit (s)	Name	Description	Access	Reset
31:4	-	Reserved	-	-
3	HOSC_EN	HOSC enable: 0: disable 1: enable	RW	1
2:1	-	Reserved	-	-
0	24MPLL_EN	24MPLL Enable: 0: disable 1: enable	RW	0

8.2.3.3 CORE_PLL_CTL

CORE_PLL Control Register
Offset = 0x0C (VDD domain)

Bit (s)	Name	Description	Access	Reset
31:9	-	Reserved	-	-
8	CORE_PLL_SCLK_SEL	CORE PLL source clock select: 0: HOSC_26M 1: CK_24M	RW	0
7	CORE_PLL_EN	CORE PLL Enable: 0: Disable 1: Enable	RW	0
6:0	SCORE	CORE PLL Frequency Select: When core PLL source clock select HOSC_26M, Formula: 6.5M* SCORE Range:39 ~ 409.5M Value must be bigger than 6 0-5: reserved 6: 6*6.5M=39M …… 63: 63*6.5M=409.5M Others reserved.	RW	0x06

		When core PLL source clock select CK_24M, Formula: 6M* SCORE Range:36 ~ 378M Value must be bigger than 6 0-5: reserved 6: 6*6M=36M …… 63: 63*6M=378M Others reserved.		

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8.3 RTC

This part have individual modules: Calendar, 2Hz, Watch Dog (WD) and Timer0/1.

8.3.1 Features

- Built-in a 32k oscillator
- Calendar with a alarm IRQ which can wake up the PMU
- 2Hz IRQ
- Two Timers with IRQ
- A watch dog which can be configured as IRQ or Reset

8.3.2 Register List

Table 8-5 RTC block base address

Name	Physical Base Address	KSEG1 Base Address
RTC	0xC0120000	0xC0120000

Table 8-6 RTC Controller Registers

Offset	Register Name	Description
0x00	RTC_CTL	RTC Control Register
0x04	RTC_REGUPDATA	RTC Register update Register
0x08	RTC_DHMSALM	RTC Day Hour Minute and Second Alarm Register
0x0C	RTC_DHMS	RTC Day Hour Minute and Second Register
0x10	RTC_YMD	RTC Year Month Date Register
0x14	RTC_ACCESS	RTC freely access Register
0x18	Hz2_CTL	2Hz Control Register
0x1c	WD_CTL	Watch Dog Control register
0x20	T0_CTL	Timer0 Control register
0x24	T0_VAL	Timer0 Value
0x28	T1_CTL	Timer1 Control register
0x2C	T1_VAL	Timer1 Value
0X30	RTC_BAK0	Backup Register
0X34	RTC_BAK1	Backup Register
0X38	RTC_BAK2	Backup Register
0X3C	RTC_BAK3	Backup Register

8.3.3 Register Description

8.3.3.1 RTC_CTL

Calendar Control Register
Offset=0x0000 (RTCVDD) (Default value 0x80)

Bits	Name	Description	Access	Reset
31:8	-	Reserved	-	-
7	LEAP	RTC Leap Year bit 1: leap year 0: not leap year	R	1
6:5	-	Reserved	-	-
4	CAL_EN	Calendar Enable 1: Enable 0: Disable	RW	0
3:2	-	Reserved	-	-
1	ALIE	Alarm IRQ Enable 1: Enable 0: Disable	RW	0
0	ALIP	Alarm IRQ Pending bit, writing 1 to this bit will clear it	RW	0

NOTE:
The CAL_EN bit must be disabled when The RTC_DHMS / RTC_YMD register being written. And RTC_DHMS / RTC_YMD register must be written before CAL_EN is enabled when set the time or error will occur.

8.3.3.2 RTC_REGUPDATA

Offset=0x0004 (RTCVDD)

Bits	Name	Description	Access	Reset
31:16	-	Reserved	-	-
15:0	UPDATA	The RTCVDD register update control Register. When writing the RTC registers (except RTCREGUPDATE register or bit “ALIP”), the RTC registers’ values are not update immediately. The value is written to backup registers (in VDD) first. Just when writing RTCREGUPDATE register “A596H”, the RTCVDD registers’ values are update with the backup registers’ value. RTCREGUPDATE register is automatically reset as “5A69H” after the RTCVDD register is update. NOTE: Do not write RTCVDD registers when this register value is “A5C3E283H” NOTE: When writing the bit “ALM_IP”, it will take effect immediately. Do not need writing this register.	RW	0x5A69H

8.3.3.3 RTC_DHMSALM

Offset=0x0008 (RTCVDD)

Bits	Name	Description	Access	Reset
31:21	-	Reserved	-	-
20:16	HOUEAL	Alarm hour setting 0x00 – 0x17	RW	0
15:14	-	Reserved	-	-

13:8	MINAL	Alarm minute setting 0x00 – 0x3B	RW	0
7:6	-	Reserved	-	-
5:0	SECAL	Alarm second setting 0x00 – 0x3B	RW	0

8.3.3.4 RTC_DHMS

Offset=0x000C (RTCVDD)

Bits	Name	Description	Access	Reset
31:21	-	Reserved	-	-
20:16	HOUR	Time hour setting 0x00 – 0x17	RW	0
15:14	-	Reserved	-	-
13:8	MIN	Time minute setting 0x00 – 0x3B	RW	0
7:6	-	Reserved	-	-
5:0	SEC	Time second setting 0x00 – 0x3B	RW	0

8.3.3.5 RTC_YMD

Offset=0x0010 (RTCVDD)

Bits	Name	Description	Access	Reset
31:23	-	Reserved	-	-
22:16	YEAR	Time year setting 0x00 – 0x63	RW	00
15:12	-	Reserved	-	-
11:8	MON	Time month setting 0x01 – 0x0C	RW	01
7:5	-	Reserved	-	-
4:0	DATE	Time day setting 0x01 – 0x1F	RW	01

8.3.3.6 RTC_ACCESS

Offset=0x0014 (RTCVDD)

Bits	Name	Description	Access	Reset
31:8	-	Reserved	-	-
7:0	ACCESS	These bits can be accessed by CPU freely.	RW	0

8.3.3.7 HZ2_CTL

Offset=0x0018 (VDD)

Bits	Name	Description	Access	Reset
31:2	-	Reserved	-	-
1	2HIE	2Hz IRQ Enable 1: Enable 0: Disable	RW	0
0	2HIP	2Hz IPQ pending bit, writing 1 to this bit will clear it	RW	0

8.3.3.8 WD_CTL

Offset=0x001C (VDD)

Bits	Name	Description	Access	Reset
37	-	Reserved	-	-
6	IRQP	Watch dog IRQ pending bit, writing 1 to this bit will clear it	RW	0
5	SIGS	Watchdog Signal (IRQ or Reset-) Select.0: Reset, 1: IRQ-. 0: Send Reset signal when watchdog overflow. 1: Send IRQ signal when watchdog overflow.	RW	0
4	WDEN	Watch Dog timer enable, when WD timer is enabled and the WD timer overflows, an internal reset (WDRST-) is generated to force the system into reset status and then reboot. 1: Enable 0: Disable	RW	0
3:1	CLKSEL	Watch Dog timer Clock Select, WDCKS Clock Selected Watch Dog Length The watch dog's overflow value is 180. 000 1kHz 176 ms 001 512Hz 352 ms 010 256Hz 703ms 011 128Hz 1.4 s 100 64Hz 2.8s 101 32Hz 5.6 s 110 16Hz 11.2s 111 Reserved	RW	0
0	CLR	Clear bit, write 1 to clear WD timer, cleared automatically	RW	0

8.3.3.9 T0_CTL

Offset=0x0020 (VDD)

Bits	Name	Description	Access	Reset
31:6	-	Reserved	-	-
5	EN	Timer 0 Enable 0:Disable,1:Enable	RW	0
4:3	-	Reserved	-	-
2	RELO	Timer 0 Reload. 0:Not reload,1:Reload	RW	0
1	ZIEN	T0 Zero IRQ Enable When this bit is enabled, Timer0_Zero_IRQ sent out the IRQ signal until the pending bit was cleared.	RW	0
0	ZIPD	Timer0 IRQ Pending, Writing 1 to clear this bit.	RW	0

Note: The timer only can count down

8.3.3.10 T0_VAL

Offset=0x0024 (VDD)

Bits	Name	Description	Access	Reset
31:24	-	Reserved	-	-
23:0	T0	Read or write current Timer0 value	RW	-

8.3.3.11 T1_CTL

Offset=0x0028 (VDD)

Bits	Name	Description	Access	Reset
31:6	-	Reserved	-	-
5	En	Timer0 Enable 0:Disable,1:Enable	RW	0
4:3	-	Reserved	-	-
2	RELO	Timer1 Reload 0:Not reload,1:Reload	RW	0
1	ZIEN	Timer1 Zero IRQ Enable When this bit is enabled, Timer1_Zero_IRQ sent out the IRQ signal until the pending bit was cleared.	RW	0
0	ZIPD	Timer1 IRQ Pending, Writing 1 to clear this bit.	RW	0

Note: The timer only can count down.

8.3.3.12 T1_VAL

Offset=0x002C (VDD)

Bits	Name	Description	Access	Reset
31:24	-	Reserved	-	-
23:0	T1	Read or write current Timer1 value	RW	0

8.4 Exceptions and Interrupts Controller (INTC)

8.4.1 Features

The ATS2823B use MIPS processor. The ATS2823B also adds additional controller to manage up to 32 interrupt sources.

Table below shows all interrupt sources.

Table 8-7 Interrupt sources

Interrupt Number	Sources	Type
0	BT	High Level
1	NFC	High Level
2	2Hz/WatchDog	High Level
3	TIMER1	High Level
4	TIMER0	High Level
5	RTC	High Level
6	UART0	High Level
7	SIRQ0	High Level
8	Reserved	-
9	Reserved	-
10	Reserved	-
11	Reserved	-
12	UART1	High Level
13	SIRQ1	High Level
14	DAC	High Level

15	ADC	High Level
16	Reserved	-
17	SD/MMC	High Level
18	DMA0	High Level
19	DMA1	High Level
20	DMA2	High Level
21	DMA3	High Level
22	DMA4	High Level
23	DMA5	High Level
24	Reserved	-
25	Reserved	-
26	Reserved	-
27	OUT_USER0	High Level
28	OUT_USER1	High Level
29	OUT_USER2	High Level
30	OUT_USER3	High Level
31	OUT_USER4	High Level

8.4.2 Register List

The ATS2823B implements a controller to handle 32 interrupt request, the registers are listed below:

Table 8-8 Interrupt Controller base address

Name	Physical Base Address	KSEG1 Base Address
InterruptController	0xC00B0000	0xC00B0000

Table 8-9 Interrupt Controller Registers

Offset	Register Name	Description
0x00000000	INTC_PD	Interrupt Pending register
0x00000004	INTC_MSK	Interrupt Mask register
0x00000014	INTC_EXTCTL	External interrupt control register
0x00000018	INTC_EXTIP	External interrupt status register
0x0000001C	REQ_INT_OUT	Request interrupt output register
0x00000020	REQ_IN	Request input register
0x00000024	REQ_IN_PD	Request input pending register
0x00000028	REQ_OUT	Request output register

8.4.3 Register Description

8.4.3.1 INTC_PD

INTC_PD (Interrupt Pending Register, offset = 0x00000000)

Bit (s)	Name	Description	Access	Reset
31	OUT_USER4_IP	OUT_USER4 interrupt pending bit	R	0
30	OUT_USER3_IP	OUT_USER3 interrupt pending bit	R	0
29	OUT_USER2_IP	OUT_USER2 interrupt pending bit	R	0
28	OUT_USER1_IP	OUT_USER1 interrupt pending bit	R	0
27	OUT_USER0_IP	OUT_USER0 interrupt pending bit	R	0
26:24	-	Reserved	-	-
23	DMA5_IP	DMA5 controller interrupt pending bit	R	0

22	DMA4_IP	DMA4 controller interrupt pending bit	R	0
21	DMA3_IP	DMA3 controller interrupt pending bit	R	0
20	DMA2_IP	DMA2 controller interrupt pending bit	R	0
19	DMA1_IP	DMA1 controller interrupt pending bit	R	0
18	DMA0_IP	DMA0 controller interrupt pending bit	R	0
17	SD_IP	SD/MMC interrupt pending bit	R	0
16	-	Reserved	-	-
15	ADC_IP	ADC interrupt pending bit	R	0
14	DAC_IP	DAC interrupt pending bit	R	0
13	SIRQ1_IP	SIRQ1 interrupt pending bit	R	0
12	UART1_IP	UART1 interrupt pending bit	R	0
11	-	Reserved	-	-
10	-	Reserved	-	-
9	-	Reserved	-	-
8	-	Reserved	-	-
7	SIRQ0_IP	SIRQ0 interrupt pending bit	R	0
6	UART0_IP	UART0 interrupt pending bit	R	0
5	RTC_IP	RTC interrupt pending bit	R	0
4	TIMER0_IP	TIMER0 interrupt pending bit	R	0
3	TIMER1_IP	TIMER1 interrupt pending bit	R	0
2	2Hz_IP	2Hz/WatchDog interrupt pending bit	R	0
1	NFC_IP	NFC pending	R	0
0	BT_IP	BT pending	R	0

Note:

(1) Interrupt Pending bits cannot be cleared by writing 1. These bits are automatically cleared only by clear all the corresponding interrupt pending bits of the device register, otherwise unchanged.

(2) 0: no interrupt request; 1: interrupt request detected

8.4.3.2 INTC_MSK

INTC_MSK (Interrupt Mask Register, offset = 0x00000004)

Bit (s)	Name	Description	Access	Reset
31	OUT_USER4_IM	OUT_USER4 interrupt enable bit	RW	0
30	OUT_USER3_IM	OUT_USER3 interrupt mask bit	RW	0
29	OUT_USER2_IM	OUT_USER2 interrupt mask bit	RW	0
28	OUT_USER1_IM	OUT_USER1 interrupt mask bit	RW	0
27	OUT_USER0_IM	OUT_USER0 interrupt mask bit	RW	0
26:24	-	Reserved	-	-
23	DMA5_IM	DMA5 controller interrupt mask bit	RW	0
22	DMA4_IM	DMA4 controller interrupt mask bit	RW	0
21	DMA3_IM	DMA3 controller interrupt mask bit	RW	0
20	DMA2_IM	DMA2 controller interrupt mask bit	RW	0
19	DMA1_IM	DMA1 controller interrupt mask bit	RW	0
18	DMA0_IM	DMA0 controller interrupt mask bit	RW	0
17	SD_IM	SD/MMC interrupt mask bit	RW	0
16	-	Reserved	-	-
15	ADC_IM	ADC interrupt mask bit	RW	0
14	DAC_IM	DAC interrupt mask bit	RW	0
13	SIRQ1_IM	SIRQ1 interrupt mask bit	RW	0
12	UART1_IM	UART1 interrupt mask bit	RW	0
11	-	Reserved	-	-
10	-	Reserved	-	-

9	-	Reserved	-	-
8	-	Reserved	-	-
7	SIRQ0_IM	SIRQ0 interrupt mask bit	RW	0
6	UART0_IM	UART0 interrupt mask bit	RW	0
5	RTC_IM	RTC interrupt mask bit	RW	0
4	TIMER0_IM	TIMER0 interrupt mask bit	RW	0
3	TIMER1_IM	TIMER1 interrupt mask bit	RW	0
2	2HZ_IM	2Hz/WatchDog interrupt mask bit	RW	0
1	NFC_IM	NFC interrupt mask bit	RW	0
0	BT_IM	BT interrupt mask bit	RW	0

Note: 0: Interrupt is masked. 1: Interrupt is unmasked.

8.4.3.3 INTC_EXTCTL

INTC_EXTCTL (External Interrupt Control register, offset = 0x00000014)

Bit (s)	Name	Description	Access	Reset
31:4	-	Reserved	-	-
3	EXTYPE1	External Interrupt 1 Type 0: Rising edge-triggered; 1: Falling edge-triggered.	RW	0
2	-	Reserved	-	-
1	EXTYPE0	External Interrupt 0 Type 0: Rising edge-triggered; 1: Falling edge-triggered.	RW	0
2	-	Reserved	-	-

8.4.3.4 INTC_EXTIP

INTC_IP (External Interrupt Pending register, offset = 0x00000018)

Bit (s)	Name	Description	Access	Reset
31:2	-	Reserved	-	-
1	E1PD	External Interrupt 1 Pending 0: External interrupt source 1 is not active. 1: External interrupt source 1 is active. Write 1 to will clear this bit. This bit must be cleared by software before trigger a new interrupt pending.	RW	0
0	E0PD	External Interrupt 0 Pending 0: External interrupt source 0 is not active. 1: External interrupt source 0 is active. Write 1 to will clear this bit. This bit must be cleared by software before trigger a new interrupt pending.	RW	0

8.4.3.5 REQ_INT_OUT

REQ_INT_OUT (Request interrupt output register, offset = 0x0000001C)

Bit (s)	Name	Description	Access	Reset
31:1	-	Reserved	-	-
0	DSP_INT3	Send interrupt request to DSP.	RW	0

8.4.3.6 REQ_IN

REQ_IN (Request input register, offset = 0x00000020)

Bit (s)	Name	Description	Access	Reset
31:5	-	Reserved	-	-
4	OUT_USER4	It is a CPU interrupt controller sampled value of OUT_USER4 signal.	R	0
3	OUT_USER3	It is a CPU interrupt controller sampled value of OUT_USER3 signal.	R	0
2	OUT_USER2	It is a CPU interrupt controller sampled value of OUT_USER2 signal.	R	0
1	OUT_USER1	It is a CPU interrupt controller sampled value of OUT_USER1 signal.	R	0
0	OUT_USER0	It is a CPU interrupt controller sampled value of OUT_USER0 signal.	R	0

8.4.3.7 REQ_IN_PD

REQ_IN_PD (Request input pending register, offset = 0x00000024)

Bit (s)	Name	Description	Access	Reset
31:5	-	Reserved	-	-
4	OUT_USER4_PD	0: interrupt pending is not detected. 1: interrupt pending is detected. External Interrupt Pending is set at rising edge of DSP OUT_USER4 signal. Writing '1' can clear this bit.	RW	0
3	OUT_USER3_PD	0: interrupt pending is not detected. 1: interrupt pending is detected. External Interrupt Pending is set at rising edge of DSP OUT_USER3 signal. Writing '1' can clear this bit.	RW	0
2	OUT_USER2_PD	0: interrupt pending is not detected. 1: interrupt pending is detected. External Interrupt Pending is set at rising edge of DSP OUT_USER2 signal. Writing '1' can clear this bit.	RW	0
1	OUT_USER1_PD	0: interrupt pending is not detected. 1: interrupt pending is detected. External Interrupt Pending is set at rising edge of DSP OUT_USER1 signal. Writing '1' can clear this bit.	RW	0
0	OUT_USER0_PD	0: interrupt pending is not detected. 1: interrupt pending is detected. External Interrupt Pending is set at rising edge of DSP OUT_USER0 signal. Writing '1' can clear this bit.	RW	0

8.4.3.8 REQ_OUT

REQ_OUT (Request output register, offset = 0x00000028)

Bit (s)	Name	Description	Access	Reset
31:2	-	Reserved	-	-
1	IN_USER1	Send information to DSP.	RW	0
0	IN_USER0	Send information DSP.	RW	0

9 Transfer and Communication

9.1 UART

9.1.1 Features

UART1 has the following features:

- 5-8 Data Bits and LSB first in Transmit and Received
- 1-2 Stop Bits
- Even, Odd, or No Parity
- Support IRQ and DMA mode to transmit data
- Support RTS/CTS Automatic Hardware Flow Control to reduce interrupts to host system
- UART RX Support DMA single mode
- Baud Rate up to 6Mbps

9.1.2 Register List

Table 9-1 UART1 Registers Block Base Address

Name	Physical Base Address	KSEG1 Base Address
UART1	0xC00F0000	0xC00F0000

Table 9-2 UART1 Registers Offset Address

Offset	Register Name	Description
0x0000	UART1_CTL	UART1 Control Register
0x0004	UART1_RXDAT	UART1 Receive FIFO Data Register
0x0008	UART1_TXDAT	UART1 Transmit FIFO Data Register
0x000c	UART1_STA	UART1 Status Register
0x0010	UART1_BR	UART1 BAUDRATE divider Register

9.1.3 Register Description

9.1.3.1 UART1_CTL

UART1 Control Register

Offset=0x0000

Bits	Name	Description	Access	Reset
31:22	-	Reserved	-	-
21	TXAHB_DMA_SEL1	UART1 TX FIFO Clock Select 0: AHB Clock 1:DMA Clock	RW	0
20	LBEN1	Loop Back Enable. Set this bit to enable a loop back mode that data coming on the input will be presented on the output. 0: Disable 1: Enable	RW	0
19	TXIE1	UART1 TX IRQ Enable. 0: Disable 1: Enable	RW	0

18	RXIE1	UART1 RX IRQ Enable. 0: Disable 1: Enable	RW	0
17	TXDE1	UART1 TX DRQ Enable. 0: Disable 1: Enable	RW	0
16	RXDE1	UART1 RX DRQ Enable. 0: Disable 1: Enable	RW	0
15	EN1	UART1 Enable. When this bit is clear, the UART clock source is inhibited. This can be used to place the module in a low power standby state. 0:disable 1: enable	RW	0
14	RXAHB_DMA_SEL1	UART1 RX FIFO Clock Select 0: AHB Clock 1:DMA Clock	RW	0
13	RTSE1	RTS Enable. When this bit is set, request to send data. Note: This bit has no effect if Autoflow enable bit is set. 0:no request 1: request to send data	RW	0
12	AFE1	Autoflow mode Enable Setting this bit enables automatic hardware flow control. Enabling this mode overrides software control of the signals. 0: Autoflow mode disable (normal mode) 1: Autoflow mode enable	RW	0
11:10	RDIC1	UART1 RX DRQ/IRQ Control 00: set when RX FIFO received at least one byte data in IRQ/DRQ mode. 01: set when RX FIFO received 4 bytes data in IRQ mode 10: set when RX FIFO received 8 bytes data in IRQ/DRQ mode 11: set when RX FIFO received 12 bytes data in IRQ/DRQ mode In DMA burst mode (normal DMA), DO not set 00, 01 because at least 8 bytes necessary. In DMA single mode (special DMA), DO set 00 for 1 Bytes transfer for each DRQ.	RW	0
9:8	TDIC1	UART1 TX DRQ/IRQ Control 00: set when TX FIFO is at least 1 byte empty in IRQ mode. 01: set when TX FIFO is 4 bytes empty in IRQ mode. 10: set when TX FIFO is 8 bytes empty in IRQ/DRQ mode. 11: set when TX FIFO is 12 bytes empty in IRQ/DRQ mode. In DMA mode, DO not set 00, 01 because at least 8 bytes necessary.	RW	0
7	-	Reserved	-	-
6:4	PRS1	Parity Select.	RW	0

		Bit 6: PEN, Parity enable Bit 5: STKP, Stick parity Bit 4: EPS, Even parity PEN STKP EPS Selected Parity 0 x x None 1 0 0 Odd 1 0 1 logic 1 1 1 0 Even 1 1 1 logic 0		
3	-	Reserved	-	-
2	STPS1	STOP Select. If this bit is 0, 1 stop bit is generated in transmission. If this bit is 1, 2 stop bits are generated. 0: 1 stop bit 1: 2 stop bit	RW	0
1:0	DWLS1	Data Width Length Select. 00: 5 bits 01: 6 bits 10: 7 bits 11: 8 bits	RW	0

9.1.3.2 UART1_RXDAT

UART1 Receive FIFO Data Register

Offset=0x0004

Bits	Name	Description	Access	Reset
31:8	-	Reserved	-	-
7:0	RXDAT1	Received Data.	R	x

9.1.3.3 UART1_TXDAT

UART1 Transmit FIFO Data Register

Offset=0x0008

Bits	Name	Description	Access	Reset
31:8	-	Reserved	-	-
7:0	TXDAT1	Transmitted Data.	W	0

9.1.3.4 UART1_STA

UART1 Status Register

Offset=0x000C

Bits	Name	Description	Access	Reset
31:22	-	Reserved	-	-
21	UTBB1	UART1 TX busy bit 0:not busy, TX FIFO is empty and all data be shift out 1:busy	R	0
20:16	TXFL1	TX FIFO Level. The field indicates the current TX FIFO empty level.	R	0x10
15:11	RXFL1	RX FIFO Level. The field indicates the current RX FIFO level of valid data.	R	0
10	TFES1	TX FIFO empty Status 0: no empty	R	1

		1: empty		
9	RFFS1	RX FIFO full Status 0: no full 1: full	R	0
8	RTSS1	RTS Status. The bit reflects the status of the external RTS- pin.	R	0
7	CTSS1	CTS Status. The bit reflects the status of the external CTS- pin.	R	x
6	TFFU1	TX FIFO Full. 1: Full 0: No Full	R	0
5	RFEM1	RX FIFO Empty. 1: Empty 0: No Empty	R	1
4	RXST1	Receive Status. 0: receive OK 1: receive error. Writing 1 to the bit will clear the bit. When stop bit detect error, or parity error, or clock error	RW	0
3	TFER1	TX FIFO Error. 0: No Error 1: Error Writing 1 to the bit will clear the bit and reset the TX FIFO.	RW	0
2	RXER1	RX FIFO Error. 0: No Error 1: Error Writing 1 to the bit will clear the bit and reset the RX FIFO.	RW	0
1	TIP1	TX IRQ Pending Bit. 0: No IRQ 1: IRQ Writing 1 to the bit to clear the bit.	RW	1
0	RIP1	RX IRQ Pending Bit. 0: No IRQ 1: IRQ Writing 1 to the bit to clear it.	RW	0

9.1.3.5 UART1_BR

UART1 BAUDRATE divider register

Offset=0x0010

Bits	Name	Description	Access	Reset
31:16	TXBRDIV1	UART1 TX BAUDRATE divider Baud Rate = Clock_source/Baud Rate divider Clock_source=HOSC or CK24M, selected by CMU_UART1CLK[0]	RW	0x0028
15:0	RXBRDIV1	UART1 BAUDRATE divider Baud Rate = Clock_source/Baud Rate divider Clock_source=HOSC or CK24M, selected by CMU_UART1CLK[0]	RW	0x0028

9.2 SPI

The SPI module is designed according to Motorola serial peripheral interface protocols. It can be configured as either a master or slave device. It can generate a large range of SPI clock so as to communicate with different devices supporting SPI protocols. Especially, this module support three operation mode: write & read, write only, read only mode.
SPI write & read mode use the MOSI pin to serially write instructions, addresses or data to the device. It also uses the MISO pin to read data or status from the device synchronous. This mode is designed to meet normal SPI application.

9.2.1 Features

- ATS2823B integrated SPI Interface: SPI0
- Support dual I/O write and read mode
- Support IRQ and DMA mode to transmit data
- SPI clock up to 60MHz

10 GPIO and I/O Multiplexer

10.1 Features

GPIO (General Purpose Input /Output) and MFP:

GPIO can output 0 or 1 and detect the signal level of the external circuit. Each GPIO has its own enable control bit and data registers. But the PADs are limited, so MFP module is designed for multiplexing these PADs.

- Some PAD has internal pull down or pull up resistors
- Driving strength can be adjusted, Level (n) corresponds to (2n) mA
- Automatically switching PAD function
- Support 4 channels PWM output, frequency ranges from 0.015625Hz~80K, adjustable. Under normal mode, PWM can output 256 kinds of duty cycles; under breath mode, PWM support kinds of breathing light.

SIO (Special Input /Output) and MFP:

There are 10 Special I/O ports to bring more flexible application possibility. The multiplexing is software controlled and can be configured for different application.

10.2 Operation Manual

10.2.1 GPIO Output

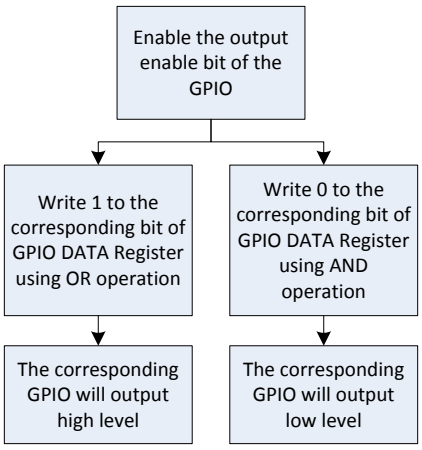


Figure 10-1 GPIO Output Configuration

10.2.2 GPIO Input

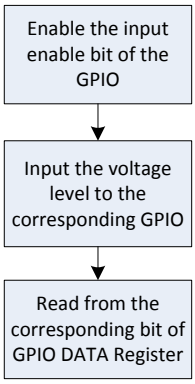


Figure 10-2 GPIO Input Configuration

10.2.3 SIO Output

Refer to the procedure as follows to configure an analog pin MICINL as a digital function such as SIO0.

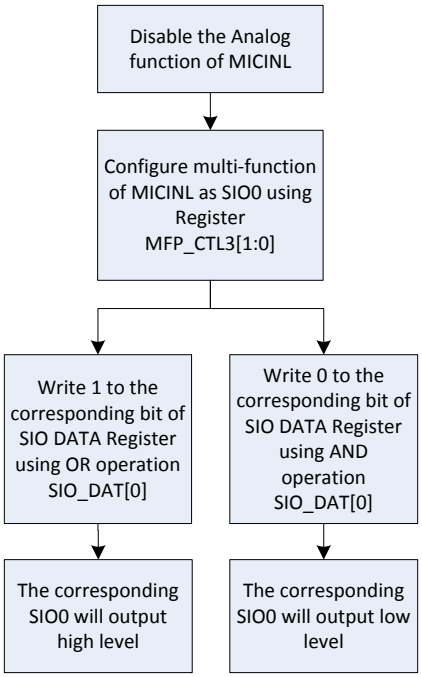


Figure 10-3 SDIO Output Configuration

10.2.4 GPIO Output/Input Loop Test

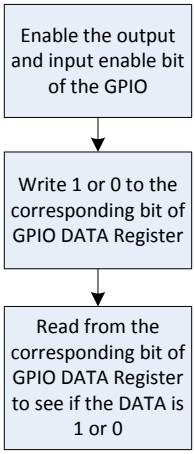


Figure 10-4 GPIO In/Out Loop Test

10.2.5 PWM Configure

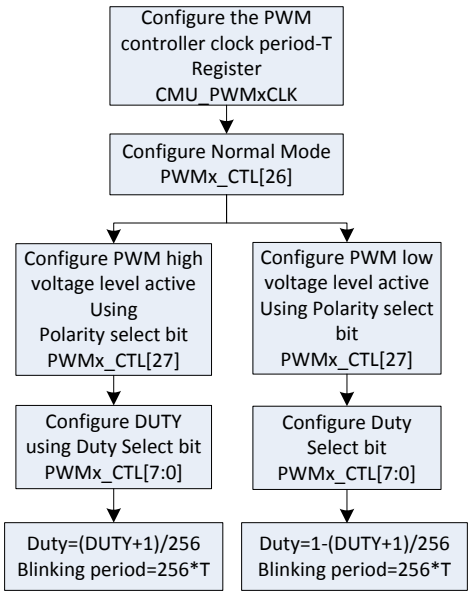


Figure 10-5 PWM Configuration

For example, if Duty =50% and the Blinking period is two seconds, T=2/256, the Frequency of the PWM controller clock is 1/T=128Hz, So CMU_PWMxCLK can be configured as 0xF9, PWMx_CTL can be configured as 0x0800007F.

10.3 Register List

Table 10-1 GPIO_MFP Controller Registers Address

Name	Physical Base Address	KSEG1 Base Address
GPIO_MFP	0xC0090000	0xC0090000

Table 10-2 GPIO&MFP Controller Registers

Offset	Register Name	Description
GPIO Register		
0x0000	GPIOAOUTEN	GPIOA Output Enable
0x0004	GPIOAINEN	GPIOA Input Enable
0x0008	GPIOADAT	GPIOA Data

0x000C	GPIOAPUEN	GPIOA 50K PU Enable
0x0010	GPIOAPDEN	GPIOA 50K PD Enable
0x0014	GPIOBOUTEN	GPIOB Output Enable
0x0018	GPIOBINEN	GPIOB Input Enable
0x001C	GPIOBDAT	GPIOB Data
0x0020	GPIOBPUEN	GPIOB 50K PU Enable
0x0024	GPIOBPDEN	GPIOB 50K PD Enable
0x0028	SIO_OUTEN	SIO Output Enable
0x002C	SIO_INEN	SIO Input Enable
0x0030	SIO_DAT	SIO Data
0x0034	SIO_PUEN	SIO 50K PU Enable
0x0038	SIO_PDEN	SIO 50K PD Enable
PWM Register		
0x0044	PWM3_CTL	PWM3 Output Control
0x0048	PWM0_CTL	PWM0 Output Control
0x004C	PWM1_CTL	PWM1 Output Control
0x0050	PWM2_CTL	PWM2 Output Control
MFP Register		
0x0054	MFP_CTL0	Multiplexing Control 0
0x0058	MFP_CTL1	Multiplexing Control 1
0x005C	MFP_CTL2	Multiplexing Control 2
0x0060	MFP_CTL3	Multiplexing Control 3
Analog/Digital Select Register		
0x0064	AD_SELECT	Analog/Digital Select
0x00A4	AD_SELECT1	Analog/Digital Select 1
PAD Drive Register		
0x0068	PADPUPD	PAD PU PD Resistance Enable
0x006C	PAD_SMIT	PAD Schmitt Control Register
0x0070	PADDRV0	PAD Drive Capacity Select 0
0x0074	PADDRV1	PAD Drive Capacity Select 1
0x0078	PADDRV2	PAD Drive Capacity Select 2
0x007C	PADDRV3	PAD Drive Capacity Select 3
0x0040	PADDRV4	PAD Drive Capacity Select 4

10.4 GPIO Register Description

10.4.1 GPIOAOUTEN

GPIOA Output Enable Register
Offset=0x00

Bit (s)	Name	Description	Access	Reset
31:0	GPIOAOUTEN	GPIOA[31:0] Output Enable. 0: Disable 1: Enable	RW	0x0

10.4.2 GPIOAINEN

GPIOA Input Enable Register
Offset=0x04

Bit (s)	Name	Description	Access	Reset
31:0	GPIOAINEN	GPIOA[31:0] Input Enable.	RW	0x0

		0: Disable 1: Enable		

10.4.3 GPIOADAT

GPIOA Data Register
Offset=0x08

Bit (s)	Name	Description	Access	Reset
31:0	GPIOADAT	GPIOA[31:0] Input/Output Data.	RW	0x0

10.4.4 GPIOAPUEN

GPIOA 50K PU Enable Register
Offset=0x0C

Bit (s)	Name	Description	Access	Reset
31:0	GPIOAPUEN	GPIOA[31:0] 100K PU Enable. 0: Disable 1: Enable	RW	0x10000

10.4.5 GPIOAPDEN

GPIOA 50K PD Enable Register
Offset=0x10

Bit (s)	Name	Description	Access	Reset
31:0	GPIOAPDEN	GPIOA[31:0] 100K PD Enable. 0: Disable 1: Enable	RW	0x0

10.4.6 GPIOBOUTEN

GPIOB Output Enable Register
Offset=0x14

Bit (s)	Name	Description	Access	Reset
31:13	-	Reserved	-	-
12:1	GPIOBOUTEN	GPIOB[12:1] Output Enable. 0: Disable 1: Enable	RW	0x0
0	-	Reserved	-	-

10.4.7 GPIOBINEN

GPIOB Input Enable Register
Offset=0x18

Bit (s)	Name	Description	Access	Reset
31:13	-	Reserved	-	-
12:1	GPIOBINEN	GPIOB[12:1] Input Enable. 0: Disable 1: Enable	RW	0x0
0	-	Reserved	-	-

10.4.8 GPIOBDAT

GPIOB Data Register
Offset=0x1C

Bit (s)	Name	Description	Access	Reset
31:13	-	Reserved	-	-
12:1	GPIOBDAT	GPIOB[12:1] Input/Output Data.	RW	0x0
0	-	Reserved	-	-

10.4.9 GPIOBPUEN

GPIOB 50K PU Enable Register
Offset=0x20

Bit (s)	Name	Description	Access	Reset
31:13	-	Reserved	-	-
12:1	GPIOBPUEN	GPIOB[12:1] 100K PU Enable. 0: Disable 1: Enable	RW	0x0
0	-	Reserved	-	-

10.4.10 GPIOBPDEN

GPIOB 50K PD Enable Register
Offset=0x24

Bit (s)	Name	Description	Access	Reset
31:13	-	Reserved	-	-
12:1	GPIOBPDEN	GPIOB[12:1] 100K PD Enable. 0: Disable 1: Enable	RW	0x0
0	-	Reserved	-	-

10.4.11 SIO_OUTEN

SpecialIO Output Enable Control Register
Offset = 0x28

Bit (s)	Name	Description	Access	Reset
31:10	-	Reserved	-	-
9:0	SIO_OUTEN1	SpecialIO[9:0] Output Enable. 0: Disable 1: Enable	RW	0x0

10.4.12 SIO_INEN

SpecialIO Input Enable Control Register
Offset = 0x2C

Bit (s)	Name	Description	Access	Reset
31:10	-	Reserved	-	-
9:0	SIO_INEN	SpecialIO[9:0] Input Enable. 0: Disable 1: Enable	RW	0x0

10.4.13 SIO_DAT

SpecialIO DATA Register
Offset = 0x30

Bit (s)	Name	Description	Access	Reset
31:10	-	Reserved	-	-
9:0	SIO_DAT	SpecialIO[9:0] Input/Output Data. SIO0~SIO5 is AVCC Domain; SIO6~SIO9 is VCC Domain.	RW	0x0

10.4.14 SIO_PUEN

SpecialIO PULL UP Enable Control Register
Offset = 0x34

Bit (s)	Name	Description	Access	Reset
31:10	-	Reserved	-	-
9:0	SIO_PUEN	SpecialIO[9:0] 50K PULL UP Enable. 0: Disable 1: Enable	RW	0x0

10.4.15 SIO_PDEN

SpecialIO PULL DOWN Enable Control Register
Offset = 0x38

Bit (s)	Name	Description	Access	Reset
31:10	-	Reserved	-	-
9:0	SIO_PDEN	SpecialIO[9:0] 50K PULL DOWN Enable. 0: Disable 1: Enable	RW	0x0

10.5 PWM Register Description

10.5.1 PWM3_CTL

PWM3 Output Control Register
Offset=0x44

Bit (s)	Name	Description	Access	Reset
31:28	-	Reserved	-	-
27	POL_SEL	Polarity select: 0:PWM low voltage level active 1:PWM high voltage level active Only Active in Normal Mode	RW	0x0
26	MODE_SEL	Mode Select: 0: Normal_Mode 1: Breath_Mode	RW	0x0
25:24	Q	Time of Every Duty =1/32 ...32/32: Time of climb up and fall down: T2= (Q+1)*32*32t t is the period of CMU_PWM	RW	0x0
23:16	H	Time of Duty =32/32 : High Level Time = H*32t t is the period of CMU_PWM	RW	0x0

15:8	L	Time of Duty =0/32 : Low Level Time = L*32t t is the period of CMU_PWM	RW	0x0
7:0	DUTY	Duty Select: T Active = (Duty+1)/256 Only Active in Normal Mode	RW	0x0

10.5.2 PWM0_CTL

PWM0 Output Control Register
Offset=0x48

Bit (s)	Name	Description	Access	Reset
31:28	-	Reserved	-	-
27	POL_SEL	Polarity select: 0:PWM low voltage level active 1:PWM high voltage level active Only Active in Normal Mode	RW	0x0
26	MODE_SEL	Mode Select: 0: Normal_Mode 1: Breath_Mode	RW	0x0
25:24	Q	Time of Every Duty =1/32 …32/32: Time of climb up and fall down: T2= (Q+1)*32*32t t is the period of CMU_PWM	RW	0x0
23:16	H	Time of Duty =32/32 : High Level Time = H*32t t is the period of CMU_PWM	RW	0x0
15:8	L	Time of Duty =0/32 : Low Level Time = L*32t t is the period of CMU_PWM	RW	0x0
7:0	DUTY	Duty Select: T Active = (Duty+1)/256 Only Active in Normal Mode	RW	0x0

10.5.3 PWM1_CTL

PWM1 Output Control Register
Offset=0x4C

Bit (s)	Name	Description	Access	Reset
31:28	-	Reserved	-	-
27	POL_SEL	Polarity select: 0:PWM low voltage level active 1:PWM high voltage level active Only Active in Normal Mode	RW	0x0
26	MODE_SEL	Mode Select: 0: Normal_Mode 1: Breath_Mode	RW	0x0
25:24	Q	Time of Every Duty =1/32 …32/32: Time of climb up and fall down: T2= (Q+1)*32*32t t is the period of CMU_PWM	RW	0x0
23:16	H	Time of Duty =32/32 : High Level Time = H*32t t is the period of CMU_PWM	RW	0x0
15:8	L	Time of Duty =0/32 :	RW	0x0

		Low Level Time = L*32t t is the period of CMU_PWM		
7:0	DUTY	Duty Select: T Active = (Duty+1)/256 Only Active in Normal Mode	RW	0x0

10.5.4 PWM2_CTL

PWM2 Output Control Register
Offset=0x50

Bit (s)	Name	Description	Access	Reset
31:28	-	Reserved	-	-
27	POL_SEL	Polarity select: 0:PWM low voltage level active 1:PWM high voltage level active Only Active in Normal Mode	RW	0x0
26	MODE_SEL	Mode Select: 0: Normal_Mode 1: Breath_Mode	RW	0x0
25:24	Q	Time of Every Duty =1/32 ...32/32: Time of climb up and fall down: T2= (Q+1)*32*32t t is the period of CMU_PWM	RW	0x0
23:16	H	Time of Duty =32/32 : High Level Time = H*32t t is the period of CMU_PWM	RW	0x0
15:8	L	Time of Duty =0/32 : Low Level Time = L*32t t is the period of CMU_PWM	RW	0x0
7:0	DUTY	Duty Select: T Active = (Duty+1)/256 Only Active in Normal Mode	RW	0x0

10.6 MFP Register Description

10.6.1 MFP_CTL0

Multi-Function PAD Control Register 0
Offset=0x54

Bit (s)	Name	Description	Access	Reset
31:30	-	Reserved	-	-
29:27	GPIOA23	000: SD_DAT3 001: EM_D11 010: Reserved 011: Reserved 100: Reserved 101: PWM2 110: UART_TX1 111: SD_DAT0	RW	0
26:24	GPIOA22	000: SD_DAT2 001: EM_D10 010: Reserved 011: Reserved	RW	0

		100: UART_TX1 101: SIRQ0 110: IR_RX 111: PWM1		
23:21	GPIOA21	000: SD_DAT1 001: EM_D9 010: Reserved 011: Reserved 100: UART_RX1 101: PWM0 110: Reserved 111: Reserved	RW	0
20:13	-	Reserved	-	-
12:11	GPIOA16	00: SD_CMD 01: UART_RX1 10: Reserved 11: Reserved	RW	0
10:0	-	Reserved	-	-

10.6.2 MFP_CTL2

Multi-Function PAD Control Register2
Offset=0x5C

Bit (s)	Name	Description	Access	Reset
31:20	-	Reserved	-	-
19	GPIO_B12	0: SPI_IO3 1: Reserved	RW	0
18:16	GPIO_B11	000: SPI_IO2 010: PWM3 011: SIRQ0 100: IR_RX 101: SD_CLK0Others: Reserved	RW	0
15	-	Reserved	-	-
14:13	GPIO_B4	00: Reserved 01: Reserved 10: Reserved 11: Reserved	RW	0
12:9	-	Reserved	-	-
8:7	GPIOA31	00: SPI_MOSI 01: SPI_MISO 10: Reserved 11: Reserved	RW	0
6:5	-	Reserved	-	-
4:2	GPIOA29	000: SPI_SCLK 001: SPI_SS 010: SD_CLK1 100: SIRQ1 Others: Reserved	RW	0
1:0	GPIOA28	00: SPI_SS 01: SPI_MOSI 10: Reserved 11: Reserved	RW	0

10.6.3 MFP_CTL3

Multi-Function PAD Control Register 3
Offset = 0x60

Bit (s)	Name	Description	Access	Reset
31:24	-	Reserved	-	-
23:22	GPIOB9	00: LCD_SEG30 01: PWM2 10: I2S_MCLK 11: Reserved	RW	0
21:20	GPIOB8	00: LCD_SEG29 01: PWM1 10: I2S_BCLK 11: Reserved		
19:18	VROS	0x0: VROS 0x1: Reserved 0x2: SpecialIO9 0x3: Reserved	RW	0
17:16	AOUTR	0x0: AOUTR / AOUTRP 0x1: Reserved 0x2: SpecialIO8 0x3: Reserved	RW	0
15:14	VRO	0x0: VRO 0x1: Reserved 0x2: SpecialIO7 0x3: Reserved	RW	0
13:12	AOUTL	0x0: AOUTL / AOUTLP 0x1: Reserved 0x2: SpecialIO6 0x3: Reserved	RW	0
11:8	-	Reserved	-	-
7	AUX1R	0x0: AUX1R 0x1: SpecialIO5	RW	0
6	AUX1L	0x0: AUX1L 0x1: SpecialIO4	RW	0
5	AUX0R	0x0: AUX0R 0x1: SpecialIO3	RW	0
4	AUX0L	0x0: AUX0L 0x1: SpecialIO2	RW	0
3:2	MICINR	0x0: MICINR/ MICINLN 0x1: DMICDAT 0x2: SpecialIO1 0x3: Reserved	RW	0
1:0	MICINL	0x0: MICINL/ MICINLP 0x1: DMICCLK 0x2: SpecialIO0 0x3: Reserved	RW	0

10.7 Analog/Digital Select Register Description

10.7.1 AD_SELECT

Analog/Digital Select Register
Offset=0x64

Bit (s)	Name	Description	Access	Reset
31:14	-	Reserved	-	-
15:14	GPIOA23	00: GPIOA23 is used as digital function, 01: GPIOA23 is used as LRADC3 (Analog Function), 10: GPIOA23 is used as TK7 (Analog Function), 11: Reserved	RW	0
13:8	-	Reserved	-	-
7:6	GPIOB9	00: GPIOB9 is used as digital function 01: GPIOB9 is used as TK_TK3 (Analog Function) Others: Reserved	RW	0
5:4	GPIOB8	00: GPIOB8 is used as digital function 01: GPIOB8 is used as TK_TK2 (Analog Function) Others: Reserved	RW	0
3:2	-	Reserved	-	-
1:0	GPIOA21	00: GPIOA21 is used as digital function, 01: GPIOA21 is used as TEMPADC (Analog Function) 10: GPIOA21 is used as TK0 (Analog Function) 11: Reserved	RW	0

10.7.2 AD_SELECT1

Analog/Digital Select Register 1
Offset=0xA4

Bit (s)	Name	Description	Access	Reset
31:3	-	Reserved	-	-
2:1	GPIOA22	00: GPIOA22 is used as digital function, 01: GPIOA22 is used as LRADC2 (Analog Function), 10: GPIOA22 is used as SHEILD (Analog Function), 11: Reserved	RW	0
0	-	Reserved	-	-

10.8 Pad Drive Register Description

10.8.1 PADPUPD

PAD PU PD Resistance Control Register
Offset=0x68

Bit (s)	Name	Description	Access	Reset
31:10	-	Reserved	-	-
9	SD_DATA4_7	MMC/SD Data4~7 50k PU Select 0:Disable 1:Enable	RW	0
8	-	Reserved	-	-
7	SD_CMD	MMC/SD CMD 50k PU Enable 0:Disable	RW	0

		1:Enable		
6	SD_DATA0_3	MMC/SD Data0~3 50k PU Select 0:Disable 1:Enable	RW	0
5	SIRQ1PD	SIRQ1 100k PD Enable 0:Disable 1:Enable	RW	0
4	SIRQ1PU	SIRQ1 100k PU Enable 0:Disable 1:Enable	RW	0
3	SIRQ0PD	SIRQ0 100k PD Enable 0:Disable 1:Enable	RW	0
2	SIRQ0PU	SIRQ0 100k PU Enable 0:Disable 1:Enable	RW	0
1	-	Reserved	-	-
0	UART_RX1	UART_RX1 10k PU Enable 0:Disable 1:Enable	RW	0

10.8.2 PAD_SMIT

PAD Schmitt Control Register
Offset=0x6C

Bit (s)	Name	Description	Access	Reset
31:23	-	Reserved	-	-
22	SPIBT_SS	SPIBT_SS & SPI_SS SMIT Enable 0:Disable 1:Enable	RW	1
21	-	Reserved	-	-
20	GPIOA29	SPI_SS & SIRQ1 SMIT Enable 0:Disable 1:Enable	RW	1
19	GPIOA28	SPI_SS SMIT Enable 0:Disable 1:Enable	RW	1
18	GPIOA22	SIRQ0 &IR_RX SMIT Enable 0:Disable 1:Enable	RW	1
17:7	-	Reserved	-	-
6	GPIOB11	SMIT Enable 0:Disable 1:Enable	RW	1
5	GPIOB9	DEJ_TDI SMIT Enable 0: Disable 1: Enable	RW	1
4	GPIOB8	DEJ_TMS SMIT Enable 0: Disable 1: Enable	RW	1
3:0	-	Reserved	-	-

10.8.3 PADDRV1

PAD Drive Control Register 1
Offset=0x74

Bit (s)	Name	Description	Access	Reset
31:21	-	Reserved	-	-
20:18	GPIOA16	GPIOA16 PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	RW	1
17:0	-	Reserved	-	-

10.8.4 PADDRV2

PAD Drive Control Register 2
Offset=0x78

Bit (s)	Name	Description	Access	Reset
31:30	-	Reserved	-	-
29:27	GPIOA29	GPIOA29 PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	RW	0x7
26:24	GPIOA28	GPIOA28 PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	RW	0x7
23:12	-	Reserved	-	-
11:9	GPIOA23	GPIOA23 PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	RW	1
8:6	GPIOA22	GPIOA22 PAD Drive Control 000: Level 1	RW	1

		001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8		
5:3	GPIOA21	GPIOA21 PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	RW	1
2:0	-	Reserved	-	-

10.8.5 PADDRV3

PAD Drive Control Register 3
Offset = 0x7C

Bit (s)	Name	Description	Access	Reset
31:30	SPIBT_SS	SPIBT_SS PAD Drive Control 00: Level 1 01: Level 2 10: Level 4 11: Level 8	RW	0x3
29:25	-	Reserved	-	-
26:24	GPIOB9	GPIOB9 PAD Drive control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	RW	0x1
23:21	GPIOB8	GPIOB8 PAD Drive control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	RW	0x1
20:0	-	Reserved	-	-

10.8.6 PADDRV4

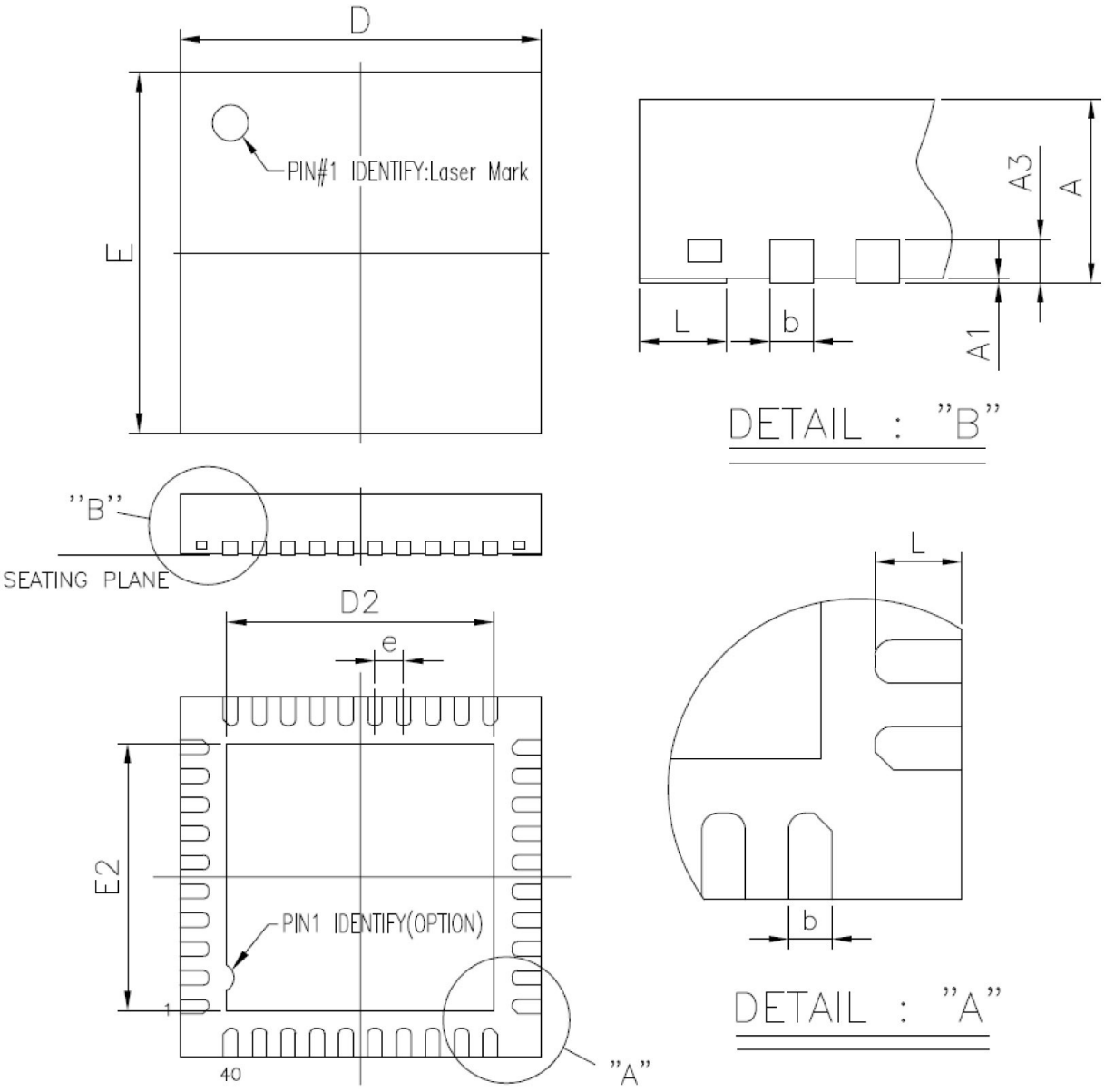
PAD Drive Control Register 4

Offset = 0x40

Bit (s)	Name	Description	Access	Reset
31:30	SPIBT_SS	SPIBT_SS PAD Drive Control 00: Level 1 01: Level 2 10: Level 4 11: Level 8	RW	0x3
29:28	SPIBT_CLK	SPIBT_CLK PAD Drive Control 00: Level 1 01: Level 2 10: Level 4 11: Level 8	RW	0x3
27:26	SPIBT_MOSI	SPIBT_MOSI PAD Drive Control 00: Level 1 01: Level 2 10: Level 4 11: Level 8	RW	0x3
25:24	SPIBT_MISO	SPIBT_MISO PAD Drive Control 00: Level 1 01: Level 2 10: Level 4 11: Level 8	RW	0x3
23:21	GPIOA31	GPIOA31 PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	RW	0x7
20:15	-	Reserved	-	-
14:12	GPIOB11	GPIOB11 PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	RW	0x1
11:9	SIO9	SIO9 PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	RW	0x1
8:6	SIO8	SIO8 PAD Drive Control 000: Level 1 001: Level 2 010: Level 3	RW	0x1

		011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8		
5:3	SIO7	SIO7 PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	RW	0x1
2:0	SIO6	SIO6 PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	RW	0x1

11 Package and Drawings



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3		0.20 REF			0.008 REF	
b	0.15	0.20	0.25	0.006	0.008	0.010
D/E		5.00 BSC			0.197 BSC	
D2/E2	3.45	3.60	3.75	0.136	0.142	0.148
e		0.40 BSC			0.016 BSC	
L	0.30	0.40	0.50	0.012	0.016	0.020

Figure 11-1 ATS2823B Package and Dimension

12 Electrical Characteristics

12.1 Absolute Maximum Ratings

Table 12-1 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Ambient Temperature	Tamb	TBD	TBD	°C
Storage temperature	Tstg	-55	+150	°C
ESD Stress voltage	Vesd (Human body model)	3500	-	V
Supply Voltage	DC5V	-0.3	9	V
	BAT	-0.3	5	V
	VCC/AVCC/BTVCC	-0.3	3.6	V
	VDD	-0.3	1.32	V
Input Voltage	3.3V IO	-0.3	3.6	V
	1.2V IO	-0.3	1.32	V

Note:

Even if one of the above parameters exceeds the absolute maximum ratings momentarily, the quality of the product may be degraded. The absolute maximum ratings, therefore, specify the value exceeding, which the product may be physically damaged. Use the product well within these ratings.

12.2 Recommended PWR Supply

Table 12-2 Recommended PWR Supply

Supply Voltage	Min	Typ	Max	Unit
BAT (Li)	3.4	3.8	4.3	V
DC5V	4.5	5.0	7.0	V
VCC/AVCC/BTVCC	2.8	3.1	3.4	V
VDD/RTCVDD/AVDD	1.08	1.2	1.32	V

Note:

1) *According to different application, the VDD can be setting different voltage. For optimum CPU performance, the VDD should be higher than 1.2V; for reduced the PWR consumption, the VDD can supply with 1.0V.*
2) *If the system is supply with Li-BAT, the range of DC5V would be 3.3V~4.2V; or the supply source of system is come from DC5V, DC5V would be 4.5V~5.2V.*

12.3 DC Characteristics

Table 12-3 DC Parameters for +3.3V IO Pin with Schmitt Trigger Off

Parameter	Symbol	Min.	Max.	Unit	Condition
Low-level input voltage	VIL	-	0.8	V	VCC = 3.1V Tamb = -10 to 70 °C
High-level input voltage	VIH	2.0	-	V	
Low-level output voltage	VOL	-	0.4	V	
High-level output voltage	VOH	2.4	-	V	

Table 12-4 DC Parameter for +3.3V IO Pin with Schmitt Trigger On

Parameter	Symbol	Min.	Max.	Unit	Condition

Schmitt trigger positive-going threshold	VT+	-	1.9	V	VCC=3.1V Tamb = -10 to 70 °C
Schmitt trigger negative-going threshold	VT-	1.2	-	V	

12.4 Battery Charger

Table 12-5 Battery Charger

Parameter	Min.	Typ.	Max.	Unit
Input Voltage	BAT+0.1	5	7	V
Charge Current (CC Mode)	25	25	600	mA
Trickle Charge Current	2.5	2.5	60	mA
Trickle Charge Threshold Voltage	-	3.0	-	V
Regulated Output (Float) Voltage	4.2	4.26	4.41	V

12.5 PWR Consumption

Table 12-6 PWR Consumption Table

VDD = 1.2V @ 25°C unless otherwise specified

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
A2DP	Ct	Peak Current	-	19	-	mA
HFP	Cr	Receive Current	-	21	-	mA
Sniff Mode	Cs	500ms	-	-	800	µA
Deep Sleep	Cd	Vbat = 3.8V	0.1	-	1	µA

12.6 Bluetooth Characteristics

12.6.1 Transmitter

Table 12-7 Basic Data Rate of Transmitter

VDD = 1.2V @ 25°C

Parameter	Condition	Min.	Typ.	Max.	Unit
Maximum RF Transmit PWR	-	-	8[1]	-	dBm
RF PWR Control Range	-	-	20	-	dB
20dB Bandwidth for Modulated Carrier	-	-	900	-	KHz
Adjacent Channel Transmit	+2 MHz	-	-	-20	dBm
	-2 MHz	-	-	-20	dBm
	+3 MHz	-	-	-40	dBm
	-3 MHz	-	-	-40	dBm
Frequency Deviation	Δf1avg Maximum Modulation	-	169	-	KHz
	Δf2max Maximum Modulation	-	126	-	KHz
	Δf1avg/Δf2avg	-	0.9	-	
Initial Carrier Frequency Tolerance	-	-75	-	75	KHz
Frequency Drift	HD1 Packet	-25	-	25	KHz
	HD3 Packet	-40	-	40	KHz

	HD5 Packet	-40	-	40	KHz
Frequency Drift Rate	-	-20	-	20	KHz/50us
Harmonic Content	-	-	-50	-	dBm

The maximum RF transmit PWR could reach to 8dBm with appropriate settings.

Table 12-8 Enhanced Data Rate of Transmitter

Core Supply Voltage = 1.2V @ 25°C

Parameter	Condition	Min.	Typ.	Max.	Unit
Relative Transmit PWR	-	-	-0.8	-	dB
π/4 DQPSK max carrier frequency stability $\|\omega_0\|$	-	-10	-	10	KHz
π/4 DQPSK max carrier frequency stability $\|\omega_i\|$	-	-75	-	75	KHz
π/4 DQPSK max carrier frequency stability $\|\omega_0+\omega_i\|$	-	-75	-	75	KHz
8DPSK max carrier frequency stability $\|\omega_0\|$	-	-10	-	10	KHz
8DPSK max carrier frequency stability $\|\omega_i\|$	-	-75	-	75	KHz
8DPSK max carrier frequency stability $\|\omega_0+\omega_i\|$	-	-75	-	75	KHz
π/4 DQPSK Modulation Accuracy	RMS DEVIN	-	-	20	%
	99% DEVM	99	-	-	%
	Peak DEVM	-	-	35	%
8DPSK Modulation Accuracy	RMS DEVIN	-	-	13	%
	99% DEVM	99	-	-	%
	Peak DEVM	-	-	25	%
In-band spurious emissions	F > F0 + 3MHz	-	-	-40	dBm
	F < F0 - 3MHz	-	-	-40	dBm
	F = F0 + 3MHz	-	-	-40	dBm
	F = F0 - 3MHz	-	-	-40	dBm
	F = F0 + 2MHz	-	-	-20	dBm
	F = F0 - 2MHz	-	-	-20	dBm
	F = F0 + 1MHz	-	-	-26	dB
	F = F0 - 1MHz	-	-	-26	dB
EDR Differential Phase Encoding	-	99	-	-	%

The maximum RF transmit PWR could reach to 8dBm with appropriate settings.

12.6.2 Receiver

Table 12-9 Basic Data Rate of Receiver

Core Supply Voltage = 1.2V @ 25°C

Parameter	Condition	Min.	Typ.	Max.	Unit
Sensitivity at 0.1% BER	2.404GHz	-	-93	-	dBm
	2.441GHz	-	-93	-	dBm
	2.480GHz	-	-92	-	dBm
Maximum Input PWR at 0.1% BER	-	-20	-	-	dBm
Co-Channel Interface	-	-	-	11	dB
Adjacent Channel Selectivity C/I	$F = F_0 + 1MHz$	-	-	0	dB
	$F = F_0 - 1MHz$	-	-	0	dB
	$F = F_0 + 2MHz$	-	-	-30	dB
	$F = F_0 - 2MHz$	-	-	-20	dB
	$F = F_0 + 3MHz$	-	-	-40	dB
	$F = F_{image}$	-	-	-9	dB
Maximum Level of Intermodulation Interface	-	-39	-	-	dBm

Blocking @ Pin = -67dBm with 0.1% BER	30-2000 MHz	-10	-	-	dBm
	2000-2400 MHz	-27	-	-	dBm
	2500-3000 MHz	-27	-	-	dBm
	3000-12750 MHz	-10	-	-	dBm

Table 12-10 Enhanced Data Rate of Receiver

Core Supply Voltage = 1.2V @ 25°C

Parameter	Condition		Min.	Typ.	Max.	Unit
Sensitivity at 0.01% BER	π/4 DQPSK			-93		dBm
	8DPSK			-85		dBm
Maximum Input PWR at 0.1% BER	π/4 DQPSK		-20			dBm
	8DPSK		-20			dBm
Co-Channel Interference	π/4 DQPSK				13	dB
	8DPSK				21	dB
Adjacent Channel Selectivity C/I	$F = F_0 + 1MHz$	π/4 DQPSK		0		dB
		8DPSK		5		dB
	$F = F_0 - 1MHz$	π/4 DQPSK		0		dB
		8DPSK		5		dB
	$F = F_0 + 2MHz$	π/4 DQPSK		-30		dB
		8DPSK		-25		dB
	$F = F_0 - 2MHz$	π/4 DQPSK		-20		dB
		8DPSK		-13		dB
	$F = F_0 + 3MHz$	π/4 DQPSK		-40		dB
		8DPSK		-33		dB
	$F = F_{image}$	π/4 DQPSK		-7		dB
		8DPSK		0		dB

12.7 Audio ADC

Table 12-11 Audio ADC Parameters

Pre-Amplifier						
Parameter	**Conditions**		**Min**	**Typ**	**Max**	**Unit**
Full Scale Input Voltage	THD+N < 1%		-	-	2.8	Vpp
Analogue gain	AUX OP	-	-12	-	6	dB
	MIC OP	Single Ended	-6	-	32	dB
		Full Differential	0	-	38	
Analogue to Digital Converter						
Resolution	-		-	-	16	Bits
Input Sample Rate	-		8	-	48	kHz
SNR	fin = 1kHz@Full Scale Input Voltage B/W = 22Hz~22kHz Fs=48kHz		-	90	-	dB
Dynamic Range	fin = 1kHz@-40dBFS Input Voltage B/W = 22Hz~22kHz Fs=48kHz		-	90	-	dB
THD+N	fin = 1kHz(input=1.6Vpp) B/W = 22Hz~22kHz Fs=48kHz		-	-82	-	dB
Digital gain	-		0	-	12	dB

12.8 Stereo DAC

Table 12-12 Stereo DAC Parameters

Digital to Analogue Converter						
Parameter	**Conditions**		**Min**	**Typ**	**Max**	**Unit**
Resolution	-		-	-	20	Bits
Output Sample Rate	-		8	-	48	kHz
SNR	fin = 1kHz@0dBFS input B/W = 22Hz~22kHz Fs=48kHz,Load=16Ω	-	-	98	-	dB
		A-Weighting	-	101	-	dB
Dynamic Range	fin = 1kHz@-48dBFS input B/W = 22Hz~22kHz Fs=48kHz,Load=16Ω	-	-	98	-	dB
		A-Weighting	-	101	-	dB
THD+N	fin = 1kHz@0dBFS input B/W = 22Hz~22kHz Fs=48kHz,Load=16Ω	-	-	-87	-	dB
Digital gain	-		<-60	-	24	dB
Stereo crosstalk	fin = 1kHz@0dBFS input	-	-	-78	-	dB
PWR Amplifier						
Analogue gain	-		-60	-	0	dB
Max Amplitude/PWR	fin = 1kHz@0dBFS input Fs=48kHz,Load=16Ω	Single Ended Output	-	-	550	mVrms
			-	-	18.5	mW
	fin = 1kHz@0dBFS input Fs=48kHz,Load=16Ω	Full Differential Output	-	-	60	mW
	fin = 1kHz@0dBFS input Fs=48kHz,Load=10KΩ	Full Differential Output	-	-	1.8	Vrms

Acronyms and Abbreviations

Abbreviations	Descriptions
AEC	acoustic echo cancellers
AXI	AMBA Advanced extensible Interface
ADC	Analog-to-Digital-Converter
ALU	Arithmetic Logic Unit
CC	Constant Current
CP0	Control Coprocessor 0
UDI	CorExtend® User Defined Instructions
DAC	Digital-to-Analog-Converter
DMA	Direct Memory Access
ER	Error Resilience
FMT	Fixed Mapping Translation
FSM	Flash State Machine
GPIO	General Purpose Input Output
GPRs	general-purpose registers
HOSC	High Frequency OSC (24MHz)
INTC	Interrupt Controller
IRQ	Interrupt Request
LOSC	Low Frequency OSC, include internal RC OSC (about 32K) and external LOSC (32.768K)
LFPLL	Low Frequency source PLL
MIC	Microphone
MFP	Multiple Function PAD
MDU	Multiply-Divide Unit
NMI	Nonmaskable Interrupt
OSC	Oscillator
PNS	Perceptual Noise Substitution (added in MPEG-4)
PA	Power Amplifier
SIE	Serial Interface Engine
SBR	Spectral band replication
TLB	translation lookaside buffer
WMA	Windows Media Audio

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