1. Description

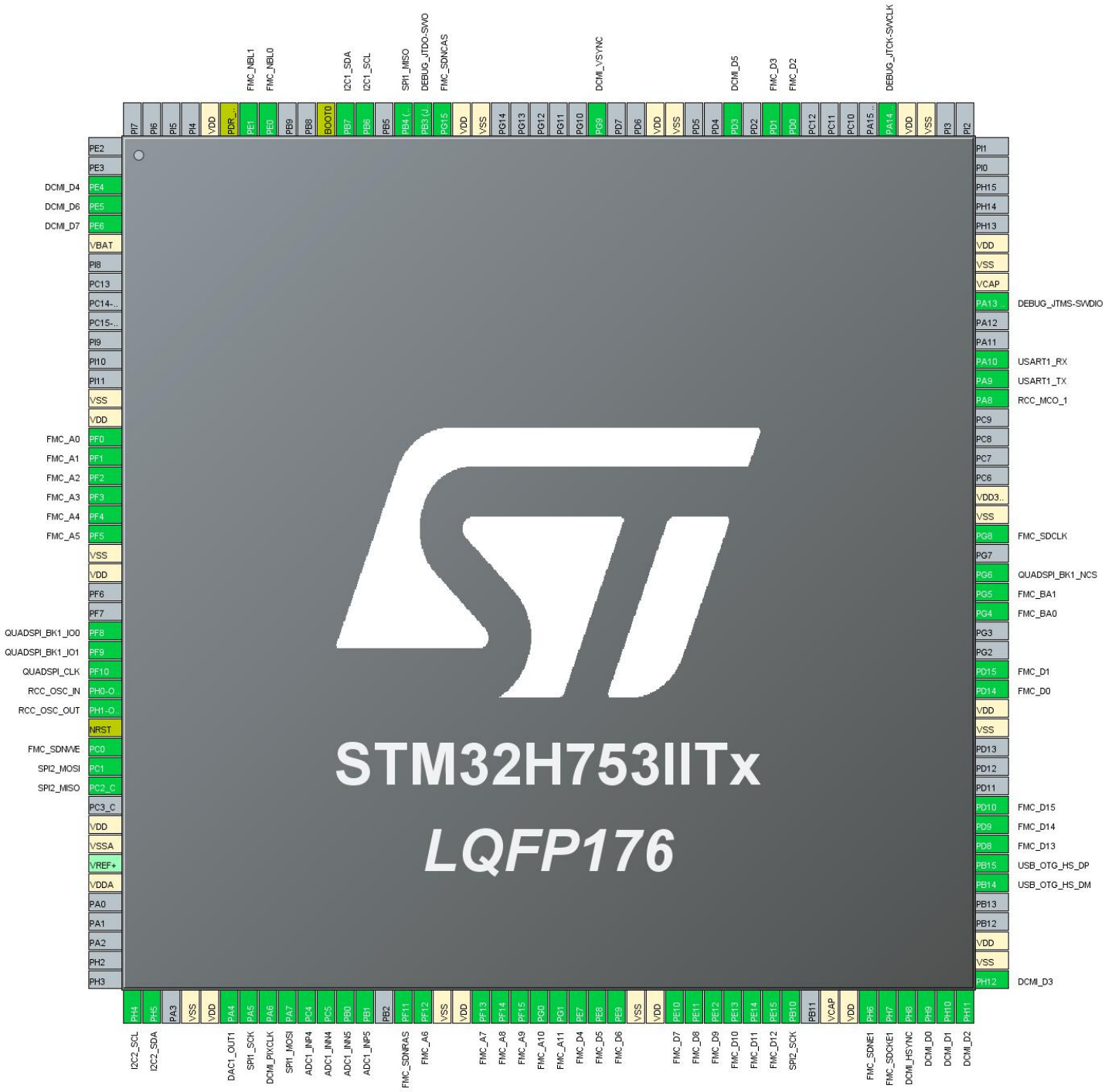
1.1. Project

Project Name	H7_pcb_test
Board Name	custom
Generated with:	STM32CubeMX 5.6.0
Date	06/02/2020

1.2. MCU

MCU Series	STM32H7
MCU Line	STM32H743/753
MCU name	STM32H753IITx
MCU Package	LQFP176
MCU Pin number	176

2. Pinout Configuration



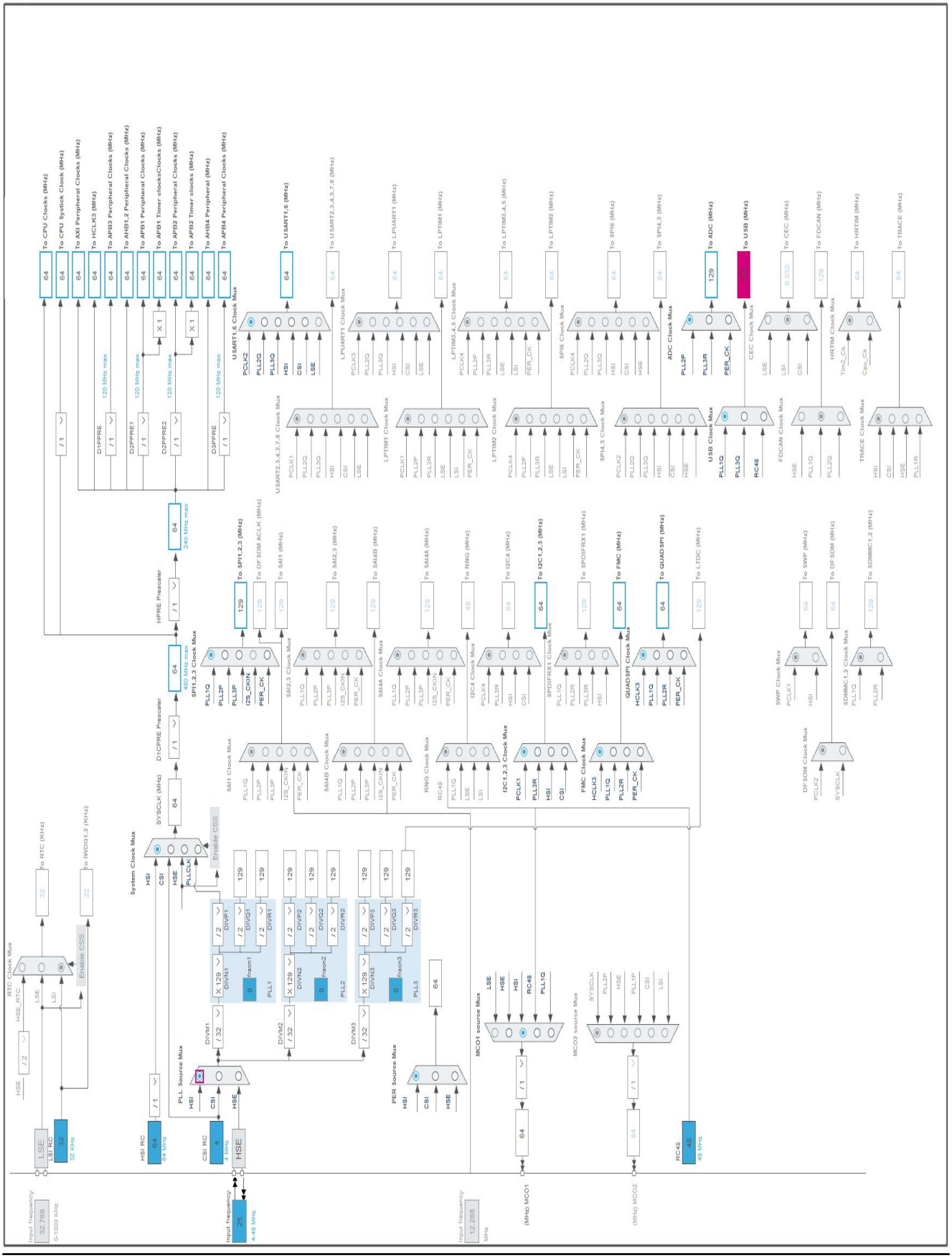
3. Pins Configuration

Pin Number LQFP176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
3	PE4	I/O	DCMI_D4	
4	PE5	I/O	DCMI_D6	
5	PE6	I/O	DCMI_D7	
6	VBAT	Power		
14	VSS	Power		
15	VDD	Power		
16	PF0	I/O	FMC_A0	
17	PF1	I/O	FMC_A1	
18	PF2	I/O	FMC_A2	
19	PF3	I/O	FMC_A3	
20	PF4	I/O	FMC_A4	
21	PF5	I/O	FMC_A5	
22	VSS	Power		
23	VDD	Power		
26	PF8	I/O	QUADSPI_BK1_IO0	
27	PF9	I/O	QUADSPI_BK1_IO1	
28	PF10	I/O	QUADSPI_CLK	
29	PH0-OSC_IN (PH0)	I/O	RCC_OSC_IN	
30	PH1-OSC_OUT (PH1)	I/O	RCC_OSC_OUT	
31	NRST	Reset		
32	PC0	I/O	FMC_SDNWE	
33	PC1	I/O	SPI2_MOSI	
34	PC2_C	I/O	SPI2_MISO	
36	VDD	Power		
37	VSSA	Power		
39	VDDA	Power		
45	PH4	I/O	I2C2_SCL	
46	PH5	I/O	I2C2_SDA	
48	VSS	Power		
49	VDD	Power		
50	PA4	I/O	DAC1_OUT1	
51	PA5	I/O	SPI1_SCK	
52	PA6	I/O	DCMI_PIXCLK	
53	PA7	I/O	SPI1_MOSI	
54	PC4	I/O	ADC1_INP4	
55	PC5	I/O	ADC1_INN4	

Pin Number LQFP176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
56	PB0	I/O	ADC1_INN5	
57	PB1	I/O	ADC1_INP5	
59	PF11	I/O	FMC_SDNRAS	
60	PF12	I/O	FMC_A6	
61	VSS	Power		
62	VDD	Power		
63	PF13	I/O	FMC_A7	
64	PF14	I/O	FMC_A8	
65	PF15	I/O	FMC_A9	
66	PG0	I/O	FMC_A10	
67	PG1	I/O	FMC_A11	
68	PE7	I/O	FMC_D4	
69	PE8	I/O	FMC_D5	
70	PE9	I/O	FMC_D6	
71	VSS	Power		
72	VDD	Power		
73	PE10	I/O	FMC_D7	
74	PE11	I/O	FMC_D8	
75	PE12	I/O	FMC_D9	
76	PE13	I/O	FMC_D10	
77	PE14	I/O	FMC_D11	
78	PE15	I/O	FMC_D12	
79	PB10	I/O	SPI2_SCK	
81	VCAP	Power		
82	VDD	Power		
83	PH6	I/O	FMC_SDNE1	
84	PH7	I/O	FMC_SDCKE1	
85	PH8	I/O	DCMI_HSYNC	
86	PH9	I/O	DCMI_D0	
87	PH10	I/O	DCMI_D1	
88	PH11	I/O	DCMI_D2	
89	PH12	I/O	DCMI_D3	
90	VSS	Power		
91	VDD	Power		
94	PB14	I/O	USB_OTG_HS_DM	
95	PB15	I/O	USB_OTG_HS_DP	
96	PD8	I/O	FMC_D13	
97	PD9	I/O	FMC_D14	
98	PD10	I/O	FMC_D15	

Pin Number LQFP176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
102	VSS	Power		
103	VDD	Power		
104	PD14	I/O	FMC_D0	
105	PD15	I/O	FMC_D1	
108	PG4	I/O	FMC_BA0	
109	PG5	I/O	FMC_BA1	
110	PG6	I/O	QUADSPI_BK1_NCS	
112	PG8	I/O	FMC_SDCLK	
113	VSS	Power		
114	VDD33_USB	Power		
119	PA8	I/O	RCC_MCO_1	
120	PA9	I/O	USART1_TX	
121	PA10	I/O	USART1_RX	
124	PA13 (JTMS/SWDIO)	I/O	DEBUG_JTMS-SWDIO	
125	VCAP	Power		
126	VSS	Power		
127	VDD	Power		
135	VSS	Power		
136	VDD	Power		
137	PA14 (JTCK/SWCLK)	I/O	DEBUG_JTCK-SWCLK	
142	PD0	I/O	FMC_D2	
143	PD1	I/O	FMC_D3	
145	PD3	I/O	DCMI_D5	
148	VSS	Power		
149	VDD	Power		
152	PG9	I/O	DCMI_VSYNC	
158	VSS	Power		
159	VDD	Power		
160	PG15	I/O	FMC_SDNCAS	
161	PB3 (JTDO/TRACESWO)	I/O	DEBUG_JTDO-SWO	
162	PB4 (NJTRST)	I/O	SPI1_MISO	
164	PB6	I/O	I2C1_SCL	
165	PB7	I/O	I2C1_SDA	
166	BOOT0	Boot		
169	PE0	I/O	FMC_NBL0	
170	PE1	I/O	FMC_NBL1	
171	PDR_ON	Reset		
172	VDD	Power		

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	H7_pcb_test
Project Folder	C:\Users\alber\Documents\FBK\H7_pcb_test
Toolchain / IDE	EWARM V8.32
Firmware Package Name and Version	STM32Cube FW_H7 V1.7.0

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32H7
Line	STM32H743/753
MCU	STM32H753IITx
Datasheet	DS12117_Rev6

6.2. Parameter Selection

Temperature	25
Vdd	3.0

6.3. Battery Selection

Battery	Alkaline(9V)
Capacity	625.0 mAh
Self Discharge	0.3 %/month
Nominal Voltage	9.0 V
Max Cont Current	200.0 mA
Max Pulse Current	0.0 mA
Cells in series	1
Cells in parallel	1

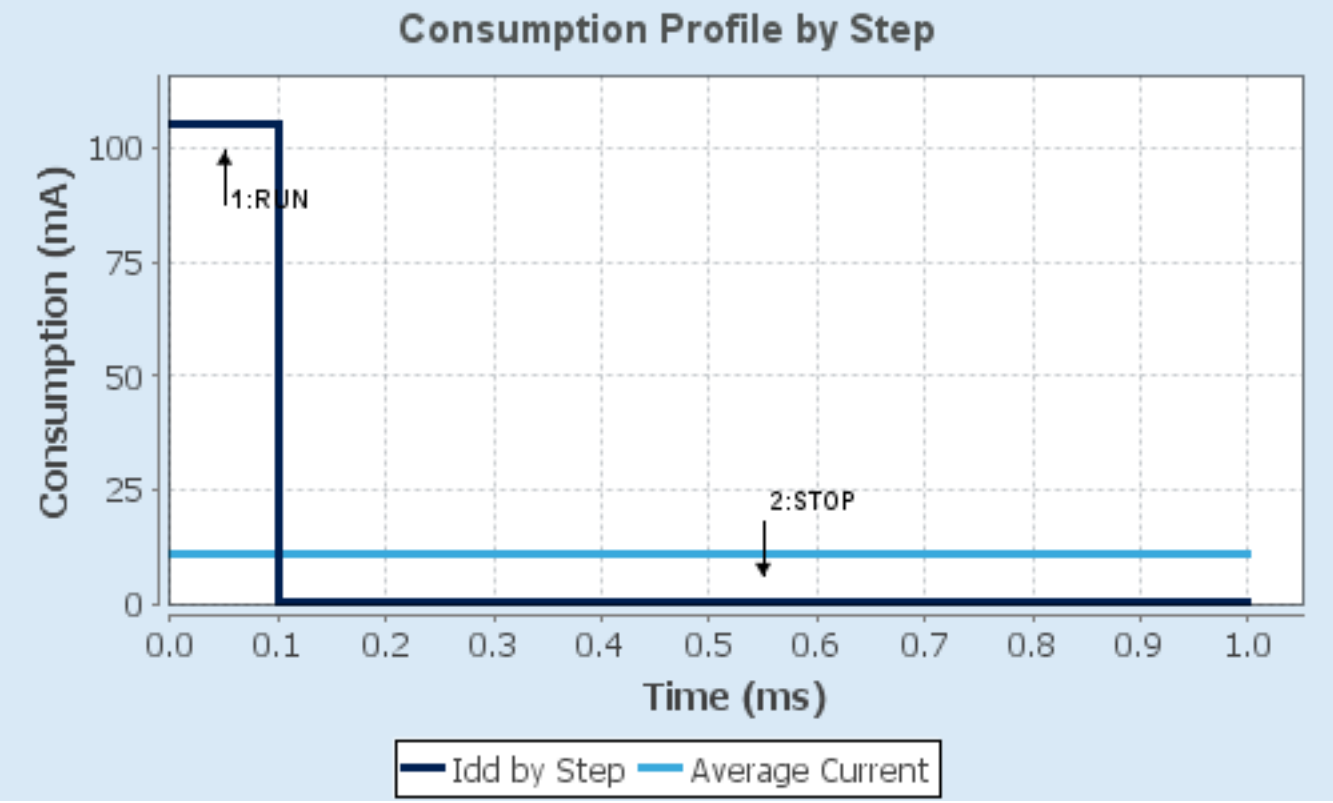
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	VOS1: Scale1-High	SVOS5: System-Scale5
D1 Mode	DRUN/CRUN	DSTANDBY
D2 Mode	DSTANDBY	DSTANDBY
D3 Mode	DRUN	DSTOP
Fetch Type	FLASH_A	NA
CPU Frequency	400 MHz	0 Hz
Clock Configuration	HSE BYP PLL Flash-ON Cache-ON	Flash-LP
Clock Source Frequency	25 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	105 mA	170 µA
Duration	0.1 ms	0.9 ms
DMIPS	856.0	0.0
Ta Max	111.46	124.98
Category	In DS Table	In DS Table

6.5. RESULTS

Sequence Time	1 ms	Average Current	10.65 mA
Battery Life	2 days, 10 hours	Average DMIPS	856.0 DMIPS

6.6. Chart


Consumption Profile by Step
Consumption (mA)
100
75
50
25
0
1:RUN
2:STOP
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

7. IPs and Middleware Configuration

7.1. ADC1

IN4: IN4 Differential

IN5: IN5 Differential

7.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	Asynchronous clock mode divided by 1
Resolution	ADC 16-bit resolution
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data preserved
Conversion Data Management Mode	Regular Conversion data stored in DR register only
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Left Bit Shift	No bit shift
Enable Regular Oversampling	Disable
Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 4
Sampling Time	1.5 Cycles
Offset Number	No offset

ADC_Injected_ConversionMode:

Enable Injected Conversions	Disable

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

7.2. DAC1

OUT1 mode: Connected to external pin only

7.2.1. Parameter Settings:

DAC Out1 Settings:

Output Buffer	Enable
Trigger	None
User Trimming	Factory trimming
Sample And Hold	Sampleandhold Disable

7.3. DCMI

DCMI: Slave 8 bits External Synchro

7.3.1. Parameter Settings:

Mode Config:

Pixel clock polarity	Active on Falling edge
Vertical synchronization polarity	Active Low
Horizontal synchronization polarity	Active Low
Frequency of frame capture	All frames are captured
JPEG mode	Disabled

Interface Capture Config:

Byte Select Mode	Interface captures all received bytes
Line Select Mode	Interface captures all received lines

7.4. DEBUG

Debug: Trace Asynchronous Sw

7.5. DMA2D

mode: Activated

7.5.1. Parameter Settings:

Basic Parameters:

Transfer Mode	Memory to Memory
Color Mode	ARGB8888

Output Offset	0
DMA2D Bytes Swap	Bytes in regular order in output FIFO
DMA2D Line Offset Mode	Line offsets expressed in pixels

Foreground layer Configuration:

DMA2D Input Color Mode	ARGB8888
DMA2D ALPHA MODE	No modification of the alpha channel value
Input Alpha	0
Input Offset	0
DMA2D ALPHA Inversion	Regular Alpha
DMA2D Red and Blue swap	Regular mode (RGB or ARGB)
DMA2D Chroma Sub-Sampling Mode	No chroma sub-sampling 4:4:4

7.6. FMC

SDRAM 1

Clock and chip enable: SDCKE1+SDNE1

Internal bank number: 4 banks

Address: 12 bits

Data: 16 bits

Byte enable: 16-bit byte enable

7.6.1. SDRAM 1:

SDRAM control:

Bank	SDRAM bank 2
Number of column address bits	8 bits
Number of row address bits	12 bits
CAS latency	1 memory clock cycle
Write protection	Disabled
SDRAM common clock	Disabled
SDRAM common burst read	Disabled
SDRAM common read pipe delay	0 HCLK clock cycle

SDRAM timing in memory clock cycles:

Load mode register to active delay	16
Exit self-refresh delay	16
Self-refresh time	16
SDRAM common row cycle delay	16
Write recovery time	16
SDRAM common row precharge delay	16
Row to column delay	16

7.6.2. Bank Mapping:

Mapping parameters:

FMC bank mapping	Default mapping

7.7. GPIO

7.8. I2C1

I2C: I2C

7.8.1. Parameter Settings:

Timing configuration:

I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	0x10707DBC

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

7.9. I2C2

I2C: I2C

7.9.1. Parameter Settings:

Timing configuration:

I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0

Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	0x10707DBC

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

7.10. QUADSPI

QuadSPI Mode: Bank1 with Single/Dual Lines

7.10.1. Parameter Settings:

General Parameters:

Clock Prescaler	255
Fifo Threshold	1
Sample Shifting	No Sample Shifting
Flash Size	1
Chip Select High Time	1 Cycle
Clock Mode	Low
Flash ID	Flash ID 1
Dual Flash	Disabled

7.11. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

mode: Master Clock Output 1

7.11.1. Parameter Settings:

SupplySource	PWR_LDO_SUPPLY

RCC Parameters:

TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000
CSI Calibration Value	16
HSI Calibration Value	32

System Parameters:

VDD voltage (V)	3.3
Flash Latency(WS)	0 WS (1 CPU cycle)

Power Parameters:

Power Regulator Voltage Scale	Power Regulator Voltage Scale 3

PLL range Parameters:

PLL1 clock Input range	Between 2 and 4 MHz
PLL2 input frequency range	Between 2 and 4 MHz
PLL1 clock Output range	Wide VCO range
PLL2 clock Output range	Wide VCO range

7.12. SPI1

Mode: Full-Duplex Master

7.12.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	4 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	**64.5 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software
Fifo Threshold	Fifo Threshold 01 Data
Tx Crc Initialization Pattern	All Zero Pattern
Rx Crc Initialization Pattern	All Zero Pattern
Nss Polarity	Nss Polarity Low
Master Ss Idleness	00 Cycle
Master Inter Data Idleness	00 Cycle
Master Receiver Auto Susp	Disable
Master Keep Io State	Master Keep Io State Disable
IO Swap	Disabled

7.13. SPI2

Mode: Full-Duplex Master

7.13.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	4 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	**64.5 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software
Fifo Threshold	Fifo Threshold 01 Data
Tx Crc Initialization Pattern	All Zero Pattern
Rx Crc Initialization Pattern	All Zero Pattern
Nss Polarity	Nss Polarity Low
Master Ss Idleness	00 Cycle
Master Inter Data Idleness	00 Cycle
Master Receiver Auto Susp	Disable
Master Keep Io State	Master Keep Io State Disable
IO Swap	Disabled

7.14. SYS

Timebase Source: SysTick

7.15. USART1

Mode: Asynchronous

7.15.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None

Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	clock /1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.16. USB_OTG_HS

Internal FS Phy: Device_Only

7.16.1. Parameter Settings:

Speed	Device Full Speed 12MBit/s
Enable internal IP DMA	Disabled
Physical interface	Internal Phy
Low power	Disabled
Link Power Management	Disabled
Use dedicated end point 1 interrupt	Disabled
VBUS sensing	Disabled
Signal start of frame	Disabled

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PC4	ADC1_INP4	Analog mode	No pull-up and no pull-down	n/a	
	PC5	ADC1_INN4	Analog mode	No pull-up and no pull-down	n/a	
	PB0	ADC1_INN5	Analog mode	No pull-up and no pull-down	n/a	
	PB1	ADC1_INP5	Analog mode	No pull-up and no pull-down	n/a	
DAC1	PA4	DAC1_OUT1	Analog mode	No pull-up and no pull-down	n/a	
DCMI	PE4	DCMI_D4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE5	DCMI_D6	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE6	DCMI_D7	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA6	DCMI_PIXCLK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PH8	DCMI_HSYNC	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PH9	DCMI_D0	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PH10	DCMI_D1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PH11	DCMI_D2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PH12	DCMI_D3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD3	DCMI_D5	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PG9	DCMI_VSYNC	Alternate Function Push Pull	No pull-up and no pull-down	Low	
DEBUG	PA13 (JTMS/SWDIO)	DEBUG_JTMS-SWDIO	n/a	n/a	n/a	
	PA14 (JTCK/SWCLK)	DEBUG_JTCK-SWCLK	n/a	n/a	n/a	
	PB3 (JTDO/TRACESWO)	DEBUG_JTDO-SWO	n/a	n/a	n/a	
FMC	PF0	FMC_A0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF1	FMC_A1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF2	FMC_A2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF3	FMC_A3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF4	FMC_A4	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF5	FMC_A5	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC0	FMC_SDNWE	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF11	FMC_SDNRAS	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF12	FMC_A6	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF13	FMC_A7	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF14	FMC_A8	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF15	FMC_A9	Alternate Function Push Pull	No pull-up and no pull-down	Very High	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PG0	FMC_A10	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG1	FMC_A11	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE7	FMC_D4	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE8	FMC_D5	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE9	FMC_D6	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE10	FMC_D7	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE11	FMC_D8	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE12	FMC_D9	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE13	FMC_D10	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE14	FMC_D11	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE15	FMC_D12	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PH6	FMC_SDNE1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PH7	FMC_SDCKE1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD8	FMC_D13	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD9	FMC_D14	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD10	FMC_D15	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD14	FMC_D0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD15	FMC_D1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG4	FMC_BA0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG5	FMC_BA1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG8	FMC_SDCLK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD0	FMC_D2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD1	FMC_D3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG15	FMC_SDNCAS	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE0	FMC_NBL0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE1	FMC_NBL1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
I2C1	PB6	I2C1_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Low	
	PB7	I2C1_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Low	
I2C2	PH4	I2C2_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Low	
	PH5	I2C2_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Low	
QUADSPI	PF8	QUADSPI_BK1_IO0	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PF9	QUADSPI_BK1_IO1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PF10	QUADSPI_CLK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PG6	QUADSPI_BK1_NCS	Alternate Function Push Pull	No pull-up and no pull-down	Low	
RCC	PH0-	RCC_OSC_IN	n/a	n/a	n/a	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	OSC_IN (PH0)					
	PH1-OSC_OUT (PH1)	RCC_OSC_OUT	n/a	n/a	n/a	
	PA8	RCC_MCO_1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
SPI1	PA5	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA7	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB4 (NJTRST)	SPI1_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Low	
SPI2	PC1	SPI2_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC2_C	SPI2_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB10	SPI2_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USART1	PA9	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA10	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USB_OTG_HS	PB14	USB_OTG_HS_DM	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB15	USB_OTG_HS_DP	Alternate Function Push Pull	No pull-up and no pull-down	Low	

8.2. DMA configuration

nothing configured in DMA service

8.3. BDMA configuration

nothing configured in DMA service

8.4. MDMA configuration

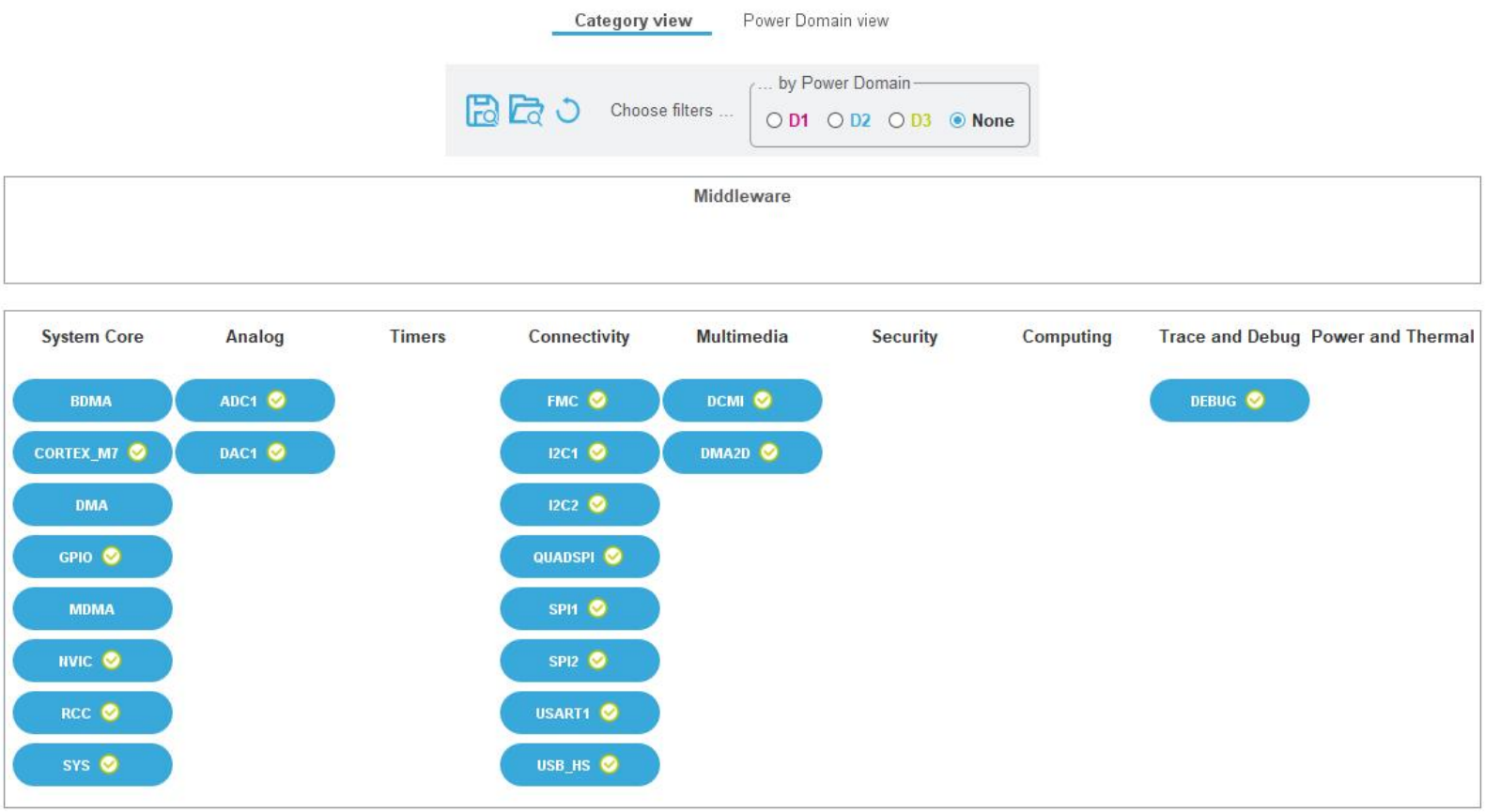
nothing configured in DMA service

8.5. NVIC configuration

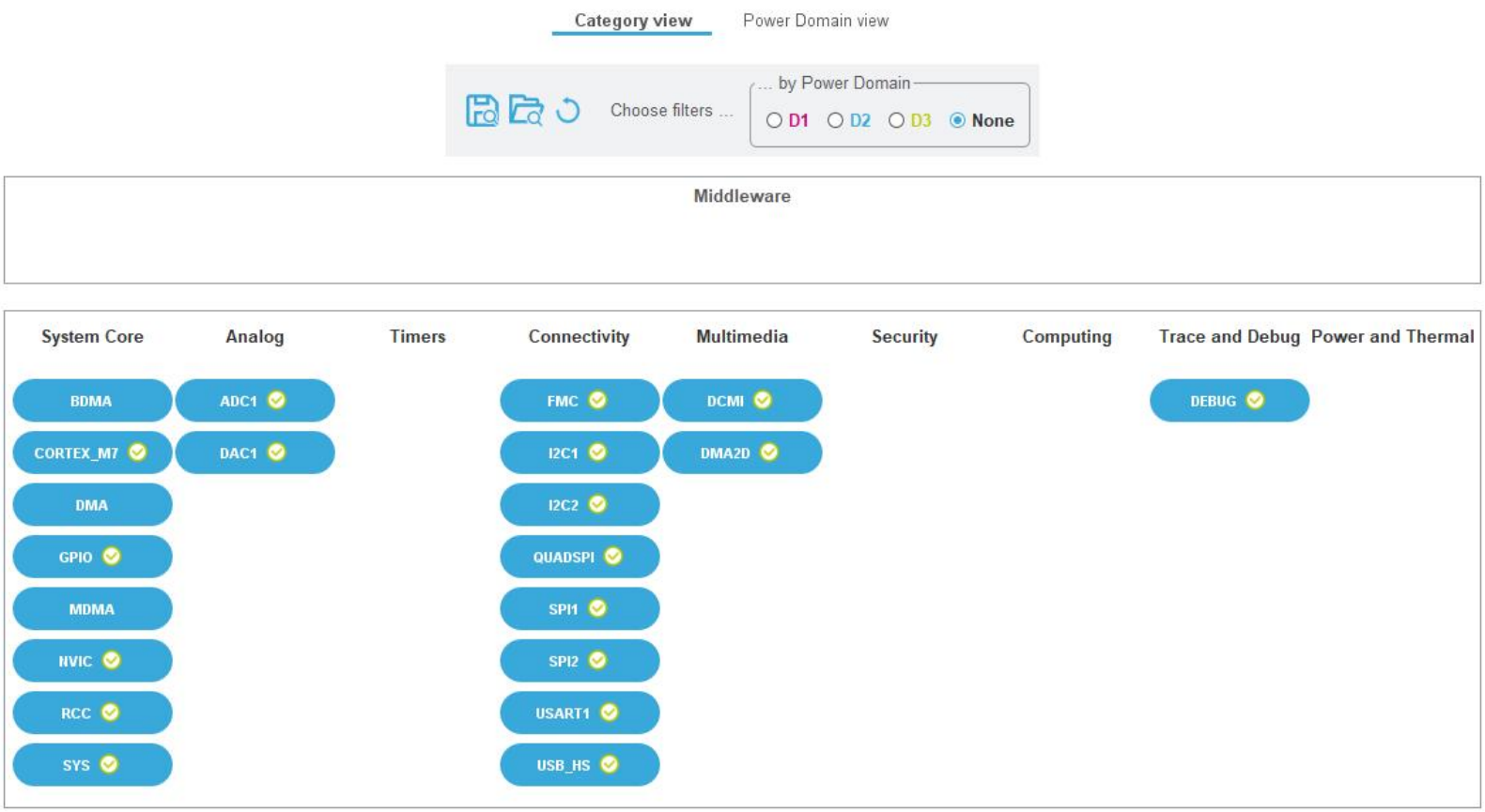
Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
PVD and AVD interrupts through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1 and ADC2 global interrupts	unused		
I2C1 event interrupt	unused		
I2C1 error interrupt	unused		
I2C2 event interrupt	unused		
I2C2 error interrupt	unused		
SPI1 global interrupt	unused		
SPI2 global interrupt	unused		
USART1 global interrupt	unused		
FMC global interrupt	unused		
TIM6 global interrupt, DAC1_CH1 and DAC1_CH2 underrun error interrupts	unused		
USB On The Go HS End Point 1 Out global interrupt	unused		
USB On The Go HS End Point 1 In global interrupt	unused		
USB On The Go HS global interrupt	unused		
DCMI global interrupt	unused		
FPU global interrupt	unused		
DMA2D global interrupt	unused		
QUADSPI global interrupt	unused		
HSEM1 global interrupt	unused		

*** User modified value**

9. Predefined Views - Category view : Current



10. Predefined Views - Category view : Without filters



11. Predefined Views - Power Domain view

12. Software Pack Report