Alberto Parravicini – Curriculum Vitae – 2020

Email	alberto.parravicini@polimi.it	**Website**	albertoparravicini.github.io
LinkedIn	linkedin.com/in/alberto-parravicini	**Github**	github.com/AlbertoParravicini

Work Experience

Feb 2018 - Apr 2020 **Oracle Labs** - Zurich & Milan - Research Assistant, Ph.D Student Collaborator
Created the first vertex embeddings-based Named Entity Disambiguation algorithm to deliver 90% accuracy and 30 disambiguations/sec. Developed a PoC translator from Natural Language to Graph Query Languages. Improved the GPU support of GraalVM with LLVM transformations of JIT-compiled CUDA code and dynamic scheduling.

Jan 2018 - Jun 2018 **Unicredit** - Milan - Research & Development Intern
Developed a C library for Entropy Measures on high-frequency financial data, and analysed how to use them as volatility proxies.

Jul 2017 - Sep 2017 **AXA** - Brussels - Data Science Intern
Developed a deep-learning OCR (Optical Character Recognition) pipeline in Python to extract tables and text from insurance claims documents and perform fraud detection.

Education

2018 - Present Doctor of Philosophy in Computer Science and Engineering
at **Politecnico di Milano**.
Researching high-performance heterogeneous architectures applied to graph analytics. Supervised 10+ graduate and undergraduate students in my research group. Lecturer and TA of *Software Engineering* and *High-Performance Graph Analytics*.

2015 - 2018 Master of Science Degree in Computer Science and Engineering
at **Politecnico di Milano**. Graduation Mark: **110/110, Cum Laude**

2017 **ATHENS:** Introduction to the Finite Elements Method
at **TU Delft**, Netherlands

2016 **IDEA League Summer School:** Responsible Artificial Intelligence
at **TU Delft**, Netherlands

2016 - 2017 Master of Science in Computer Science and Engineering
at **Ecole Polytechnique de Bruxelles**. (Exchange Student)

2012 - 2015 Bachelor of Science Degree in Engineering of Computing Systems
at **Politecnico di Milano**. Graduation Mark: **106/110**

Selected Publications

- **A. Parravicini**, R. Patra, D. B. Bartolini, M. D. Santambrogio, "Fast and Accurate Entity Linking via Graph Embedding", 2019 GRADES-NDA.
- L. Stornaiuolo, **A. Parravicini**, G. Durelli and M. D. Santambrogio, "Exploiting FPGAs from Higher Level Languages A Signal Analysis Case Study", 2017 IPDPS Workshops.

Personal interests

- **Scientific interests** High-performance computing, graph analytics, computational finance
- **Other interests** Macro photography, hot enamel handicraft