

# DAG-based Scheduling with Resource Sharing for Multi-task Applications in a Polyglot GPU Runtime

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**Abstract**—GPUs are readily available in cloud computing and personal devices, but their use for data processing acceleration has been slowed down by their limited integration with common programming languages such as Python or Java. Moreover, using GPUs to their full capabilities requires expert knowledge of asynchronous programming. In this work, we present a novel GPU run time scheduler for multi-task GPU computations that transparently provides asynchronous execution, space-sharing, and transfer-computation overlap without requiring in advance any information about the program dependency structure. We leverage the GrCUDA polyglot API to integrate our scheduler with multiple high-level languages and provide a platform for fast prototyping and easy GPU acceleration. We validate our work on 6 benchmarks created to evaluate task-parallelism and show an average of 44% speedup against synchronous execution, with no execution time slowdown compared to hand-optimized host code written using the C++ CUDA Graphs API.

**Index Terms**—GPU, Scheduling, Software Runtime, Hardware Acceleration

## I. INTRODUCTION

Graphics Processing Units (GPUs) are often heralded as the optimal solution to achieve extremely high throughputs in domains such as Deep Learning, financial simulations, and graph analytics. Even if GPUs are made available by most cloud providers and are commonly found in personal devices, using GPUs for data processing acceleration has been hampered by their limited integration with high-level programming languages such as Python or Java. Fully exploiting the hardware resources of GPUs requires a deep understanding of their architecture and creates a steep learning curve that takes a long time for programmers to overcome. As a consequence, the adoption of GPUs is often limited to specific domains for which libraries or Domain-Specific Languages (DSLs) that abstract and mask the GPU computation are available.

On the other hand, APIs offering complete control over the GPU still require efforts to unleash the full hardware potential, e.g. to overlap and synchronize multiple computations, or to overlap computation with data transfer from and to the GPU. In this work, we present a novel GPU runtime scheduler that transparently provides all these optimizations without requiring in advance any information about the structure of the computation. We leverage the Graal polyglot Virtual Machine (VM) [1]–[3], and the GrCUDA environment [4], to run GPU kernels from languages such as Python, Java, and Ruby and obtain full control over the GPU runtime to optimize

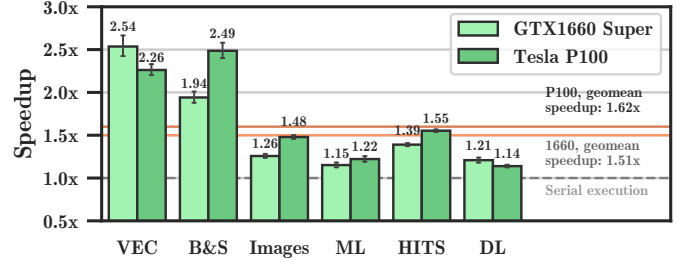


Fig. 1: Achievable speedup in C++ CUDA with hand-tuned GPU data transfer and execution overlap. Fine-tuned space-sharing and execution-transfer overlaps can accelerate GPU computations by more than 50%.

scheduling, data transfer, and execution. We target the CUDA platform, but similar considerations would work for OpenCL [5], given the availability of a managed execution environment.

## A. Motivation

Modern GPUs allow multiple computations to run asynchronously and concurrently to leverage task-level parallelism: experienced programmers accelerate their programs by prefetching and overlapping data transfers with computations on different data or even take advantage of hardware space-sharing by overlapping multiple independent computations.

Figure 1 shows how much speedup can be extracted in different CUDA benchmarks (presented in section V-B) by hand-crafting these optimizations. Computations with opportunities for task-level parallelism are common: even the simple machine learning pipeline in Figure 2 has two independent branches whose results are combined at the end. Instead of executing computations sequentially, a skilled programmer schedules independent tasks on separate execution streams. However, achieving full utilization of the GPU often requires extensive debugging and profiling, even by experienced users [6]; performance may also depend on the data available at run time, and it cannot be perfectly fine-tuned by the programmers.

Our work aims to provide a low-profile runtime that can automatically leverage untapped GPU resources in multi-task computations to provide speedups identical to what a skilled programmer can achieve by hand, lowering the barrier of access to GPUs with no performance compromises.

## B. Contributions

In this work, we present a novel low-profile run time scheduler for multi-task and asynchronous GPU computations.

Our scheduler automatically infers data dependencies between GPU kernels, models them using a Directed Acyclic Graph (DAG), and enable asynchronous CPU and GPU execution without users having to define any synchronization event or dependencies manually. More importantly, dependencies and scheduling are computed entirely at run time, without defining the computation structure in advance, and without constraints on the host language control flow.

This work is implemented as an extension of GrCUDA, a polyglot CUDA API based on GraalVM [1]. GrCUDA is implemented as a Truffle DSL [2] and provides access to GPU acceleration to languages supported by GraalVM, such as Java, Scala, JavaScript, R, and Python. Our scheduler is available in all these languages; moreover, any new feature or optimization to our scheduler will be available without language-specific modifications. Our scheduler enables GrCUDA to become a valid solution for general-purpose GPU acceleration, focusing on fast prototyping and integration with high-level languages that do not currently have a strong GPU support.

We evaluate our scheduler on 6 benchmarks from different domains that exhibit opportunities for task-level parallelism and show an average of 44% speedup against the serial GrCUDA scheduler and no significant slowdown against hand-optimized scheduling written using the C++ CUDA Graphs API; finally, we analyze hardware utilization to understand how well each benchmark can exploit data transfer-computation overlap and untapped GPU resources. The source code for our scheduler and benchmarks is openly available<sup>1</sup>.

In summary, we make the following contributions:

- A run time scheduler based on GrCUDA that automatically infers dependencies between GPU computations and dynamically schedules them to maximize transfer-computation overlap and space-sharing (section IV).
- A suite of 6 benchmarks to evaluate GPU asynchronous computations, task-parallelism, and space-sharing hardware utilization (sections V-B and V-F).
- An evaluation of how our scheduler provides an average of 44% speedup against the serial GrCUDA scheduler and no slowdown against hand-optimized scheduling based on the CUDA Graphs API (sections V-C and V-D).

## II. RELATED WORK

Expressing a multi-task computation as a DAG that can be used to estimate an effective scheduling and to optimize execution is a concept that has already been explored with a great degree of success: well-known work that covers GPU computations includes Nvidia’s CUDA Graphs [7] and Google’s Tensorflow [8]; academic research has also shown interest in domains such as distributed and heterogeneous computing [9]–[11], and presented valuable theoretical results [12], [13]. CUDA Graphs are a programming model

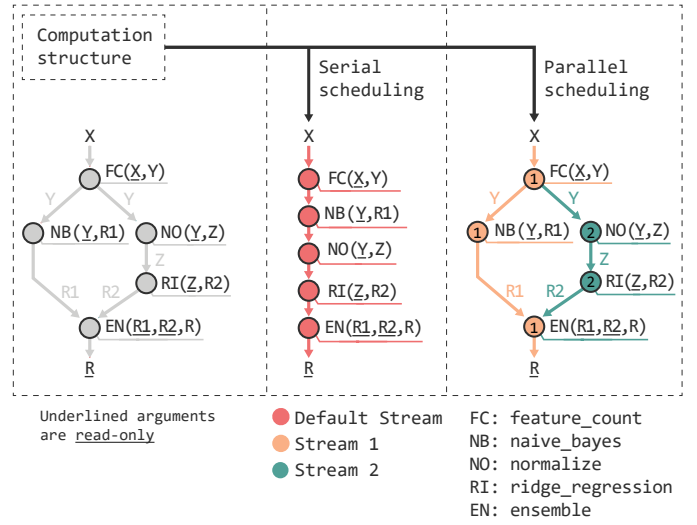


Fig. 2: The two branches in this computation are independent, and can be scheduled and executed in parallel. Edges are labeled with the argument that cause a data dependency.

recently released by Nvidia used to define a DAG of inter-dependent computations and execute them asynchronously. Computations between dependencies must be specified manually using CUDA events, or with a fairly complex custom API [7]. CUDA Graphs also present initialization overheads due to graph creation [14]. Instead, TensorFlow allows users to express a DAG of computations through a DSL embedded in languages such as Python. TensorFlow is mostly intended for Deep Learning (DL); expressing custom kernels for other domains, while supported, is not straightforward and requires significant manual integration effort. We do not deem a direct comparison with our work to be meaningful, as TensorFlow presents design choices specifically targeted towards DL.

Indeed, the most common approach to DAG-based scheduling, as seen in CUDA Graphs and TensorFlow, is to specify the program flow in advance: this choice simplifies the computation of an optimal scheduling and amortizes overheads in case of repeated computations, and is certainly suitable for specific domains such as DL. On the other hand, the approach presented in this work is to capture GPU computations through a low-profile runtime, without the need to specify dependencies manually. As such, we do not impose any limitation over the host program control-flow (e.g. conditional statements, function calls, recursion, library calls) so that the program flow can change over time. In the simplest scenario, a programmer might use multiple kernel implementations optimized for different input sizes or use different pre-processing procedures based on the input data language; selecting the appropriate kernel is done simply through conditional statements in the host language (e.g. a switch-case in Python), without requiring custom APIs or defining multiple DAGs in advance.

Computing dependencies at runtime on heterogeneous architectures has been explored by the XKaapi runtime [15]. Contrary to our approach, XKaapi uses a work-stealing strat-

<sup>1</sup>github.com/AlbertoParravicini/grcuda

egy that computes dependencies every time an idle thread looks for a task to execute. It handles GPU memory as a queue of blocks instead of leveraging the fine-grained flexibility of Unified Memory (UM), and its complex API is limited to C++.

Recently, many techniques to virtualize or abstract GPUs usage have emerged, although efficient space-sharing is still considered an open challenge [16]. Ravi et al. [17] consolidate kernels from different VMs to increase utilization. TornadoVM [18], which is also compatible with GraalVM, translates annotated Java code for heterogeneous hardware; it profiles the code to understand the most suitable backend, but it is unable to optimize the scheduling of multi-kernel computations and automatically handle data-dependencies.

Today, most programming languages have ways to achieve GPU acceleration, including Python (PyCUDA, PyOpenCL [19]), Java (Jcuda [20]) and JavaScript (GPU.js<sup>2</sup>). However, none of these libraries can automatically handle asynchronous computations and space-sharing. Moreover, each library has different APIs, supported features, and update cycles, greatly limiting code portability and interoperability; instead, the unified GrCUDA runtime and API immediately provides each new feature (such as our scheduler) to all languages supported by GraalVM without any change in the host code.

Recent research on GPU space-sharing includes the work of Wen et al. [21], who showed how concurrent execution of some GPU kernels without data dependencies delivers up to 1.5x speedup; Qiao et al. [22] uses concurrent kernel execution to achieve 2.5x speedup over serial execution on multiresolution image filters. Other works (Baymax [23], Effisha [24]) focus on multi-application space sharing. DCUDA [25] provides scheduling for different applications on multiple GPUs, and shows how CUDA UM causes an average slowdown below 1%. We focus on single-application space-sharing, i.e. applications composed of many kernels that can run in parallel, but considerations on hardware utilization are valid in both single and multi-application space-sharing. As GrCUDA seamlessly integrates with CUDA, our work directly benefits from improvements on the CUDA API and drivers. For example, we could leverage alternative UM implementations optimized to overlap data transfer with computations, such as HUM [26].

### III. BACKGROUND

GPUs allow the execution of multiple kernels at the same time. If enough resources are available - e.g. free Stream Multiprocessor (SM), the main GPU computation units - the GPU will perform space-sharing and run kernels in parallel. Modern GPUs often have enough resources to perform space-sharing without significantly degrading the performance of individual kernels [22]: space-sharing can improve the occupancy of SMs and exploit under-utilized hardware resources. Kernels run in parallel and asynchronously thanks to CUDA streams: kernels are executed in issue-order on a stream, but different streams proceed independently. Space-sharing is key for better GPU resource usage, but requires even greater care to ensure that

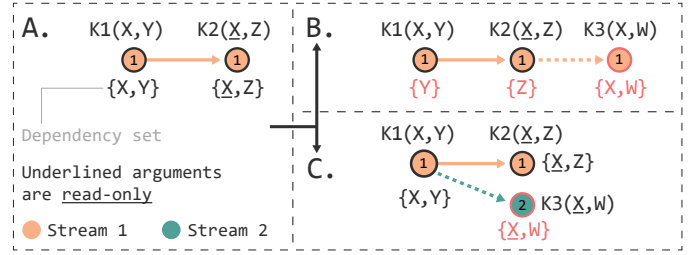


Fig. 3: Dependency computations with read-only arguments. Updates to the DAG and to dependency sets are highlighted.

programs run correctly. Synchronizing a single stream through the `cudaStreamSynchronize` function blocks the host execution and is generally acceptable only if the host requires the output of a GPU kernel. A more flexible approach is the use of CUDA events<sup>3</sup>, which allow streams to synchronize with each other without blocking the host execution. Using CUDA events to efficiently synchronize multiple complex streams by hand can be cumbersome: instead, our solution masks CUDA events and greatly simplifies the optimal scheduling of asynchronous computations (section IV).

In CUDA, computations are divided in *blocks*, each composed of an equal number of *threads* (from 32 to 1024). Bigger blocks imply fewer blocks running concurrently, but more possibilities of sharing data through fast block-wide shared-memory. Users can choose the number of threads per block; depending on the kernel implementation, users can also choose the number of blocks. While a small number of blocks increases space-sharing, achieving a performance improvement depends on the characteristics of the kernels. These considerations also apply to OpenCL: *streams* are called *command queues*, *threads* are *work items*, and the event model is similar to CUDA. Streams can also improve performance by overlapping asynchronous data transfer (from CPU to GPU or vice-versa) and computations: in Figure 2 the transfer of array `r1` (required by kernel NB) can be overlapped with execution of kernel NO. This approach is fruitful with repeated execution of simple kernels on different data batches, as the data transfer takes a significant amount of the total execution time. When using UM on GPUs that offer page migration, it is beneficial to prefetch data instead of relying on migrations caused by page faults: our scheduler can prefetch data automatically, reducing the burden of GPU optimization.

We leverage GraalVM, a Java VM able to run and combine languages that compile to Java bytecode (e.g. Scala) and custom implementations of other languages such as JavaScript, R, and Python [1]. This interoperability is possible thanks to the Truffle Abstract Syntax Tree interpreter [2], which guarantees high-performance through partial evaluation of repeated portions of code. Our work is an extension of GrCUDA, a CUDA language binding implemented as a Truffle DSL. GrCUDA can be seen as a polyglot API, as it provides GPU acceleration to all languages supported by GraalVM.

<sup>2</sup>GPU.js: <https://gpu.rocks>

<sup>3</sup>[docs.nvidia.com/cuda/cuda-runtime-api/group\\_\\_CUDART\\_\\_EVENT.html](https://docs.nvidia.com/cuda/cuda-runtime-api/group__CUDART__EVENT.html)

#### IV. SCHEDULER DESIGN METHODOLOGY

This section details the design and implementation of our scheduler. We provide a definition of our computation DAG (section IV-A). Then, we define our scheduler’s architecture and its integration with the CUDA runtime (sections IV-B and IV-C). Finally, we show how to leverage the language design of GrCUDA to provide asynchronous GPU computation without any detriment to accessibility (section IV-D).

##### A. Computation DAG and dependency sets

The cornerstone of our scheduler is a Computation DAG that represents relationships between computations that involve the GPU. Vertices of the DAG are *computational elements*: GPU kernels, memory accesses by the CPU host program to GrCUDA UM-backed arrays, and pre-registered or user-defined library functions such as RAPIDS<sup>4</sup>. Using GrCUDA and GraalVM, each element can be encapsulated through an object to keep track of its state. In the case of kernels, the object tracks its configuration (e.g. the number of blocks), its input arguments, and if the computation is active.

Edges of the DAG are *data dependencies* between computational elements. Dependencies are inferred automatically instead of being manually specified by the user through handles or other APIs. Inferring data dependencies is possible as GrCUDA uses a managed execution environment that allows object encapsulation of inputs, removing the risk of pointer aliasing typical of native languages (e.g. having multiple pointers referring to the same memory area). The scheduler employs data dependencies modeled through the DAG to associate computational elements to CUDA streams and introduces synchronization events if required. To compute dependencies, we associate with each computational element a *dependency set*. This set initially contains all arguments of the computational element. An argument in the set is removed when a subsequent computation uses and modifies the same argument, defining a data dependency on it; once a set is empty, the corresponding computational element can no longer introduce dependencies. Read-only kernel arguments (specified as in section IV-D) can be treated with special rules to avoid adding unnecessary dependencies to the DAG. If possible, they will be ignored in the dependency computations: for example, if two kernels use the same read-only input array, they will be executed concurrently on different streams. Figure 3 shows a kernel that modifies an argument and is followed by another kernel that uses the same argument as read-only (A). If a third kernel with the same input is added, it will depend on the second kernel if it modifies the argument (a write-after-read anti-dependency) (B), and it will depend on the first kernel if it uses the argument as read-only (C); it will not, however, depend on both kernels. In case (C), the read-only argument adds a new dependency through X, but the *dependency set* of the parent kernel K1 is not updated: if a new kernel requires X as read-only argument, it will depend

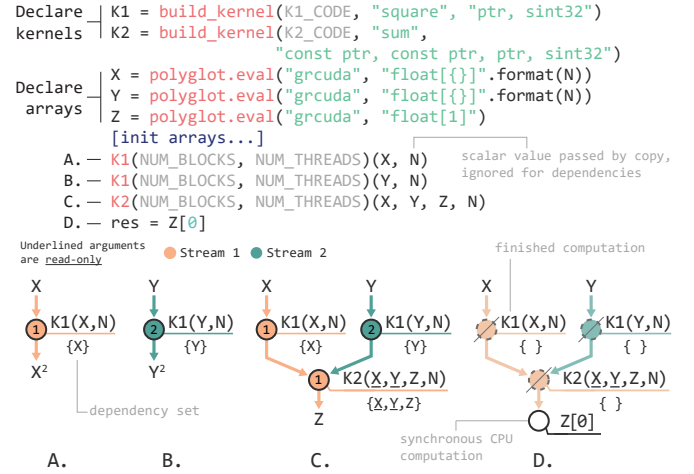


Fig. 4: Example of scheduling for the VEC benchmark. We show both the GrCUDA code and the resulting DAG.

on K1, otherwise it will depend on both K2 and K3, and all *dependency sets* will be updated.

The DAG is built at run time, not at compile-time or eagerly. Users do not have to worry about their host program’s control flow, as we dynamically add and schedule new computations as users provide them. Our scheduler is unaware of the full *logical* DAG structure of a given program, although we usually show complete DAGs for clarity (e.g. Figures 2 and 6). Instead, the scheduler updates the current graph frontier, i.e. the computations that are currently active. This choice is key to enable the dynamic creation of the DAG and does not introduce limitations on the optimizations that our scheduler could perform. We track each kernel’s historical performance and scheduling to allow the creation of heuristics that guide future scheduling of the same kernel.

In GrCUDA, arrays are backed by UM, which simplifies data movement and accesses from the CPU without large performance penalties [25]. As the CPU can schedule accesses to these arrays at any point (even while the GPU is running), we model these accesses as *computational elements*. If the access introduces a data dependency on a GPU computation, the scheduler ensures that the CPU waits for that computation to end. To keep overheads as low as possible, array accesses that do not introduce data dependencies with respect to GPU kernels are executed immediately, without modeling them as DAG elements: this is the case of consecutive accesses or accesses performed while no GPU computation is active. Pre-registered libraries can also take advantage of our scheduler if they expose the choice of execution stream in their API. If not, they are scheduled synchronously to guarantee correctness.

Figure 4 shows the GrCUDA code (with Python as host) of the VEC benchmark (section V-B). For each kernel invocation in the host, the scheduler adds a computational element to the DAG, updates the dependency sets of active computations, and provides a CUDA stream for execution. Executing K2 (Figure 4, (C)) requires a CUDA event to ensure that K1 is

<sup>4</sup>developer.nvidia.com/rapids



completed. Accessing  $Z$  on the CPU ensures that all computations are completed: they will no longer contribute to new dependencies. The host code does not need to care about the scheduling, and it can be written as if it were run sequentially, with no explicit mention of synchronization points or streams.

## B. System architecture

Figure 5 shows the main components of our scheduler and their integration with the existing GrCUDA architecture. The *GPU execution context* tracks declarations and invocations of GPU computational elements ①. When a new computation is created or called, it notifies the execution context ② so that it updates the DAG with data dependencies of the new computation ③. The GPU execution context uses the DAG to understand if the new computation can start immediately or if it must wait for other computations to finish. Computations are overlapped using different CUDA streams, assigned by the *stream manager* based on dependencies and free resources (section IV-C) ④. The *stream manager* ⑤ and the *execution context* ⑥ interact with the GPU through an intermediate layer that exposes the CUDA API to GrCUDA.

GPU computations are asynchronous and do not require synchronization against previous computations on the stream where they are executed, as CUDA guarantees sequential execution of computations scheduled on a stream. We synchronize streams with CUDA events without blocking the host CPU. Each computation is associated with an event to provide a precise synchronization point instead of blocking the entire stream. If the CPU requires data for a computation, we synchronize only the streams that are currently operating on this data. The scheduler considers GPU computations as active until the CPU requires their result or one of their children. We use active computations to identify dependencies (unless their *dependency set* is empty) and empty streams.

## C. Scheduling policies and stream management

A scheduler is *serial* if computations are executed one after the other in the order defined by the user, and their execution or data transfer do not overlap. A *parallel* scheduler allows overlaps to happen, and data dependencies determine the order in which computations are executed. In a *synchronous* scheduler the CPU host program waits for GPU computations to finish, while an *asynchronous* scheduler allows the CPU to perform other computations while the GPU is active. The original GrCUDA scheduler is *serial* and *synchronous*, while our scheduler is *parallel* and *asynchronous*.

CUDA streams are key to enable parallel and asynchronous computation. In our scheduler, the allocation and management of streams are performed transparently by a stream manager. The stream manager also tracks what computations are currently active in each stream and handles events used for synchronization. Users can specify different policies to create new streams and to associate them with computations. Existing streams are managed in FIFO order, and new streams are created only if no currently empty stream is available to schedule a given computation. If a computation

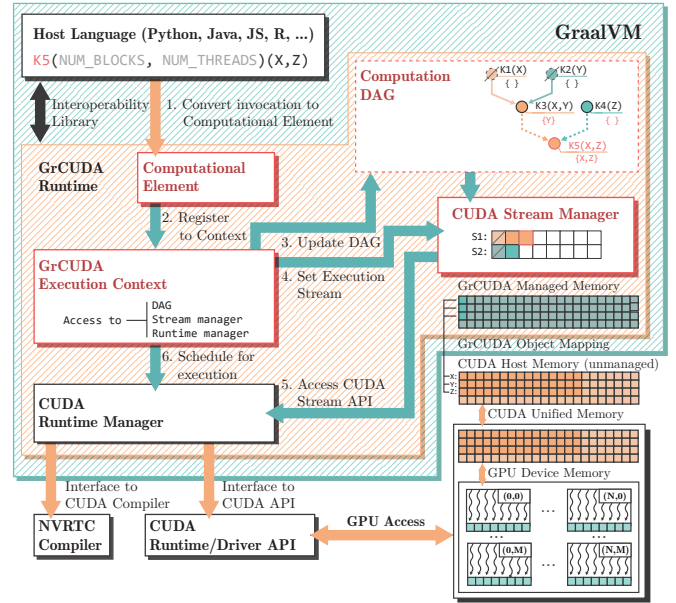


Fig. 5: Our scheduler integrates with the existing GrCUDA architecture. New components are highlighted in red.

has multiple children (i.e. computations that depend on it), the first child is scheduled on the parent’s stream to minimize synchronization events, while following children are scheduled on other streams to guarantee concurrency. Simpler policies (e.g. schedule all children on a single stream) further reduce the scheduling costs; that said, our experiments always use the more general policies and show negligible scheduling overheads (section V-D). The stream manager is architecture-aware: on GPU architectures older than Pascal, the CPU cannot access UM if a kernel is active in the GPU. The stream manager restricts each array’s visibility to the stream where it is used until the CPU needs to access the array. The CPU is made temporarily unaware of the existence of arrays being used by the GPU, and can access currently unused arrays even if the GPU is active. While this optimization is not required on architectures since Pascal (thanks to its page fault mechanism), our scheduler can automatically prefetch data to optimize transfers.

## D. Language design and integration

Our scheduler leverages the GrCUDA language’s existing features and does not introduce any user-facing modification to the language. Kernel signatures are specified using Native Interface Definition Language (NIDL) or Truffle Native Function Interface (NFI), simple typing systems that support basic data types and pointers. Optional argument annotations such as `input`, `output` or `const` are used by the scheduler to optimize computations that contain read-only arguments (`input` or `const`). For arguments without annotations, the scheduler treats them as modifiable by the kernel; not specifying arguments as read-only does not affect correctness, but might limit the scheduler from performing further optimizations.

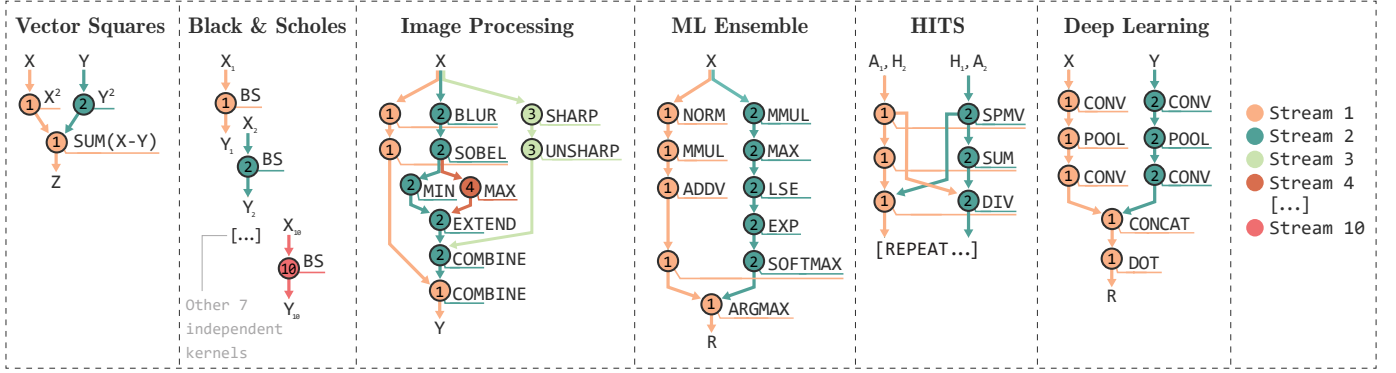


Fig. 6: Computation structure of each benchmark, expressed as a DAG of GPU kernel computations (denoted as circles). Colors denote CUDA streams, and kernels whose incoming arrows have different colors will require a synchronization event.

## V. EXPERIMENTAL EVALUATION

In this section, we evaluate the performance of our GrCUDA GPU scheduler against multiple benchmarks that exhibit task-level parallelism and opportunities to leverage space-sharing and transfer-computation overlap to achieve lower execution time than a serial scheduler (section V-B). First, we compare against the serial GrCUDA scheduler (section V-C) and show how our scheduler can exploit untapped GPU resources to deliver better performance than a naïve serial scheduler.

Then, we compare the performance of the GrCUDA against the C++ CUDA API, measure how the GrCUDA scheduling is identical to the best hand-tuned scheduling possible, and how GrCUDA does not add any significant slowdown in the benchmark execution times (section V-D).

Finally, we investigate, for each benchmark, the nature of the achieved speedup. First, we measure the amount of resource contention introduced by hardware space-sharing (section V-E); second, we measure what overlaps are present (transfer-computation or space-sharing), and we analyze how well each benchmark is using hardware resources such as device memory and L2 cache to understand which workloads are more suitable for asynchronous execution (section V-F).

### A. Evaluation Setup

Tests are performed on 3 different Nvidia GPUs with different architectures: a Tesla P100 (Pascal, 12 GB of device memory), a GTX 1660 Super (Turing, 6 GB), and a GTX 960 (Maxwell, 2 GB). GPUs are connected to their respective host machines through PCI Express (PCIe) 3.0. Testing consumer-grade GPUs such as the GTX 1660 Super and the GTX 960 shows how our scheduler does not demand high-end data-center hardware to provide benefits, and it is useful for quick prototyping on commodity GPUs and to accelerate desktop applications. Benchmarks are executed 30 times on random data. We select the input sizes in each benchmark to use between 10% and 90% of the available memory on each GPU, up to the largest size that fits in device memory. Execution time is the total amount of time spent by GPU execution, from the first kernel scheduling until the end of execution. Parameters (e.g. the number of blocks) are optimized for best performance

TABLE I: Amount of device memory for different input sizes in each benchmark. GPUs are tested with different input sizes up to the largest size that fits in GPU memory.

Benchmark name	Memory footprint (GB)		
	GTX 960	GTX 1660 Super	Tesla P100
<b>Vector Squares (VEC)</b>	0.4 GB - 1.9 GB	0.4 GB - 3.1 GB	0.4 GB - 11 GB
<b>Black &amp; Scholes (B&amp;S)</b>	0.4 GB - 1.9 GB	0.4 GB - 3.1 GB	0.4 GB - 11 GB
<b>Images (IMG)</b>	0.2 GB - 1.0 GB	0.2 GB - 5.1 GB	0.2 GB - 9.1 GB
<b>ML Ensemble (ML)</b>	0.4 GB - 1.9 GB	0.4 GB - 3.3 GB	0.4 GB - 9.9 GB
<b>HITS</b>	0.4 GB - 1.5 GB	0.4 GB - 4.2 GB	0.4 GB - 9.9 GB
<b>Deep Learning (DL)</b>	0.3 GB - 1.4 GB	0.3 GB - 4.9 GB	0.3 GB - 6.5 GB
<b>GPU device memory</b>	2 GB	6 GB	12.2 GB

in serial execution to provide a worst-case comparison. The x-axes in Figures 7 to 9 report the benchmark scale, a value proportional to the benchmark’s memory footprint (e.g. the number of pixels in each input image).

### B. Benchmark Suite

We tested our scheduler on 6 benchmarks and a total of 33 different kernels representing common GPU workloads (image processing, machine learning, etc.) and containing opportunities for task-level parallelism through space-sharing and computation-transfer overlap. To the best of our knowledge, no existing GPU benchmark suite has the goal of evaluating intra-application task-level parallelism, as most benchmark suites (e.g. Rodinia [27]) focus on single kernels and sequential execution. Still, we take or derive the CUDA kernels in our benchmarks from open-source implementations.

We scale the input size linearly to visualize more clearly if any hardware bottleneck impacts performance as input size exceeds a threshold. For instance, we change the number of rows for the matrix multiplications in the ML benchmark, but keep fixed the number of features and output classes.

Figure 6 presents each benchmark’s task dependency structure and highlights the optimal stream assignment for each kernel. Table I summarizes each benchmark. The chosen input sizes guarantee that the *memory footprint* covers both small

and large computations compared to the total memory of each GPU. For each benchmark, we present a brief description.

- **Vector Squares (VEC)**: a simple benchmark that measures a basic case of task-level parallelism and computes the sum of differences of 2 squared vectors. Each iteration has new input data, simulating a streaming computation that requires transfer from CPU to GPU. Inspired by [28].
- **Black & Scholes (B&S)**: Black & Scholes equation for European call options, for 10 underlying stocks, and 10 vectors of prices. Adapted from [29] to simulate a computationally intensive streaming benchmark with double-precision arithmetic and many independent kernels that can be overlapped with no dependencies.
- **Image Processing (IMG)**: an image processing pipeline that combines a sharpened picture with copies blurred at low and medium frequencies [30], to sharpen the edges, soften everything else, and enhance the subject. The benchmark has complex dependencies on 4 streams.
- **Machine Learning Ensemble (ML)**: an ML pipeline that combines Categorical Naïve Bayes and Ridge Regression classifiers by applying softmax normalization and averaging scores. The input matrix has 200 features. This benchmark contains branch imbalance (the Naïve Bayes classifiers takes longer) and read-only arguments.
- **HITS**: it computes the HITS algorithm on a graph [31] using repeated Sparse matrix-vector multiplication (SpMV) on a matrix and its transpose, and is implemented with LightSpMV [32]. It contains complex cross-synchronizations and multiple iterations.
- **Deep Learning (DL)**: a convolutional neural network that projects 2 input images to low dimensional embeddings and combines the embeddings using a dense layer. Similar neural networks can be used, for example, to classify if 2 images contain the same subject.

### C. Performance against Serial GrCUDA Scheduling

We compare the performance of our parallel scheduler against the GrCUDA serial scheduler (Figure 7). Automatic data prefetching is enabled on the Tesla P100 and the GTX 1660 Super, while on the GTX 960, data is necessarily transferred ahead of the computation as it does not have a page fault mechanism. We always deliver better performance over the serial scheduler, with a geomean speedup of 44% on the 3 GPUs. The GTX 960 is 25% faster, while the P100 performs the best, with a geomean speedup of 61%. More hardware resources, together with automatic prefetching, results in better parallelization, and we show how our approach works out-of-the-box on data-center GPUs. While still faster than the serial baseline, disabling automatic prefetching is not recommended: concurrent kernel execution turns the page fault controller into the main bottleneck, limiting the benefits of overlapping data transfer with computation. When using *serial scheduling*, GrCUDA does not compute dependencies, making overheads even smaller. We average results for *block sizes* (the number of threads in each 1D block) from 32 to 1024. In benchmarks with 2D and 3D blocks (e.g. IMG and DL), we keep 2D blocks

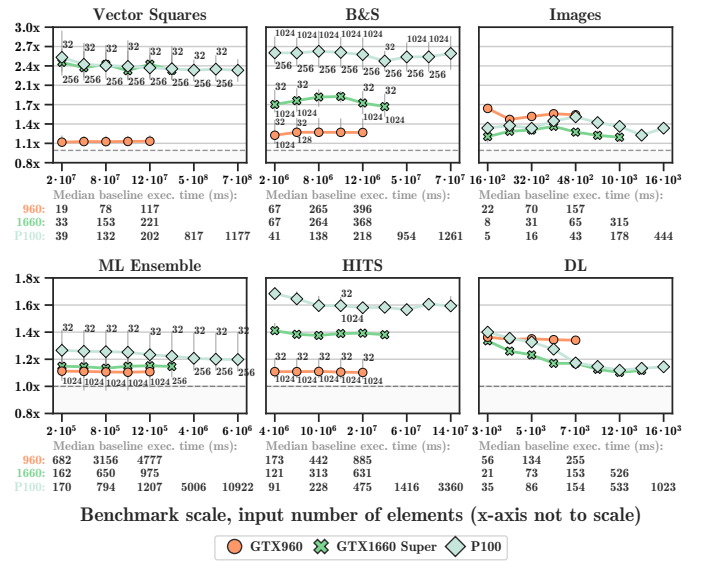


Fig. 7: Parallel scheduler speedup over serial scheduler. Our parallel scheduler provides a geomean speedup of 44% over the original GrCUDA serial scheduler. We highlight block sizes giving the best/worst speedup (when significant).

with size 8x8 and 3D blocks with size 4x4x4, as bigger blocks resulted in longer execution times in every case.

Speedups are mostly independent of the input data size, as we sweep through inputs with size from less than 10% to almost 100% of the available GPU memory. Even if kernels fill the GPU resources, it is still possible to achieve a speedup by overlapping data transfer with other kernels' execution.

DAG scheduling appears to be more robust to different kernel configurations: in many cases (such as VEC and HITS), using `block_size=32` results in higher speedup, but similar execution time as with larger block size. With serial scheduling, small blocks result in under-utilization of GPU resources such as shared memory, while DAG scheduling provides better utilization by having multiple kernels run in parallel. Thanks to DAG scheduling, programmers have to spend less time profiling their code to find the optimal kernel configuration.

### D. Performance against CUDA Graphs

To understand how our GrCUDA scheduler performs against existing solutions, we re-implemented our benchmarks using the C++ CUDA Graphs API. The kernel code and the setup (e.g. input and block sizes) are the same as GrCUDA, but the host code is written using the C++ CUDA Graphs API. We test CUDA Graphs using *stream-capture* to wrap hand-optimized multi-stream scheduling synchronized with CUDA events and using the Graph API to specify dependencies between computations manually. These CUDA Graphs are built only once per execution, and overheads are completely amortized over many iterations. Finally, we provide a hand-optimized implementation purely based on CUDA events to have full control over data movement and simulate CUDA Graph's performance if it supported data prefetching.

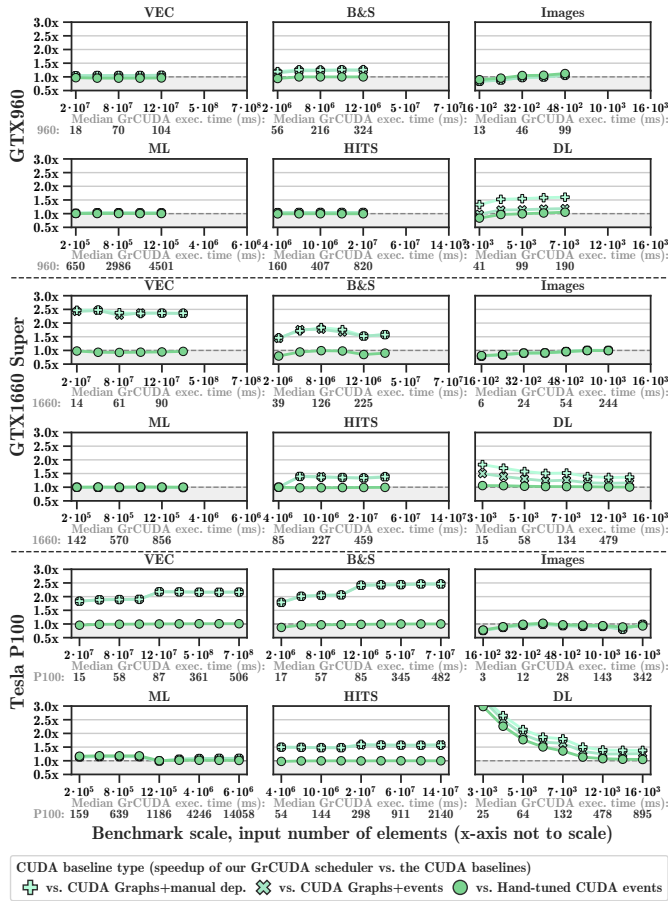


Fig. 8: Speedup of our GrCUDA scheduling against hand-optimized CUDA Graphs (higher is better). We are always faster, and the GrCUDA runtime overheads are negligible for computations lasting more than a few milliseconds.

Our GrCUDA scheduler, in addition to being fully automated, is never significantly slower than any of the CUDA Graphs baselines and is often faster (Figure 8). The large performance gaps compared to CUDA Graphs seen on the GTX 1660 Super and the P100 are mostly explained by our automatic prefetching, which the CUDA Graphs API seems unable to perform. Even when enabling prefetching in the CUDA baseline, our parallel scheduler achieves equal performance to the hand-optimized baseline. Execution time speedups are hardly affected by input size, with minor differences only in computations lasting a few milliseconds and containing many dependencies (such as IMG).

#### E. Impact of space-sharing resource contention

By looking at dependencies between kernels and measuring their execution time with serial scheduling so that each kernel has full access to the GPU resources, we estimate the resource contention on the GPU hardware and the PCIe bandwidth introduced by space-sharing. Figure 9 shows how far each benchmark is from its theoretical contention-free peak performance. Results are mostly consistent between GPUs,

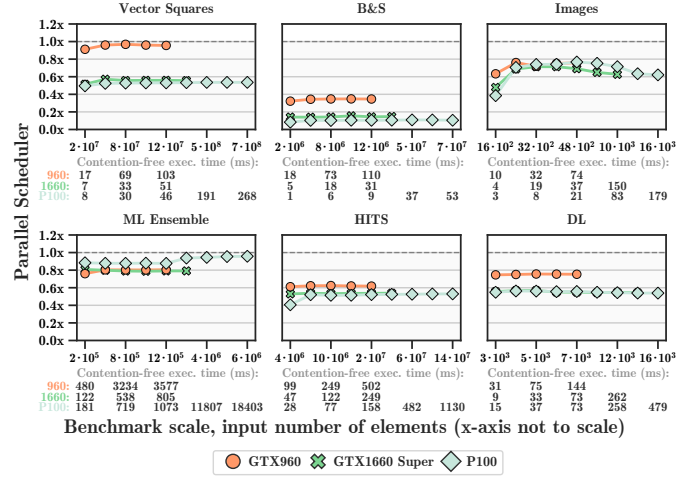


Fig. 9: Slowdown compared to execution without hardware resource contention. Space-sharing introduces a performance loss of around 30-40% due to hardware space-sharing.

with a relative execution time that is often around 70% of the contention-free performance bound; while resource contention is present, it is small enough to make space-sharing worthwhile. Unsurprisingly, B&S, which is composed of 10 independent computations, achieves around 15-20% of its contention-free peak performance due to limitations on PCIe bandwidth and double-precision arithmetic units availability.

#### F. Analysis of hardware utilization

It is fascinating to understand, for each benchmark, the nature of the speedup achieved through resource sharing, i.e., if the speedup is caused by overlapping computation with data transfer or if the speedup is explained by higher utilization of GPU resources such as device memory bandwidth through space-sharing. First, we measure how much overlap is present in each benchmark. We measure 4 different types of overlap:

- **CT**, computation against transfer: percentage of GPU kernel computation that overlaps with any data transfer
- **TC**, transfer against computation: percentage of data transfer that overlaps with any kernel computation(s)
- **CC**, percentage of GPU computation overlapped with other GPU computation
- **TOT**, any type of overlap: here we consider any type of overlap between data-transfer and/or computations. If a computation/data-transfer overlaps more than one computation/data-transfer, the overlap is counted only once (we consider the union of the overlap intervals)

Figure 10 shows how we compute these overlaps starting from the execution timeline. Although the TOT overlap can be a good proxy of the achieved speedup, it is sometimes inflated by high CC overlap, as overlapping computations does not always translate to faster execution. In VEC, the speedup comes only from transfer and computation overlap, while the overlap of kernels that leave a large amount of shared memory unused if executed serially explains the speedup in IMG.



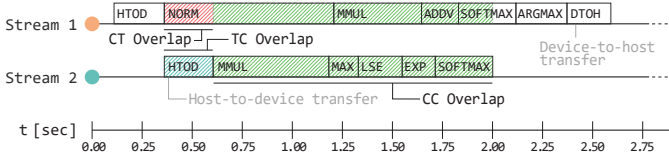


Fig. 10: Example of a possible execution timeline for the ML benchmark. We highlight different types of overlap between transfer and computation, as defined in section V-F.

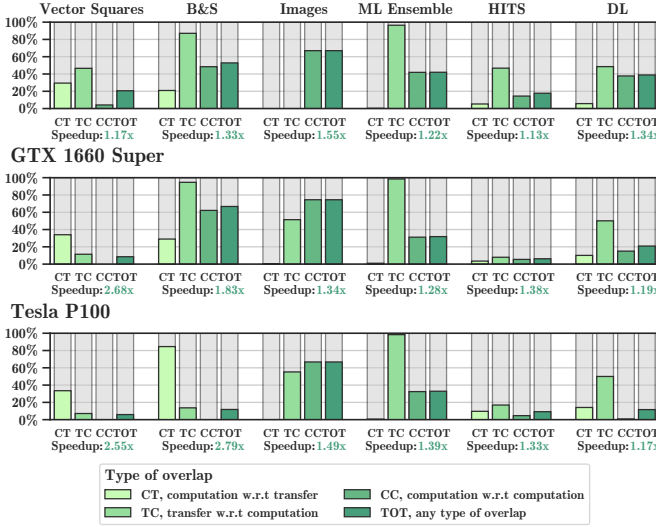


Fig. 11: Amount of transfer and computation overlap for each benchmark, for serial and parallel scheduling. We report below each plot the speedup obtained in the benchmark.

Computation time and transfer time do not increase with the same proportionality factor as the input size; small input data do not use the PCIe bandwidth fully, and a 10x increase in data size might translate into a transfer time increase below 10x, up to the available bandwidth. On faster GPUs the computation time is lower, while the transfer time is roughly identical to less powerful hardware (assuming the same transfer interface): more computation is overlapped to data transfer, leading to better speedups. For example, in the B&S benchmark, the CT overlap increases on faster GPUs, and so does the speedup.

We then analyze how our parallel scheduler affects hardware-level metrics such as device memory throughput, L2 cache throughput, Instructions per cycle (IPC), and GFLOPS. We use `nvprof` and `ncu`<sup>5</sup> to measure the number of bytes read/written by each kernel from/to device memory and L2 cache, and the total number of instructions executed. As collecting these metrics introduces high execution time overhead and prevents the execution of concurrent kernels, we combine the execution timeline without metric collection with hardware metrics collected in separate runs (variance in these metrics between different runs is insignificant). Metrics are collected only on the GTX 1660 Super as we did not have root-level

<sup>5</sup><https://docs.nvidia.com/cuda/profiler-users-guide/index.html>, <https://docs.nvidia.com/nsight-compute/NsightComputeCli/index.html>

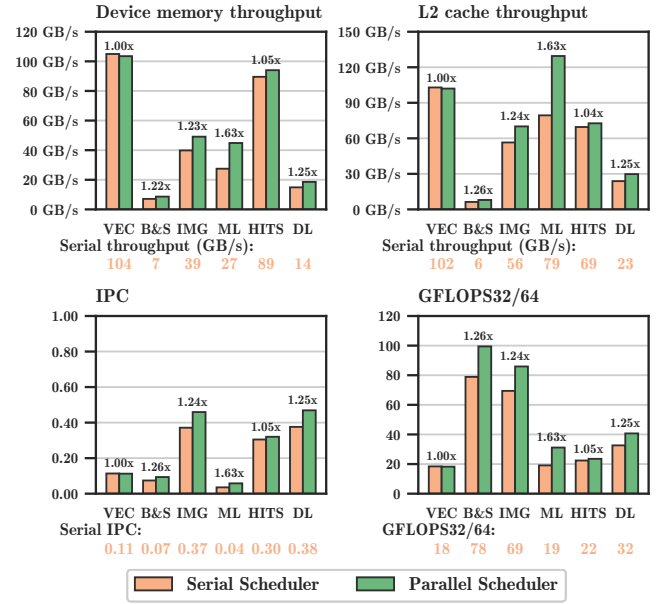


Fig. 12: Hardware metrics for each benchmark and execution policy, as measured on the GTX 1660 Super. All benchmarks in which different kernels overlap their execution show an increase in hardware utilization.

access to the Tesla P100. The amount of bytes read/written and the total number of instructions executed by each kernel mostly depends on the kernel itself and is not significantly impacted by space-sharing; as such, this evaluation is useful to estimate the global GPU behavior when space-sharing is performed. GFLOPS is estimated from the total number of floating-point operations (single and double precision).

Figure 12 shows how in kernels with computation overlap (e.g. ML and IMG), the increase in memory throughput is significant and in-line with the total speedup observed for these benchmarks. VEC does not have any increase in memory throughput, as its speedup comes exclusively from transfer overlap. Benchmarks that operate on dense matrices make heavier use of L2 cache, whose throughput increases with parallel scheduling. The low IPC in ML is caused by a slow kernel that operates on tall matrices and does not use the GPU parallelism to its full extent: running multiple kernels in parallel hides its latency and provides the speedup in Figure 7.

From these analyses, we understand what limits performance in each benchmark. For example, B&S performs complex mathematical operations on independent values, with a very high GFLOPS count (Figure 12) and almost no cache utilization. On the GTX 1660, B&S has high TC and low CT (Figure 11); the computation lasts longer than the data transfer, and part of the computation is not overlapped; on the other hand, the Tesla P100, which has 20x higher double-precision performance than the 1660, completely masks the computation with transfer (high CT), and indeed we observe a better speedup. Improving performance even further requires lowering the transfer time, for example, through PCIe 4.0.

## VI. CONCLUSION AND FUTURE WORK

We presented a novel scheduler for GPU computations that can automatically infer data dependencies to build a computation DAG at run time. The scheduler allows computations to execute in parallel through GPU space-sharing and overlaps data-transfer and execution whenever possible.

We validate our scheduler on 6 benchmarks and a total of 33 GPU kernels. Our scheduler provides a geometric speedup of 44% (up to 270%) over serial synchronous scheduling, and is always faster. It automatically achieves the same scheduling as hand-optimized CUDA Graphs code, without any slowdown.

Our scheduler seamlessly integrates with the GrCUDA environment, a polyglot CUDA API based on GraalVM that provides easy access to GPU acceleration to languages such as Java, Python, JavaScript, and R. Users can leverage our work without knowledge of the underlying scheduler, and without changing their code. It is not required to specify in advance the code structure or control flow, as our scheduler dynamically executes computations as provided by the host program. Our work simplifies GPU code prototyping and acceleration by giving easy access to untapped GPU resources at no cost, while masking the complexity of asynchronous GPU computations.

As future work, we plan to extend our technique to multiple GPUs: the problem is significantly harder, as it requires to compute data location and migration costs at run time to identify the optimal scheduling. We will also leverage run time information for additional optimizations, such as estimating the ideal block size based on data size and previous executions.

## ACKNOWLEDGMENTS

We thank Oracle Labs for its support and contributions to this work. The authors from Politecnico di Milano are funded in part by a research grant from Oracle. We also thank Rene Mueller and Lukas Stadler, the original authors of GrCUDA, for their valuable feedback and opinions. Oracle and Java are registered trademarks of Oracle and/or its affiliates.

## REFERENCES

- [1] T. Würthinger, C. Wimmer, A. Wöß, L. Stadler, G. Duboscq, C. Humer, G. Richards, D. Simon, and M. Wolczko, "One vm to rule them all," in *Proceedings of the 2013 ACM international symposium on New ideas, new paradigms, and reflections on programming & software*, 2013.
- [2] C. Wimmer and T. Würthinger, "Truffle: a self-optimizing runtime system," in *Proceedings of the 3rd annual conference on Systems, programming, and applications: software for humanity*. ACM, 2012.
- [3] G. Duboscq, L. Stadler, T. Würthinger, D. Simon, C. Wimmer, and H. Mössenböck, "Graal ir: An extensible declarative intermediate representation," in *Proceedings of the Asia-Pacific Programming Languages and Compilers Workshop*, 2013.
- [4] R. Mueller and L. Stadler, "Grcuda," [github.com/NVIDIA/grcuda](https://github.com/NVIDIA/grcuda).
- [5] J. E. Stone, D. Gohara, and G. Shi, "Opencl: A parallel programming standard for heterogeneous computing systems," *Computing in science & engineering*, vol. 12, no. 3, p. 66, 2010.
- [6] J. Luitjens, "Cuda streams: Best practices and common pitfalls," in *GPU Technology Conference*, 2015.
- [7] "Cuda graphs," [https://docs.nvidia.com/cuda/cuda-runtime-api/group\\_\\_CUDART\\_\\_GRAPH.html](https://docs.nvidia.com/cuda/cuda-runtime-api/group__CUDART__GRAPH.html), retrieved on 2020-10-12.
- [8] M. Abadi, P. Barham, J. Chen, Z. Chen, A. Davis, J. Dean, M. Devin, S. Ghemawat, G. Irving, M. Isard *et al.*, "Tensorflow: A system for large-scale machine learning," in *12th {USENIX} Symposium on Operating Systems Design and Implementation ({OSDI} 16)*, 2016, pp. 265–283.
- [9] L. Marchal, H. Nagy, B. Simon, and F. Vivien, "Parallel scheduling of dags under memory constraints," in *2018 IEEE International Parallel and Distributed Processing Symposium (IPDPS)*. IEEE, 2018.
- [10] Y. Xu, L. Liu, and Z. Ding, "Dag-aware joint task scheduling and cache management in spark clusters," in *2020 IEEE International Parallel and Distributed Processing Symposium (IPDPS)*. IEEE, 2020, pp. 378–387.
- [11] M. Y. Özkaya, A. Benoit, B. Uçar, J. Herrmann, and Ü. V. Çatalyürek, "A scalable clustering-based task scheduler for homogeneous processors using dag partitioning," in *2019 IEEE International Parallel and Distributed Processing Symposium (IPDPS)*. IEEE, 2019, pp. 155–165.
- [12] R. Mayer, C. Mayer, and L. Laich, "The tensorflow partitioning and scheduling problem: it's the critical path!" in *Proceedings of the 1st Workshop on Distributed Infrastructures for Deep Learning*, 2017.
- [13] A. Marchetti-Spaccamela, N. Megow, J. Schlöter, M. Skutella, and L. Stougie, "On the complexity of conditional dag scheduling in multi-processor systems," in *2020 IEEE International Parallel and Distributed Processing Symposium (IPDPS)*. IEEE, 2020, pp. 1061–1070.
- [14] A. Gray, "Getting started with cuda graphs," [developer.nvidia.com/blog/cuda-graphs](https://developer.nvidia.com/blog/cuda-graphs), 2019-09-05, retrieved on 2020-10-12.
- [15] T. Gautier, J. V. Lima, N. Maillard, and B. Raffin, "Xkaapi: A runtime system for data-flow task programming on heterogeneous architectures," in *2013 IEEE 27th International Symposium on Parallel and Distributed Processing*. IEEE, 2013, pp. 1299–1308.
- [16] C.-H. Hong, I. Spence, and D. S. Nikolopoulos, "Gpu virtualization and scheduling methods: A comprehensive survey," *ACM Computing Surveys (CSUR)*, vol. 50, no. 3, pp. 1–37, 2017.
- [17] V. T. Ravi, M. Becchi, G. Agrawal, and S. Chakradhar, "Supporting gpu sharing in cloud environments with a transparent runtime consolidation framework," in *Proceedings of the 20th international symposium on High performance distributed computing*, 2011, pp. 217–228.
- [18] J. Fumero, M. Papadimitriou, F. S. Zakkak, M. Xekalaki, J. Clarkson, and C. Kotselidis, "Dynamic application reconfiguration on heterogeneous hardware," in *Proceedings of the 15th ACM SIGPLAN/SIGOPS International Conference on Virtual Execution Environments*, 2019.
- [19] A. Klöckner, N. Pinto, Y. Lee, B. Catanzaro, P. Ivanov, and A. Fasih, "PyCUDA and PyOpenCL: A Scripting-Based Approach to GPU Run-Time Code Generation," *Parallel Computing*, vol. 38, 2012.
- [20] "Jcuda," [www.jcuda.org](http://www.jcuda.org), retrieved on 2020-10-12.
- [21] Y. Wen and M. F. O'Boyle, "Merge or separate? multi-job scheduling for opencl kernels on cpu/gpu platforms," in *Proceedings of the general purpose GPUs*, 2017, pp. 22–31.
- [22] B. Qiao, O. Reiche, J. Teich, and F. Hannig, "Unveiling kernel concurrency in multiresolution filters on gpus with an image processing dsl," in *Proceedings of the 13th Annual Workshop on General Purpose Processing using Graphics Processing Unit*, 2020, pp. 11–20.
- [23] Q. Chen, H. Yang, J. Mars, and L. Tang, "Baymax: Qos awareness and increased utilization for non-preemptive accelerators in warehouse scale computers," *ACM SIGPLAN Notices*, vol. 51, no. 4, pp. 681–696, 2016.
- [24] G. Chen, Y. Zhao, X. Shen, and H. Zhou, "Effisha: A software framework for enabling efficient preemptive scheduling of gpu," in *Proceedings of the 22nd ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming*, 2017, pp. 3–16.
- [25] F. Guo, Y. Li, J. C. Lui, and Y. Xu, "Decuda: Dynamic gpu scheduling with live migration support," in *Proceedings of the ACM Symposium on Cloud Computing*, 2019, pp. 114–125.
- [26] J. Jung, D. Park, Y. Do, J. Park, and J. Lee, "Overlapping host-to-device copy and computation using hidden unified memory," in *Proceedings of the 25th ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming*, 2020, pp. 321–335.
- [27] S. Che, M. Boyer, J. Meng, D. Tarjan, J. W. Sheaffer, S.-H. Lee, and K. Skadron, "Rodinia: A benchmark suite for heterogeneous computing," in *2009 IEEE international symposium on workload characterization (IISWC)*. Ieee, 2009, pp. 44–54.
- [28] J. Luitjens, "Faster parallel reductions on kepler," [developer.nvidia.com/blog/faster-parallel-reductions-kepler](https://developer.nvidia.com/blog/faster-parallel-reductions-kepler), 2014-02-14.
- [29] "Black & scholes option pricing," [docs.nvidia.com/cuda/cuda-samples/index.html#black-scholes-option-pricing](https://docs.nvidia.com/cuda/cuda-samples/index.html#black-scholes-option-pricing), retrieved on 2020-10-12.
- [30] "Cuda gaussian blur," [github.com/harrytang/cuda-gaussian-blur](https://github.com/harrytang/cuda-gaussian-blur).
- [31] J. M. Kleinberg, "Authoritative sources in a hyperlinked environment," *Journal of the ACM (JACM)*, vol. 46, no. 5, pp. 604–632, 1999.
- [32] Y. Liu and B. Schmidt, "Lightspmv: Faster csr-based sparse matrix-vector multiplication on cuda-enabled gpus," in *2015 IEEE 26th International Conference on Application-specific Systems, Architectures and Processors (ASAP)*. IEEE, 2015, pp. 82–89.