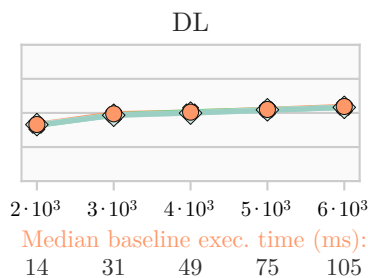
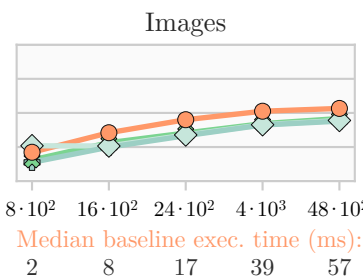
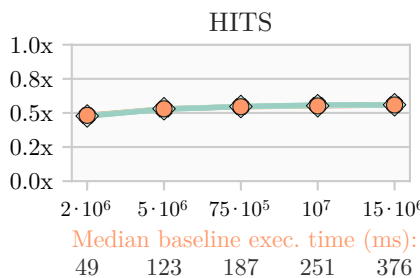
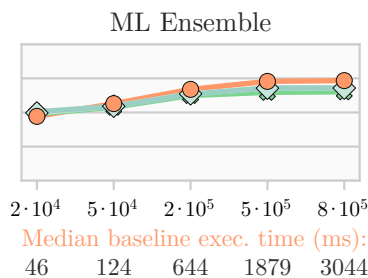
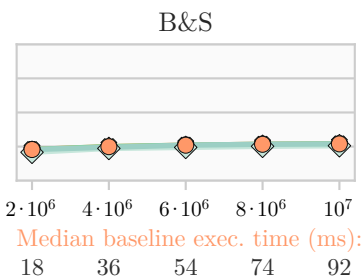
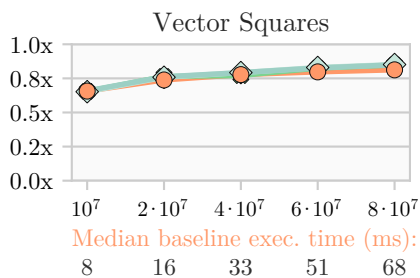


Speedup w.r.t minimum theoretical time

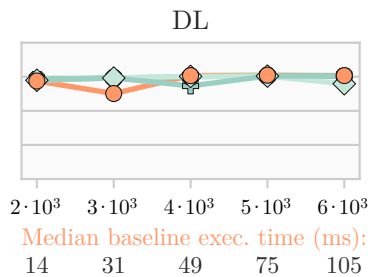
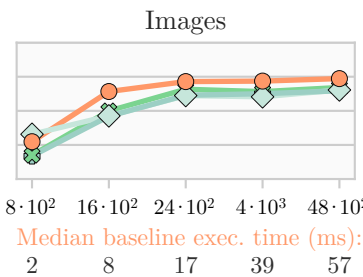
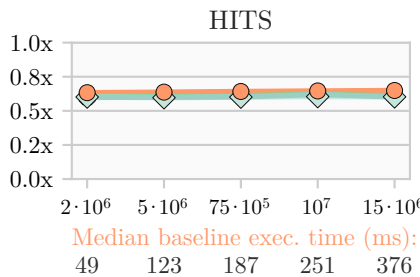
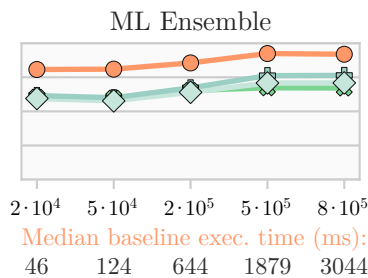
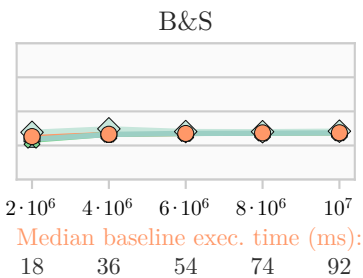
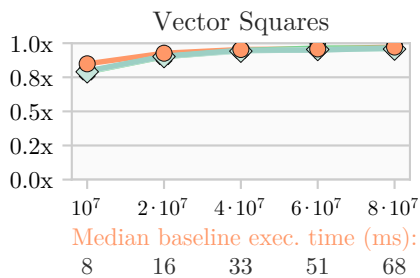
Block size:
2D=8x8, 3D=4x4x4

● 1D=32 ◆ 1D=256
✕ 1D=128 + 1D=1024

DAG Scheduling



Serial Scheduling



Input number of elements