74CBTLV3257-Q100

Quad 1-of-2 multiplexer/demultiplexer

Rev. 5 — 1 February 2024 Product data sheet

1. General description

The 74CBTLV3257-Q100 provides a quad 1-of-2 high-speed multiplexer/demultiplexer with common select (S) and output enable ($\overline{OE}$) inputs. The low ON resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise. When pin $\overline{OE}$ = LOW, one of the two switches is selected (low-impedance ON-state) with pin S. When pin $\overline{OE}$ = HIGH, all switches are in the high-impedance OFF-state, independent of pin S. To ensure the high-impedance OFF-state during power-up or power-down, $\overline{OE}$ should be tied to the V_{CC} through a pull-up resistor. The current-sinking capability of the driver determines the minimum value of the resistor.

Schmitt trigger action at control input, makes the circuit tolerant to slower input rise and fall times across the entire V_{CC} range from 2.3 V to 3.6 V.

This device is fully specified for partial power-down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Supply voltage range from 2.3 V to 3.6 V
- High noise immunity
- Complies with JEDEC standard:
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8-B/JESD36 (2.7 V to 3.6 V)
- 5 Ω switch connection between two ports
- Rail to rail switching on data I/O ports
- CMOS low power consumption
- Latch-up performance exceeds 250 mA per JESD78B Class I level A
- I_{OFF} circuitry provides partial Power-down mode operation
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Multiple package options
- DHVQFN package with Side-Wettable Flanks enabling Automatic Optical Inspection (AOI) of solder joints

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74CBTLV3257D-Q100	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74CBTLV3257PW-Q100	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74CBTLV3257BQ-Q100	-40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1

4. Marking

Table 2. Marking codes

Type number	Marking code[1]
74CBTLV3257D-Q100	74CBTLV3257D
74CBTLV3257PW-Q100	TLV3257
74CBTLV3257BQ-Q100	TV3257

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram

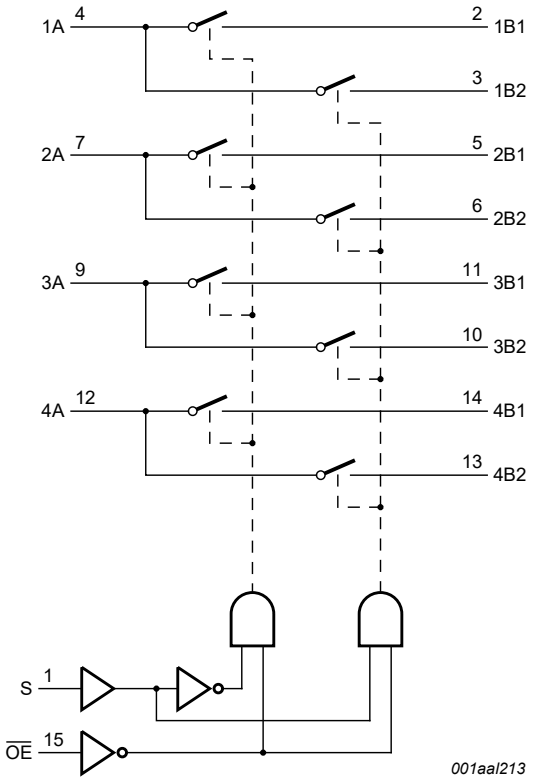
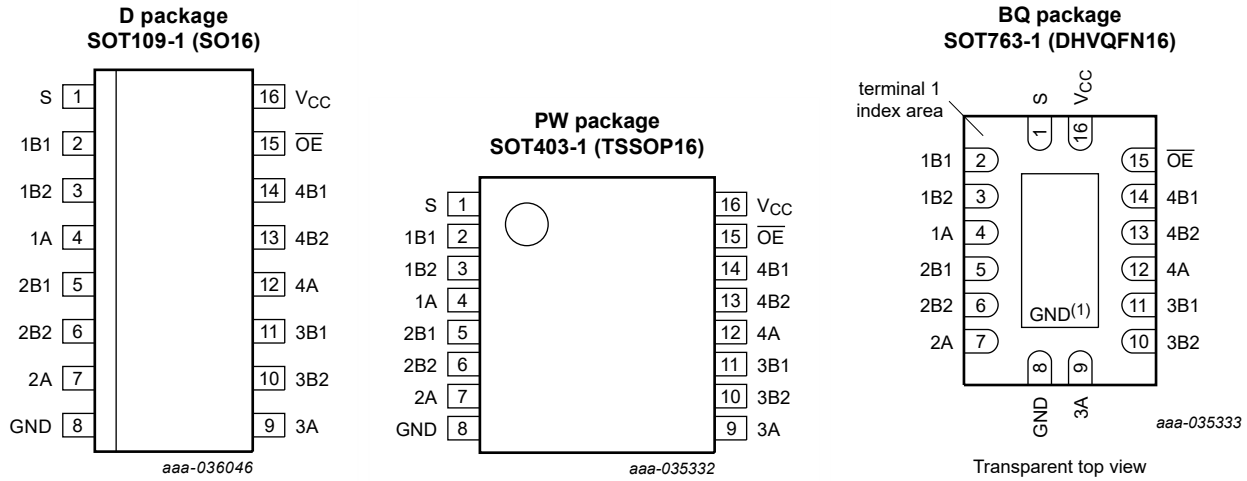


Fig. 1. Logic diagram

6. Pinning information

6.1. Pinning



(1) This is not a ground pin. There is no electrical or mechanical requirement to solder the pad. In case soldered, the solder land should remain floating or connected to GND.

6.2. Pin description

Table 3. Pin description

Symbol	Pin	Description
S	1	select input
1B1 to 4B1	2, 5, 11, 14	B1 input/output
1B2 to 4B2	3, 6, 10, 13	B2 input/output
1A to 4A	4, 7, 9, 12	A input/output
GND	8	ground (0 V)
$\overline{OE}$	15	output enable input (active LOW)
V_{CC}	16	supply voltage

7. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care.

Inputs		Function switch
$\overline{OE}$	S	
L	L	nA = nB1
L	H	nA = nB2
H	X	disconnect nA and nBn

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			-0.5	+4.6	V
V_I	input voltage	control inputs	[1]	-0.5	+4.6	V
V_{SW}	switch voltage	enable and disable mode	[2]	-0.5	V_{CC} + 0.5	V
I_{IK}	input clamping current	V_I < -0.5 V		-50	-	mA
I_{SK}	switch clamping current	V_I < -0.5 V		-50	-	mA
I_{SW}	switch current	V_{SW} = 0 V to V_{CC}		-	±128	mA
I_{CC}	supply current			-	+100	mA
I_{GND}	ground current			-100	-	mA
T_{stg}	storage temperature			-65	+150	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C				
		SOT109-1 (SO16) SOT403-1 (TSSOP16) SOT763-1 (DHVQFN16)	[3]	-	500	mW

[1] The minimum input voltage rating may be exceeded if the input clamping current ratings are observed.
[2] The switch voltage ratings may be exceeded if switch clamping current ratings are observed
[3] For SOT109-1 (SO16) package: P_{tot} derates linearly with 12.4 mW/K above 110 °C.
For SOT403-1 (TSSOP16) package: P_{tot} derates linearly with 8.5 mW/K above 91 °C.
For SOT763-1 (DHVQFN16) package: P_{tot} derates linearly with 11.2 mW/K above 106 °C.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			2.3	3.6	V
V_I	input voltage			0	3.6	V
V_{SW}	switch voltage	enable and disable mode		0	V_{CC}	V
T_{amb}	ambient temperature			-40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 2.3 V to 3.6 V	[1]	0	200	ns/V

[1] Applies to control signal levels.

10. Static characteristics

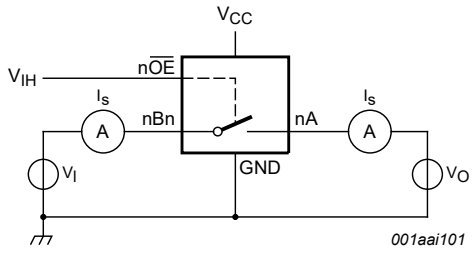
Table 7. Static characteristics

At recommended operating conditions voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T_{amb} = -40 °C to +85 °C			T_{amb} = -40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V_{IH}	HIGH-level input voltage	V_{CC} = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		V_{CC} = 3.0 V to 3.6 V	2.0	-	-	2.0	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		V_{CC} = 3.0 V to 3.6 V	-	-	0.9	-	0.9	V
I_I	input leakage current	pin $\overline{OE}$, S; V_{CC} = 3.6 V; V_I = GND to V_{CC}	-	-	±1	-	±20	µA
$I_{S(OFF)}$	OFF-state leakage current	V_{CC} = 3.6 V; see Fig. 2	-	-	±1	-	±20	µA
$I_{S(ON)}$	ON-state leakage current	V_{CC} = 3.6 V; see Fig. 3	-	-	±1	-	±20	µA
I_{OFF}	power-off leakage current	V_I or V_O = 0 V to 3.6 V; V_{CC} = 0 V	-	-	±10	-	±50	µA
I_{CC}	supply current	V_I = GND or V_{CC}; V_{SW} = GND or V_{CC}; V_{CC} = 3.6 V; I_O = 0 A	-	-	10	-	50	µA
ΔI_{CC}	additional supply current	pin $\overline{OE}$, S; V_{CC} = 3.6 V; V_I = V_{CC} - 0.6 V; V_{SW} = GND or V_{CC} [2]	-	-	300	-	2000	µA
C_I	input capacitance	pin $\overline{OE}$, S; V_{CC} = 3.3 V; V_I = 0 V to 3.3 V	-	0.9	-	-	-	pF
$C_{S(OFF)}$	OFF-state capacitance	V_{CC} = 3.3 V; V_I = 0 V to 3.3 V	-	5.2	-	-	-	pF
$C_{S(ON)}$	ON-state capacitance	V_{CC} = 3.3 V; V_I = 0 V to 3.3 V	-	14.3	-	-	-	pF

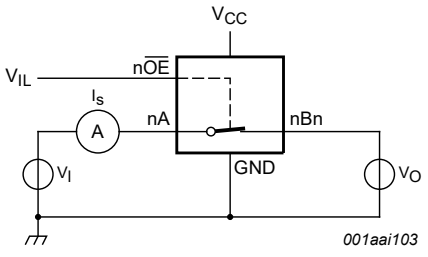
[1] All typical values are measured at T_{amb} = 25 °C.
[2] One input at 3 V, other inputs at V_{CC} or GND.

10.1. Test circuits



V_I = V_{CC} or GND and V_O = GND or V_{CC}.

Fig. 2. Test circuit for measuring OFF-state leakage current (one switch)



V_I = V_{CC} or GND and V_O = open circuit.

Fig. 3. Test circuit for measuring ON-state leakage current (one switch)

10.2. ON resistance

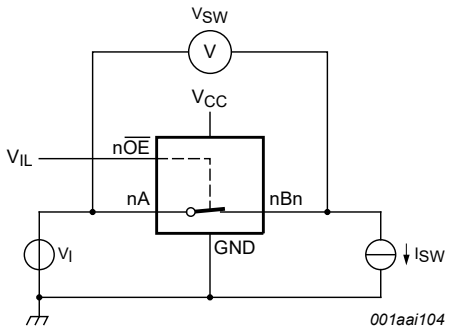
Table 8. Resistance R_{ON}

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 4.

Symbol	Parameter	Conditions	T_{amb} = -40 °C to +85 °C			T_{amb} = -40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
R_{ON}	ON resistance	V_{CC} = 2.3 V to 2.7 V; see Fig. 5 to Fig. 7 [2]						
		I_{SW} = 64 mA; V_I = 0 V	-	4.2	8.0	-	15.0	Ω
		I_{SW} = 24 mA; V_I = 0 V	-	4.2	8.0	-	15.0	Ω
		I_{SW} = 15 mA; V_I = 1.7 V	-	8.4	40.0	-	60.0	Ω
		V_{CC} = 3.0 V to 3.6 V; see Fig. 8 to Fig. 10						
		I_{SW} = 64 mA; V_I = 0 V	-	4.0	7.0	-	11.0	Ω
		I_{SW} = 24 mA; V_I = 0 V	-	4.0	7.0	-	11.0	Ω
		I_{SW} = 15 mA; V_I = 2.4 V	-	6.2	15.0	-	25.5	Ω

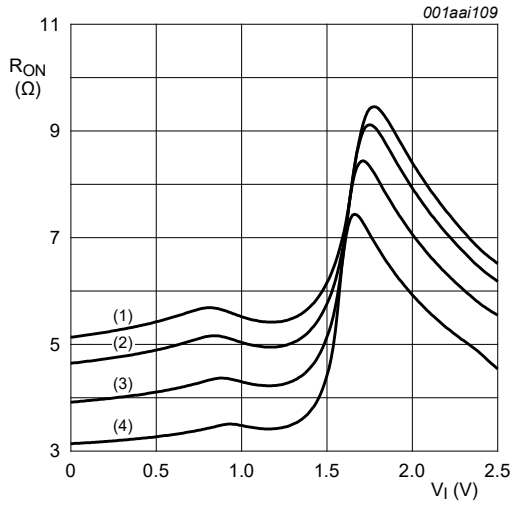
[1] Typical values are measured at T_{amb} = 25 °C and nominal V_{CC}.
[2] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

10.3. ON resistance test circuit and graphs



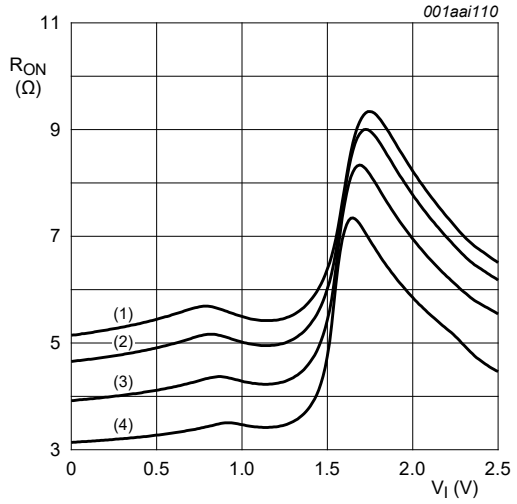
$R_{ON} = V_{SW} / I_{SW}$.

Fig. 4. Test circuit for measuring ON resistance (one switch)



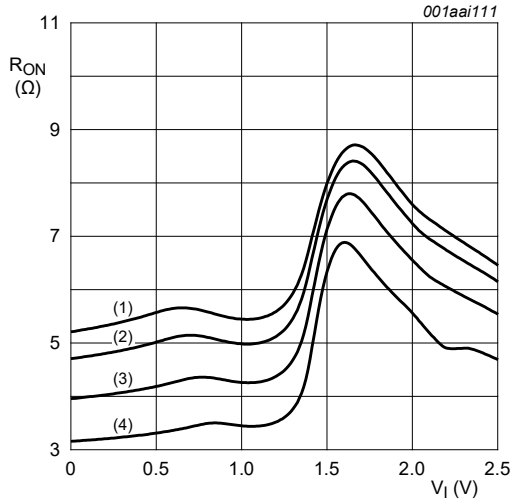
(1) T_{amb} = 125 °C
(2) T_{amb} = 85 °C
(3) T_{amb} = 25 °C
(4) T_{amb} = -40 °C

Fig. 5. ON resistance as a function of input voltage; V_{CC} = 2.5 V; I_{SW} = 15 mA



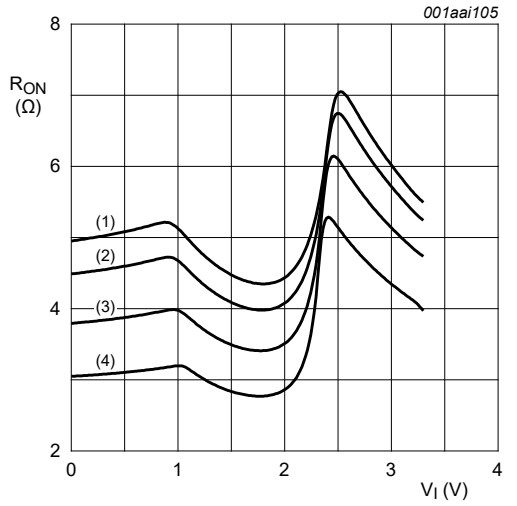
(1) T_{amb} = 125 °C
(2) T_{amb} = 85 °C
(3) T_{amb} = 25 °C
(4) T_{amb} = -40 °C

Fig. 6. ON resistance as a function of input voltage; V_{CC} = 2.5 V; I_{SW} = 24 mA



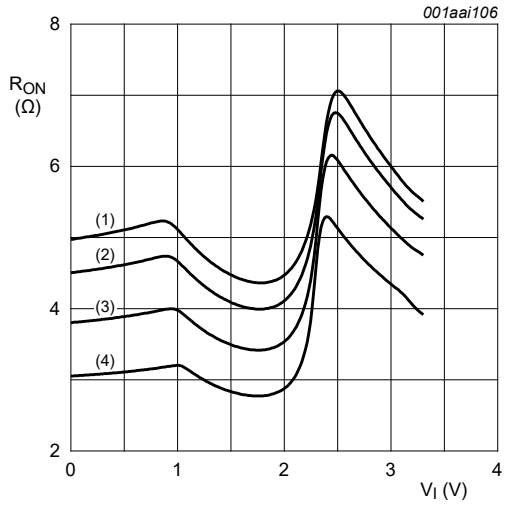
(1) T_{amb} = 125 °C
(2) T_{amb} = 85 °C
(3) T_{amb} = 25 °C
(4) T_{amb} = -40 °C

Fig. 7. ON resistance as a function of input voltage; V_{CC} = 2.5 V; I_{SW} = 64 mA



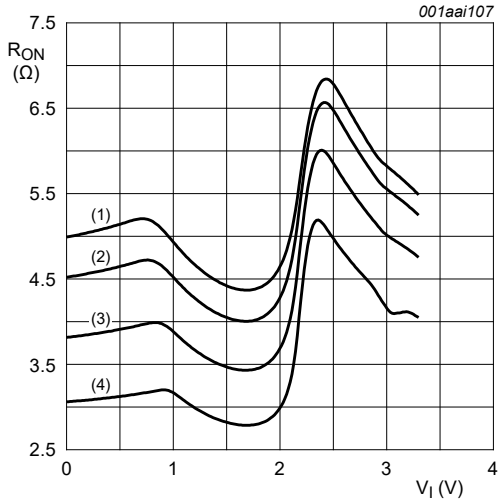
(1) T_{amb} = 125 °C
(2) T_{amb} = 85 °C
(3) T_{amb} = 25 °C
(4) T_{amb} = -40 °C

Fig. 8. ON resistance as a function of input voltage; V_{CC} = 3.3 V; I_{SW} = 15 mA



(1) T_{amb} = 125 °C
(2) T_{amb} = 85 °C
(3) T_{amb} = 25 °C
(4) T_{amb} = -40 °C

Fig. 9. ON resistance as a function of input voltage; V_{CC} = 3.3 V; I_{SW} = 24 mA



(1) T_{amb} = 125 °C
(2) T_{amb} = 85 °C
(3) T_{amb} = 25 °C
(4) T_{amb} = -40 °C

Fig. 10. ON resistance as a function of input voltage; V_{CC} = 3.3 V; I_{SW} = 64 mA

11. Dynamic characteristics

Table 9. Dynamic characteristics

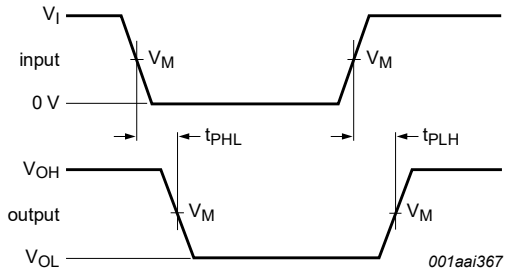
GND = 0 V; for test circuit see Fig. 13.

Symbol	Parameter	Conditions	T_{amb} = -40 °C to +85 °C			T_{amb} = -40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
t_{pd}	propagation delay	nA to nBn or nBn to nA; see Fig. 11 [2] [3]						
		V_{CC} = 2.3 V to 2.7 V	-	-	0.15	-	0.25	ns
		V_{CC} = 3.0 V to 3.6 V	-	-	0.15	-	0.25	ns
		S to nA; see Fig. 11 [3]						
		V_{CC} = 2.3 V to 2.7 V	1.0	3.8	6.1	1.0	6.7	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	3.2	5.3	1.0	5.8	ns
t_{en}	enable time	$\overline{OE}$ to nA or nBn; see Fig. 12 [4]						
		V_{CC} = 2.3 V to 2.7 V	1.0	2.2	5.6	1.0	6.2	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	2.0	5.0	1.0	5.5	ns
		S to nBn; see Fig. 12 [4]						
		V_{CC} = 2.3 V to 2.7 V	1.0	3.5	6.1	1.0	6.7	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	3.0	5.3	1.0	5.8	ns

Symbol	Parameter	Conditions	T_{amb} = -40 °C to +85 °C			T_{amb} = -40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
t_{dis}	disable time	$\overline{OE}$ to nA or nBn; see Fig. 12 [5]						
		V_{CC} = 2.3 V to 2.7 V	1.0	2.6	5.5	1.0	6.1	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	3.1	5.5	1.0	6.1	ns
		S to nBn; see Fig. 12 [5]						
		V_{CC} = 2.3 V to 2.7 V	1.0	2.6	4.8	1.0	5.3	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	3.2	4.5	1.0	5.0	ns

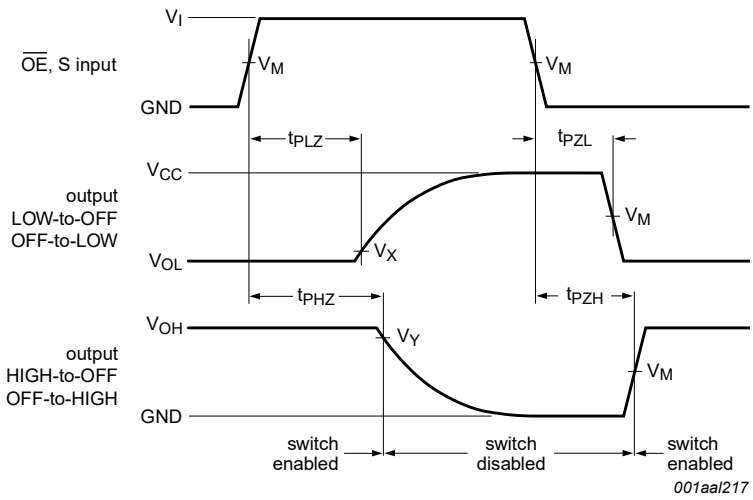
[1] All typical values are measured at T_{amb} = 25 °C and at nominal V_{CC}.
[2] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the load capacitance, when driven by an ideal voltage source (zero output impedance).
[3] t_{pd} is the same as t_{PLH} and t_{PHL}.
[4] t_{en} is the same as t_{PZH} and t_{PZL}.
[5] t_{dis} is the same as t_{PHZ} and t_{PLZ}.

11.1. Waveforms and test circuit



Measurement points are given in Table 10.
Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 11. The data input (nA or nBn) to output (nBn or nA) propagation delays

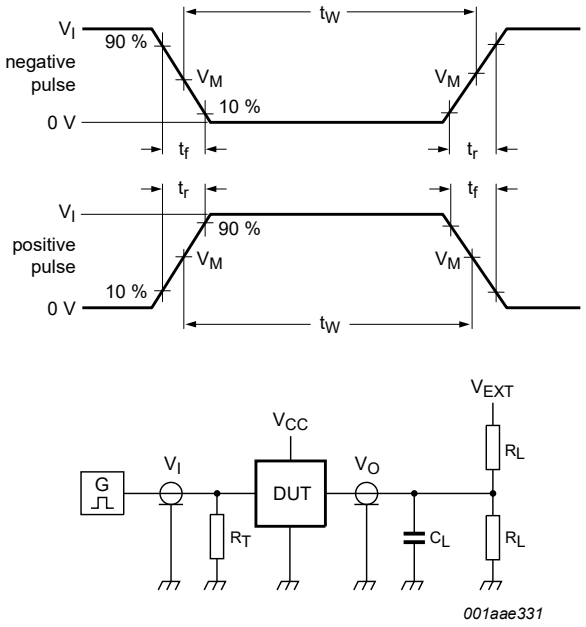


Measurement points are given in Table 10.
Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 12. Enable and disable times

Table 10. Measurement points

Supply voltage	Input			Output		
V_{CC}	V_M	V_I	$t_r = t_f$	V_M	V_X	V_Y
2.3 V to 2.7 V	0.5 × V_{CC}	V_{CC}	≤ 2.0 ns	0.5 × V_{CC}	V_{OL} + 0.15 V	V_{OH} - 0.15 V
3.0 V to 3.6 V	0.5 × V_{CC}	V_{CC}	≤ 2.0 ns	0.5 × V_{CC}	V_{OL} + 0.3 V	V_{OH} - 0.3 V



Test data is given in Table 11.

Definitions for test circuit:

R_L = Load resistance;

C_L = Load capacitance including jig and probe capacitance;

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator;

V_{EXT} = External voltage for measuring switching times.

Fig. 13. Test circuit for measuring switching times

Table 11. Test data

Supply voltage	Load		V_{EXT}		
V_{CC}	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
2.3 V to 2.7 V	30 pF	500 Ω	open	GND	2 × V_{CC}
3.0 V to 3.6 V	50 pF	500 Ω	open	GND	2 × V_{CC}

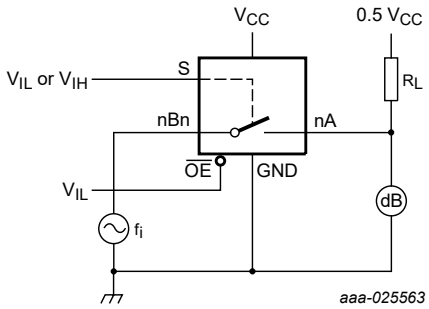
11.2. Additional dynamic characteristics

Table 12. Additional dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); V_I = GND or V_{CC} (unless otherwise specified); $t_r = t_f \leq 2.5$ ns.

Symbol	Parameter	Conditions	T_{amb} = 25 °C			Unit
			Min	Typ	Max	
$f_{(-3dB)}$	-3 dB frequency response	V_{CC} = 3.3 V; R_L = 50 Ω; see Fig. 14 [1]	-	398	-	MHz

[1] f_i is biased at 0.5 × V_{CC}.

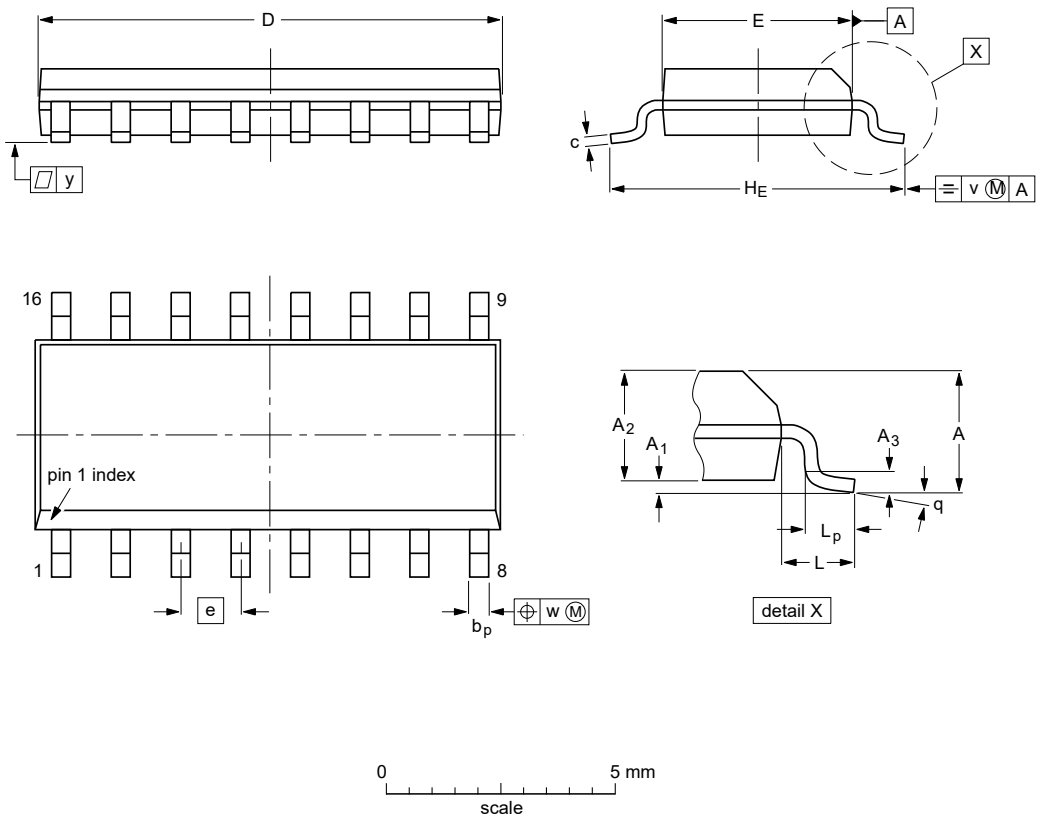


$\overline{OE}$ connected to GND; Adjust f_i voltage to obtain 0 dBm level at output.
Increase f_i frequency until dB meter reads -3 dB.

Fig. 14. Test circuit for measuring the frequency response when channel is in ON-state

12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



Dimensions (inch dimensions are derived from the original mm dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	v	w	y	θ
mm	max	1.75	0.25			0.51	0.25	10.0	4.0		6.2		1.27				8°
	nom				0.25					1.27		1.05		0.2	0.25	0.1	
	min		0.10	1.25		0.31	0.10	9.8	3.8		5.8		0.4				0°
inches	max	0.069	0.010			0.020	0.010	0.394	0.16		0.244		0.05				8°
	nom				0.01					0.05		0.041		0.008	0.01	0.004	
	min		0.004	0.049		0.012	0.004	0.386	0.15		0.228		0.016				0°

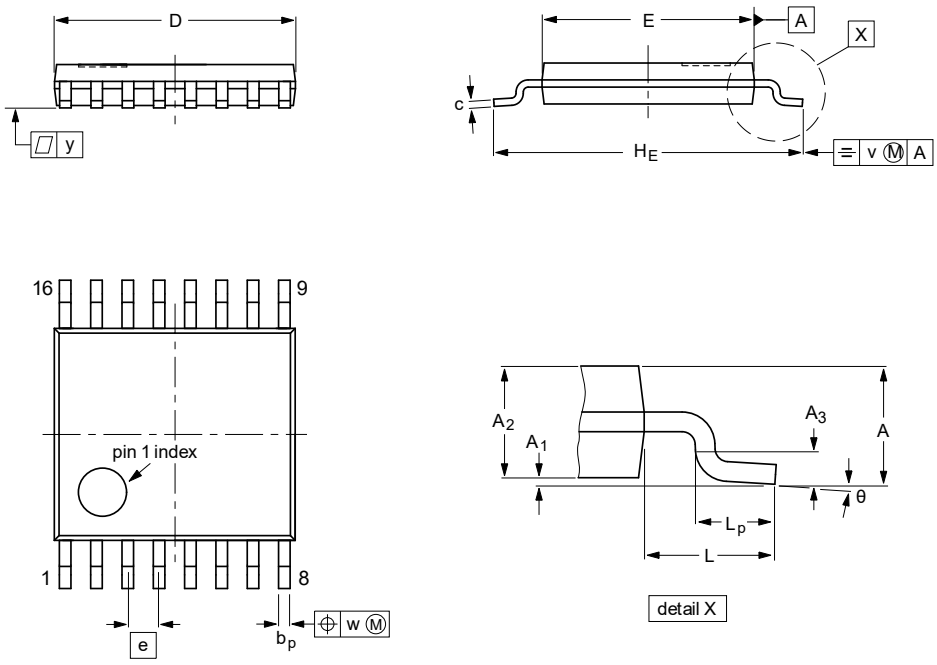
Note
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

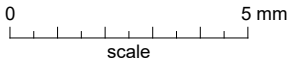
sot109-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT109-1		MS-012				~~03-02-19~~ 23-10-27

Fig. 15. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**





Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	θ
mm	max	1.20	0.15	1.05		0.30	0.2	5.1	4.5		6.6		0.75				8°
	nom				0.25					0.65		1		0.2	0.1	0.1	
	min		0.05	0.80		0.19	0.09	4.9	4.3		6.2		0.45				0°

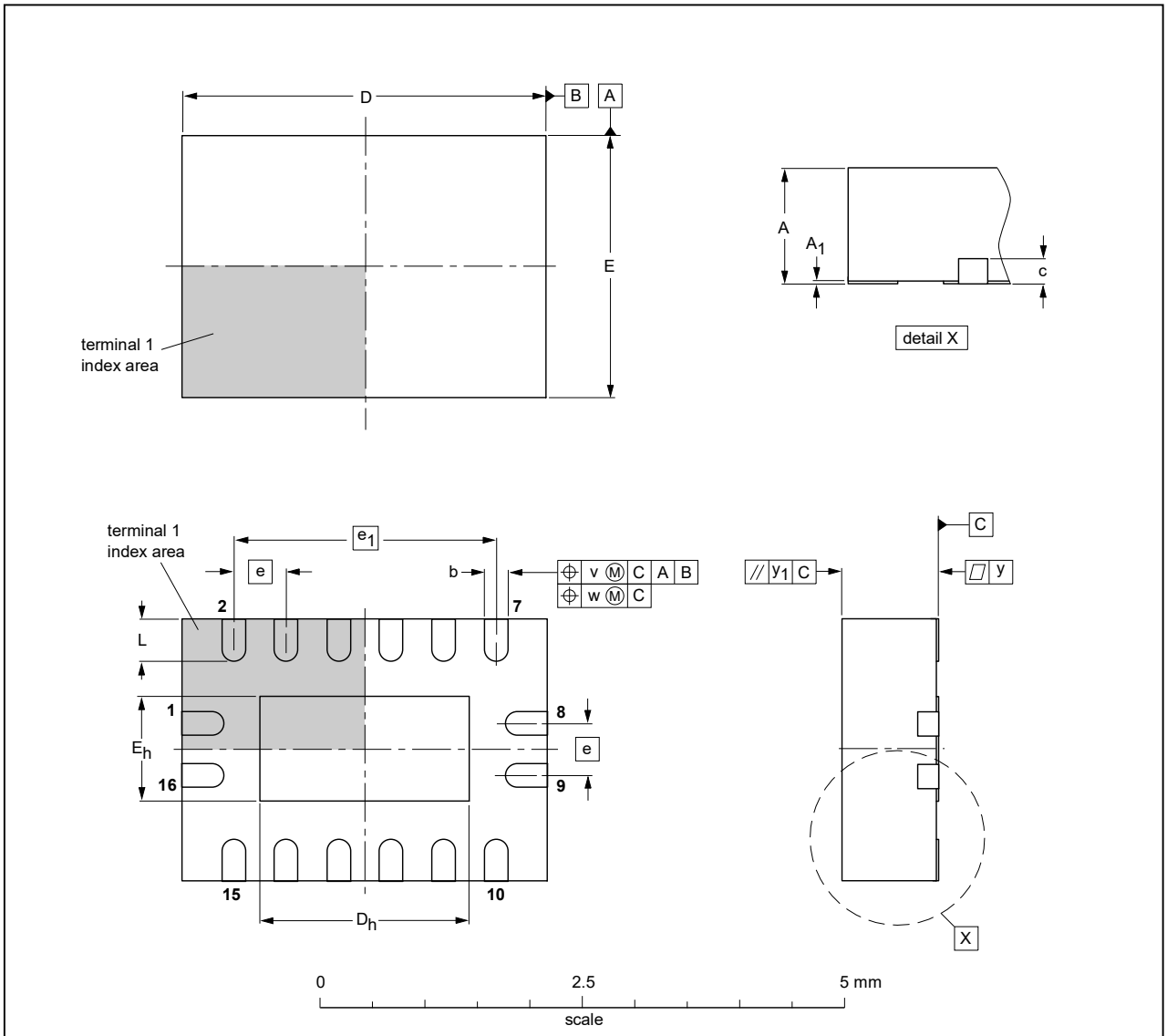
Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

sot403-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~03-02-18~~ 23-10-27

Fig. 16. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm **SOT763-1**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max.	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	3.6 3.4	2.15 1.85	2.6 2.4	1.15 0.85	0.5	2.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT763-1	- - -	MO-241	- - -			~~02-10-17~~ 03-01-27

Fig. 17. Package outline SOT763-1 (DHVQFN16)

13. Abbreviations

Table 13. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model

14. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74CBTLV3257_Q100 v.5	20240201	Product data sheet	-	74CBTLV3257_Q100 v.4
Modifications:	• Section 2: ESD specification updated according to the latest JEDEC standard. • Fig. 15, Fig. 16: Aligned SO and TSSOP package outline drawings to JEDEC MS-012 and MO-153			
74CBTLV3257_Q100 v.4	20200714	Product data sheet	-	74CBTLV3257_Q100 v.3
Modifications:	• Section 2 updated. • Section 4 added. • Table 5: Derating values for P_{tot} total power dissipation updated.			
74CBTLV3257_Q100 v.3	20190409	Product data sheet	-	74CBTLV3257_Q100 v.2
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Type number 74CBTLV3257DS-Q100 (SSOP16/SOT519-1) removed.			
74CBTLV3257_Q100 v.2	20161110	Product data sheet	-	74CBTLV3257_Q100 v.1
Modifications:	• Section 11.2 added.			
74CBTLV3257_Q100 v.1	20130704	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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