SMIC 0.18um Generic Logic Process
UHD RVT
Standard Cell Library Data-Book
V0.4a

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Revision History

This document contains the release history for SMIC 0.18um Generic Process UHD RVT Standard Cell Library Data-Book.

IP Code	Release Version	Date of Release	Update Description
scc018ug_uhd_rvt	0.0	Sep 2013	Initial Release
scc018ug_uhd_rvt	0.1	Dec 2014	Update Spice Model
scc018ug_uhd_rvt	0.2	Nov 2015	Update Spice Model Update GDS (1833_V1.18_1.drc)
scc018ug_uhd_rvt	0.3	Nov 2016	Update GDS
scc018ug_uhd_rvt	0.4	June 2017	Update GDS Update Spice Model
scc018ug_uhd_rvt	0.4a	Nov 2017	Verilog Model: Change timing arc condition from “===” to “==”. Liberty: Change timing arc condition from “===” to “==”.

Table of Contents

Introduction

SMIC's standard cell library is custom-designed and tested to provide the optimum combination of high-performance and high-density cells. Cell optimization is derived from extensive internal and external custom designs and place-and-route analysis; whereas, library optimization is characterized by thorough simulation of library functions and of various drive strengths using leading simulation and place-and-route tools to produce superior GDSII results.

Organization of the Data-Book

The introduction is organized into several sections:

1. Global Parameters provides library overview and some general specifications.
2. Timing Constraint describes what type of timing specification is measured from each cell.
3. Naming Conventions provides standard cells' name conventions.
4. Special Cells defines the various types of special cells in the library.
5. Standard Cell Library Interpretation explains the components in each of the datasheets.

Global Parameters

This section defines the general specifications for this Standard Cell Library. It includes physical cell specifications, electrical specifications, propagation delay specifications, timing specifications, and power calculation.

Physical Cell Specifications

Table 1. shows the physical design cell specification for this standard cell library.

Table 1. Physical Cell Specification

Drawn Gate Length (um)	0.18
Metal Layer(s) in cell	M1
Layout Grid (um)	0.005
Vertical Pin Grid (um)	0.56n
Horizontal Pin Grid (um)	0.56n+0.28
Cell power and Ground Rail Width (um)	0.38
Cell Height (um)	3.36
N-well and substrate distance	10.0

Note

The library supports designs with multi metal-layer. For different layers of top-level metal, it is possible that a change in the design rules description within the technology file is required, because the top metal has greater minimum width, minimum spacing, and minimum area requirements. Please refer to " 0.18um Logic Salicide 1.8V/3.3V Design Rule " for more information. It is crucial to define these rules correctly within the technology file for the place-and-route tool to function properly.

Table 2. lists the electrical specifications for this standard cell library.

Table 2. Electrical Specifications

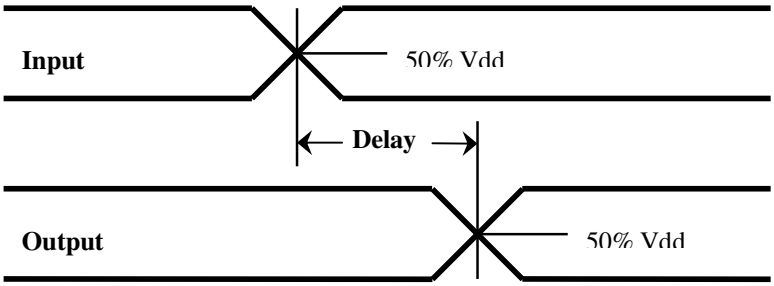
Corners	Best	Best: Zero Temp	Typical	Typical 85C	Worst
Supply Voltage (V)	1.98	1.98	1.80	1.80	1.62
Junction Temperature (°C)	-40	0	25	85	125

Timing Constrains

Propagation Delay and Transition Time

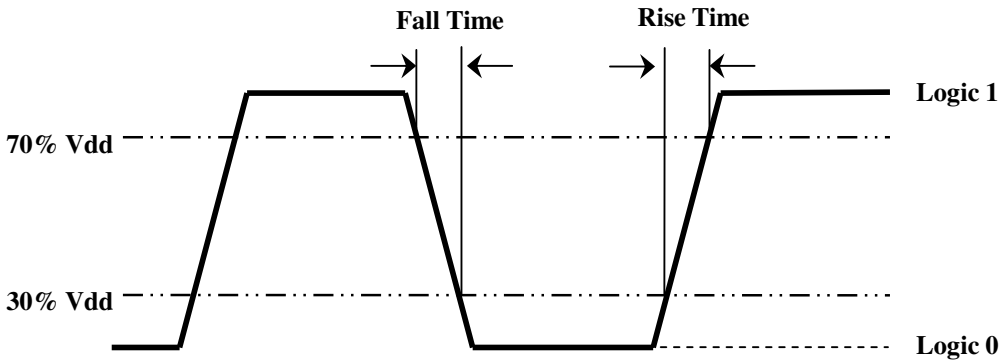
Propagation delay is the sum of the intrinsic delay, the load delay, and the input-slew delay of a cell. Delays are defined as the time interval between the input stimulus and output crossing 50% of the Vdd value. The propagation delay is illustrated in Figure 1. below.

Figure 1. Propagation Delay



Transition time or slew rate is defined as the time interval between crossings of 30% to 70% of Vdd value on a signal. Transition time is shown in Figure 2. for both rising and falling signals.

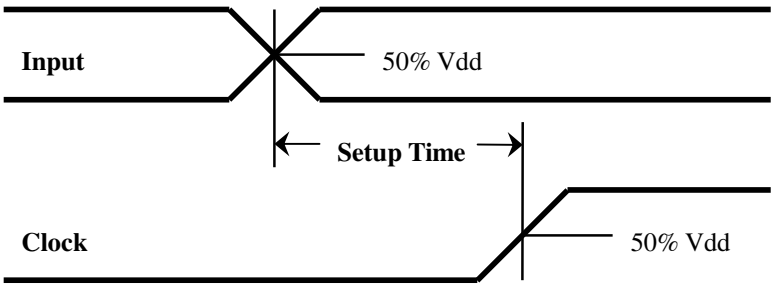
Figure 2. Transition Time



Setup Time

Setup time for a sequential cell is the minimum period of time the data signal must remain stable before the active edge of the clock (or another specified signal) to ensure correct function at the output. Setup constraint values are measured as the interval between the data signal crossing 50% of Vdd for rising or falling data and the clock signal crossing 50% of Vdd for rising or falling clocks. For measurement of setup time, the data signal is kept stable indefinitely after the clock edge. Definition of setup time for a positive-edge triggered sequential cell is shown in Figure 3.

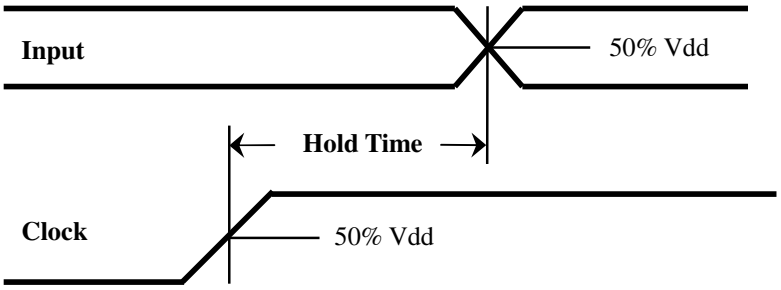
Figure 3. Setup Time



Hold Time

Hold time for a sequential cell is the minimum period of time the data signal must remain stable after the active edge of the clock (or another specified signal) to ensure correct function at the output. Hold constraint values are measured as the interval between the data signal crossing 50% of Vdd value and the clock signal crossing 50% of Vdd for either rise or fall transitions on both signals. For measurement of hold time, the data signal is kept stable indefinitely before the clock edge. Definition of fall time for a positive-edge triggered sequential cell is shown in Figure 4.

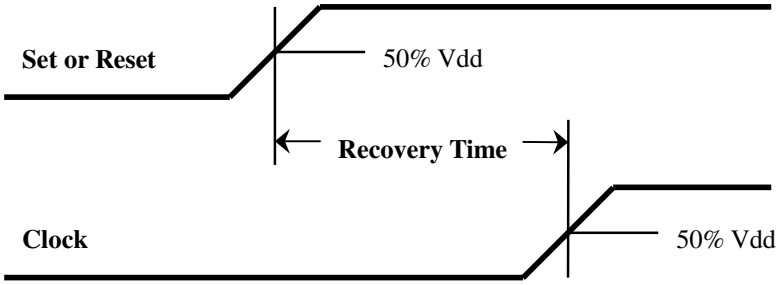
Figure 4. Hold Time



Recovery Time

Recovery time for sequential cell is the minimum length of time that the active-low set or reset signal must remain high before the active edge of the clock to ensure correct cell function. Recovery constraint value is measured as the interval between the set or reset signal crossing 50% of Vdd and the clock signal crossing 50% of Vdd for rising or falling clocks. For measurement of recovery time, the set or reset signal is held stable indefinitely after the clock edge. Definition of recovery time is shown below in Figure 5.

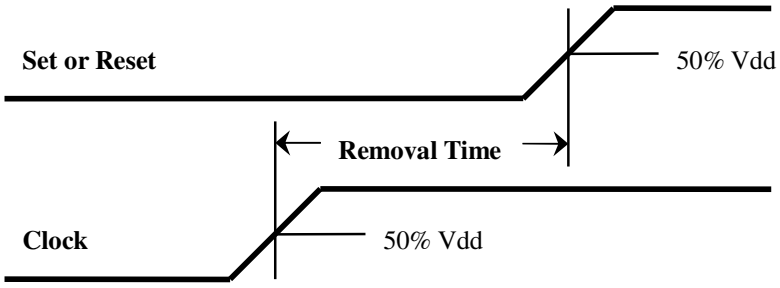
Figure 5. Recovery Time



Removal Time

Removal time for sequential cell is the minimum length of time that the set or reset signals must remain low after the active edge of the clock to ensure correct cell function. Removal constraint value is measured as the interval between the set or reset signal crossing 50% of Vdd and the clock signal crossing 50% of Vdd for rising or falling clocks. For measurement of removal time, the set or reset signal is held stable indefinitely before the clock edge. Definition of removal time is shown in Figure 6.

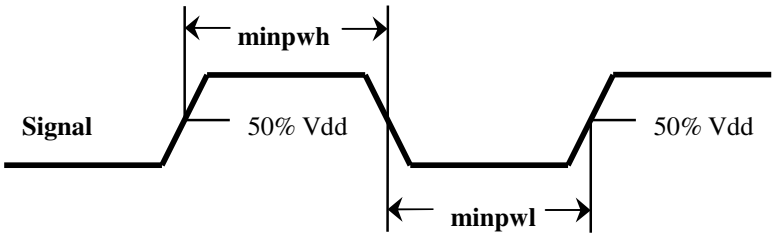
Figure 6. Removal Time



Minimum Pulse Width

Minimum pulse width is the minimum period of time between the leading the trailing edges of a pulse waveform. Minimum pulse width high (minpwh) is measured as the interval between the rising edge of signal crossing 50% of Vdd and the falling edge of signal crossing 50% of Vdd. Minimum pulse width low (minpwl) is measured as the interval between the falling edge of signal crossing 50% of Vdd and the rising edge of signal crossing 50% of Vdd. Minimum pulse width is illustrated in Figure 7.

Figure 7. Minimum Pulse Width



Special Cells

This section discusses the special cell types within the SMIC Standard Cell Library.

N-Well and Substrate Tie Cells

FILLTIE* are N-WELL/Substrate Tie Cells. This standard cell library is TAP-LESS. It is required to tie N-Well to VDD and substrate to VSS before place-and-route using the FILLTIE cells. You must pre-place the FILLTIE cell in every placement row and the space between FILLTIE cells must meet the latch-up design rules. Figures 8 and 9 illustrate two placement styles of the FILLTIE cells.

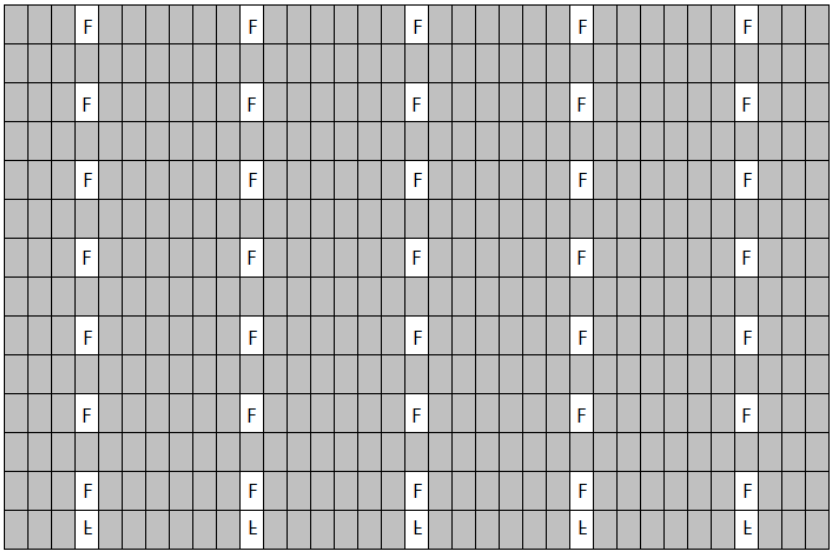


Figure 8. Normal placement of FILLTIE cells

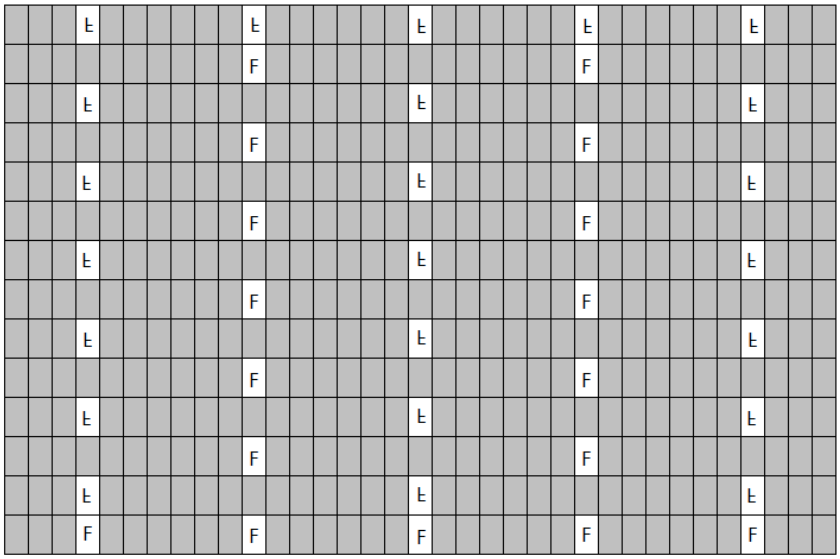
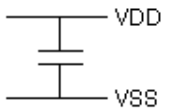


Figure 9. Flipped placement of FILLTIE cells

De-CAP Cells

FDCAP* are De-CAP cells in this library. De-CAP is composed of a PMOS and NMOS device to form decoupling capacitors between V_{DD} and V_{SS} rails so as to reduce the voltage bounce on the power rails. The De-CAP functional schematic is shown in Figure 10. below.

Figure 10. De-CAP Functional Schematic



FILLER Cells

F_FILL* are FILL cell. The FILL cells are used to connect power and ground rails across an area with no cells during place and route. It is used to ensure that gaps do not occur between well or implant layers which in some cases can cause DRC violations.
Suggestion: You'd better insert larger FILL CELL before insert the smallest FILL CELL, or your physical design will suffer from Density Error.

PULL0/1 Cells

The PULL0 and PULL1 cells provide ESD protection of signal inputs from power and ground rails. These cells provide diffusion-driven inputs for signal pins. If these cells are not used and Via(s) are dropped on the power rails, DRC error or shorts may occur. Any input pin that will be preset to 0/1 need connect PULL0 / PULL1 cell rather than VSS/VDD.
Suggestion: The fan-out of PULL0 and PULL1 should be less than 4 or the input pin will not be correctly pre-set.

Antenna Cells

F_DIODE* are antenna cells. During place-and-route, when the router fails to fix antenna violations, you can use antenna cell to insert a diode near the gate of the affected transistor.

Naming Conventions

This section provides the naming convention for this Standard Cell Library.
. The syntax is: **<Cell Type><Options> <Drive Selection>**

Example:

AND2V1: AND is Cell Type, 2 is the number of inputs, V1 is driving strength.

Cell Type	Description	Options
INV	Inverter cell	CKINV :Inverting Clock Inverter TINV: Tri-state inverter
BUF	Buffer cell	CLKBUF: Clock buffer TBUF: Tri-state buffer
AND	AND cell	2/3/4: The number of input pins
NAND	NAND cell	2/3/4: The number of input pins
I2NAND	NAND cell	3/4: with 2 Inverted Inputs
OR	OR cell	2/3/4: The number of input pins
NOR	NOR cell	2/3/4: The number of input pins
AO	AND-OR cell	21/211/221: The number of AND groups and additional inputs
OA	OR-AND cell	21/211/221: The number of OR groups and additional inputs
AOI	AND-OR-Inverter cell	21/211/221: The number of AND groups and additional inputs
OAI	OR-AND-Inverter cell	21/211/221: The number of OR groups and additional inputs
XOR	Exclusive OR cell	2/3:The number of input pins
XNOR	Exclusive NOR cell	2/3:The number of input pins
DEL	Delay cell	1/2/3/4: Delay class
AC	Full adder carry-generator	AC1CIN:with active low carry-in (CIN) AC1CON: with carry in (CI)
AD	Full adder cell	AD1CSCIN: with CO and CIN AD1CON: with CON and CI AD2 provides a carry-select adder function
ADH	Half adder cell	ADH1CIN with CO and CIN ADH1CON with CON and CI
MUX	Multiplexer cell	2/4:The number of input pins N: Inverted
D	Flip-Flop cell	SD: D flip-flop with scan ED: D flip-flop with enable SED: D flip-flop with scan enable DN: Negative edge clock trigger DQ: Output Q only DG: With synchronous (Reset/Set) S: Set R: Reset X: Mux Inputs
LA	Transparent Latch cell	L: Active low enable

		H: Active high enable CLKLA: Clock-gating latch R: Reset S: Set T: Tri-state transparent latch
HOLD	Weak bus holder	

All cells' names must be in upper case. For flip-flop cells, the default is:

Positive edge clock trigger

Asynchronous Set or Reset

With Q and QN

For latch cells, the default is:

Active high enable

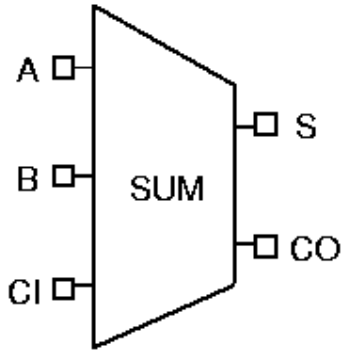
Asynchronous Set or Reset

Standard Cell Datasheet

AD1UHD

Cell Description

1-Bit Full Adder provides the arithmetic sum (S) and carry-out (CO) of two operands (A, B) with carry-in (CI).
CO=((A&B)|(A&CI)|(B&CI))
S=(A^B^CI)



Function Table

A	B	CI	CO	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Cell Size

CellName	Height(um)	Width(um)
AD1UHDV1	3.360	14.000
AD1UHDV2	3.360	16.240

Pin Power (uW/MHz)

Pin	V1	V2
A	0.01713	0.02745
B	0.01701	0.02770
CI	0.01666	0.02668

Pin Capacitance (pf)

Pin	V1	V2

A	0.00995	0.01211
B	0.00933	0.01086
CI	0.00820	0.01099

Max Leakage Power (uW)

V1	V2
0.00009530	0.00015488

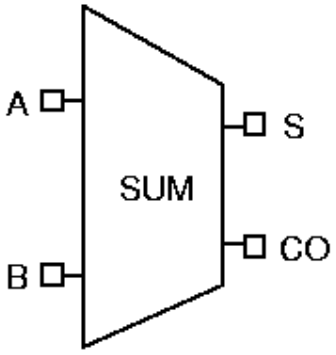
Delay Table (ns)

Description	V1	V2
A→CO_FALL	0.24355	0.25307
A→CO_RISE	0.15240	0.12970
B→CO_FALL	0.24166	0.27016
B→CO_RISE	0.14688	0.13737
CI→CO_FALL	0.20592	0.19244
CI→CO_RISE	0.13095	0.12685
A→S_FALL	0.28900	0.28570
A→S_RISE	0.26656	0.27204
B→S_FALL	0.28942	0.29385
B→S_RISE	0.26395	0.28239
CI→S_FALL	0.28002	0.28310
CI→S_RISE	0.24585	0.23674

ADH1UHD

Cell Description

1-Bit Half Adder provides the arithmetic sum (S) and carry-out (CO) of two operands (A, B).
CO=(A&B)
S=(A^B)



Function Table

B	A	S	CO
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Cell Size

CellName	Height(um)	Width(um)
ADH1UHDV1	3.360	6.160
ADH1UHDV2	3.360	7.840
ADH1UHDV3	3.360	9.520

Pin Power (uW/MHz)

Pin	V1	V2	V3
A	0.01235	0.01935	0.02811
B	0.01257	0.01956	0.02842

Pin Capacitance (pf)

Pin	V1	V2	V3
A	0.00482	0.00627	0.00651
B	0.00513	0.00661	0.00679

Max Leakage Power (uW)

V1	V2	V3
0.00007768	0.00012893	0.00017788

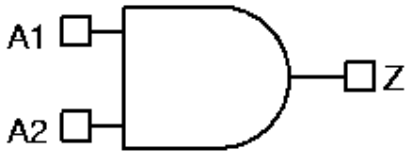
Delay Table (ns)

Description	V1	V2	V3
A→CO_FALL	0.11122	0.09198	0.10965
A→CO_RISE	0.10203	0.09655	0.10673
B→CO_FALL	0.12141	0.10067	0.11863
B→CO_RISE	0.10593	0.10085	0.11059
A→S_FALL	0.16540	0.17547	0.19104
A→S_RISE	0.13008	0.13330	0.15497
B→S_FALL	0.16259	0.17286	0.18816
B→S_RISE	0.13614	0.13766	0.16035

AND2UHD

Cell Description

2-Input AND
Z=(A1&A2)



Function Table

A1	A2	Z
0	X	0
1	0	0
1	1	1

Cell Size

CellName	Height(um)	Width(um)
AND2UHDV0P4	3.360	2.800
AND2UHDV0P7	3.360	2.800
AND2UHDV1	3.360	2.800
AND2UHDV2	3.360	3.920
AND2UHDV3	3.360	4.480
AND2UHDV4	3.360	6.720
AND2UHDV6	3.360	8.400
AND2UHDV8	3.360	11.200

Pin Power (uW/MHz)

Pin	V0P4	V0P7	V1	V2	V3	V4	V6	V8
A1	0.00651	0.00805	0.00929	0.01535	0.02232	0.02964	0.04324	0.05912
A2	0.00703	0.00891	0.01020	0.01657	0.02362	0.03170	0.04579	0.06292

Pin Capacitance (pf)

Pin	V0P4	V0P7	V1	V2	V3	V4	V6	V8
A1	0.00254	0.00281	0.00288	0.00418	0.00420	0.00652	0.00786	0.01226
A2	0.00262	0.00300	0.00299	0.00428	0.00429	0.00725	0.00868	0.01258

Max Leakage Power (uW)

V0P4	V0P7	V1	V2	V3	V4	V6	V8
0.00003117	0.00003508	0.00003841	0.00008071	0.00011144	0.00015576	0.00023265	0.00032251

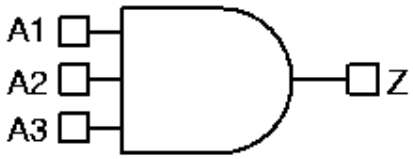
Delay Table (ns)

Description	V0P4	V0P7	V1	V2	V3	V4	V6	V8
A1→Z_FALL	0.08942	0.08920	0.08896	0.07657	0.08736	0.08346	0.08487	0.08143
A1→Z_RISE	0.09877	0.07678	0.07809	0.07753	0.09028	0.07967	0.08543	0.08242
A2→Z_FALL	0.09791	0.10206	0.10605	0.08515	0.09581	0.09104	0.09159	0.08892
A2→Z_RISE	0.10130	0.07973	0.08088	0.07964	0.09245	0.08235	0.08807	0.08448

AND3UHD

Cell Description

3-Input AND
Z=(A1&A2&A3)



Function Table

A1	A2	A3	Z
0	X	X	0
1	0	X	0
1	1	0	0
1	1	1	1

Cell Size

CellName	Height(um)	Width(um)
AND3UHDV0P7	3.360	3.920
AND3UHDV1	3.360	3.920
AND3UHDV2	3.360	4.480
AND3UHDV3	3.360	5.040
AND3UHDV4	3.360	8.960

Pin Power (uW/MHz)

Pin	V0P7	V1	V2	V3	V4
A1	0.00942	0.01053	0.01772	0.02573	0.03318
A2	0.01018	0.01130	0.01895	0.02724	0.03601
A3	0.01114	0.01226	0.02032	0.02854	0.03862

Pin Capacitance (pf)

Pin	V0P7	V1	V2	V3	V4
A1	0.00298	0.00304	0.00403	0.00402	0.00625
A2	0.00287	0.00295	0.00408	0.00413	0.00627
A3	0.00301	0.00308	0.00417	0.00421	0.00642

Max Leakage Power (uW)

V0P7	V1	V2	V3	V4
0.00004453	0.00004916	0.00009478	0.00012618	0.00017577

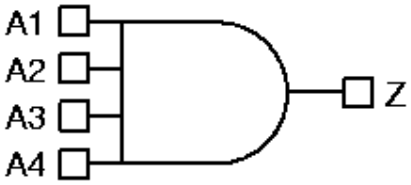
Delay Table (ns)

Description	V0P7	V1	V2	V3	V4
A1→Z_FALL	0.09618	0.09333	0.08523	0.09682	0.08938
A1→Z_RISE	0.10183	0.10302	0.10417	0.12255	0.11317
A2→Z_FALL	0.10590	0.10213	0.09396	0.10631	0.09941
A2→Z_RISE	0.10551	0.10679	0.10932	0.12889	0.12352
A3→Z_FALL	0.11707	0.11194	0.10189	0.11329	0.10765
A3→Z_RISE	0.11100	0.11214	0.11401	0.13255	0.12930

AND4UHD

Cell Description

4-Input AND
Z=(A1&A2&A3&A4)



Function Table

A1	A2	A3	A4	Z
0	X	X	X	0
1	0	X	X	0
1	1	0	X	0
1	1	1	0	0
1	1	1	1	1

Cell Size

CellName	Height(um)	Width(um)
AND4UHDV0P7	3.360	4.480
AND4UHDV1	3.360	4.480
AND4UHDV2	3.360	5.040
AND4UHDV3	3.360	6.160

Pin Power (uW/MHz)

Pin	V0P7	V1	V2	V3
A1	0.00983	0.01113	0.01835	0.02710
A2	0.01068	0.01197	0.01957	0.02846
A3	0.01157	0.01288	0.02095	0.02997
A4	0.01251	0.01383	0.02215	0.03128

Pin Capacitance (pf)

Pin	V0P7	V1	V2	V3
A1	0.00279	0.00293	0.00380	0.00374
A2	0.00285	0.00296	0.00392	0.00392
A3	0.00287	0.00296	0.00378	0.00377

A4	0.00291	0.00300	0.00393	0.00386

Max Leakage Power (uW)

V0P7	V1	V2	V3
0.00005188	0.00005697	0.00010348	0.00013310

Delay Table (ns)

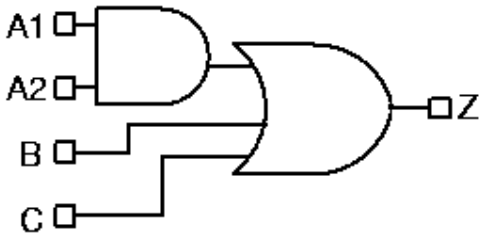
Description	V0P7	V1	V2	V3
A1→Z_FALL	0.09920	0.09711	0.09086	0.10585
A1→Z_RISE	0.11894	0.12269	0.12651	0.14995
A2→Z_FALL	0.11069	0.10735	0.10020	0.11562
A2→Z_RISE	0.12742	0.13095	0.13499	0.15856
A3→Z_FALL	0.12038	0.11619	0.10808	0.12387
A3→Z_RISE	0.13438	0.13805	0.14240	0.16597
A4→Z_FALL	0.12822	0.12387	0.11448	0.13061
A4→Z_RISE	0.13964	0.14329	0.14677	0.17026

AO112UHD

Cell Description

1-1-2 AO

Z=((A1&A2)|B|C)



Function Table

A1	A2	B	C	Z
0	X	0	0	0
0	X	0	1	1
0	X	1	X	1
1	0	0	0	0
1	0	0	1	1
1	0	1	X	1
1	1	X	X	1

Cell Size

CellName	Height(um)	Width(um)
AO112UHDV0P4	3.360	4.480
AO112UHDV0P7	3.360	4.480
AO112UHDV1	3.360	4.480
AO112UHDV2	3.360	5.040
AO112UHDV3	3.360	5.600

Pin Power (uW/MHz)

Pin	V0P4	V0P7	V1	V2	V3
A1	0.00772	0.00997	0.01110	0.02006	0.03121
A2	0.00826	0.01083	0.01202	0.02145	0.03298
B	0.01085	0.01316	0.01402	0.02477	0.03571
C	0.01000	0.01230	0.01322	0.02333	0.03419

Pin Capacitance (pf)

Pin	V0P4	V0P7	V1	V2	V3

A1	0.00239	0.00259	0.00253	0.00366	0.00384
A2	0.00243	0.00262	0.00261	0.00377	0.00400
B	0.00246	0.00271	0.00278	0.00397	0.00430
C	0.00244	0.00263	0.00289	0.00382	0.00407

Max Leakage Power (uW)

V0P4	V0P7	V1	V2	V3
0.00005957	0.00007042	0.00007340	0.00010536	0.00012818

Delay Table (ns)

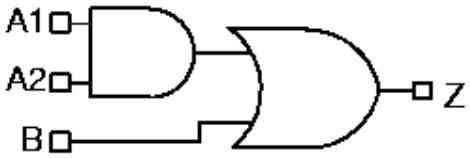
Description	V0P4	V0P7	V1	V2	V3
A1→Z_FALL	0.18154	0.19152	0.19023	0.17330	0.21190
A1→Z_RISE	0.10828	0.08962	0.09138	0.09257	0.10014
A2→Z_FALL	0.20010	0.21700	0.21452	0.19210	0.23129
A2→Z_RISE	0.10934	0.09096	0.09337	0.09447	0.10207
B→Z_FALL	0.25666	0.26824	0.25128	0.23126	0.26806
B→Z_RISE	0.10145	0.08148	0.08170	0.08397	0.08859
C→Z_FALL	0.24503	0.25645	0.24322	0.22176	0.25827
C→Z_RISE	0.09937	0.08024	0.08103	0.08208	0.08666

AO12UHD

Cell Description

1-2 AO

Z=((A1&A2)|B)



Function Table

A1	A2	B	Z
0	X	0	0
0	X	1	1
1	0	0	0
1	0	1	1
1	1	X	1

Cell Size

CellName	Height(um)	Width(um)
AO12UHDV0P4	3.360	3.360
AO12UHDV0P7	3.360	3.360
AO12UHDV1	3.360	3.360
AO12UHDV2	3.360	4.480
AO12UHDV3	3.360	5.040
AO12UHDV4	3.360	8.400

Pin Power (uW/MHz)

Pin	V0P4	V0P7	V1	V2	V3	V4
A1	0.00757	0.00900	0.00997	0.01722	0.02648	0.03491
A2	0.00832	0.00978	0.01073	0.01836	0.02783	0.03717
B	0.00979	0.01121	0.01236	0.02017	0.02920	0.04001

Pin Capacitance (pf)

Pin	V0P4	V0P7	V1	V2	V3	V4
A1	0.00277	0.00277	0.00291	0.00379	0.00410	0.00574
A2	0.00276	0.00277	0.00283	0.00376	0.00406	0.00631

B	0.00289	0.00289	0.00306	0.00411	0.00428	0.00615

Max Leakage Power (uW)

V0P4	V0P7	V1	V2	V3	V4
0.00004852	0.00005228	0.00005403	0.00008036	0.00011266	0.00014817

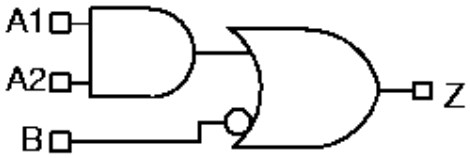
Delay Table (ns)

Description	V0P4	V0P7	V1	V2	V3	V4
A1→Z_FALL	0.13187	0.14086	0.13169	0.12524	0.15061	0.14735
A1→Z_RISE	0.09021	0.08542	0.08776	0.08595	0.09526	0.08591
A2→Z_FALL	0.14738	0.15580	0.14346	0.13572	0.16078	0.16156
A2→Z_RISE	0.09197	0.08710	0.08917	0.08731	0.09666	0.08840
B→Z_FALL	0.16004	0.16822	0.15738	0.14503	0.16684	0.17184
B→Z_RISE	0.08280	0.07738	0.07978	0.07680	0.08224	0.07665

AO21BUHD

Cell Description

AO21B
(A1&A2)|(!B)



Function Table

A1	A2	B	Z
0	0	0	1
1	0	0	1
0	1	0	1
1	1	0	1
0	0	1	0
1	0	1	0
0	1	1	0
1	1	1	1

Cell Size

CellName	Height(um)	Width(um)
AO21BUHDV0P4	3.360	3.360
AO21BUHDV0P7	3.360	3.920
AO21BUHDV1	3.360	3.920
AO21BUHDV2	3.360	5.600
AO21BUHDV3	3.360	6.720

Pin Power (uW/MHz)

Pin	V0P4	V0P7	V1	V2	V3
A1	0.00698	0.00971	0.01124	0.02030	0.02864
A2	0.00753	0.01047	0.01201	0.02133	0.02983
B	0.00234	0.00340	0.00401	0.00714	0.01077

Pin Capacitance (pf)

Pin	V0P4	V0P7	V1	V2	V3

A1	0.00237	0.00280	0.00288	0.00401	0.00421
A2	0.00258	0.00297	0.00313	0.00420	0.00441
B	0.00220	0.00317	0.00378	0.00683	0.01032

Max Leakage Power (uW)

V0P4	V0P7	V1	V2	V3
0.00003456	0.00004197	0.00004780	0.00008421	0.00011521

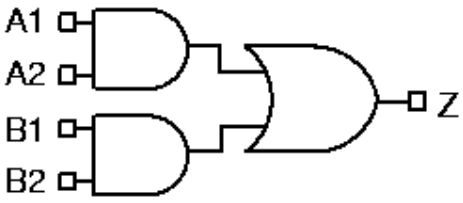
Delay Table (ns)

Description	V0P4	V0P7	V1	V2	V3
A1→Z_FALL	0.10366	0.10058	0.09628	0.09413	0.10305
A1→Z_RISE	0.11041	0.09453	0.09586	0.10220	0.10906
A2→Z_FALL	0.11368	0.11192	0.10652	0.10260	0.11188
A2→Z_RISE	0.11400	0.09753	0.09917	0.10465	0.11135
B→Z_FALL	0.04402	0.03572	0.03350	0.02844	0.02777
B→Z_RISE	0.05236	0.04152	0.03837	0.03531	0.03406

AO22UHD

Cell Description

2-2 AO provides the logical OR of two AND groups.
Z=((A1&A2)|(B1&B2))



Function Table

A1	A2	B1	B2	Z
0	X	0	X	0
0	X	1	0	0
0	X	1	1	1
1	0	0	X	0
1	0	1	0	0
1	0	1	1	1
1	1	X	X	1

Cell Size

CellName	Height(um)	Width(um)
AO22UHDV0P4	3.360	5.040
AO22UHDV0P7	3.360	5.040
AO22UHDV1	3.360	5.600
AO22UHDV2	3.360	6.160
AO22UHDV3	3.360	6.720
AO22UHDV4	3.360	10.080
AO22UHDV6	3.360	11.760

Pin Power (uW/MHz)

Pin	V0P4	V0P7	V1	V2	V3	V4	V6
A1	0.00999	0.01228	0.01322	0.02188	0.03072	0.04299	0.06036
A2	0.01047	0.01304	0.01401	0.02303	0.03224	0.04482	0.06337
B1	0.00704	0.00924	0.01039	0.01754	0.02610	0.03646	0.05165
B2	0.00753	0.01016	0.01119	0.01870	0.02746	0.03831	0.05462

Pin Capacitance (pf)

Pin	V0P4	V0P7	V1	V2	V3	V4	V6
A1	0.00251	0.00273	0.00286	0.00384	0.00402	0.00585	0.00770
A2	0.00234	0.00261	0.00279	0.00384	0.00407	0.00690	0.00851
B1	0.00273	0.00284	0.00301	0.00405	0.00425	0.00582	0.00761
B2	0.00262	0.00289	0.00302	0.00412	0.00430	0.00688	0.00848

Max Leakage Power (uW)

V0P4	V0P7	V1	V2	V3	V4	V6
0.00004496	0.00005442	0.00005740	0.00008258	0.00011403	0.00015568	0.00023474

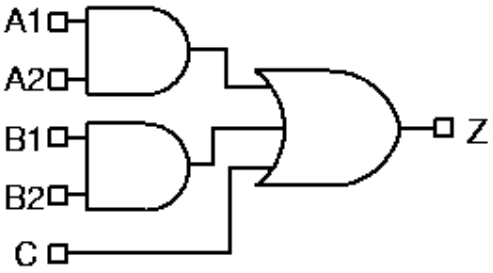
Delay Table (ns)

Description	V0P4	V0P7	V1	V2	V3	V4	V6
A1→Z_FALL	0.17291	0.18090	0.16458	0.15312	0.17163	0.18304	0.16852
A1→Z_RISE	0.12750	0.10356	0.10346	0.10661	0.11298	0.10690	0.10917
A2→Z_FALL	0.18030	0.19258	0.17599	0.16225	0.18232	0.18507	0.17982
A2→Z_RISE	0.12852	0.10513	0.10524	0.10854	0.11568	0.11003	0.11184
B1→Z_FALL	0.12892	0.13563	0.12944	0.12125	0.14089	0.14931	0.13875
B1→Z_RISE	0.10169	0.08557	0.08661	0.08700	0.09449	0.08979	0.09137
B2→Z_FALL	0.13817	0.15266	0.14209	0.13147	0.15102	0.15481	0.15080
B2→Z_RISE	0.10309	0.08898	0.08857	0.08902	0.09644	0.09315	0.09407

AO221UHD

Cell Description

2-2-1 AO
Z=((A1&A2)|(B1&B2)|C)



Function Table

A1	A2	B1	B2	C	Z
0	X	0	X	0	0
0	X	0	X	1	1
0	X	1	0	0	0
0	X	1	0	1	1
0	X	1	1	X	1
1	0	0	X	0	0
1	0	0	X	1	1
1	0	1	0	0	0
1	0	1	0	1	1
1	0	1	1	X	1
1	1	X	X	X	1

Cell Size

CellName	Height(um)	Width(um)
AO221UHDV0P4	3.360	5.600
AO221UHDV0P7	3.360	5.600
AO221UHDV1	3.360	5.600
AO221UHDV2	3.360	6.720
AO221UHDV3	3.360	7.280

Pin Power (uW/MHz)

Pin	V0P4	V0P7	V1	V2	V3
A1	0.01274	0.01524	0.01729	0.02692	0.03864
A2	0.01334	0.01629	0.01836	0.02833	0.04043
B1	0.01067	0.01318	0.01494	0.02330	0.03476
B2	0.01124	0.01418	0.01597	0.02467	0.03648

C	0.00860	0.01114	0.01263	0.01998	0.03087

Pin Capacitance (pf)

Pin	V0P4	V0P7	V1	V2	V3
A1	0.00246	0.00280	0.00294	0.00389	0.00409
A2	0.00250	0.00288	0.00302	0.00395	0.00412
B1	0.00243	0.00275	0.00290	0.00379	0.00394
B2	0.00243	0.00278	0.00294	0.00388	0.00400
C	0.00264	0.00289	0.00305	0.00397	0.00415

Max Leakage Power (uW)

V0P4	V0P7	V1	V2	V3
0.00006183	0.00007674	0.00008019	0.00010707	0.00012042

Delay Table (ns)

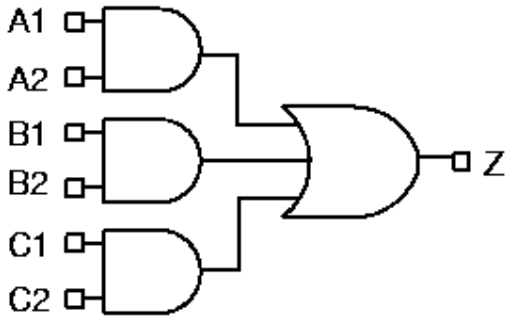
Description	V0P4	V0P7	V1	V2	V3
A1→Z_FALL	0.28059	0.29643	0.28072	0.23953	0.27865
A1→Z_RISE	0.14460	0.10673	0.11109	0.11649	0.12478
A2→Z_FALL	0.30051	0.32528	0.30612	0.25893	0.29866
A2→Z_RISE	0.14733	0.10940	0.11386	0.11898	0.12686
B1→Z_FALL	0.25041	0.26594	0.25068	0.21318	0.25195
B1→Z_RISE	0.13543	0.10283	0.10588	0.10788	0.11610
B2→Z_FALL	0.26868	0.29402	0.27554	0.23143	0.27125
B2→Z_RISE	0.13777	0.10540	0.10840	0.11028	0.11841
C→Z_FALL	0.18595	0.20166	0.18945	0.16436	0.20240
C→Z_RISE	0.09276	0.07372	0.07397	0.07296	0.07918

AO222UHD

Cell Description

2-2-2 AO

Z=((A1&A2)|(B1&B2)|(C1&C2))



Function Table

A1	A2	B1	B2	C1	C2	Z
0	X	0	X	0	X	0
0	X	0	X	1	0	0
0	X	0	X	1	1	1
0	X	1	0	0	X	0
0	X	1	0	1	0	0
0	X	1	0	1	1	1
0	X	1	1	X	X	1
1	0	0	X	0	X	0
1	0	0	X	1	0	0
1	0	0	X	1	1	1
1	0	1	0	0	X	0
1	0	1	0	1	0	0
1	0	1	0	1	1	1
1	0	1	1	X	X	1
1	1	X	X	X	X	1

Cell Size

CellName	Height(um)	Width(um)
AO222UHDV0P4	3.360	6.160
AO222UHDV0P7	3.360	6.160
AO222UHDV1	3.360	6.160
AO222UHDV2	3.360	7.280
AO222UHDV3	3.360	8.400

Pin Power (uW/MHz)

Pin	V0P4	V0P7	V1	V2	V3

A1	0.01407	0.01665	0.01885	0.03006	0.04113
A2	0.01465	0.01757	0.01977	0.03153	0.04283
B1	0.01179	0.01451	0.01630	0.02650	0.03718
B2	0.01234	0.01533	0.01717	0.02795	0.03889
C1	0.00875	0.01136	0.01285	0.02214	0.03233
C2	0.00932	0.01220	0.01374	0.02352	0.03395

Pin Capacitance (pf)

Pin	V0P4	V0P7	V1	V2	V3
A1	0.00255	0.00271	0.00292	0.00398	0.00409
A2	0.00244	0.00288	0.00287	0.00400	0.00409
B1	0.00234	0.00271	0.00275	0.00379	0.00386
B2	0.00237	0.00266	0.00281	0.00385	0.00397
C1	0.00247	0.00277	0.00286	0.00397	0.00412
C2	0.00251	0.00273	0.00289	0.00389	0.00399

Max Leakage Power (uW)

V0P4	V0P7	V1	V2	V3
0.00006106	0.00007565	0.00007464	0.00010552	0.00012102

Delay Table (ns)

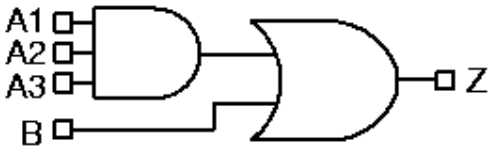
Description	V0P4	V0P7	V1	V2	V3
A1→Z_FALL	0.30203	0.31214	0.29504	0.26821	0.29306
A1→Z_RISE	0.15841	0.12122	0.12916	0.12203	0.13560
A2→Z_FALL	0.31946	0.33835	0.31612	0.28775	0.31234
A2→Z_RISE	0.15973	0.12418	0.13108	0.12417	0.13756
B1→Z_FALL	0.26960	0.28155	0.26505	0.24119	0.26627
B1→Z_RISE	0.14662	0.11651	0.12103	0.11373	0.12629
B2→Z_FALL	0.28237	0.30419	0.28084	0.26015	0.28442
B2→Z_RISE	0.14871	0.11745	0.12341	0.11575	0.12826
C1→Z_FALL	0.18422	0.19702	0.18489	0.18118	0.20644
C1→Z_RISE	0.11785	0.09768	0.09904	0.09534	0.10676
C2→Z_FALL	0.19929	0.21928	0.20234	0.19838	0.22274
C2→Z_RISE	0.12077	0.09886	0.10187	0.09667	0.10793

AO31UHD

Cell Description

3-1 AO

Z=((A1&A2&A3)|B)



Function Table

A1	A2	A3	B	Z
0	X	X	0	0
0	X	X	1	1
1	0	X	0	0
1	0	X	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	X	1

Cell Size

CellName	Height(um)	Width(um)
AO31UHDV0P4	3.360	4.480
AO31UHDV0P7	3.360	4.480
AO31UHDV1	3.360	4.480
AO31UHDV2	3.360	5.040

Pin Power (uW/MHz)

Pin	V0P4	V0P7	V1	V2
A1	0.00909	0.01092	0.01257	0.02066
A2	0.00958	0.01184	0.01349	0.02205
A3	0.01015	0.01267	0.01434	0.02334
B	0.00693	0.00892	0.01020	0.01681

Pin Capacitance (pf)

Pin	V0P4	V0P7	V1	V2
A1	0.00247	0.00267	0.00279	0.00375

A2	0.00241	0.00287	0.00300	0.00378
A3	0.00249	0.00279	0.00292	0.00396
B	0.00258	0.00286	0.00300	0.00371

Max Leakage Power (uW)

V0P4	V0P7	V1	V2
0.00004370	0.00005275	0.00005579	0.00008433

Delay Table (ns)

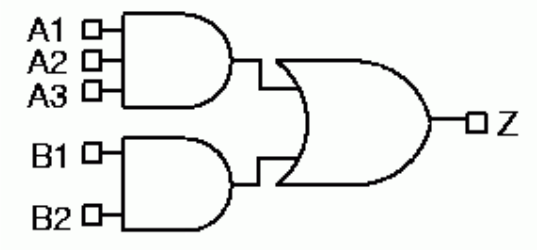
Description	V0P4	V0P7	V1	V2
A1→Z_FALL	0.16806	0.17019	0.16280	0.14955
A1→Z_RISE	0.14635	0.11451	0.11987	0.12269
A2→Z_FALL	0.17981	0.19084	0.18078	0.16428
A2→Z_RISE	0.14991	0.12118	0.12650	0.12881
A3→Z_FALL	0.19226	0.20668	0.19428	0.17695
A3→Z_RISE	0.15387	0.12413	0.12949	0.13276
B→Z_FALL	0.12390	0.13014	0.12373	0.11341
B→Z_RISE	0.08147	0.06787	0.06832	0.07800

AO32UHD

Cell Description

3-2 AO

Z=((A1&A2&A3)|(B1&B2))



Function Table

A1	A2	A3	B1	B2	Z
0	X	X	0	X	0
0	X	X	1	0	0
0	X	X	1	1	1
1	0	X	0	X	0
1	0	X	1	0	0
1	0	X	1	1	1
1	1	0	0	X	0
1	1	0	1	0	0
1	1	0	1	1	1
1	1	1	X	X	1

Cell Size

CellName	Height(um)	Width(um)
AO32UHDV0P7	3.360	5.600
AO32UHDV1	3.360	5.600
AO32UHDV2	3.360	6.160
AO32UHDV3	3.360	6.720
AO32UHDV4	3.360	13.440

Pin Power (uW/MHz)

Pin	V0P7	V1	V2	V3	V4
A1	0.01291	0.01473	0.02359	0.03347	0.04738
A2	0.01382	0.01574	0.02483	0.03498	0.05018
A3	0.01476	0.01655	0.02622	0.03667	0.05331
B1	0.01004	0.01142	0.01822	0.02715	0.03722
B2	0.01085	0.01227	0.01946	0.02862	0.04018

Pin Capacitance (pf)

Pin	V0P7	V1	V2	V3	V4
A1	0.00277	0.00289	0.00388	0.00411	0.00605
A2	0.00286	0.00301	0.00392	0.00414	0.00596
A3	0.00284	0.00296	0.00398	0.00420	0.00604
B1	0.00300	0.00312	0.00403	0.00422	0.00700
B2	0.00293	0.00306	0.00398	0.00419	0.00689

Max Leakage Power (uW)

V0P7	V1	V2	V3	V4
0.00005566	0.00005881	0.00008573	0.00011790	0.00016228

Delay Table (ns)

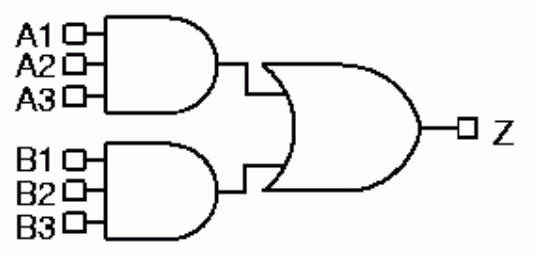
Description	V0P7	V1	V2	V3	V4
A1→Z_FALL	0.19203	0.18277	0.16327	0.18391	0.17344
A1→Z_RISE	0.13259	0.13893	0.14004	0.14904	0.15068
A2→Z_FALL	0.21085	0.20035	0.17587	0.19698	0.18962
A2→Z_RISE	0.13939	0.14648	0.14578	0.15473	0.15844
A3→Z_FALL	0.22726	0.21209	0.18864	0.21059	0.20520
A3→Z_RISE	0.14372	0.14947	0.15059	0.15935	0.16486
B1→Z_FALL	0.14644	0.13848	0.12236	0.14207	0.12762
B1→Z_RISE	0.09260	0.09410	0.09074	0.09882	0.09621
B2→Z_FALL	0.16000	0.15052	0.13232	0.15214	0.14193
B2→Z_RISE	0.09474	0.09650	0.09336	0.10153	0.10142

AO33UHD

Cell Description

3-3 AO

Z=((A1&A2&A3)|(B1&B2&B3))



Function Table

A1	A2	A3	B1	B2	B3	Z
0	X	X	0	X	X	0
0	X	X	1	0	X	0
0	X	X	1	1	0	0
0	X	X	1	1	1	1
1	0	X	0	X	X	0
1	0	X	1	0	X	0
1	0	X	1	1	0	0
1	0	X	1	1	1	1
1	1	0	0	X	X	0
1	1	0	1	0	X	0
1	1	0	1	1	0	0
1	1	0	1	1	1	1
1	1	1	X	X	X	1

Cell Size

CellName	Height(um)	Width(um)
AO33UHDV0P7	3.360	6.160
AO33UHDV1	3.360	6.160
AO33UHDV2	3.360	6.720
AO33UHDV3	3.360	7.280
AO33UHDV4	3.360	15.120

Pin Power (uW/MHz)

Pin	V0P7	V1	V2	V3	V4
A1	0.01471	0.01667	0.02631	0.03646	0.05141
A2	0.01563	0.01763	0.02770	0.03791	0.05419

A3	0.01644	0.01861	0.02906	0.03954	0.05737
B1	0.01148	0.01301	0.02056	0.03004	0.04117
B2	0.01242	0.01391	0.02199	0.03172	0.04437
B3	0.01321	0.01475	0.02321	0.03316	0.04728

Pin Capacitance (pf)

Pin	V0P7	V1	V2	V3	V4
A1	0.00275	0.00291	0.00386	0.00410	0.00610
A2	0.00288	0.00298	0.00390	0.00414	0.00597
A3	0.00286	0.00310	0.00394	0.00419	0.00612
B1	0.00286	0.00299	0.00387	0.00406	0.00637
B2	0.00303	0.00315	0.00402	0.00422	0.00633
B3	0.00286	0.00295	0.00394	0.00413	0.00628

Max Leakage Power (uW)

V0P7	V1	V2	V3	V4
0.00005720	0.00006028	0.00009486	0.00012824	0.00017376

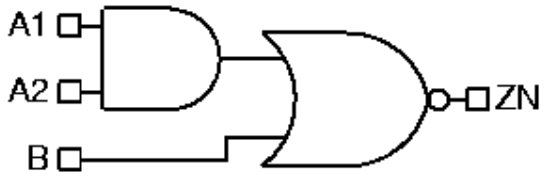
Delay Table (ns)

Description	V0P7	V1	V2	V3	V4
A1→Z_FALL	0.20641	0.19585	0.17320	0.19247	0.18924
A1→Z_RISE	0.14985	0.15722	0.15727	0.16565	0.16167
A2→Z_FALL	0.22391	0.21149	0.18596	0.20405	0.20540
A2→Z_RISE	0.15696	0.16467	0.16420	0.17103	0.16941
A3→Z_FALL	0.23697	0.22495	0.19733	0.21631	0.22133
A3→Z_RISE	0.16041	0.16943	0.16864	0.17548	0.17600
B1→Z_FALL	0.16256	0.15335	0.13373	0.15279	0.14794
B1→Z_RISE	0.12131	0.12442	0.12002	0.13006	0.12412
B2→Z_FALL	0.18039	0.16819	0.14730	0.16639	0.16610
B2→Z_RISE	0.12894	0.13147	0.12795	0.13760	0.13399
B3→Z_FALL	0.19128	0.17815	0.15559	0.17494	0.17905
B3→Z_RISE	0.13181	0.13489	0.13171	0.14127	0.13970

AOI21UHD

Cell Description

2-1 AOI
ZN=(!((A1&A2)|B))



Function Table

A1	A2	B	ZN
0	X	0	1
0	X	1	0
1	0	0	1
1	0	1	0
1	1	X	0

Cell Size

CellName	Height(um)	Width(um)
AOI21UHDV0P4	3.360	2.800
AOI21UHDV0P7	3.360	2.800
AOI21UHDV1	3.360	3.360
AOI21UHDV2	3.360	5.040
AOI21UHDV3	3.360	7.280
AOI21UHDV4	3.360	9.520
AOI21UHDV6	3.360	14.000

Pin Power (uW/MHz)

Pin	V0P4	V0P7	V1	V2	V3	V4	V6
A1	0.00402	0.00494	0.00761	0.01274	0.01967	0.02497	0.03722
A2	0.00446	0.00576	0.00874	0.01523	0.02315	0.03001	0.04479
B	0.00243	0.00320	0.00479	0.00716	0.01191	0.01442	0.02174

Pin Capacitance (pf)

Pin	V0P4	V0P7	V1	V2	V3	V4	V6
A1	0.00227	0.00303	0.00380	0.00713	0.01116	0.01483	0.02229

A2	0.00222	0.00273	0.00405	0.00811	0.01166	0.01596	0.02387
B	0.00219	0.00297	0.00375	0.00717	0.01056	0.01400	0.02075

Max Leakage Power (uW)

V0P4	V0P7	V1	V2	V3	V4	V6
0.00003350	0.00004474	0.00005171	0.00011434	0.00017132	0.00024038	0.00036726

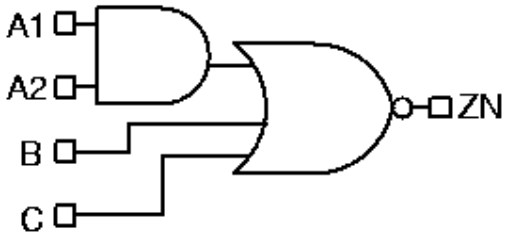
Delay Table (ns)

Description	V0P4	V0P7	V1	V2	V3	V4	V6
A1→ZN_FALL	0.05435	0.03938	0.04381	0.03532	0.03667	0.03379	0.03336
A1→ZN_RISE	0.10429	0.08978	0.08619	0.07148	0.07193	0.06843	0.06763
A2→ZN_FALL	0.05493	0.04032	0.04567	0.03756	0.03828	0.03578	0.03523
A2→ZN_RISE	0.11368	0.12469	0.10061	0.08601	0.08733	0.08422	0.08376
B→ZN_FALL	0.03324	0.02548	0.02701	0.02095	0.02213	0.01992	0.01958
B→ZN_RISE	0.07497	0.07190	0.06221	0.04849	0.05091	0.04720	0.04684

AOI211UHD

Cell Description

2-1-1 AOI
ZN=(!((A1&A2)|B|C))



Function Table

A1	A2	B	C	ZN
0	X	0	0	1
0	X	0	1	0
0	X	1	X	0
1	0	0	0	1
1	0	0	1	0
1	0	1	X	0
1	1	X	X	0

Cell Size

CellName	Height(um)	Width(um)
AOI211UHDV0P4	3.360	3.920
AOI211UHDV0P7	3.360	3.920
AOI211UHDV1	3.360	3.360
AOI211UHDV2	3.360	6.720
AOI211UHDV3	3.360	9.520

Pin Power (uW/MHz)

Pin	V0P4	V0P7	V1	V2	V3
A1	0.00564	0.00744	0.00944	0.01791	0.02701
A2	0.00608	0.00818	0.01052	0.02039	0.03037
B	0.00411	0.00539	0.00680	0.01272	0.01967
C	0.00331	0.00417	0.00520	0.00899	0.01439

Pin Capacitance (pf)

Pin	V0P4	V0P7	V1	V2	V3

A1	0.00245	0.00329	0.00381	0.00719	0.01095
A2	0.00228	0.00309	0.00391	0.00821	0.01168
B	0.00230	0.00315	0.00391	0.00816	0.01162
C	0.00230	0.00315	0.00392	0.00716	0.01100

Max Leakage Power (uW)

V0P4	V0P7	V1	V2	V3
0.00005080	0.00006508	0.00008234	0.00017636	0.00026911

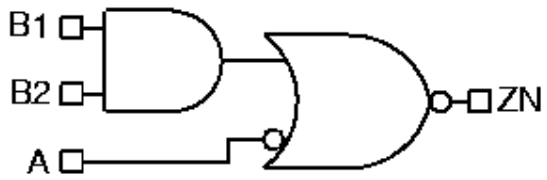
Delay Table (ns)

Description	V0P4	V0P7	V1	V2	V3
A1→ZN_FALL	0.06162	0.04965	0.04412	0.03775	0.03825
A1→ZN_RISE	0.17628	0.14737	0.13622	0.12421	0.12446
A2→ZN_FALL	0.06224	0.05064	0.04559	0.03979	0.04015
A2→ZN_RISE	0.18951	0.16323	0.15421	0.14587	0.14560
B→ZN_FALL	0.04168	0.03482	0.03163	0.02846	0.02813
B→ZN_RISE	0.14888	0.12386	0.11411	0.10445	0.10469
C→ZN_FALL	0.03861	0.03191	0.02872	0.02377	0.02428
C→ZN_RISE	0.12670	0.10146	0.09202	0.07680	0.07905

AOI21BUHD

Cell Description

AOI21B
!((B1&B2)|(!A))



Function Table

B1	B2	A	ZN
0	0	0	0
1	0	0	0
0	1	0	0
1	1	0	0
0	0	1	1
1	0	1	1
0	1	1	1
1	1	1	0

Cell Size

CellName	Height(um)	Width(um)
AOI21BUHDV0P4	3.360	3.920
AOI21BUHDV0P7	3.360	3.920
AOI21BUHDV1	3.360	4.480
AOI21BUHDV2	3.360	6.720

Pin Power (uW/MHz)

Pin	V0P4	V0P7	V1	V2
A	0.00660	0.00824	0.01005	0.01669
B1	0.00450	0.00548	0.00685	0.01264
B2	0.00491	0.00614	0.00813	0.01577

Pin Capacitance (pf)

Pin	V0P4	V0P7	V1	V2
A	0.00275	0.00302	0.00332	0.00427

B1	0.00244	0.00299	0.00392	0.00711
B2	0.00232	0.00289	0.00384	0.00811

Max Leakage Power (uW)

V0P4	V0P7	V1	V2
0.00004346	0.00005209	0.00006669	0.00013337

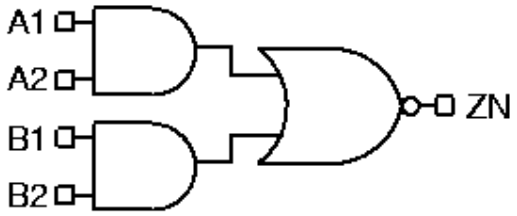
Delay Table (ns)

Description	V0P4	V0P7	V1	V2
A→ZN_FALL	0.08427	0.08104	0.08126	0.07361
A→ZN_RISE	0.10337	0.08908	0.08828	0.08344
B1→ZN_FALL	0.05800	0.05040	0.04033	0.03472
B1→ZN_RISE	0.10867	0.09292	0.08122	0.07559
B2→ZN_FALL	0.05747	0.05081	0.04270	0.03901
B2→ZN_RISE	0.11538	0.10128	0.09521	0.09134

AOI22UHD

Cell Description

2-2 AOI
ZN=(!((A1&A2)|(B1&B2)))



Function Table

A1	A2	B1	B2	ZN
0	X	0	X	1
0	X	1	0	1
0	X	1	1	0
1	0	0	X	1
1	0	1	0	1
1	0	1	1	0
1	1	X	X	0

Cell Size

CellName	Height(um)	Width(um)
AOI22UHDV0P4	3.360	3.360
AOI22UHDV0P7	3.360	3.360
AOI22UHDV1	3.360	3.920
AOI22UHDV2	3.360	6.720
AOI22UHDV3	3.360	9.520
AOI22UHDV4	3.360	12.320
AOI22UHDV6	3.360	18.480

Pin Power (uW/MHz)

Pin	V0P4	V0P7	V1	V2	V3	V4	V6
A1	0.00599	0.00745	0.00909	0.01796	0.02626	0.03530	0.05260
A2	0.00644	0.00831	0.01035	0.02039	0.02961	0.03983	0.05927
B1	0.00307	0.00386	0.00485	0.01014	0.01472	0.02008	0.03016
B2	0.00354	0.00470	0.00589	0.01239	0.01800	0.02453	0.03683

Pin Capacitance (pf)

Pin	V0P4	V0P7	V1	V2	V3	V4	V6
A1	0.00227	0.00307	0.00379	0.00716	0.01124	0.01464	0.02230
A2	0.00223	0.00305	0.00386	0.00815	0.01154	0.01598	0.02388
B1	0.00228	0.00304	0.00370	0.00701	0.01085	0.01428	0.02155
B2	0.00232	0.00310	0.00377	0.00787	0.01124	0.01567	0.02328

Max Leakage Power (uW)

V0P4	V0P7	V1	V2	V3	V4	V6
0.00003601	0.00004778	0.00005709	0.00012010	0.00018321	0.00024732	0.00037477

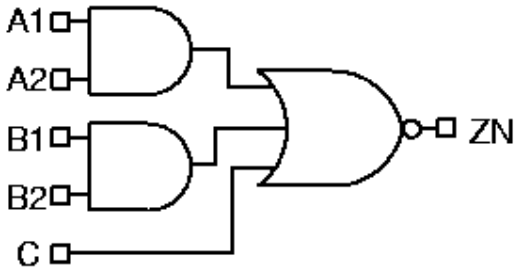
Delay Table (ns)

Description	V0P4	V0P7	V1	V2	V3	V4	V6
A1→ZN_FALL	0.06815	0.04771	0.04708	0.04470	0.04291	0.04282	0.04228
A1→ZN_RISE	0.12627	0.11440	0.09361	0.08932	0.08672	0.08661	0.08595
A2→ZN_FALL	0.06873	0.04910	0.04977	0.04715	0.04477	0.04502	0.04441
A2→ZN_RISE	0.13275	0.12577	0.10600	0.10226	0.09915	0.09976	0.09896
B1→ZN_FALL	0.04891	0.03634	0.03510	0.03359	0.03226	0.03231	0.03199
B1→ZN_RISE	0.08138	0.07361	0.06218	0.06008	0.05765	0.05804	0.05774
B2→ZN_FALL	0.05060	0.03810	0.03684	0.03596	0.03412	0.03446	0.03406
B2→ZN_RISE	0.09044	0.08697	0.07329	0.07308	0.07101	0.07182	0.07161

AOI221UHD

Cell Description

2-2-1 AOI
ZN=(!((A1&A2)|(B1&B2)|C))



Function Table

A1	A2	B1	B2	C	ZN
0	X	0	X	0	1
0	X	0	X	1	0
0	X	1	0	0	1
0	X	1	0	1	0
0	X	1	1	X	0
1	0	0	X	0	1
1	0	0	X	1	0
1	0	1	0	0	1
1	0	1	0	1	0
1	0	1	1	X	0
1	1	X	X	X	0

Cell Size

CellName	Height(um)	Width(um)
AOI221UHDV0P4	3.360	5.040
AOI221UHDV0P7	3.360	5.040
AOI221UHDV1	3.360	5.040
AOI221UHDV2	3.360	8.960
AOI221UHDV3	3.360	12.320
AOI221UHDV4	3.360	15.680

Pin Power (uW/MHz)

Pin	V0P4	V0P7	V1	V2	V3	V4
A1	0.00824	0.00990	0.01250	0.02289	0.03415	0.04519
A2	0.00868	0.01077	0.01371	0.02529	0.03750	0.04977
B1	0.00555	0.00658	0.00854	0.01582	0.02313	0.03072

B2	0.00605	0.00749	0.00967	0.01813	0.02651	0.03562
C	0.00381	0.00469	0.00578	0.01017	0.01550	0.02012

Pin Capacitance (pf)

Pin	V0P4	V0P7	V1	V2	V3	V4
A1	0.00222	0.00302	0.00383	0.00730	0.01143	0.01483
A2	0.00224	0.00305	0.00388	0.00809	0.01158	0.01609
B1	0.00237	0.00302	0.00374	0.00710	0.01111	0.01458
B2	0.00231	0.00306	0.00385	0.00787	0.01119	0.01571
C	0.00234	0.00308	0.00376	0.00708	0.01058	0.01392

Max Leakage Power (uW)

V0P4	V0P7	V1	V2	V3	V4
0.00005260	0.00007128	0.00008568	0.00017866	0.00027318	0.00036805

Delay Table (ns)

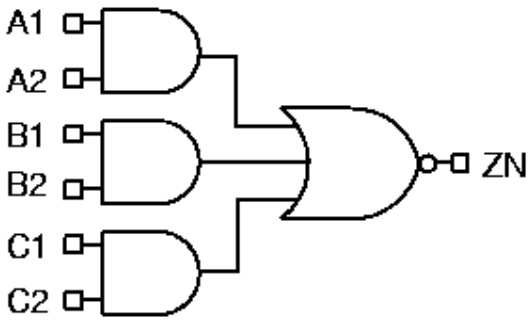
Description	V0P4	V0P7	V1	V2	V3	V4
A1→ZN_FALL	0.07048	0.04732	0.04812	0.04168	0.04079	0.03980
A1→ZN_RISE	0.22137	0.19471	0.16290	0.14649	0.14402	0.14162
A2→ZN_FALL	0.07145	0.04888	0.05042	0.04346	0.04259	0.04181
A2→ZN_RISE	0.23199	0.21287	0.18143	0.16523	0.16399	0.16249
B1→ZN_FALL	0.06644	0.04597	0.04597	0.04054	0.03964	0.03893
B1→ZN_RISE	0.17864	0.15540	0.13241	0.11958	0.11539	0.11385
B2→ZN_FALL	0.06866	0.04802	0.04809	0.04257	0.04118	0.04110
B2→ZN_RISE	0.19332	0.17571	0.15076	0.13955	0.13604	0.13581
C→ZN_FALL	0.04024	0.03005	0.02891	0.02466	0.02445	0.02349
C→ZN_RISE	0.11888	0.10818	0.08772	0.07497	0.07483	0.07153

AOI222UHD

Cell Description

2-2-2 AOI

ZN=(!((A1&A2)|(B1&B2)|(C1&C2)))



Function Table

A1	A2	B1	B2	C1	C2	ZN
0	X	0	X	0	X	1
0	X	0	X	1	0	1
0	X	0	X	1	1	0
0	X	1	0	0	X	1
0	X	1	0	1	0	1
0	X	1	0	1	1	0
0	X	1	1	X	X	0
1	0	0	X	0	X	1
1	0	0	X	1	0	1
1	0	0	X	1	1	0
1	0	1	0	0	X	1
1	0	1	0	1	0	1
1	0	1	0	1	1	0
1	0	1	1	X	X	0
1	1	X	X	X	X	0

Cell Size

CellName	Height(um)	Width(um)
AOI222UHDV0P4	3.360	5.600
AOI222UHDV0P7	3.360	5.600
AOI222UHDV1	3.360	6.160
AOI222UHDV2	3.360	10.640
AOI222UHDV3	3.360	15.120

Pin Power (uW/MHz)

Pin	V0P4	V0P7	V1	V2	V3

A1	0.00412	0.00464	0.00710	0.01287	0.01956
A2	0.00455	0.00536	0.00807	0.01510	0.02280
B1	0.00706	0.00753	0.01134	0.02094	0.03153
B2	0.00750	0.00824	0.01243	0.02339	0.03489
C1	0.00984	0.00981	0.01475	0.02849	0.04241
C2	0.01021	0.01053	0.01587	0.03077	0.04564

Pin Capacitance (pf)

Pin	V0P4	V0P7	V1	V2	V3
A1	0.00230	0.00246	0.00378	0.00699	0.01086
A2	0.00235	0.00265	0.00368	0.00774	0.01127
B1	0.00235	0.00254	0.00374	0.00715	0.01102
B2	0.00229	0.00255	0.00399	0.00811	0.01142
C1	0.00238	0.00297	0.00376	0.00721	0.01119
C2	0.00229	0.00294	0.00404	0.00801	0.01165

Max Leakage Power (uW)

V0P4	V0P7	V1	V2	V3
0.00005438	0.00006600	0.00008235	0.00018346	0.00026581

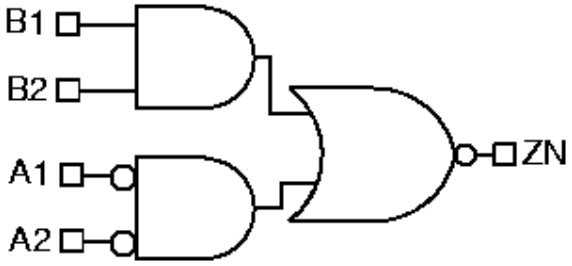
Delay Table (ns)

Description	V0P4	V0P7	V1	V2	V3
A1→ZN_FALL	0.05676	0.04253	0.04236	0.03729	0.03700
A1→ZN_RISE	0.12004	0.13316	0.10075	0.08756	0.08812
A2→ZN_FALL	0.05762	0.04425	0.04359	0.03967	0.03889
A2→ZN_RISE	0.13493	0.15789	0.11555	0.10606	0.10804
B1→ZN_FALL	0.07744	0.05346	0.05609	0.04970	0.04927
B1→ZN_RISE	0.20160	0.20633	0.16106	0.14443	0.14551
B2→ZN_FALL	0.07837	0.05471	0.05811	0.05250	0.05113
B2→ZN_RISE	0.21795	0.23050	0.17696	0.16401	0.16563
C1→ZN_FALL	0.08355	0.05479	0.05954	0.05230	0.05167
C1→ZN_RISE	0.24522	0.22716	0.18494	0.17290	0.17430
C2→ZN_FALL	0.08385	0.05620	0.06163	0.05475	0.05353
C2→ZN_RISE	0.25652	0.24870	0.20247	0.19015	0.19123

AOI22BBUHD

Cell Description

AOI22BB
!((!A1&!A2)|(B1&B2))



Function Table

A1	A2	B1	B2	ZN
0	0	0	0	0
1	0	0	0	1
0	1	0	0	1
1	1	0	0	1
0	0	1	0	0
1	0	1	0	1
0	1	1	0	1
1	1	1	0	1
0	0	0	1	0
1	0	0	1	1
0	1	0	1	1
1	1	0	1	1
0	0	1	1	0
1	0	1	1	0
0	1	1	1	0
1	1	1	1	0

Cell Size

CellName	Height(um)	Width(um)
AOI22BBUHDV0P4	3.360	4.480
AOI22BBUHDV0P7	3.360	4.480
AOI22BBUHDV1	3.360	4.480
AOI22BBUHDV2	3.360	7.840

Pin Power (uW/MHz)

Pin	V0P4	V0P7	V1	V2

A1	0.00944	0.01206	0.01396	0.02588
A2	0.01021	0.01286	0.01487	0.02729
B1	0.00325	0.00405	0.00452	0.00939
B2	0.00372	0.00490	0.00559	0.01258

Pin Capacitance (pf)

Pin	V0P4	V0P7	V1	V2
A1	0.00291	0.00309	0.00324	0.00419
A2	0.00271	0.00302	0.00317	0.00405
B1	0.00240	0.00319	0.00370	0.00678
B2	0.00230	0.00323	0.00374	0.00685

Max Leakage Power (uW)

V0P4	V0P7	V1	V2
0.00004335	0.00005510	0.00006380	0.00012413

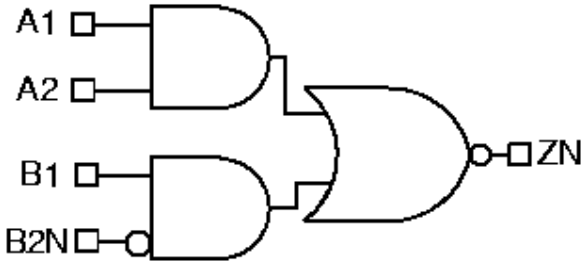
Delay Table (ns)

Description	V0P4	V0P7	V1	V2
A1→ZN_FALL	0.15272	0.15157	0.14526	0.14046
A1→ZN_RISE	0.14871	0.12250	0.11795	0.12027
A2→ZN_FALL	0.16238	0.16238	0.15583	0.15058
A2→ZN_RISE	0.15232	0.12520	0.12115	0.12420
B1→ZN_FALL	0.05252	0.03918	0.03569	0.03305
B1→ZN_RISE	0.09276	0.07142	0.06268	0.06085
B2→ZN_FALL	0.05389	0.04105	0.03741	0.03791
B2→ZN_RISE	0.10303	0.08428	0.07529	0.08059

AOI22XBUHD

Cell Description

AOI22XB
Function ZN= (!((A1&A2)|((!B2N)&B1)))



Function Table

A1	A2	B2N	B1	ZN
0	0	0	0	1
1	0	0	0	1
0	1	0	0	1
1	1	0	0	0
0	0	1	0	1
1	0	1	0	1
0	1	1	0	1
1	1	1	0	0
0	0	0	1	0
1	0	0	1	0
0	1	0	1	0
1	1	0	1	0
0	0	1	1	1
1	0	1	1	1
0	1	1	1	1
1	1	1	1	0

Cell Size

CellName	Height(um)	Width(um)
AOI22XBUHDV0P4	3.360	5.040
AOI22XBUHDV0P7	3.360	5.040
AOI22XBUHDV1	3.360	5.600
AOI22XBUHDV2	3.360	8.400
AOI22XBUHDV4	3.360	14.560

Pin Power (uW/MHz)

Pin	V0P4	V0P7	V1	V2	V4
A1	0.00625	0.00738	0.00903	0.01806	0.03629
A2	0.00671	0.00826	0.01024	0.02065	0.04085
B1	0.00334	0.00386	0.00483	0.00983	0.02088
B2N	0.00742	0.00979	0.01118	0.02153	0.04243

Pin Capacitance (pf)

Pin	V0P4	V0P7	V1	V2	V4
A1	0.00236	0.00297	0.00380	0.00721	0.01571
A2	0.00234	0.00299	0.00388	0.00818	0.01581
B1	0.00223	0.00301	0.00381	0.00705	0.01540
B2N	0.00275	0.00359	0.00261	0.00365	0.00687

Max Leakage Power (uW)

V0P4	V0P7	V1	V2	V4
0.00005292	0.00007160	0.00007421	0.00013861	0.00028577

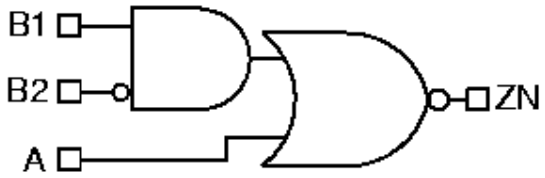
Delay Table (ns)

Description	V0P4	V0P7	V1	V2	V4
A1→ZN_FALL	0.07192	0.04740	0.04687	0.04409	0.04402
A1→ZN_RISE	0.13613	0.11362	0.09390	0.09017	0.08986
A2→ZN_FALL	0.07287	0.04905	0.04936	0.04713	0.04540
A2→ZN_RISE	0.14335	0.12532	0.10596	0.10414	0.10451
B1→ZN_FALL	0.05051	0.03610	0.03504	0.03264	0.03312
B1→ZN_RISE	0.08737	0.07366	0.06213	0.05805	0.05970
B2N→ZN_FALL	0.09953	0.08358	0.10594	0.09615	0.09300
B2N→ZN_RISE	0.12351	0.10997	0.11089	0.10797	0.10681

AOI2XB1UHD

Cell Description

AOI2XB1
!((B1&!B2)|A)



Function Table

B1	B2	A	ZN
0	0	0	1
1	0	0	0
0	1	0	1
1	1	0	1
0	0	1	0
1	0	1	0
0	1	1	0
1	1	1	0

Cell Size

CellName	Height(um)	Width(um)
AOI2XB1UHDV0P4	3.360	4.480
AOI2XB1UHDV0P7	3.360	4.480
AOI2XB1UHDV1	3.360	4.480
AOI2XB1UHDV2	3.360	6.720
AOI2XB1UHDV4	3.360	11.760

Pin Power (uW/MHz)

Pin	V0P4	V0P7	V1	V2	V4
A	0.00252	0.00314	0.00413	0.00709	0.01511
B1	0.00394	0.00521	0.00690	0.01260	0.02562
B2	0.00766	0.01004	0.01289	0.02445	0.04711

Pin Capacitance (pf)

Pin	V0P4	V0P7	V1	V2	V4

A	0.00213	0.00298	0.00384	0.00706	0.01406
B1	0.00212	0.00296	0.00378	0.00711	0.01555
B2	0.00218	0.00204	0.00235	0.00363	0.00687

Max Leakage Power (uW)

V0P4	V0P7	V1	V2	V4
0.00004995	0.00005625	0.00006789	0.00013327	0.00028078

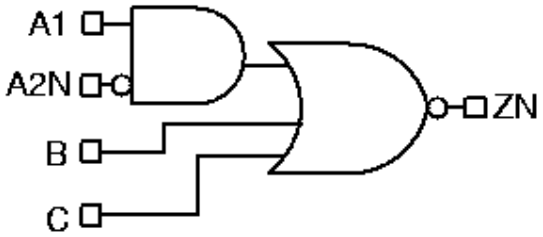
Delay Table (ns)

Description	V0P4	V0P7	V1	V2	V4
A→ZN_FALL	0.03293	0.02739	0.02515	0.02072	0.02049
A→ZN_RISE	0.08455	0.06379	0.05687	0.04796	0.04864
B1→ZN_FALL	0.05174	0.04357	0.04052	0.03493	0.03475
B1→ZN_RISE	0.11601	0.08935	0.08037	0.07109	0.07033
B2→ZN_FALL	0.12415	0.11975	0.10854	0.10035	0.09505
B2→ZN_RISE	0.15748	0.13530	0.12894	0.12406	0.12008

AOI2XB11UHD

Cell Description

AOI2XB11
Function ZN= (!((A1&!A2N)|B|C))



Function Table

A1	A2N	B	C	ZN
0	0	0	0	1
1	0	0	0	0
0	1	0	0	1
1	1	0	0	1
0	0	1	0	0
1	0	1	0	0
0	1	1	0	0
1	1	1	0	0
0	0	0	1	0
1	0	0	1	0
0	1	0	1	0
1	1	0	1	0
0	0	1	1	0
1	0	1	1	0
0	1	1	1	0
1	1	1	1	0

Cell Size

CellName	Height(um)	Width(um)
AOI2XB11UHDV0P4	3.360	5.040
AOI2XB11UHDV0P7	3.360	5.040
AOI2XB11UHDV1	3.360	5.040
AOI2XB11UHDV2	3.360	7.840

Pin Power (uW/MHz)

Pin	V0P4	V0P7	V1	V2

A1	0.00597	0.00795	0.01015	0.02032
A2N	0.00955	0.01168	0.01435	0.02683
B	0.00405	0.00527	0.00648	0.01272
C	0.00324	0.00415	0.00483	0.00899

Pin Capacitance (pf)

Pin	V0P4	V0P7	V1	V2
A1	0.00226	0.00308	0.00396	0.00822
A2N	0.00265	0.00252	0.00250	0.00380
B	0.00230	0.00313	0.00365	0.00814
C	0.00220	0.00300	0.00349	0.00708

Max Leakage Power (uW)

V0P4	V0P7	V1	V2
0.00006396	0.00008185	0.00008302	0.00019026

Delay Table (ns)

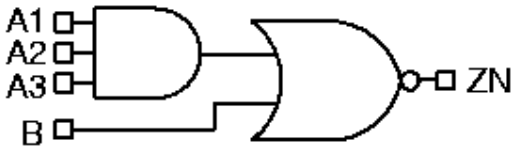
Description	V0P4	V0P7	V1	V2
A1→ZN_FALL	0.06161	0.04576	0.04560	0.04079
A1→ZN_RISE	0.19232	0.17967	0.14898	0.14404
A2N→ZN_FALL	0.11449	0.10882	0.11654	0.10082
A2N→ZN_RISE	0.21163	0.19439	0.17046	0.16063
B→ZN_FALL	0.04124	0.03180	0.03736	0.02834
B→ZN_RISE	0.15139	0.13610	0.10973	0.10389
C→ZN_FALL	0.03768	0.02916	0.03296	0.02369
C→ZN_RISE	0.12690	0.11226	0.08659	0.07623

AOI31UHD

Cell Description

3-1 AOI

ZN=(!((A1&A2&A3)|B))



Function Table

A1	A2	A3	B	ZN
0	X	X	0	1
0	X	X	1	0
1	0	X	0	1
1	0	X	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	X	0

Cell Size

CellName	Height(um)	Width(um)
AOI31UHDV0P4	3.360	3.360
AOI31UHDV0P7	3.360	3.360
AOI31UHDV1	3.360	3.920
AOI31UHDV2	3.360	6.720
AOI31UHDV3	3.360	9.520

Pin Power (uW/MHz)

Pin	V0P4	V0P7	V1	V2	V3
A1	0.00470	0.00575	0.00741	0.01402	0.02063
A2	0.00513	0.00662	0.00855	0.01638	0.02568
A3	0.00559	0.00759	0.00972	0.01897	0.03021
B	0.00269	0.00349	0.00447	0.00754	0.01310

Pin Capacitance (pf)

Pin	V0P4	V0P7	V1	V2	V3

A1	0.00230	0.00301	0.00383	0.00633	0.01033
A2	0.00234	0.00299	0.00381	0.00777	0.01066
A3	0.00224	0.00296	0.00382	0.00866	0.01120
B	0.00230	0.00306	0.00384	0.00725	0.01103

Max Leakage Power (uW)

V0P4	V0P7	V1	V2	V3
0.00003561	0.00004684	0.00005590	0.00010451	0.00020212

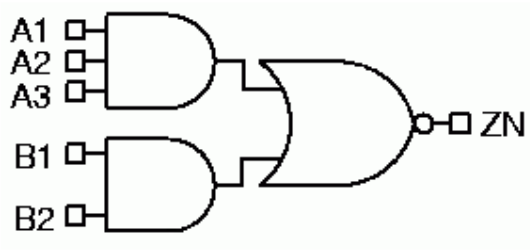
Delay Table (ns)

Description	V0P4	V0P7	V1	V2	V3
A1→ZN_FALL	0.07669	0.05238	0.05239	0.05160	0.03841
A1→ZN_RISE	0.11384	0.10042	0.08474	0.07527	0.07785
A2→ZN_FALL	0.07871	0.05621	0.05718	0.05686	0.04644
A2→ZN_RISE	0.12289	0.11547	0.09831	0.08963	0.09797
A3→ZN_FALL	0.08140	0.06016	0.06086	0.06234	0.05112
A3→ZN_RISE	0.13137	0.12973	0.10938	0.10215	0.11016
B→ZN_FALL	0.03374	0.02559	0.02516	0.02058	0.01945
B→ZN_RISE	0.07296	0.06758	0.05735	0.04748	0.05307

AOI32UHD

Cell Description

3-2 AOI
ZN=(!((A1&A2&A3)|(B1&B2)))



Function Table

A1	A2	A3	B1	B2	ZN
0	X	X	0	X	1
0	X	X	1	0	1
0	X	X	1	1	0
1	0	X	0	X	1
1	0	X	1	0	1
1	0	X	1	1	0
1	1	0	0	X	1
1	1	0	1	0	1
1	1	0	1	1	0
1	1	1	X	X	0

Cell Size

CellName	Height(um)	Width(um)
AOI32UHDV0P4	3.360	3.920
AOI32UHDV0P7	3.360	4.480
AOI32UHDV1	3.360	4.480
AOI32UHDV2	3.360	8.400
AOI32UHDV3	3.360	11.760

Pin Power (uW/MHz)

Pin	V0P4	V0P7	V1	V2	V3
A1	0.00626	0.00800	0.00974	0.01929	0.02766
A2	0.00672	0.00888	0.01086	0.02159	0.03271
A3	0.00719	0.00981	0.01202	0.02418	0.03716
B1	0.00317	0.00431	0.00514	0.01059	0.01593
B2	0.00366	0.00515	0.00633	0.01286	0.02059

Pin Capacitance (pf)

Pin	V0P4	V0P7	V1	V2	V3
A1	0.00233	0.00328	0.00385	0.00635	0.01052
A2	0.00238	0.00330	0.00382	0.00779	0.01072
A3	0.00227	0.00320	0.00383	0.00857	0.01119
B1	0.00225	0.00314	0.00371	0.00712	0.01061
B2	0.00227	0.00326	0.00382	0.00803	0.01086

Max Leakage Power (uW)

V0P4	V0P7	V1	V2	V3
0.00003803	0.00004960	0.00005949	0.00010956	0.00022345

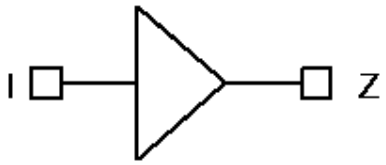
Delay Table (ns)

Description	V0P4	V0P7	V1	V2	V3
A1→ZN_FALL	0.08940	0.06592	0.06246	0.06792	0.04648
A1→ZN_RISE	0.13124	0.10500	0.09930	0.09341	0.09690
A2→ZN_FALL	0.09268	0.07059	0.06722	0.07305	0.05467
A2→ZN_RISE	0.14044	0.11752	0.11145	0.10643	0.11543
A3→ZN_FALL	0.09542	0.07425	0.07094	0.07862	0.05941
A3→ZN_RISE	0.14819	0.12760	0.12132	0.11806	0.12606
B1→ZN_FALL	0.04745	0.03750	0.03511	0.03343	0.02792
B1→ZN_RISE	0.07990	0.06717	0.06223	0.05884	0.06330
B2→ZN_FALL	0.04911	0.03921	0.03761	0.03598	0.03229
B2→ZN_RISE	0.08808	0.07718	0.07355	0.07079	0.07723

BUFUHD

Cell Description

Non-Inverting Buffer
Z=I



Function Table

I	Z
0	0
1	1

Cell Size

CellName	Height(um)	Width(um)
BUFUHDV0P4	3.360	2.240
BUFUHDV0P7	3.360	2.240
BUFUHDV1	3.360	2.240
BUFUHDV2	3.360	3.360
BUFUHDV3	3.360	3.920
BUFUHDV4	3.360	5.040
BUFUHDV6	3.360	6.720
BUFUHDV8	3.360	8.960
BUFUHDV16	3.360	16.800
BUFUHDV20	3.360	21.280
BUFUHDV24	3.360	24.640

Pin Power (uW/MHz)

Pin	V0P4	V0P7	V1	V2	V3	V4	V6	V8
I	0.00582	0.00739	0.00860	0.01413	0.02112	0.02671	0.03922	0.05375

Pin	V16	V20	V24
I	0.10426	0.13140	0.16076

Pin Capacitance (pf)

Pin	V0P4	V0P7	V1	V2	V3	V4	V6	V8
I	0.00283	0.00306	0.00322	0.00432	0.00453	0.00688	0.00844	0.01264

Pin	V16	V20	V24
I	0.02497	0.03367	0.03800

Max Leakage Power (uW)

V0P4	V0P7	V1	V2	V3	V4	V6	V8
0.00002361	0.00002965	0.00003274	0.00006575	0.00009682	0.00013446	0.00020457	0.00028137

V16	V20	V24
0.00057274	0.00072454	0.00086298

Delay Table (ns)

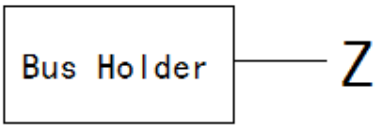
Description	V0P4	V0P7	V1	V2	V3	V4	V6	V8
I→Z_FALL	0.08113	0.08040	0.07805	0.07232	0.08380	0.07574	0.07806	0.07510
I→Z_RISE	0.07380	0.06191	0.06272	0.06152	0.06749	0.05864	0.06202	0.05977

Description	V16	V20	V24
I→Z_FALL	0.07377	0.07279	0.07656
I→Z_RISE	0.05867	0.05844	0.06174

BUSHOLDUHD

Cell Description

Bus-Hold
Z=Z_pre



Function Table

Z
1
0

Cell Size

CellName	Height(um)	Width(um)
BUSHOLDUHDV0	3.360	2.800

Pin Power (uW/MHz)

Pin	V0

Pin Capacitance (pf)

Pin	V0

Max Leakage Power (uW)

V0
63.30115800

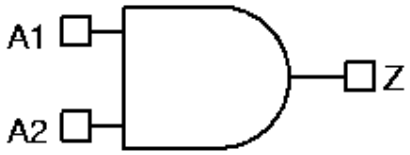
Delay Table (ns)

Description	V0

CLKAND2UHD

Cell Description

2-Input Clock AND
Z=(A1&A2)



Function Table

A1	A2	Z
0	X	0
1	0	0
1	1	1

Cell Size

CellName	Height(um)	Width(um)
CLKAND2UHDV0P7	3.360	2.800
CLKAND2UHDV1	3.360	2.800
CLKAND2UHDV2	3.360	3.920
CLKAND2UHDV3	3.360	4.480
CLKAND2UHDV4	3.360	5.040
CLKAND2UHDV6	3.360	7.280
CLKAND2UHDV8	3.360	10.080

Pin Power (uW/MHz)

Pin	V0P7	V1	V2	V3	V4	V6	V8
A1	0.00772	0.00831	0.01366	0.01860	0.02499	0.03898	0.05080
A2	0.00849	0.00909	0.01436	0.01936	0.02603	0.04014	0.05340

Pin Capacitance (pf)

Pin	V0P7	V1	V2	V3	V4	V6	V8
A1	0.00274	0.00271	0.00377	0.00380	0.00405	0.00618	0.00963
A2	0.00291	0.00289	0.00382	0.00382	0.00399	0.00651	0.00992

Max Leakage Power (uW)

V0P7	V1	V2	V3	V4	V6	V8
0.00003278	0.00003395	0.00006693	0.00007274	0.00009714	0.00016321	0.00021334

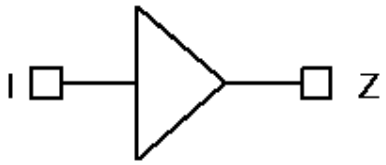
Delay Table (ns)

Description	V0P7	V1	V2	V3	V4	V6	V8
A1→Z_FALL	0.09211	0.09825	0.07668	0.08897	0.10055	0.08471	0.08578
A1→Z_RISE	0.07900	0.07573	0.09445	0.10587	0.10572	0.13141	0.10181
A2→Z_FALL	0.10413	0.11067	0.08219	0.09496	0.10775	0.08948	0.08815
A2→Z_RISE	0.08191	0.07878	0.09643	0.10797	0.10755	0.13421	0.10573

CLKBUFUHD

Cell Description

Clock Buffer with Balanced Rise/Fall Time
Z=I



Function Table

I	Z
0	0
1	1

Cell Size

CellName	Height(um)	Width(um)
CLKBUFUHDV1	3.360	2.240
CLKBUFUHDV2	3.360	3.360
CLKBUFUHDV3	3.360	3.920
CLKBUFUHDV4	3.360	5.040
CLKBUFUHDV6	3.360	6.160
CLKBUFUHDV8	3.360	8.400
CLKBUFUHDV16	3.360	16.800
CLKBUFUHDV20	3.360	19.040
CLKBUFUHDV24	3.360	20.160

Pin Power (uW/MHz)

Pin	V1	V2	V3	V4	V6	V8	V16	V20
I	0.00794	0.01189	0.01700	0.02184	0.03080	0.04146	0.08632	0.10726

Pin	V24
I	0.12175

Pin Capacitance (pf)

Pin	V1	V2	V3	V4	V6	V8	V16	V20
I	0.00337	0.00340	0.00404	0.00568	0.00760	0.01041	0.02235	0.02695

Pin	V24
I	0.03009

Max Leakage Power (uW)

V1	V2	V3	V4	V6	V8	V16	V20
0.00003008	0.00004581	0.00005898	0.00008044	0.00011812	0.00016837	0.00036726	0.00045847

V24
0.00050206

Delay Table (ns)

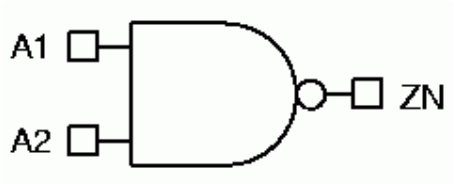
Description	V1	V2	V3	V4	V6	V8	V16	V20
I→Z_FALL	0.07788	0.08239	0.08667	0.07624	0.07492	0.07180	0.07176	0.07186
I→Z_RISE	0.07378	0.08166	0.07979	0.08031	0.07448	0.07454	0.07260	0.07204

Description	V24
I→Z_FALL	0.07216
I→Z_RISE	0.07296

CLKNAND2UHD

Cell Description

2-Input NAND
ZN=(!(A1&A2))



Function Table

A1	A2	ZN
0	X	1
1	0	1
1	1	0

Cell Size

CellName	Height(um)	Width(um)
CLKNAND2UHDV0P7	3.360	2.240
CLKNAND2UHDV1	3.360	2.240
CLKNAND2UHDV2	3.360	3.920
CLKNAND2UHDV3	3.360	5.040
CLKNAND2UHDV4	3.360	6.720
CLKNAND2UHDV6	3.360	8.400
CLKNAND2UHDV8	3.360	12.320

Pin Power (uW/MHz)

Pin	V0P7	V1	V2	V3	V4	V6	V8
A1	0.00289	0.00362	0.00685	0.00961	0.01302	0.01657	0.02571
A2	0.00346	0.00440	0.00941	0.01306	0.01709	0.02314	0.03412

Pin Capacitance (pf)

Pin	V0P7	V1	V2	V3	V4	V6	V8
A1	0.00265	0.00338	0.00620	0.00877	0.01187	0.01552	0.02309
A2	0.00275	0.00350	0.00669	0.00941	0.01265	0.01658	0.02500

Max Leakage Power (uW)

V0P7	V1	V2	V3	V4	V6	V8
0.00002101	0.00002871	0.00005443	0.00007796	0.00010484	0.00012977	0.00020815

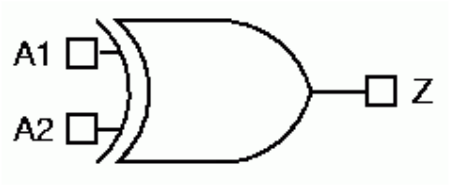
Delay Table (ns)

Description	V0P7	V1	V2	V3	V4	V6	V8
A1→ZN_FALL	0.04221	0.03850	0.03382	0.03258	0.03220	0.02832	0.03104
A1→ZN_RISE	0.04100	0.03626	0.03435	0.03246	0.03203	0.03243	0.03140
A2→ZN_FALL	0.04321	0.03970	0.03933	0.03740	0.03592	0.03271	0.03492
A2→ZN_RISE	0.04527	0.04042	0.04000	0.03817	0.03740	0.03903	0.03644

CLKXOR2UHD

Cell Description

2-Input Exclusive OR
Z=(A1^A2)



Function Table

A2	A1	Z
0	0	0
0	1	1
1	0	1
1	1	0

Cell Size

CellName	Height(um)	Width(um)
CLKXOR2UHDV0P7	3.360	5.600
CLKXOR2UHDV1	3.360	5.600
CLKXOR2UHDV2	3.360	7.280
CLKXOR2UHDV4	3.360	15.120

Pin Power (uW/MHz)

Pin	V0P7	V1	V2	V4
A1	0.00957	0.01085	0.01350	0.03275
A2	0.01138	0.01288	0.01980	0.04474

Pin Capacitance (pf)

Pin	V0P7	V1	V2	V4
A1	0.00629	0.00697	0.01045	0.02290
A2	0.00316	0.00356	0.00741	0.01371

Max Leakage Power (uW)

V0P7	V1	V2	V4

0.00007497	0.00008000	0.00012742	0.00027616

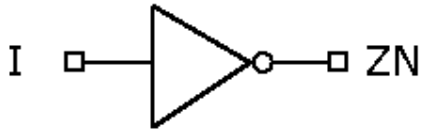
Delay Table (ns)

Description	V0P7	V1	V2	V4
A1→Z_FALL	0.06585	0.06814	0.04413	0.05923
A1→Z_RISE	0.06549	0.06151	0.05098	0.05887
A2→Z_FALL	0.09065	0.09410	0.07972	0.11413
A2→Z_RISE	0.11277	0.10637	0.08374	0.12131

CLKINUHD

Cell Description

CLKIN
ZN=(!I)



Function Table

I	ZN
0	1
1	0

Cell Size

CellName	Height(um)	Width(um)
CLKINUHDV1	3.360	1.680
CLKINUHDV2	3.360	2.240
CLKINUHDV3	3.360	3.360
CLKINUHDV4	3.360	3.920
CLKINUHDV6	3.360	4.480
CLKINUHDV8	3.360	6.160
CLKINUHDV16	3.360	11.200
CLKINUHDV20	3.360	12.320
CLKINUHDV24	3.360	15.120

Pin Power (uW/MHz)

Pin	V1	V2	V3	V4	V6	V8	V16	V20
I	0.00261	0.00383	0.00600	0.00752	0.01134	0.01533	0.03053	0.03698

Pin	V24
I	0.04591

Pin Capacitance (pf)

Pin	V1	V2	V3	V4	V6	V8	V16	V20
I	0.00307	0.00573	0.00853	0.01129	0.01646	0.02242	0.04479	0.05400

Pin	V24
I	0.06579

Max Leakage Power (uW)

V1	V2	V3	V4	V6	V8	V16	V20
0.00001520	0.00003158	0.00004172	0.00005659	0.00008308	0.00012371	0.00026859	0.00031929

V24
0.00040124

Delay Table (ns)

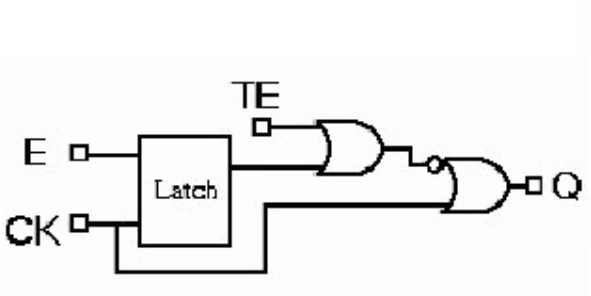
Description	V1	V2	V3	V4	V6	V8	V16	V20
I→ZN_FALL	0.03340	0.02686	0.02631	0.02518	0.02474	0.02396	0.02525	0.02625
I→ZN_RISE	0.03073	0.02448	0.02406	0.02295	0.02236	0.02232	0.02421	0.02513

Description	V24
I→ZN_FALL	0.02784
I→ZN_RISE	0.02678

CLKLAHAQUHD

Cell Description

Post-controlled negative-edge triggered clock-gating latch
IQ=CK ? !E : pre_IQ
Q=CK ? 1 : (IQ & !TE)



Function Table

CK<1>	CK	TE	E	Q
1	0	0	0	1
1	0	0	1	0
1	0	1	X	0
1	1	X	X	1
0	0	0	X	Q<1>
0	0	1	X	0

Cell Size

CellName	Height(um)	Width(um)
CLKLAHAQUHDV1	3.360	11.760
CLKLAHAQUHDV2	3.360	14.560
CLKLAHAQUHDV3	3.360	15.120
CLKLAHAQUHDV4	3.360	15.680
CLKLAHAQUHDV6	3.360	21.280
CLKLAHAQUHDV8	3.360	22.960

Pin Power (uW/MHz)

Pin	V1	V2	V3	V4	V6	V8
CK	0.01385	0.01791	0.01736	0.01795	0.02313	0.02314
E	0.00698	0.00891	0.00896	0.00900	0.01101	0.01101
Q	0.01654	0.02507	0.03087	0.03677	0.05453	0.06768
TE	0.00417	0.00634	0.00635	0.00633	0.01018	0.01020

Pin Capacitance (pf)

Pin	V1	V2	V3	V4	V6	V8

CK	0.00353	0.00417	0.00362	0.00419	0.00418	0.00419
E	0.00281	0.00311	0.00310	0.00315	0.00315	0.00314
TE	0.00352	0.00349	0.00349	0.00344	0.00404	0.00404

Max Leakage Power (uW)

V1	V2	V3	V4	V6	V8
0.00012111	0.00014746	0.00015274	0.00017633	0.00023967	0.00028714

Delay Table (ns)

Description	V1	V2	V3	V4	V6	V8
CK→Q_FALL	0.20747	0.19354	0.21831	0.22046	0.22823	0.23991
CK→Q_RISE	0.20070	0.18613	0.21700	0.20635	0.22182	0.23410
TE→Q_FALL	0.16010	0.14590	0.16070	0.17215	0.17370	0.18620
TE→Q_RISE	0.16925	0.20325	0.22045	0.23435	0.23925	0.25790

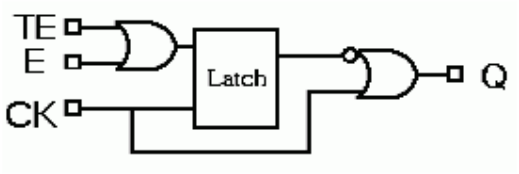
Timing Constraints (ns)

Pin	Requirement	V1	V2	V3	V4	V6	V8
E	hold_FALL→CK	-0.10765	-0.12758	-0.11958	-0.12360	-0.16349	-0.16349
E	hold_RISE→CK	0.01199	0.01196	0.01597	0.01196	0.00797	0.00399
E	setup_FALL→CK	0.11165	0.13156	0.12761	0.13157	0.17144	0.17146
E	setup_RISE→CK	-0.00399	0.00398	-0.00399	0.00000	0.00798	0.01197
CK	minpwh	0.12390	0.12785	0.13230	0.12445	0.16050	0.16050

CLKLAHQUHD

Cell Description

a pre-controlled negative-edge triggered clock-gating latch for Low Power Design
IQ=CK ? !(TE|E) : pre_IQ
Q=IQ|CK



Function Table

CK<1>	CK	TE	E	Q
1	0	0	0	1
1	0	0	1	0
1	0	1	X	0
0	0	X	X	Q<1>
1	1	X	X	1

Cell Size

CellName	Height(um)	Width(um)
CLKLAHQUHDV1	3.360	10.640
CLKLAHQUHDV2	3.360	11.760
CLKLAHQUHDV3	3.360	12.320
CLKLAHQUHDV4	3.360	14.000
CLKLAHQUHDV6	3.360	15.120
CLKLAHQUHDV8	3.360	17.920

Pin Power (uW/MHz)

Pin	V1	V2	V3	V4	V6	V8
CK	0.01227	0.01339	0.01338	0.01480	0.01537	0.01890
E	0.00385	0.00407	0.00407	0.00441	0.00445	0.00529
Q	0.01301	0.01877	0.02520	0.03153	0.04417	0.05811
TE	0.00436	0.00458	0.00458	0.00492	0.00496	0.00588

Pin Capacitance (pf)

Pin	V1	V2	V3	V4	V6	V8
CK	0.00349	0.00349	0.00349	0.00349	0.00350	0.00350

E	0.00289	0.00289	0.00288	0.00289	0.00289	0.00327
TE	0.00291	0.00290	0.00291	0.00290	0.00290	0.00330

Max Leakage Power (uW)

V1	V2	V3	V4	V6	V8
0.00010130	0.00011669	0.00012808	0.00015217	0.00018977	0.00024182

Delay Table (ns)

Description	V1	V2	V3	V4	V6	V8
CK→Q_FALL	0.26087	0.21886	0.24134	0.22851	0.23700	0.25215
CK→Q_RISE	0.18500	0.21818	0.23330	0.24195	0.26858	0.27700

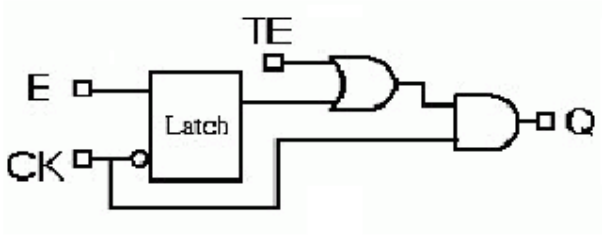
Timing Constraints (ns)

Pin	Requirement	V1	V2	V3	V4	V6	V8
E	hold_FALL→CK	-0.18753	-0.19939	-0.19938	-0.22330	-0.22729	-0.24325
E	hold_RISE→CK	0.00401	0.00401	0.00401	-0.00401	-0.00000	0.00398
E	setup_FALL→CK	0.19140	0.20736	0.20735	0.23127	0.23526	0.25122
E	setup_RISE→CK	0.00401	0.00797	0.00797	0.01197	0.01197	0.00797
TE	hold_FALL→CK	-0.19539	-0.21134	-0.21134	-0.23527	-0.23925	-0.25520
TE	hold_RISE→CK	0.00799	0.00400	0.00400	-0.00000	-0.00000	0.00398
TE	setup_FALL→CK	0.20336	0.21931	0.21931	0.24323	0.24723	0.25918
TE	setup_RISE→CK	0.00397	0.00797	0.00797	0.01595	0.01197	0.00797
CK	minpwh	0.15525	0.16680	0.16685	0.18735	0.19005	0.21160

CLKLANAQUHD

Cell Description

Post-controlled positive-edge triggered clock-gating latch
IQ=!CK ? E: pre_IQ
Q=!CK ? 0 : (IQ|TE)



Function Table

CK<1>	CK	TE	E	Q
0	1	0	0	0
0	1	0	1	1
0	1	1	X	1
0	0	X	X	0
1	1	0	X	Q<1>
1	1	1	X	1

Cell Size

CellName	Height(um)	Width(um)
CLKLANAQUHDV1	3.360	11.200
CLKLANAQUHDV2	3.360	11.200
CLKLANAQUHDV3	3.360	12.320
CLKLANAQUHDV4	3.360	16.800
CLKLANAQUHDV6	3.360	17.920
CLKLANAQUHDV8	3.360	20.720

Pin Power (uW/MHz)

Pin	V1	V2	V3	V4	V6	V8
CK	0.01476	0.01524	0.01547	0.01906	0.02037	0.02378
E	0.00733	0.00756	0.00763	0.00890	0.00949	0.01089
Q	0.01748	0.02217	0.02868	0.03955	0.05294	0.06648
TE	0.00005	0.00008	0.00009	0.00014	0.00016	0.00017

Pin Capacitance (pf)

Pin	V1	V2	V3	V4	V6	V8

CK	0.00357	0.00357	0.00357	0.00357	0.00357	0.00357
E	0.00334	0.00334	0.00333	0.00333	0.00336	0.00332
TE	0.00323	0.00364	0.00407	0.00678	0.00705	0.00838

Max Leakage Power (uW)

V1	V2	V3	V4	V6	V8
0.00010704	0.00011684	0.00013316	0.00018422	0.00021166	0.00027965

Delay Table (ns)

Description	V1	V2	V3	V4	V6	V8
CK→Q_FALL	0.21497	0.19715	0.20642	0.21590	0.21735	0.22350
CK→Q_RISE	0.19932	0.22859	0.23626	0.27491	0.31458	0.32846
TE→Q_FALL	0.24960	0.18475	0.20070	0.17655	0.19085	0.22960
TE→Q_RISE	0.07380	0.09780	0.09770	0.09750	0.11370	0.10000

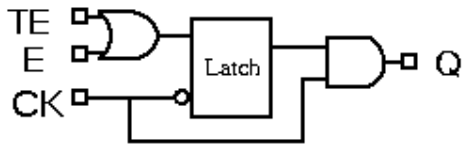
Timing Constraints (ns)

Pin	Requirement	V1	V2	V3	V4	V6	V8
E	hold_FALL→CK	-0.01196	-0.01196	-0.01196	-0.00000	0.00799	0.00797
E	hold_RISE→CK	-0.04786	-0.04786	-0.04786	-0.05581	-0.05582	-0.05580
E	setup_FALL→CK	0.01994	0.01994	0.01994	0.00796	0.00000	0.00000
E	setup_RISE→CK	0.05182	0.05182	0.05182	0.05980	0.05981	0.06377
CK	minpwl	0.11710	0.11920	0.11915	0.13105	0.13390	0.14365

CLKLANQUHD

Cell Description

pre-controlled positiveedge triggered clock-gating latch for Low Power Design
IQ=!CK ? (TE|E)
Q=IQ&CK



Function Table

CK<1>	CK	TE	E	Q
0	1	0	0	0
0	1	0	1	1
0	1	1	X	1
0	0	X	X	0
1	1	X	X	Q<1>

Cell Size

CellName	Height(um)	Width(um)
CLKLANQUHDV1	3.360	10.640
CLKLANQUHDV2	3.360	11.760
CLKLANQUHDV3	3.360	12.320
CLKLANQUHDV4	3.360	12.880
CLKLANQUHDV6	3.360	15.680
CLKLANQUHDV8	3.360	16.800

Pin Power (uW/MHz)

Pin	V1	V2	V3	V4	V6	V8
CK	0.01490	0.01717	0.01719	0.01719	0.02044	0.02070
E	0.00411	0.00452	0.00452	0.00452	0.00519	0.00523
Q	0.01282	0.01853	0.02343	0.02893	0.04126	0.05596
TE	0.00471	0.00522	0.00522	0.00522	0.00589	0.00589

Pin Capacitance (pf)

Pin	V1	V2	V3	V4	V6	V8
CK	0.00356	0.00412	0.00412	0.00412	0.00412	0.00411

E	0.00325	0.00354	0.00354	0.00354	0.00354	0.00357
TE	0.00331	0.00362	0.00362	0.00362	0.00362	0.00364

Max Leakage Power (uW)

V1	V2	V3	V4	V6	V8
0.00009705	0.00013122	0.00014121	0.00016187	0.00021991	0.00028041

Delay Table (ns)

Description	V1	V2	V3	V4	V6	V8
CK→Q_FALL	0.21613	0.18118	0.19143	0.20110	0.20122	0.21295
CK→Q_RISE	0.20098	0.18447	0.19323	0.20306	0.20356	0.21232

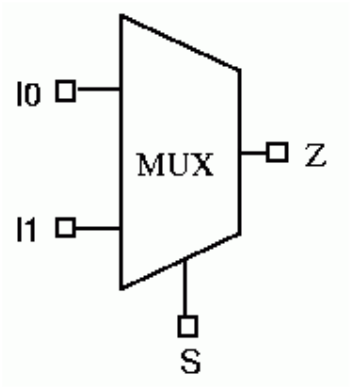
Timing Constraints (ns)

Pin	Requirement	V1	V2	V3	V4	V6	V8
E	hold_FALL→CK	-0.07976	-0.07975	-0.07975	-0.07973	-0.07973	-0.07977
E	hold_RISE→CK	-0.05582	-0.05984	-0.05984	-0.05984	-0.06380	-0.06776
E	setup_FALL→CK	0.08776	0.09569	0.09569	0.09568	0.09573	0.09969
E	setup_RISE→CK	0.06379	0.06778	0.06778	0.06778	0.07177	0.07573
TE	hold_FALL→CK	-0.08773	-0.09172	-0.09172	-0.09172	-0.09172	-0.08771
TE	hold_RISE→CK	-0.06380	-0.07177	-0.07177	-0.06778	-0.07576	-0.07576
TE	setup_FALL→CK	0.09968	0.10367	0.10769	0.10367	0.10769	0.10764
TE	setup_RISE→CK	0.07179	0.07575	0.07575	0.07575	0.08372	0.08373
CK	minpwl	0.15025	0.14550	0.14550	0.14550	0.15995	0.16760

CLKMUX2UHD

Cell Description

CLKMUX2
Z=((I0&(!S))|(I1&S))



Function Table

S	I0	I1	Z
0	0	X	0
0	1	X	1
1	X	0	0
1	X	1	1

Cell Size

CellName	Height(um)	Width(um)
CLKMUX2UHDV0P7	3.360	5.040
CLKMUX2UHDV1	3.360	5.040
CLKMUX2UHDV2	3.360	5.600
CLKMUX2UHDV3	3.360	6.720
CLKMUX2UHDV4	3.360	7.840
CLKMUX2UHDV6	3.360	14.000
CLKMUX2UHDV8	3.360	17.360

Pin Power (uW/MHz)

Pin	V0P7	V1	V2	V3	V4	V6	V8
I0	0.01062	0.01148	0.01713	0.02533	0.03316	0.05272	0.06998
I1	0.01038	0.01124	0.01693	0.02378	0.03206	0.05210	0.06931
S	0.01338	0.01425	0.02023	0.02821	0.03645	0.05613	0.07412

Pin Capacitance (pf)

Pin	V0P7	V1	V2	V3	V4	V6	V8
I0	0.00293	0.00297	0.00308	0.00321	0.00350	0.00605	0.00917
I1	0.00269	0.00272	0.00389	0.00386	0.00430	0.00647	0.00988

S	0.00510	0.00517	0.00605	0.00690	0.00761	0.01101	0.01511

Max Leakage Power (uW)

V0P7	V1	V2	V3	V4	V6	V8
0.00007009	0.00007325	0.00008604	0.00010360	0.00011831	0.00020900	0.00027036

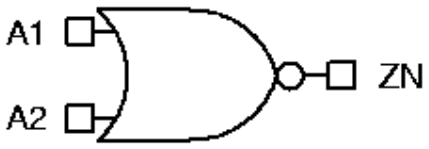
Delay Table (ns)

Description	V0P7	V1	V2	V3	V4	V6	V8
I0→Z_FALL	0.18468	0.19101	0.20676	0.23045	0.18351	0.16202	0.16230
I0→Z_RISE	0.09514	0.09306	0.10157	0.11659	0.15150	0.17384	0.14947
I1→Z_FALL	0.17898	0.18570	0.15087	0.16913	0.16486	0.15748	0.16004
I1→Z_RISE	0.09014	0.08822	0.10988	0.12457	0.15013	0.17212	0.14794
S→Z_FALL	0.16603	0.17299	0.16837	0.18690	0.16234	0.14503	0.14802
S→Z_RISE	0.11304	0.11037	0.11917	0.12918	0.15959	0.17511	0.14608

CLKNOR2UHD

Cell Description

2-Input NOR
ZN=(!(A1|A2))



Function Table

A1	A2	ZN
0	0	1
0	1	0
1	X	0

Cell Size

CellName	Height(um)	Width(um)
CLKNOR2UHDV0P7	3.360	2.240
CLKNOR2UHDV1	3.360	2.240
CLKNOR2UHDV2	3.360	3.920
CLKNOR2UHDV3	3.360	5.040
CLKNOR2UHDV4	3.360	6.720
CLKNOR2UHDV6	3.360	9.520
CLKNOR2UHDV8	3.360	11.200

Pin Power (uW/MHz)

Pin	V0P7	V1	V2	V3	V4	V6	V8
A1	0.00261	0.00305	0.00426	0.00711	0.00833	0.01352	0.01711
A2	0.00369	0.00463	0.00891	0.01322	0.01707	0.02652	0.03394

Pin Capacitance (pf)

Pin	V0P7	V1	V2	V3	V4	V6	V8
A1	0.00245	0.00290	0.00494	0.00729	0.00981	0.01496	0.01969
A2	0.00250	0.00302	0.00550	0.00808	0.01080	0.01659	0.02158

Max Leakage Power (uW)

V0P7	V1	V2	V3	V4	V6	V8
0.00002997	0.00003008	0.00003935	0.00005127	0.00008528	0.00012404	0.00018207

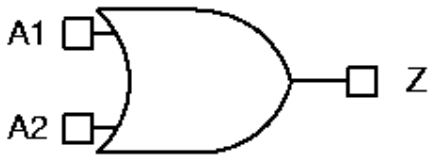
Delay Table (ns)

Description	V0P7	V1	V2	V3	V4	V6	V8
A1→ZN_FALL	0.03825	0.04181	0.03498	0.03678	0.03247	0.03328	0.03179
A1→ZN_RISE	0.06108	0.05075	0.03693	0.03840	0.03477	0.03598	0.03337
A2→ZN_FALL	0.04254	0.04942	0.04915	0.04998	0.04532	0.04616	0.04427
A2→ZN_RISE	0.06954	0.05971	0.05378	0.05258	0.05036	0.05140	0.04720

CLKOR2UHD

Cell Description

2-Input OR
Z=(A1|A2)



Function Table

A1	A2	Z
0	0	0
0	1	1
1	X	1

Cell Size

CellName	Height(um)	Width(um)
CLKOR2UHDV0P7	3.360	3.360
CLKOR2UHDV1	3.360	3.360
CLKOR2UHDV2	3.360	3.920
CLKOR2UHDV3	3.360	4.480
CLKOR2UHDV4	3.360	6.160
CLKOR2UHDV6	3.360	8.960
CLKOR2UHDV8	3.360	10.080

Pin Power (uW/MHz)

Pin	V0P7	V1	V2	V3	V4	V6	V8
A1	0.00795	0.00880	0.01494	0.01924	0.02460	0.03651	0.05036
A2	0.00881	0.01013	0.01661	0.02094	0.02784	0.04149	0.05717

Pin Capacitance (pf)

Pin	V0P7	V1	V2	V3	V4	V6	V8
A1	0.00271	0.00329	0.00355	0.00352	0.00444	0.00577	0.00958
A2	0.00291	0.00345	0.00379	0.00375	0.00434	0.00611	0.00994

Max Leakage Power (uW)

V0P7	V1	V2	V3	V4	V6	V8
0.00004994	0.00005282	0.00006704	0.00007997	0.00009434	0.00012592	0.00019729

Delay Table (ns)

Description	V0P7	V1	V2	V3	V4	V6	V8
A1→Z_FALL	0.13521	0.11076	0.11233	0.13666	0.12478	0.12519	0.11500
A1→Z_RISE	0.06362	0.06427	0.07433	0.07830	0.08947	0.09161	0.08281
A2→Z_FALL	0.14863	0.12280	0.12414	0.14836	0.14109	0.14289	0.12876
A2→Z_RISE	0.06758	0.07025	0.08204	0.08587	0.10326	0.10647	0.09434

DEL1UHD

Cell Description

Delay cell
Z=I

Function Table

I	Z
0	0
1	1

Cell Size

CellName	Height(um)	Width(um)
DEL1UHDV1	3.360	5.040
DEL2UHDV1	3.360	5.600
DEL4UHDV1	3.360	7.280
DEL1UHDV2	3.360	5.600
DEL2UHDV2	3.360	6.160
DEL4UHDV2	3.360	7.840

Pin Power (uW/MHz)

Pin	V1	V1	V1	V2	V2	V2
I	0.01683	0.02239	0.03194	0.02148	0.02788	0.04171

Pin Capacitance (pf)

Pin	V1	V1	V1	V2	V2	V2
I	0.00243	0.00306	0.00258	0.00247	0.00310	0.00257

Max Leakage Power (uW)

V1	V1	V1	V2	V2	V2
0.00005695	0.00004172	0.00004089	0.00007091	0.00005460	0.00005652

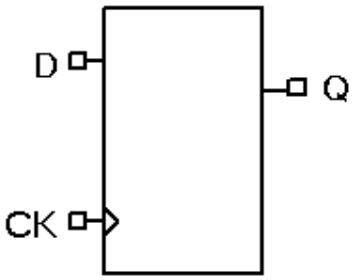
Delay Table (ns)

Description	V1	V1	V1	V2	V2	V2
I→Z_FALL	0.19028	0.27632	0.61928	0.19455	0.29670	0.66164
I→Z_RISE	0.15058	0.27375	0.62046	0.15899	0.28980	0.65667

DQUHD

Cell Description

D Flip-Flop, Single Output
Q = rising (CK) ? D : pre_Q



Function Table

CK<1>	CK	D	Q
0	0	X	Q<1>
0	1	0	0
0	1	1	1
1	X	X	Q<1>

Cell Size

CellName	Height(um)	Width(um)
DQUHDV0P7	3.360	11.760
DQUHDV1	3.360	11.760
DQUHDV2	3.360	12.320
DQUHDV3	3.360	12.880

Pin Power (uW/MHz)

Pin	V0P7	V1	V2	V3
CK	0.01443	0.01444	0.01490	0.01413
D	0.00659	0.00659	0.00659	0.00624
Q	0.02092	0.02175	0.02730	0.03453

Pin Capacitance (pf)

Pin	V0P7	V1	V2	V3
CK	0.00257	0.00258	0.00256	0.00257
D	0.00268	0.00268	0.00264	0.00271

Max Leakage Power (uW)

V0P7	V1	V2	V3
0.00010791	0.00011003	0.00013790	0.00016781

Delay Table (ns)

Description	V0P7	V1	V2	V3
CK→Q_FALL	0.24650	0.24950	0.26160	0.27690
CK→Q_RISE	0.22640	0.22390	0.23270	0.27620

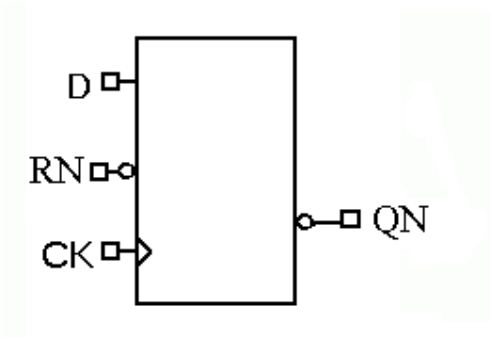
Timing Constraints (ns)

Pin	Requirement	V0P7	V1	V2	V3
D	hold_FALL→CK	-0.00400	-0.00400	-0.00000	-0.00800
D	hold_RISE→CK	-0.03190	-0.03190	-0.03190	-0.03190
D	setup_FALL→CK	0.09970	0.09970	0.09970	0.09170
D	setup_RISE→CK	0.09170	0.09170	0.08770	0.07980
CK	minpwh	0.09240	0.09230	0.09650	0.13450
CK	minpwl	0.23810	0.23820	0.24340	0.20920

DGRNQNUHD

Cell Description

D Flip-Flop with Sync Clear, Single Output QN
QN = rising (CK) ? !(D&RN) : pre_QN



Function Table

CK<1>	CK	RN	D	QN
0	0	X	X	QN<1>
0	1	0	X	1
0	1	1	0	1
0	1	1	1	0
1	X	X	X	QN<1>

Cell Size

CellName	Height(um)	Width(um)
DGRNQNUHDV0P7	3.360	12.320
DGRNQNUHDV1	3.360	12.320
DGRNQNUHDV2	3.360	12.880

Pin Power (uW/MHz)

Pin	V0P7	V1	V2
CK	0.01454	0.01454	0.01452
D	0.00366	0.00366	0.00366
QN	0.02223	0.02354	0.03162
RN	0.00377	0.00377	0.00376

Pin Capacitance (pf)

Pin	V0P7	V1	V2
CK	0.00257	0.00257	0.00257
D	0.00195	0.00195	0.00195
RN	0.00232	0.00232	0.00231

Max Leakage Power (uW)

V0P7	V1	V2
0.00010679	0.00010946	0.00012695

Delay Table (ns)

Description	V0P7	V1	V2
CK→QN_FALL	0.19790	0.20150	0.22600
CK→QN_RISE	0.22270	0.22280	0.23310

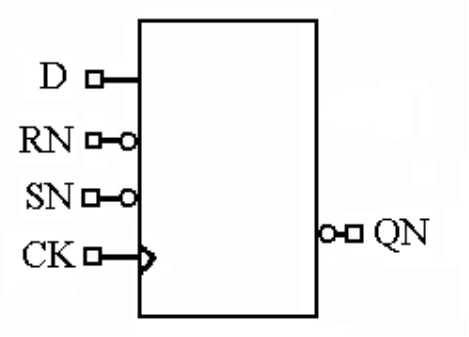
Timing Constraints (ns)

Pin	Requirement	V0P7	V1	V2
D	hold_FALL→CK	-0.01200	-0.01200	-0.01200
D	hold_RISE→CK	-0.07180	-0.07180	-0.07180
D	setup_FALL→CK	0.11160	0.11560	0.11960
D	setup_RISE→CK	0.16350	0.16350	0.14750
RN	hold_FALL→CK	-0.00800	-0.00800	-0.00800
RN	hold_RISE→CK	-0.07570	-0.07570	-0.07180
RN	setup_FALL→CK	0.11960	0.12350	0.12750
RN	setup_RISE→CK	0.16750	0.16350	0.15150
CK	minpwh	0.08810	0.08810	0.09240
CK	minpwl	0.27760	0.27760	0.28290

DGRSNQNUHD

Cell Description

D Flip-Flop with Sync Clear and Set, Single Output QN
QN = rising (CK) ? !RN&!(D|!SN) : pre_QN



Function Table

CK<1>	CK	SN	D	RN	QN
0	0	X	X	X	QN<1>
0	1	0	X	0	1
0	1	0	X	1	0
0	1	1	0	X	1
0	1	1	1	0	1
0	1	1	1	1	0
1	X	X	X	X	QN<1>

Cell Size

CellName	Height(um)	Width(um)
DGRSNQNUHDV0P7	3.360	15.680
DGRSNQNUHDV1	3.360	15.680
DGRSNQNUHDV2	3.360	16.800

Pin Power (uW/MHz)

Pin	V0P7	V1	V2
CK	0.01465	0.01465	0.01465
D	0.00241	0.00240	0.00241
QN	0.01782	0.01911	0.02698
RN	0.00756	0.00756	0.00756
SN	0.00602	0.00602	0.00602

Pin Capacitance (pf)

Pin	V0P7	V1	V2
CK	0.00257	0.00257	0.00257

D	0.00204	0.00204	0.00204
RN	0.00276	0.00276	0.00276
SN	0.00245	0.00245	0.00245

Max Leakage Power (uW)

V0P7	V1	V2
0.00011987	0.00012271	0.00015103

Delay Table (ns)

Description	V0P7	V1	V2
CK→QN_FALL	0.18510	0.18880	0.21800
CK→QN_RISE	0.22260	0.22250	0.23300

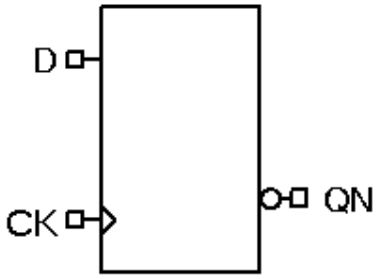
Timing Constraints (ns)

Pin	Requirement	V0P7	V1	V2
D	hold_FALL→CK	-0.09170	-0.09170	-0.09570
D	hold_RISE→CK	-0.08770	-0.08770	-0.08770
D	setup_FALL→CK	0.25520	0.25520	0.25520
D	setup_RISE→CK	0.15950	0.15950	0.14360
RN	hold_FALL→CK	-0.03190	-0.03190	-0.03590
RN	hold_RISE→CK	-0.10370	-0.10370	-0.10370
RN	setup_FALL→CK	0.17540	0.17540	0.17950
RN	setup_RISE→CK	0.17940	0.17940	0.16350
SN	hold_FALL→CK	-0.15150	-0.15150	-0.14750
SN	hold_RISE→CK	-0.12760	-0.12760	-0.13150
SN	setup_FALL→CK	0.22330	0.22330	0.20730
SN	setup_RISE→CK	0.29110	0.29110	0.29510
CK	minpwh	0.09230	0.09230	0.09650
CK	minpwl	0.34870	0.34870	0.35130

DQNUHD

Cell Description

D Flip-Flop, Single Output QN
QN = rising (CK) ? !D : pre_QN



Function Table

CK<1>	CK	D	QN
0	0	X	QN<1>
0	1	0	1
0	1	1	0
1	X	X	QN<1>

Cell Size

CellName	Height(um)	Width(um)
DQNUHDV0P7	3.360	11.760
DQNUHDV1	3.360	11.760
DQNUHDV2	3.360	12.320

Pin Power (uW/MHz)

Pin	V0P7	V1	V2
CK	0.01446	0.01444	0.01452
D	0.00659	0.00659	0.00659
QN	0.02243	0.02363	0.03303

Pin Capacitance (pf)

Pin	V0P7	V1	V2
CK	0.00257	0.00258	0.00257
D	0.00268	0.00268	0.00264

Max Leakage Power (uW)

V0P7	V1	V2

0.00010090	0.00010255	0.00012768

Delay Table (ns)

Description	V0P7	V1	V2
CK→QN_FALL	0.18500	0.18590	0.20560
CK→QN_RISE	0.22240	0.22110	0.23090

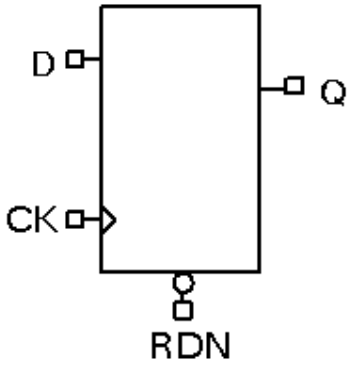
Timing Constraints (ns)

Pin	Requirement	V0P7	V1	V2
D	hold_FALL→CK	-0.00000	0.00400	0.00400
D	hold_RISE→CK	-0.03190	-0.03190	-0.03190
D	setup_FALL→CK	0.10370	0.10770	0.11170
D	setup_RISE→CK	0.09970	0.09970	0.09170
CK	minpwh	0.08810	0.08820	0.09230
CK	minpwl	0.31970	0.31970	0.32500

DRNQUHD

Cell Description

D Flip-Flop with Async Clear, Single Output
Q = !RDN ? 0 : rising (CK) ? D : pre_Q



Function Table

RDN	CK<1>	CK	D	Q
0	X	X	X	0
1	0	0	X	Q<1>
1	0	1	0	0
1	0	1	1	1
1	1	X	X	Q<1>

Cell Size

CellName	Height(um)	Width(um)
DRNQUHDV0P7	3.360	13.440
DRNQUHDV1	3.360	13.440
DRNQUHDV2	3.360	14.000
DRNQUHDV3	3.360	15.120

Pin Power (uW/MHz)

Pin	V0P7	V1	V2	V3
CK	0.01647	0.01575	0.01571	0.01567
D	0.00550	0.00514	0.00516	0.00515
Q	0.02449	0.02479	0.03029	0.03774
RDN	0.00013	0.00013	0.00013	0.00013

Pin Capacitance (pf)

Pin	V0P7	V1	V2	V3
CK	0.00234	0.00234	0.00231	0.00231
D	0.00262	0.00248	0.00248	0.00248
RDN	0.00658	0.00644	0.00643	0.00640

Max Leakage Power (uW)

V0P7	V1	V2	V3
0.00011204	0.00011481	0.00013613	0.00016479

Delay Table (ns)

Description	V0P7	V1	V2	V3
CK→Q_FALL	0.24310	0.24210	0.24890	0.26220
CK→Q_RISE	0.30010	0.29510	0.30840	0.33100
RDN→Q_FALL	0.07450	0.07560	0.08120	0.09308

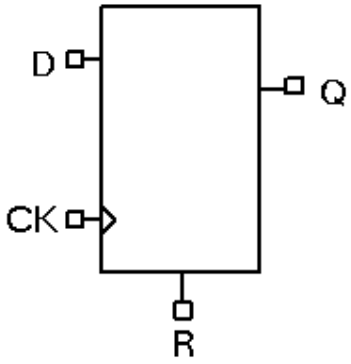
Timing Constraints (ns)

Pin	Requirement	V0P7	V1	V2	V3
D	hold_FALL→CK	0.00400	0.01590	0.01590	0.01200
D	hold_RISE→CK	-0.03590	-0.04780	-0.04780	-0.04780
D	setup_FALL→CK	0.11160	0.09570	0.09570	0.09570
D	setup_RISE→CK	0.09170	0.10770	0.10770	0.10370
RDN	setup_RISE→CK	-0.10766	-0.10371	-0.10767	-0.10767
RDN	hold_RISE→CK	0.13557	0.13160	0.13557	0.13161
CK	minpwh	0.15130	0.15130	0.16390	0.18080
CK	minpwl	0.21970	0.23550	0.23550	0.23290
RDN	minpwl	0.07130	0.07550	0.08810	0.10500

DRQUHD

Cell Description

D Flip-Flop with Async Clear, Single Output
Q = R ? 0 : rising (CK) ? D : pre_Q



Function Table

R	CK<1>	CK	D	Q
1	X	X	X	0
0	0	0	X	Q<1>
0	0	1	0	0
0	0	1	1	1
0	1	X	X	Q<1>

Cell Size

CellName	Height(um)	Width(um)
DRQUHDV0P7	3.360	13.440
DRQUHDV1	3.360	13.440
DRQUHDV2	3.360	14.560
DRQUHDV3	3.360	15.120

Pin Power (uW/MHz)

Pin	V0P7	V1	V2	V3
CK	0.01505	0.01505	0.01505	0.01505
D	0.00493	0.00493	0.00493	0.00493
Q	0.02162	0.02389	0.02948	0.03676
RD	0.00168	0.00168	0.00168	0.00168

Pin Capacitance (pf)

Pin	V0P7	V1	V2	V3
CK	0.00264	0.00264	0.00264	0.00264
D	0.00272	0.00272	0.00272	0.00272
RD	0.00452	0.00451	0.00452	0.00452

Max Leakage Power (uW)

V0P7	V1	V2	V3
0.00012694	0.00013302	0.00015286	0.00018215

Delay Table (ns)

Description	V0P7	V1	V2	V3
CK→Q_FALL	0.25400	0.25140	0.25990	0.27290
CK→Q_RISE	0.26920	0.27320	0.28330	0.29910
RD→Q_FALL	0.12975	0.12620	0.13410	0.14667

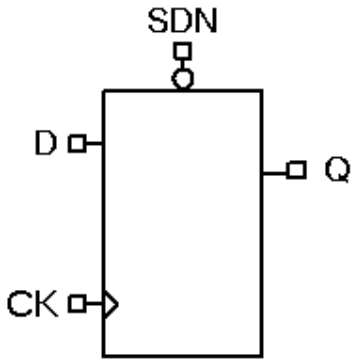
Timing Constraints (ns)

Pin	Requirement	V0P7	V1	V2	V3
D	hold_FALL→CK	-0.01200	-0.01200	-0.01200	-0.01200
D	hold_RISE→CK	-0.03590	-0.03590	-0.03590	-0.03590
D	setup_FALL→CK	0.07970	0.07970	0.07970	0.07970
D	setup_RISE→CK	0.19540	0.19140	0.19140	0.19140
RD	setup_FALL→CK	0.15150	0.14756	0.14752	0.14351
RD	hold_FALL→CK	-0.00796	-0.00796	-0.00800	-0.00800
CK	minpwh	0.13450	0.14290	0.15130	0.15970
CK	minpwl	0.32760	0.32500	0.32500	0.32240
RD	minpwh	0.07550	0.07970	0.08390	0.08390

DSNQUHD

Cell Description

D Flip-Flop with Async Set, Single Output Q
Q = !SDN ? 1 : rising (CK) ? D : pre_Q



Function Table

SDN	CK<1>	CK	D	Q
0	X	X	X	1
1	0	0	X	Q<1>
1	0	1	0	0
1	0	1	1	1
1	1	X	X	Q<1>

Cell Size

CellName	Height(um)	Width(um)
DSNQUHDV0P7	3.360	14.000
DSNQUHDV1	3.360	14.000
DSNQUHDV2	3.360	14.560
DSNQUHDV3	3.360	15.680

Pin Power (uW/MHz)

Pin	V0P7	V1	V2	V3
CK	0.01640	0.01637	0.01638	0.01635
D	0.00934	0.00930	0.00930	0.00930
Q	0.02980	0.03103	0.03643	0.04377
SDN	0.00200	0.00200	0.00200	0.00200

Pin Capacitance (pf)

Pin	V0P7	V1	V2	V3
CK	0.00271	0.00261	0.00261	0.00259
D	0.00431	0.00425	0.00425	0.00425
SDN	0.00615	0.00615	0.00616	0.00617

Max Leakage Power (uW)

V0P7	V1	V2	V3
0.00014837	0.00015074	0.00017919	0.00020843

Delay Table (ns)

Description	V0P7	V1	V2	V3
CK→Q_FALL	0.27070	0.27200	0.28120	0.29530
CK→Q_RISE	0.23120	0.23120	0.24020	0.25500
SDN→Q_RISE	0.22285	0.22305	0.23130	0.24547

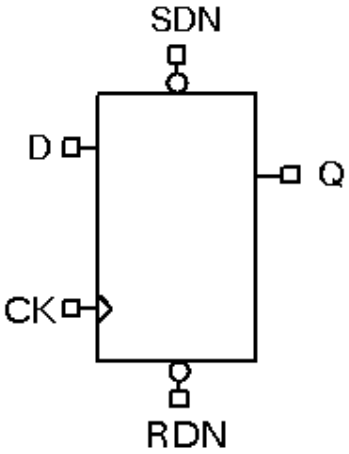
Timing Constraints (ns)

Pin	Requirement	V0P7	V1	V2	V3
D	hold_FALL→CK	-0.00000	-0.00000	-0.00000	-0.00000
D	hold_RISE→CK	-0.03590	-0.03590	-0.03590	-0.03590
D	setup_FALL→CK	0.05980	0.05980	0.05980	0.05980
D	setup_RISE→CK	0.11170	0.11160	0.11160	0.11160
SDN	setup_RISE→CK	-0.04386	-0.04388	-0.04388	-0.04384
SDN	hold_RISE→CK	0.07976	0.07973	0.07976	0.07976
CK	minpwh	0.09650	0.10070	0.10500	0.10920
CK	minpwl	0.24340	0.24340	0.24340	0.24080
SDN	minpwl	0.10920	0.10920	0.11760	0.12600

DSRNQUHD

Cell Description

D Flip-Flop with Async Clear and Set
Q = !RDN ? 0 : !SDN ? 1 : rising (CK) ? D : pre_Q



Function Table

RDN	SDN	CK<1>	CK	D	Q
0	0	X	X	X	0
0	1	X	X	X	0
1	0	X	X	X	1
1	1	0	0	X	Q<1>
1	1	0	1	0	0
1	1	0	1	1	1
1	1	1	X	X	Q<1>

Cell Size

CellName	Height(um)	Width(um)
DSRNQUHDV1	3.360	15.680
DSRNQUHDV2	3.360	16.800

Pin Power (uW/MHz)

Pin	V1	V2
CK	0.01796	0.01817
D	0.00508	0.00509
Q	0.02583	0.03318
RDN	0.00023	0.00023
SDN	0.00205	0.00212

Pin Capacitance (pf)

Pin	V1	V2
CK	0.00257	0.00258
D	0.00269	0.00269

RDN	0.00703	0.00707
SDN	0.00539	0.00542

Max Leakage Power (uW)

V1	V2
0.00013809	0.00016673

Delay Table (ns)

Description	V1	V2
CK→Q_FALL	0.29940	0.32370
CK→Q_RISE	0.25040	0.26660
RDN→Q_FALL	0.12826	0.15057
RDN→Q_RISE	0.08705	0.09753
SDN→Q_RISE	0.29480	0.31100

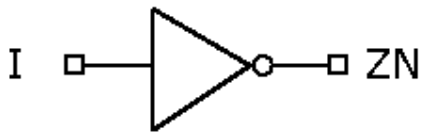
Timing Constraints (ns)

Pin	Requirement	V1	V2
D	hold_FALL→CK	-0.00000	-0.00000
D	hold_RISE→CK	-0.03590	-0.03590
D	setup_FALL→CK	0.10370	0.09970
D	setup_RISE→CK	0.14760	0.14750
RDN	setup_RISE→CK	-0.12762	-0.12759
RDN	hold_RISE→CK	0.15551	0.15550
SDN	setup_RISE→CK	-0.05983	-0.06381
SDN	hold_RISE→CK	0.12362	0.12762
SDN	non_seq_hold_RISE→RDN	0.00798	0.01993
SDN	non_seq_setup_RISE→RDN	0.01199	0.00000
CK	minpwh	0.10920	0.12180
CK	minpwl	0.28820	0.28290
RDN	minpwl	0.15130	0.18920
SDN	minpwl	0.21020	0.22290

INUHD

Cell Description

Inverter
ZN=(!I)



Function Table

I	ZN
0	1
1	0

Cell Size

CellName	Height(um)	Width(um)
INUHDV0P4	3.360	1.680
INUHDV0P7	3.360	1.680
INUHDV1	3.360	1.680
INUHDV2	3.360	2.240
INUHDV3	3.360	3.360
INUHDV4	3.360	3.920
INUHDV6	3.360	5.040
INUHDV8	3.360	6.720
INUHDV16	3.360	12.320
INUHDV20	3.360	15.120
INUHDV24	3.360	18.480

Pin Power (uW/MHz)

Pin	V0P4	V0P7	V1	V2	V3	V4	V6	V8
I	0.00180	0.00246	0.00299	0.00466	0.00757	0.00925	0.01374	0.01830

Pin	V16	V20	V24
I	0.03667	0.04578	0.05501

Pin Capacitance (pf)

Pin	V0P4	V0P7	V1	V2	V3	V4	V6	V8
I	0.00218	0.00317	0.00377	0.00721	0.01074	0.01423	0.02108	0.02809

Pin	V16	V20	V24
I	0.05617	0.06992	0.08368

Max Leakage Power (uW)

V0P4	V0P7	V1	V2	V3	V4	V6	V8
0.00001447	0.00001897	0.00002233	0.00004963	0.00007854	0.00010872	0.00017016	0.00023255

V16	V20	V24
0.00048272	0.00060781	0.00073291

Delay Table (ns)

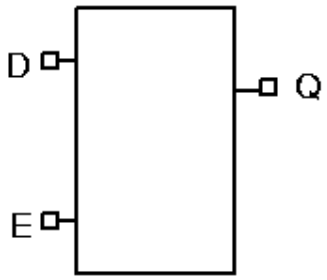
Description	V0P4	V0P7	V1	V2	V3	V4	V6	V8
I→ZN_FALL	0.02977	0.02361	0.02220	0.01732	0.01728	0.01593	0.01542	0.01524
I→ZN_RISE	0.04151	0.03519	0.03278	0.02724	0.02755	0.02596	0.02542	0.02534

Description	V16	V20	V24
I→ZN_FALL	0.01537	0.01586	0.01660
I→ZN_RISE	0.02551	0.02598	0.02663

LAHQUHD

Cell Description

High Enable Latch with single output(Q)
Q = E ? D : pre_Q



Function Table

E	D	Q
0	X	Q<1>
1	0	0
1	1	1

Cell Size

CellName	Height(um)	Width(um)
LAHQUHDV0P7	3.360	7.840
LAHQUHDV1	3.360	8.400
LAHQUHDV2	3.360	8.960
LAHQUHDV3	3.360	9.520

Pin Power (uW/MHz)

Pin	V0P7	V1	V2	V3
D	0.00023	0.00018	0.00025	0.00025
E	0.01275	0.01324	0.01393	0.01393
Q	0.01844	0.01958	0.02660	0.03632

Pin Capacitance (pf)

Pin	V0P7	V1	V2	V3
D	0.00272	0.00288	0.00387	0.00385
E	0.00336	0.00336	0.00336	0.00336

Max Leakage Power (uW)

V0P7	V1	V2	V3

0.00008213	0.00008581	0.00011589	0.00014535

Delay Table (ns)

Description	V0P7	V1	V2	V3
D→Q_FALL	0.18731	0.18939	0.16127	0.18594
D→Q_RISE	0.11390	0.10970	0.10320	0.11763
E→Q_FALL	0.18780	0.19840	0.17830	0.20330
E→Q_RISE	0.19150	0.18560	0.17960	0.19380

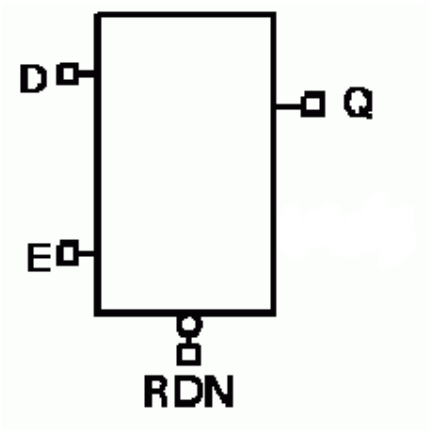
Timing Constraints (ns)

Pin	Requirement	V0P7	V1	V2	V3
D	hold_FALL→E	-0.11968	-0.11564	-0.08773	-0.10769
D	hold_RISE→E	0.00801	0.01597	0.02392	0.01196
D	setup_FALL→E	0.13959	0.13956	0.11566	0.14355
D	setup_RISE→E	0.00398	-0.00398	-0.00800	0.00399
E	minpwh	0.09240	0.08810	0.08390	0.09660

LAHRNQUHD

Cell Description

High Enable Latch with active-low reset(RDN) and a single output (Q)
Q = !RDN ? 0 : E ? D : pre_Q



Function Table

RDN	E	D	Q
0	X	X	0
1	0	X	Q<1>
1	1	0	0
1	1	1	1

Cell Size

CellName	Height(um)	Width(um)
LAHRNQUHDV0P7	3.360	8.960
LAHRNQUHDV1	3.360	8.960
LAHRNQUHDV2	3.360	9.520
LAHRNQUHDV3	3.360	10.080

Pin Power (uW/MHz)

Pin	V0P7	V1	V2	V3
D	0.00050	0.00050	0.00050	0.00051
E	0.01332	0.01332	0.01334	0.01323
Q	0.02125	0.02289	0.03070	0.04074
RDN	0.00002	0.00002	0.00003	0.00003

Pin Capacitance (pf)

Pin	V0P7	V1	V2	V3
D	0.00256	0.00256	0.00254	0.00253
E	0.00404	0.00404	0.00404	0.00410
RDN	0.00352	0.00351	0.00394	0.00401

Max Leakage Power (uW)

V0P7	V1	V2	V3
0.00009288	0.00009579	0.00012684	0.00015420

Delay Table (ns)

Description	V0P7	V1	V2	V3
D→Q_FALL	0.19677	0.20169	0.23121	0.26440
D→Q_RISE	0.15067	0.15258	0.17197	0.19073
E→Q_FALL	0.19750	0.20250	0.23220	0.26660
E→Q_RISE	0.22810	0.23000	0.24890	0.26170
RDN→Q_FALL	0.14298	0.14547	0.12298	0.13835
RDN→Q_RISE	0.16567	0.16759	0.18885	0.20641

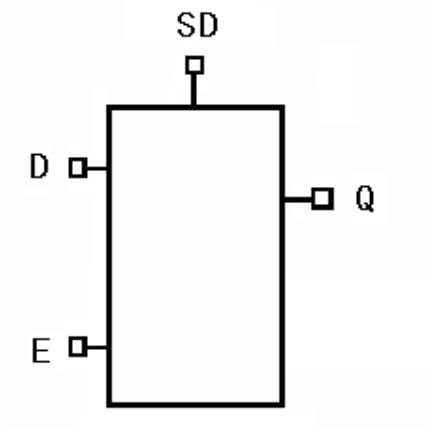
Timing Constraints (ns)

Pin	Requirement	V0P7	V1	V2	V3
D	hold_FALL→E	-0.13558	-0.13957	-0.16349	-0.19140
D	hold_RISE→E	-0.04783	-0.04783	-0.06777	-0.08372
D	setup_FALL→E	0.15554	0.15950	0.19539	0.22729
D	setup_RISE→E	0.06776	0.07572	0.11562	0.13958
RDN	setup_RISE→E	0.08373	0.08772	0.13556	0.15552
RDN	hold_RISE→E	-0.05981	-0.06381	-0.08374	-0.09971
E	minpwh	0.15130	0.15970	0.20180	0.21870
RDN	minpwl	0.13870	0.13870	0.12180	0.13440

LAHSQUHD

Cell Description

Latch with Async Set(High Active)
Q = SD ? 1 : E ? D : pre_Q



Function Table

SD	E	D	Q
1	X	X	1
0	0	X	Q<1>
0	1	0	0
0	1	1	1

Cell Size

CellName	Height(um)	Width(um)
LAHSQUHDV0P7	3.360	8.400
LAHSQUHDV1	3.360	8.400
LAHSQUHDV2	3.360	9.520
LAHSQUHDV3	3.360	10.080

Pin Power (uW/MHz)

Pin	V0P7	V1	V2	V3
D	0.00025	0.00027	0.00027	0.00027
E	0.01273	0.01276	0.01279	0.01279
Q	0.02136	0.02430	0.03462	0.04732
SD	0.00021	0.00021	0.00021	0.00021

Pin Capacitance (pf)

Pin	V0P7	V1	V2	V3
D	0.00255	0.00254	0.00253	0.00252
E	0.00410	0.00410	0.00410	0.00410
SD	0.00350	0.00349	0.00358	0.00358

Max Leakage Power (uW)

V0P7	V1	V2	V3
0.00009746	0.00010342	0.00012057	0.00015035

Delay Table (ns)

Description	V0P7	V1	V2	V3
D→Q_FALL	0.30016	0.31851	0.37095	0.43183
D→Q_RISE	0.12204	0.12589	0.13920	0.15902
E→Q_FALL	0.26380	0.28160	0.33530	0.39640
E→Q_RISE	0.19380	0.19770	0.21130	0.23100
SD→Q_RISE	0.08108	0.08260	0.08791	0.09882
SD→Q_FALL	0.33378	0.35345	0.40592	0.46723

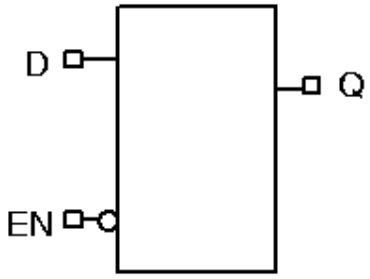
Timing Constraints (ns)

Pin	Requirement	V0P7	V1	V2	V3
D	hold_FALL→E	-0.23926	-0.25521	-0.29907	-0.34692
D	hold_RISE→E	-0.01596	-0.01994	-0.03585	-0.05580
D	setup_FALL→E	0.27116	0.30306	0.36286	0.43862
D	setup_RISE→E	0.03186	0.03584	0.05180	0.07174
SD	setup_FALL→E	0.30305	0.33496	0.39876	0.47451
SD	hold_FALL→E	-0.27515	-0.28712	-0.33097	-0.38280
E	minpwh	0.10920	0.10920	0.13020	0.14710
SD	minpwh	0.07130	0.07130	0.07970	0.08810

LALQUHD

Cell Description

Low Enable Latch with a single output (Q)
Q = !EN ? D : pre_Q



Function Table

EN	D	Q
0	0	0
0	1	1
1	X	Q<1>

Cell Size

CellName	Height(um)	Width(um)
LALQUHDV0P7	3.360	8.400
LALQUHDV1	3.360	8.400
LALQUHDV2	3.360	8.960
LALQUHDV3	3.360	9.520

Pin Power (uW/MHz)

Pin	V0P7	V1	V2	V3
D	0.00029	0.00030	0.00044	0.00044
EN	0.01306	0.01326	0.01377	0.01374
Q	0.01874	0.02040	0.02768	0.03729

Pin Capacitance (pf)

Pin	V0P7	V1	V2	V3
D	0.00278	0.00282	0.00378	0.00376
EN	0.00321	0.00320	0.00320	0.00320

Max Leakage Power (uW)

V0P7	V1	V2	V3

0.00008187	0.00008553	0.00011726	0.00014671

Delay Table (ns)

Description	V0P7	V1	V2	V3
D→Q_FALL	0.19433	0.19811	0.16672	0.18972
D→Q_RISE	0.11577	0.11463	0.10729	0.12114
EN→Q_FALL	0.27070	0.27620	0.24670	0.26910
EN→Q_RISE	0.19730	0.19750	0.19140	0.20620

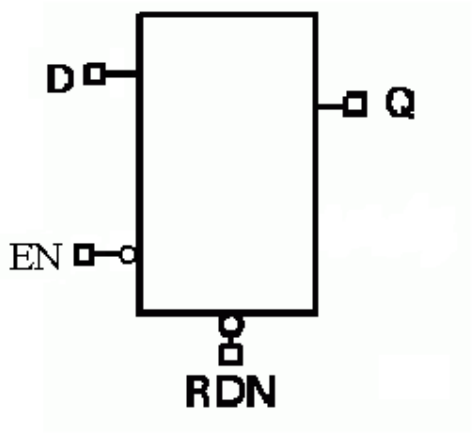
Timing Constraints (ns)

Pin	Requirement	V0P7	V1	V2	V3
D	hold_FALL→EN	-0.11166	-0.11169	-0.07575	-0.09569
D	hold_RISE→EN	-0.05584	-0.05583	-0.05185	-0.06378
D	setup_FALL→EN	0.13161	0.13559	0.10366	0.13160
D	setup_RISE→EN	0.07179	0.06778	0.06778	0.08371
EN	minpwl	0.15550	0.15550	0.15970	0.17240

LALRNQUHD

Cell Description

Low Enable Latch with active-low reset (RDN) and a single output (Q)
Q = !RDN ? 0 : !EN ? D : pre_Q



Function Table

RDN	EN	D	Q
0	X	X	0
1	0	0	0
1	0	1	1
1	1	X	Q<1>

Cell Size

CellName	Height(um)	Width(um)
LALRNQUHDV0P7	3.360	8.960
LALRNQUHDV1	3.360	8.960
LALRNQUHDV2	3.360	9.520
LALRNQUHDV3	3.360	10.080

Pin Power (uW/MHz)

Pin	V0P7	V1	V2	V3
D	0.00049	0.00049	0.00049	0.00051
EN	0.01304	0.01304	0.01305	0.01298
Q	0.02079	0.02242	0.03047	0.04104
RDN	0.00003	0.00003	0.00003	0.00003

Pin Capacitance (pf)

Pin	V0P7	V1	V2	V3
D	0.00261	0.00260	0.00258	0.00258
EN	0.00394	0.00394	0.00394	0.00399
RDN	0.00348	0.00347	0.00389	0.00397

Max Leakage Power (uW)

V0P7	V1	V2	V3
0.00009283	0.00009566	0.00012680	0.00015509

Delay Table (ns)

Description	V0P7	V1	V2	V3
D→Q_FALL	0.21549	0.22118	0.25772	0.29889
D→Q_RISE	0.14297	0.14412	0.16373	0.18320
EN→Q_FALL	0.27830	0.28380	0.31900	0.35830
EN→Q_RISE	0.18350	0.18480	0.20500	0.22310
RDN→Q_FALL	0.14008	0.14217	0.12068	0.13601
RDN→Q_RISE	0.15724	0.15847	0.17985	0.19827

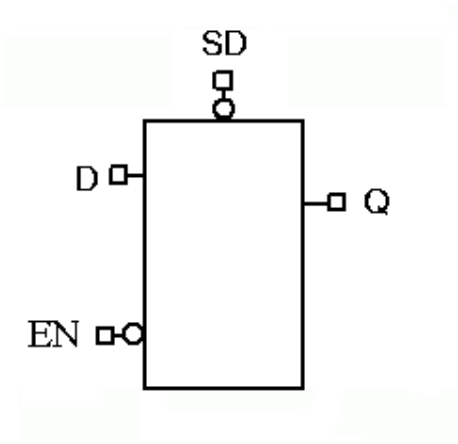
Timing Constraints (ns)

Pin	Requirement	V0P7	V1	V2	V3
D	hold_FALL→EN	-0.12758	-0.13558	-0.16748	-0.20337
D	hold_RISE→EN	-0.08373	-0.08374	-0.10369	-0.11963
D	setup_FALL→EN	0.14755	0.15550	0.19140	0.23124
D	setup_RISE→EN	0.10369	0.10766	0.14755	0.17146
RDN	setup_RISE→EN	0.11563	0.12360	0.16353	0.18741
RDN	hold_RISE→EN	-0.09569	-0.09968	-0.11965	-0.13558
EN	minpwl	0.14710	0.15130	0.19340	0.21450
RDN	minpwl	0.13450	0.13440	0.11760	0.13450

LALSQUHD

Cell Description

LALSQ
Q = SD ? 1 : !EN ? D : pre_Q



Function Table

SD	EN	D	Q
1	X	X	1
0	0	0	0
0	0	1	1
0	1	X	Q<1>

Cell Size

CellName	Height(um)	Width(um)
LALSQUHDV0P7	3.360	8.400
LALSQUHDV1	3.360	8.400
LALSQUHDV2	3.360	9.520
LALSQUHDV3	3.360	10.080

Pin Power (uW/MHz)

Pin	V0P7	V1	V2	V3
D	0.00023	0.00024	0.00024	0.00024
EN	0.01240	0.01241	0.01246	0.01246
Q	0.02226	0.02538	0.03710	0.05157
SD	0.00019	0.00019	0.00020	0.00020

Pin Capacitance (pf)

Pin	V0P7	V1	V2	V3
D	0.00253	0.00253	0.00252	0.00251
EN	0.00400	0.00400	0.00400	0.00400
SD	0.00351	0.00350	0.00358	0.00357

Max Leakage Power (uW)

V0P7	V1	V2	V3
0.00009700	0.00010279	0.00012020	0.00014998

Delay Table (ns)

Description	V0P7	V1	V2	V3
D→Q_FALL	0.31598	0.33503	0.39576	0.46367
D→Q_RISE	0.11697	0.12030	0.13399	0.15407
EN→Q_FALL	0.36560	0.38380	0.44360	0.51030
EN→Q_RISE	0.15780	0.16130	0.17600	0.19620
SD→Q_FALL	0.34924	0.36951	0.43071	0.49879
SD→Q_RISE	0.07936	0.08056	0.08615	0.09726

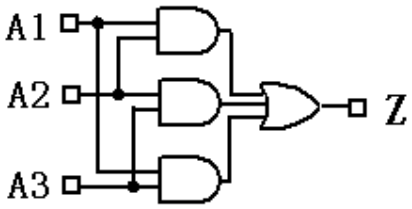
Timing Constraints (ns)

Pin	Requirement	V0P7	V1	V2	V3
D	hold_FALL→EN	-0.23522	-0.25117	-0.30304	-0.35887
D	hold_RISE→EN	-0.05982	-0.05982	-0.07578	-0.09570
D	setup_FALL→EN	0.25916	0.29104	0.36282	0.43858
D	setup_RISE→EN	0.07578	0.07972	0.09173	0.10766
SD	setup_FALL→EN	0.29507	0.32697	0.39477	0.47451
SD	hold_FALL→EN	-0.26717	-0.28313	-0.33894	-0.39477
EN	minpwl	0.11340	0.11760	0.13440	0.15130
SD	minpwh	0.06710	0.07130	0.07550	0.08810

MAJ23UHD

Cell Description

3-input majority gate (2-out-of-3)
Z=(((A1&A2)|(A2&A3)|(A1&A3)))



Function Table

A2	A3	A1	Z
0	0	X	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	X	1

Cell Size

CellName	Height(um)	Width(um)
MAJ23UHDV0P4	3.360	5.040
MAJ23UHDV0P7	3.360	5.040
MAJ23UHDV1	3.360	5.040
MAJ23UHDV2	3.360	6.720
MAJ23UHDV3	3.360	7.280

Pin Power (uW/MHz)

Pin	V0P4	V0P7	V1	V2	V3
A1	0.00889	0.01077	0.01233	0.02229	0.03136
A2	0.00934	0.01130	0.01291	0.02300	0.03220
A3	0.00763	0.00948	0.01111	0.02020	0.02920

Pin Capacitance (pf)

Pin	V0P4	V0P7	V1	V2	V3
A1	0.00460	0.00502	0.00530	0.00785	0.00829
A2	0.00500	0.00533	0.00548	0.00784	0.00831

A3	0.00238	0.00254	0.00255	0.00369	0.00390

Max Leakage Power (uW)

V0P4	V0P7	V1	V2	V3
0.00004544	0.00005319	0.00005635	0.00008149	0.00011225

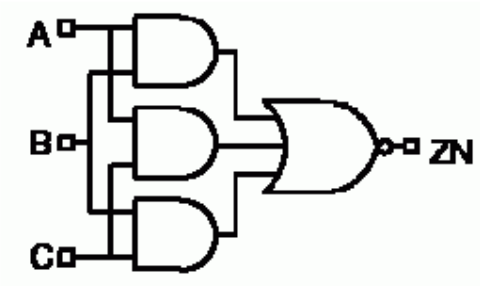
Delay Table (ns)

Description	V0P4	V0P7	V1	V2	V3
A1→Z_FALL	0.16978	0.17314	0.16660	0.16509	0.18481
A1→Z_RISE	0.11975	0.09618	0.09893	0.10914	0.11472
A2→Z_FALL	0.18326	0.18793	0.18584	0.17832	0.19825
A2→Z_RISE	0.12263	0.10037	0.10339	0.10963	0.11507
A3→Z_FALL	0.14320	0.14614	0.14989	0.14163	0.16190
A3→Z_RISE	0.10773	0.09144	0.09411	0.09744	0.10396

MAOI222UHD

Cell Description

Inverting 2 of 3 MAJORITY
ZN=(!((A&B)|(B&C)|(A&C)))



Function Table

A	B	C	ZN
0	0	X	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	X	0

Cell Size

CellName	Height(um)	Width(um)
MAOI222UHDV0P4	3.360	5.600
MAOI222UHDV0P7	3.360	6.160
MAOI222UHDV1	3.360	6.160
MAOI222UHDV2	3.360	10.080
MAOI222UHDV3	3.360	14.560

Pin Power (uW/MHz)

Pin	V0P4	V0P7	V1	V2	V3
A	0.00619	0.00823	0.00956	0.01744	0.02625
B	0.00730	0.01011	0.01178	0.02158	0.03248
C	0.00886	0.01180	0.01386	0.02582	0.03868

Pin Capacitance (pf)

Pin	V0P4	V0P7	V1	V2	V3
A	0.00432	0.00558	0.00662	0.01271	0.01925
B	0.00469	0.00702	0.00828	0.01554	0.02406

C	0.00469	0.00635	0.00761	0.01490	0.02185

Max Leakage Power (uW)

V0P4	V0P7	V1	V2	V3
0.00004011	0.00005186	0.00006082	0.00011675	0.00018423

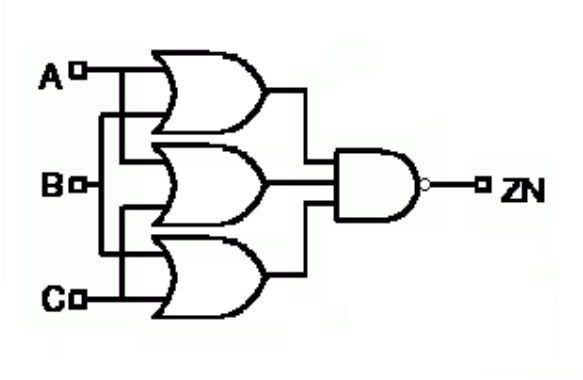
Delay Table (ns)

Description	V0P4	V0P7	V1	V2	V3
A→ZN_FALL	0.07356	0.05481	0.05069	0.06163	0.05397
A→ZN_RISE	0.17799	0.14966	0.13821	0.12254	0.12314
B→ZN_FALL	0.07419	0.05967	0.05469	0.04708	0.04708
B→ZN_RISE	0.19526	0.17232	0.15799	0.14072	0.14109
C→ZN_FALL	0.08484	0.06281	0.05807	0.06489	0.05821
C→ZN_RISE	0.23007	0.18998	0.17661	0.16018	0.16198

MOAI222UHD

Cell Description

MOAI222
ZN=(!((A|B)&(B|C)&(A|C)))



Function Table

A	B	C	ZN
0	0	X	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	X	0

Cell Size

CellName	Height(um)	Width(um)
MOAI222UHDV0P4	3.360	5.600
MOAI222UHDV0P7	3.360	6.160
MOAI222UHDV1	3.360	6.160
MOAI222UHDV2	3.360	10.640
MOAI222UHDV3	3.360	15.120

Pin Power (uW/MHz)

Pin	V0P4	V0P7	V1	V2	V3
A	0.00628	0.00864	0.00952	0.01808	0.02750
B	0.00739	0.01016	0.01116	0.02180	0.03337
C	0.00853	0.01151	0.01286	0.02494	0.03795

Pin Capacitance (pf)

Pin	V0P4	V0P7	V1	V2	V3
A	0.00392	0.00572	0.00618	0.01325	0.01981
B	0.00476	0.00680	0.00763	0.01490	0.02325

C	0.00453	0.00648	0.00734	0.01455	0.02027

Max Leakage Power (uW)

V0P4	V0P7	V1	V2	V3
0.00003454	0.00004733	0.00005595	0.00011096	0.00017280

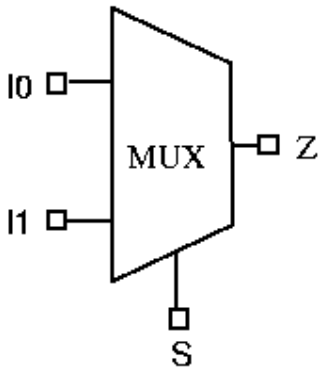
Delay Table (ns)

Description	V0P4	V0P7	V1	V2	V3
A→ZN_FALL	0.08936	0.07063	0.06248	0.05774	0.05755
A→ZN_RISE	0.13855	0.12122	0.13139	0.10812	0.11221
B→ZN_FALL	0.10011	0.07859	0.06939	0.06498	0.06507
B→ZN_RISE	0.16143	0.13903	0.13149	0.13293	0.12697
C→ZN_FALL	0.11070	0.08499	0.07594	0.07057	0.07045
C→ZN_RISE	0.18784	0.15952	0.15715	0.14723	0.15484

MUX2UHD

Cell Description

2-to-1 Multiplexer
Z=((I0&(!S))|(I1&S))



Function Table

S	I0	I1	Z
0	0	X	0
0	1	X	1
1	X	0	0
1	X	1	1

Cell Size

CellName	Height(um)	Width(um)
MUX2UHDV0P4	3.360	5.040
MUX2UHDV0P7	3.360	5.040
MUX2UHDV1	3.360	5.040
MUX2UHDV2	3.360	6.160
MUX2UHDV3	3.360	6.720
MUX2UHDV6	3.360	15.120

Pin Power (uW/MHz)

Pin	V0P4	V0P7	V1	V2	V3	V6
I0	0.00870	0.01078	0.01235	0.02140	0.03143	0.06203
I1	0.00851	0.01077	0.01232	0.02135	0.02955	0.06154
S	0.01142	0.01357	0.01512	0.02478	0.03415	0.06545

Pin Capacitance (pf)

Pin	V0P4	V0P7	V1	V2	V3	V6
I0	0.00267	0.00275	0.00276	0.00406	0.00320	0.00775
I1	0.00240	0.00268	0.00280	0.00395	0.00431	0.00802
S	0.00481	0.00512	0.00514	0.00626	0.00704	0.01216

Max Leakage Power (uW)

V0P4	V0P7	V1	V2	V3	V6
0.00005763	0.00006632	0.00006953	0.00010274	0.00013173	0.00025989

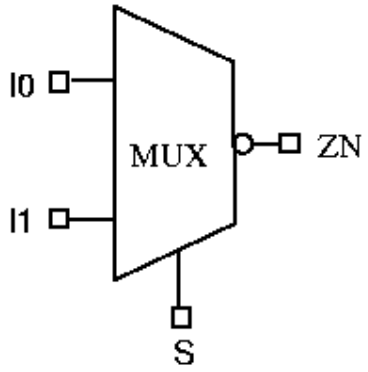
Delay Table (ns)

Description	V0P4	V0P7	V1	V2	V3	V6
I0→Z_FALL	0.16995	0.17310	0.18104	0.17769	0.22780	0.18550
I0→Z_RISE	0.11858	0.11450	0.11642	0.09453	0.10296	0.11048
I1→Z_FALL	0.16510	0.17382	0.17405	0.16088	0.18239	0.18620
I1→Z_RISE	0.11303	0.09240	0.09403	0.09439	0.10512	0.10766
S→Z_FALL	0.15959	0.15856	0.16221	0.15879	0.18219	0.16553
S→Z_RISE	0.13381	0.12360	0.12554	0.11428	0.11835	0.11772

MUX2NUHD

Cell Description

2-to-1 Inverting Multiplexer
ZN=(!((I0&(!S))|(I1&S)))



Function Table

S	I0	I1	ZN
0	0	X	1
0	1	X	0
1	X	0	1
1	X	1	0

Cell Size

CellName	Height(um)	Width(um)
MUX2NUHDV0P4	3.360	4.480
MUX2NUHDV0P7	3.360	4.480
MUX2NUHDV1	3.360	4.480
MUX2NUHDV2	3.360	7.280

Pin Power (uW/MHz)

Pin	V0P4	V0P7	V1	V2
I0	0.00444	0.00626	0.00635	0.00995
I1	0.00431	0.00628	0.00533	0.01081
S	0.00714	0.00979	0.00927	0.01337

Pin Capacitance (pf)

Pin	V0P4	V0P7	V1	V2
I0	0.00234	0.00296	0.00384	0.00742
I1	0.00246	0.00353	0.00257	0.00739
S	0.00488	0.00676	0.00683	0.00884

Max Leakage Power (uW)

V0P4	V0P7	V1	V2
0.00004893	0.00006755	0.00006152	0.00009870

Delay Table (ns)

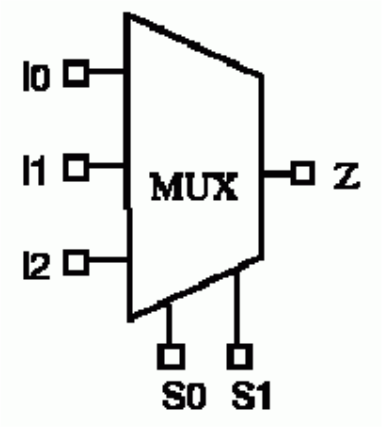
Description	V0P4	V0P7	V1	V2
I0→ZN_FALL	0.05795	0.04602	0.04142	0.04398
I0→ZN_RISE	0.11043	0.11350	0.08357	0.08730
I1→ZN_FALL	0.05792	0.04658	0.05358	0.03815
I1→ZN_RISE	0.11346	0.09977	0.11655	0.09181
S→ZN_FALL	0.07645	0.06173	0.05579	0.04931
S→ZN_RISE	0.10477	0.09237	0.09092	0.07763

MUX3UHD

Cell Description

3-to-1 Multiplexer

Z=((I0&(!S0)&(!S1))|(I1&S0&(!S1))|(I2&S1))



Function Table

S1	S0	I0	I1	I2	Z
0	0	0	X	X	0
0	0	1	X	X	1
0	1	X	0	X	0
0	1	X	1	X	1
1	X	X	X	0	0
1	X	X	X	1	1

Cell Size

CellName	Height(um)	Width(um)
MUX3UHDV0P7	3.360	7.840
MUX3UHDV1	3.360	7.840
MUX3UHDV2	3.360	8.960

Pin Power (uW/MHz)

Pin	V0P7	V1	V2
I0	0.01791	0.01976	0.03146
I1	0.01773	0.01959	0.03161
I2	0.01090	0.01232	0.01985
S0	0.02060	0.02247	0.03429
S1	0.01339	0.01493	0.02417

Pin Capacitance (pf)

Pin	V0P7	V1	V2
I0	0.00295	0.00294	0.00300
I1	0.00253	0.00253	0.00252

I2	0.00308	0.00321	0.00358
S0	0.00522	0.00521	0.00521
S1	0.00525	0.00549	0.00541

Max Leakage Power (uW)

V0P7	V1	V2
0.00011282	0.00011777	0.00014815

Delay Table (ns)

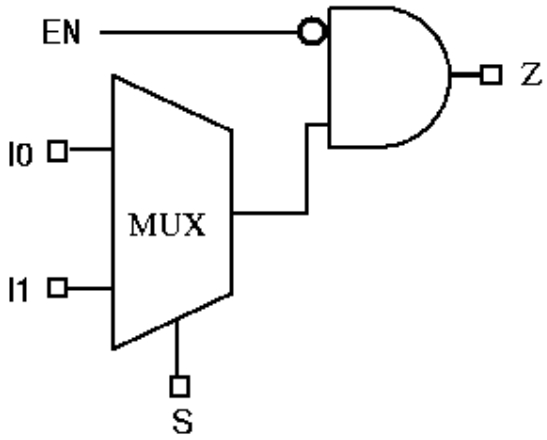
Description	V0P7	V1	V2
I0→Z_FALL	0.28333	0.29252	0.33421
I0→Z_RISE	0.15628	0.15633	0.17695
I1→Z_FALL	0.28047	0.28717	0.33051
I1→Z_RISE	0.17112	0.17163	0.19552
I2→Z_FALL	0.17606	0.17330	0.16314
I2→Z_RISE	0.09328	0.09464	0.11395
S0→Z_FALL	0.26657	0.27430	0.31627
S0→Z_RISE	0.17844	0.17884	0.20083
S1→Z_FALL	0.14907	0.14807	0.15954
S1→Z_RISE	0.10760	0.10555	0.12568

MUXINOR2UHD

Cell Description

MUXINOR2

Z=(((I0&(!S))|(I1&S))&(!EN))



Function Table

EN	S	I0	I1	Z
0	0	0	X	0
0	0	1	X	1
0	1	X	0	0
0	1	X	1	1
1	X	X	X	0

Cell Size

CellName	Height(um)	Width(um)
MUXINOR2UHDV0P7	3.360	6.160
MUXINOR2UHDV1	3.360	6.160
MUXINOR2UHDV2	3.360	8.400

Pin Power (uW/MHz)

Pin	V0P7	V1	V2
EN	0.00443	0.00536	0.01077
I0	0.01159	0.01305	0.02077
I1	0.01166	0.01293	0.02068
S	0.01432	0.01598	0.02367

Pin Capacitance (pf)

Pin	V0P7	V1	V2
EN	0.00338	0.00402	0.00743
I0	0.00263	0.00282	0.00284
I1	0.00312	0.00324	0.00313
S	0.00509	0.00497	0.00508

Max Leakage Power (uW)

V0P7	V1	V2
0.00007820	0.00008677	0.00014696

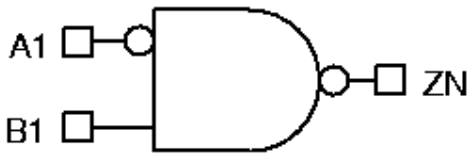
Delay Table (ns)

Description	V0P7	V1	V2
EN→Z_FALL	0.02937	0.02798	0.02408
EN→Z_RISE	0.07496	0.06924	0.06475
I0→Z_FALL	0.17883	0.16904	0.20237
I0→Z_RISE	0.12467	0.12377	0.13118
I1→Z_FALL	0.18930	0.17416	0.20803
I1→Z_RISE	0.12475	0.12244	0.12946
S→Z_FALL	0.16568	0.15807	0.19057
S→Z_RISE	0.14503	0.14540	0.15314

NAND2XBUHD

Cell Description

NAND2XB
ZN=(!((!A1)&B1))



Function Table

A1	B1	ZN
0	0	1
0	1	0
1	X	1

Cell Size

CellName	Height(um)	Width(um)
NAND2XBUHDV0P4	3.360	3.360
NAND2XBUHDV0P7	3.360	3.360
NAND2XBUHDV1	3.360	3.360
NAND2XBUHDV2	3.360	4.480
NAND2XBUHDV4	3.360	8.400
NAND2XBUHDV6	3.360	11.200
NAND2XBUHDV8	3.360	14.000

Pin Power (uW/MHz)

Pin	V0P4	V0P7	V1	V2	V4	V6	V8
A1	0.00703	0.00886	0.01060	0.01944	0.03594	0.05277	0.06951
B1	0.00253	0.00323	0.00398	0.00719	0.01401	0.02073	0.02741

Pin Capacitance (pf)

Pin	V0P4	V0P7	V1	V2	V4	V6	V8
A1	0.00303	0.00322	0.00343	0.00443	0.00641	0.00846	0.00835
B1	0.00231	0.00308	0.00371	0.00694	0.01393	0.02105	0.02800

Max Leakage Power (uW)

V0P4	V0P7	V1	V2	V4	V6	V8
0.00003290	0.00004093	0.00004641	0.00008137	0.00015505	0.00022922	0.00028599

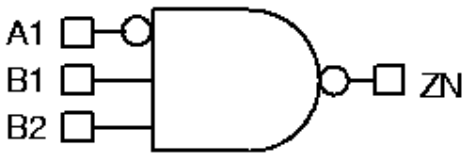
Delay Table (ns)

Description	V0P4	V0P7	V1	V2	V4	V6	V8
A1→ZN_FALL	0.09883	0.09460	0.09032	0.08916	0.09301	0.09522	0.10868
A1→ZN_RISE	0.08770	0.07323	0.07541	0.08062	0.08392	0.07909	0.08856
B1→ZN_FALL	0.04579	0.03650	0.03323	0.02865	0.02771	0.02742	0.02718
B1→ZN_RISE	0.04961	0.04008	0.03801	0.03407	0.03237	0.03182	0.03146

NAND3BUHD

Cell Description

NAND3B
ZN=(!((!A1)&B1&B2))



Function Table

A1	B1	B2	ZN
0	0	X	1
0	1	0	1
0	1	1	0
1	X	X	1

Cell Size

CellName	Height(um)	Width(um)
NAND3BUHDV0P7	3.360	3.920
NAND3BUHDV1	3.360	3.920
NAND3BUHDV2	3.360	6.160

Pin Power (uW/MHz)

Pin	V0P7	V1	V2
A1	0.00982	0.01125	0.01886
B1	0.00540	0.00649	0.01184
B2	0.00618	0.00768	0.01417

Pin Capacitance (pf)

Pin	V0P7	V1	V2
A1	0.00324	0.00339	0.00450
B1	0.00319	0.00372	0.00739
B2	0.00331	0.00392	0.00821

Max Leakage Power (uW)

V0P7	V1	V2
0.00005267	0.00006053	0.00010231

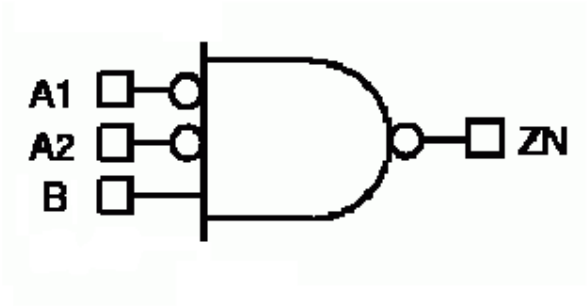
Delay Table (ns)

Description	V0P7	V1	V2
A1→ZN_FALL	0.11542	0.10575	0.09625
A1→ZN_RISE	0.07601	0.07618	0.07636
B1→ZN_FALL	0.05860	0.05230	0.04609
B1→ZN_RISE	0.05288	0.05028	0.04650
B2→ZN_FALL	0.06187	0.05663	0.05080
B2→ZN_RISE	0.05719	0.05579	0.05212

NAND3BBUHD

Cell Description

NAND3BB
ZN=(!((!A1)&(!A2)&B))



Function Table

A1	A2	B	ZN
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

Cell Size

CellName	Height(um)	Width(um)
NAND3BBUHDV0P7	3.360	5.040
NAND3BBUHDV1	3.360	5.040
NAND3BBUHDV2	3.360	8.400

Pin Power (uW/MHz)

Pin	V0P7	V1	V2
A1	0.00970	0.01115	0.01821
A2	0.01033	0.01206	0.02150
B	0.00635	0.00772	0.01542

Pin Capacitance (pf)

Pin	V0P7	V1	V2
A1	0.00311	0.00315	0.00431
A2	0.00315	0.00330	0.00336

B	0.00321	0.00381	0.00736

Max Leakage Power (uW)

V0P7	V1	V2
0.00006933	0.00007724	0.00011853

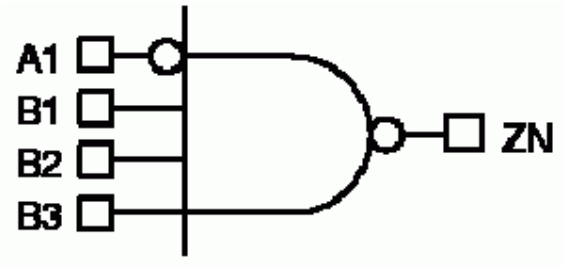
Delay Table (ns)

Description	V0P7	V1	V2
A1→ZN_FALL	0.10922	0.10242	0.09144
A1→ZN_RISE	0.07475	0.07429	0.07343
A2→ZN_FALL	0.11355	0.10834	0.12901
A2→ZN_RISE	0.08049	0.08118	0.09711
B→ZN_FALL	0.06058	0.05749	0.05596
B→ZN_RISE	0.05800	0.05515	0.05206

NAND4BUHD

Cell Description

NAND4B
ZN=(!((!A1)&B1&B2&B3))



Function Table

A1	B1	B2	B3	ZN
0	0	X	X	1
0	1	0	X	1
0	1	1	0	1
0	1	1	1	0
1	X	X	X	1

Cell Size

CellName	Height(um)	Width(um)
NAND4BUHDV0P7	3.360	4.480
NAND4BUHDV1	3.360	4.480
NAND4BUHDV2	3.360	8.400

Pin Power (uW/MHz)

Pin	V0P7	V1	V2
A1	0.01099	0.01237	0.02360
B1	0.00637	0.00756	0.01515
B2	0.00732	0.00865	0.01724
B3	0.00829	0.00977	0.01947

Pin Capacitance (pf)

Pin	V0P7	V1	V2
A1	0.00330	0.00339	0.00428
B1	0.00321	0.00376	0.00824
B2	0.00327	0.00377	0.00764
B3	0.00339	0.00393	0.00699

Max Leakage Power (uW)

V0P7	V1	V2
0.00006365	0.00007462	0.00012858

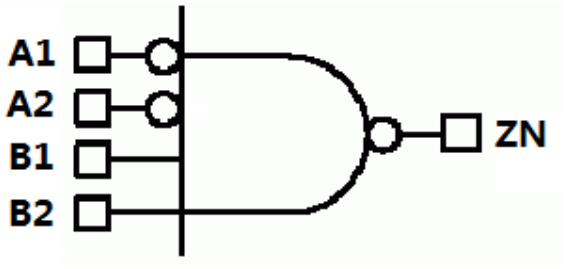
Delay Table (ns)

Description	V0P7	V1	V2
A1→ZN_FALL	0.12826	0.12228	0.12401
A1→ZN_RISE	0.08049	0.08025	0.08597
B1→ZN_FALL	0.06863	0.06903	0.06877
B1→ZN_RISE	0.06062	0.05556	0.05506
B2→ZN_FALL	0.07558	0.07570	0.07423
B2→ZN_RISE	0.06769	0.06149	0.05882
B3→ZN_FALL	0.07949	0.07962	0.07956
B3→ZN_RISE	0.07198	0.06499	0.06342

NAND4XXBBUHD

Cell Description

NAND4XXBB
ZN=(!((!A1)&(!A2)&B1&B2))



Function Table

A1	A2	B1	B2	ZN
0	0	0	0	1
1	0	0	0	1
0	1	0	0	1
1	1	0	0	1
0	0	1	0	1
1	0	1	0	1
0	1	1	0	1
1	1	1	0	1
0	0	0	1	1
1	0	0	1	1
0	1	0	1	1
1	1	0	1	1
0	0	1	1	0
1	0	1	1	1
0	1	1	1	1
1	1	1	1	1

Cell Size

CellName	Height(um)	Width(um)
NAND4XXBBUHDV0P7	3.360	4.480
NAND4XXBBUHDV1	3.360	4.480
NAND4XXBBUHDV2	3.360	7.280
NAND4XXBBUHDV3	3.360	8.960

Pin Power (uW/MHz)

Pin	V0P7	V1	V2	V3

A1	0.01313	0.01492	0.02701	0.03814
A2	0.01225	0.01395	0.02553	0.03635
B1	0.00476	0.00563	0.00979	0.01390
B2	0.00566	0.00670	0.01224	0.01823

Pin Capacitance (pf)

Pin	V0P7	V1	V2	V3
A1	0.00320	0.00334	0.00443	0.00440
A2	0.00312	0.00328	0.00433	0.00428
B1	0.00325	0.00369	0.00672	0.00945
B2	0.00325	0.00376	0.00789	0.00994

Max Leakage Power (uW)

V0P7	V1	V2	V3
0.00007516	0.00008329	0.00013327	0.00016861

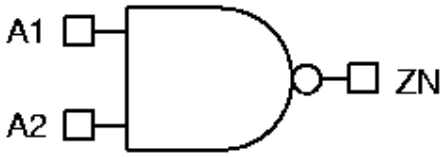
Delay Table (ns)

Description	V0P7	V1	V2	V3
A1→ZN_FALL	0.17927	0.17276	0.16893	0.19070
A1→ZN_RISE	0.09427	0.09269	0.09470	0.10259
A2→ZN_FALL	0.16584	0.16023	0.15724	0.17651
A2→ZN_RISE	0.09079	0.08884	0.09043	0.09754
B1→ZN_FALL	0.04872	0.04803	0.04011	0.03736
B1→ZN_RISE	0.04888	0.04560	0.04162	0.04048
B2→ZN_FALL	0.05267	0.05221	0.04687	0.04489
B2→ZN_RISE	0.05602	0.05240	0.04746	0.05162

NAND2UHD

Cell Description

2-Input NAND
ZN=(!(A1&A2))



Function Table

A1	A2	ZN
0	X	1
1	0	1
1	1	0

Cell Size

CellName	Height(um)	Width(um)
NAND2UHDV0P4	3.360	2.240
NAND2UHDV0P7	3.360	2.240
NAND2UHDV1	3.360	2.240
NAND2UHDV2	3.360	3.920
NAND2UHDV3	3.360	5.040
NAND2UHDV4	3.360	6.720
NAND2UHDV6	3.360	9.520
NAND2UHDV8	3.360	12.320

Pin Power (uW/MHz)

Pin	V0P4	V0P7	V1	V2	V3	V4	V6	V8
A1	0.00242	0.00328	0.00385	0.00732	0.01114	0.01457	0.02207	0.02911
A2	0.00284	0.00420	0.00492	0.00954	0.01429	0.01894	0.02872	0.03798

Pin Capacitance (pf)

Pin	V0P4	V0P7	V1	V2	V3	V4	V6	V8
A1	0.00219	0.00315	0.00366	0.00702	0.01087	0.01414	0.02156	0.02893
A2	0.00218	0.00334	0.00385	0.00786	0.01119	0.01564	0.02352	0.03135

Max Leakage Power (uW)

V0P4	V0P7	V1	V2	V3	V4	V6	V8
0.00001658	0.00002297	0.00002852	0.00005720	0.00008542	0.00011922	0.00018383	0.00024720

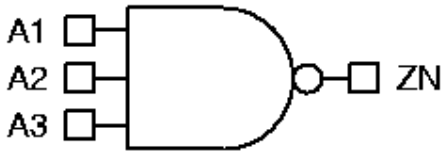
Delay Table (ns)

Description	V0P4	V0P7	V1	V2	V3	V4	V6	V8
A1→ZN_FALL	0.04493	0.03351	0.03282	0.02922	0.02876	0.02768	0.02746	0.02706
A1→ZN_RISE	0.04781	0.04017	0.03744	0.03445	0.03386	0.03324	0.03304	0.03272
A2→ZN_FALL	0.04498	0.03508	0.03450	0.03160	0.03038	0.03013	0.02975	0.02935
A2→ZN_RISE	0.05180	0.04665	0.04352	0.04072	0.04044	0.04007	0.04012	0.03989

NAND3UHD

Cell Description

3-Input NAND
ZN=(!(A1&A2&A3))



Function Table

A1	A2	A3	ZN
0	X	X	1
1	0	X	1
1	1	0	1
1	1	1	0

Cell Size

CellName	Height(um)	Width(um)
NAND3UHDV0P4	3.360	2.800
NAND3UHDV0P7	3.360	3.360
NAND3UHDV1	3.360	3.360
NAND3UHDV2	3.360	5.040

Pin Power (uW/MHz)

Pin	V0P4	V0P7	V1	V2
A1	0.00329	0.00470	0.00559	0.00957
A2	0.00376	0.00560	0.00661	0.01211
A3	0.00417	0.00664	0.00781	0.01520

Pin Capacitance (pf)

Pin	V0P4	V0P7	V1	V2
A1	0.00224	0.00318	0.00366	0.00663
A2	0.00250	0.00324	0.00374	0.00752
A3	0.00221	0.00327	0.00377	0.00723

Max Leakage Power (uW)

V0P4	V0P7	V1	V2
0.00002409	0.00003414	0.00004213	0.00007931

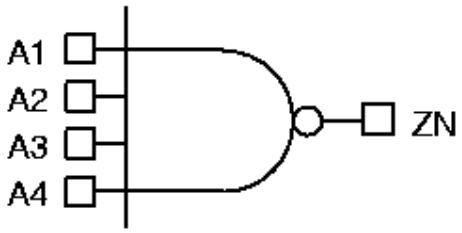
Delay Table (ns)

Description	V0P4	V0P7	V1	V2
A1→ZN_FALL	0.06474	0.04808	0.04767	0.03941
A1→ZN_RISE	0.05595	0.04813	0.04514	0.04127
A2→ZN_FALL	0.06851	0.05213	0.05186	0.04622
A2→ZN_RISE	0.06168	0.05498	0.05155	0.04940
A3→ZN_FALL	0.07032	0.05650	0.05614	0.05214
A3→ZN_RISE	0.06403	0.06070	0.05676	0.05350

NAND4UHD

Cell Description

4-Input NAND
ZN=(!(A1&A2&A3&A4))



Function Table

A1	A2	A3	A4	ZN
0	X	X	X	1
1	0	X	X	1
1	1	0	X	1
1	1	1	0	1
1	1	1	1	0

Cell Size

CellName	Height(um)	Width(um)
NAND4UHDV0P7	3.360	3.360
NAND4UHDV1	3.360	3.920
NAND4UHDV2	3.360	6.720

Pin Power (uW/MHz)

Pin	V0P7	V1	V2
A1	0.00405	0.00632	0.01215
A2	0.00492	0.00736	0.01459
A3	0.00586	0.00857	0.01817
A4	0.00684	0.00973	0.02015

Pin Capacitance (pf)

Pin	V0P7	V1	V2
A1	0.00258	0.00382	0.00661
A2	0.00259	0.00368	0.00745
A3	0.00258	0.00375	0.00791
A4	0.00257	0.00377	0.00761

Max Leakage Power (uW)

V0P7	V1	V2
0.00002842	0.00005562	0.00010597

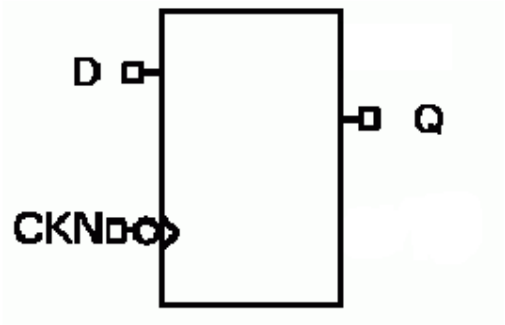
Delay Table (ns)

Description	V0P7	V1	V2
A1→ZN_FALL	0.05212	0.05978	0.05208
A1→ZN_RISE	0.06464	0.04884	0.04752
A2→ZN_FALL	0.05909	0.06626	0.06173
A2→ZN_RISE	0.07684	0.05547	0.05539
A3→ZN_FALL	0.06609	0.07350	0.07410
A3→ZN_RISE	0.08772	0.06138	0.06106
A4→ZN_FALL	0.07089	0.07781	0.07564
A4→ZN_RISE	0.09478	0.06457	0.06467

NDQUHD

Cell Description

Negative Edge Trigger D Flip-Flop
Q = falling (CKN) ? D : pre_Q



Function Table

CKN<1>	CKN	D	Q
0	X	X	Q<1>
1	0	0	0
1	0	1	1
1	1	X	Q<1>

Cell Size

CellName	Height(um)	Width(um)
NDQUHDV0P7	3.360	12.320
NDQUHDV1	3.360	12.320
NDQUHDV2	3.360	12.880
NDQUHDV3	3.360	13.440

Pin Power (uW/MHz)

Pin	V0P7	V1	V2	V3
CKN	0.01483	0.01482	0.01490	0.01505
D	0.00878	0.00878	0.00881	0.00882
Q	0.02569	0.02695	0.03354	0.04150

Pin Capacitance (pf)

Pin	V0P7	V1	V2	V3
CKN	0.00274	0.00255	0.00255	0.00253
D	0.00295	0.00297	0.00295	0.00296

Max Leakage Power (uW)

V0P7	V1	V2	V3
0.00011162	0.00011333	0.00014476	0.00017291

Delay Table (ns)

Description	V0P7	V1	V2	V3
CKN→Q_FALL	0.27340	0.27580	0.27550	0.29050
CKN→Q_RISE	0.32440	0.32510	0.33960	0.35680

Timing Constraints (ns)

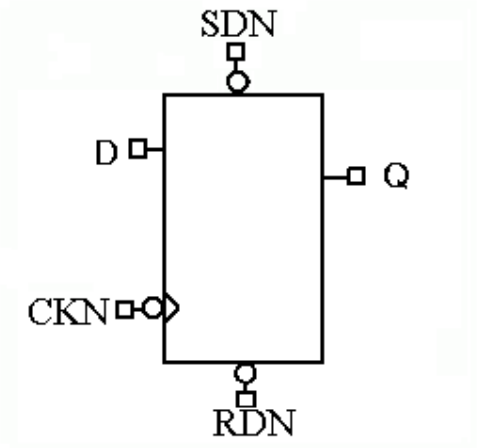
Pin	Requirement	V0P7	V1	V2	V3
D	hold_FALL→CKN	-0.01990	-0.01990	-0.00800	-0.00800
D	hold_RISE→CKN	0.07580	0.07580	0.07580	0.07970
D	setup_FALL→CKN	0.06780	0.06780	0.06780	0.06780
D	setup_RISE→CKN	-0.01200	-0.01200	-0.00800	-0.01200
CKN	minpwh	0.15130	0.16710	0.16970	0.17240
CKN	minpwl	0.20180	0.18920	0.20180	0.21020

NDSRNQUHD

Cell Description

Negative Edge Trigger D Flip-Flop with Async Clear and Set

Q = !RDN ? 0 : !SDN ? 1 : falling (CKN) ? D : pre_Q



Function Table

RDN	SDN	CKN<1>	CKN	D	Q
0	0	X	X	X	0
0	1	X	X	X	0
1	0	X	X	X	1
1	1	0	X	X	Q<1>
1	1	1	0	0	0
1	1	1	0	1	1
1	1	1	1	X	Q<1>

Cell Size

CellName	Height(um)	Width(um)
NDSRNQUHDV1	3.360	15.680
NDSRNQUHDV2	3.360	16.800

Pin Power (uW/MHz)

Pin	V1	V2
CKN	0.01861	0.01884
D	0.00517	0.00517
Q	0.02596	0.03394
RDN	0.00019	0.00019
SDN	0.00207	0.00214

Pin Capacitance (pf)

Pin	V1	V2
CKN	0.00245	0.00245
D	0.00219	0.00220

RDN	0.00698	0.00700
SDN	0.00527	0.00529

Max Leakage Power (uW)

V1	V2
0.00013616	0.00016564

Delay Table (ns)

Description	V1	V2
CKN→Q_FALL	0.30840	0.31600
CKN→Q_RISE	0.32490	0.34320
RDN→Q_FALL	0.14378	0.17110
RDN→Q_RISE	0.08626	0.09653
SDN→Q_RISE	0.29147	0.31048

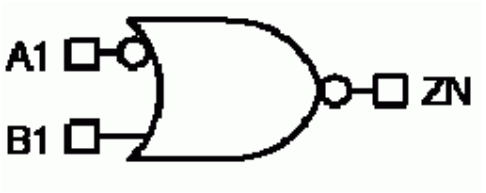
Timing Constraints (ns)

Pin	Requirement	V1	V2
D	hold_FALL→CKN	-0.08770	-0.08770
D	hold_RISE→CKN	0.08380	0.08370
D	setup_FALL→CKN	0.13960	0.13950
D	setup_RISE→CKN	0.03190	0.03190
RDN	setup_RISE→CKN	-0.24723	-0.25120
RDN	hold_RISE→CKN	0.30305	0.30303
SDN	setup_RISE→CKN	-0.03988	-0.03986
SDN	hold_RISE→CKN	0.09573	0.09967
SDN	non_seq_hold_RISE→RDN	-0.00000	-0.00000
SDN	non_seq_setup_RISE→RDN	0.02394	0.01595
CKN	minpwh	0.22240	0.22240
CKN	minpwl	0.17230	0.18500
RDN	minpwl	0.23550	0.23550
SDN	minpwl	0.20600	0.21020

NOR2XBUHD

Cell Description

NOR2XB
ZN=(!((!A1)|B1))



Function Table

A1	B1	ZN
0	X	0
1	0	1
1	1	0

Cell Size

CellName	Height(um)	Width(um)
NOR2XBUHDV0P4	3.360	3.360
NOR2XBUHDV0P7	3.360	3.360
NOR2XBUHDV1	3.360	3.360
NOR2XBUHDV2	3.360	4.480
NOR2XBUHDV3	3.360	6.160
NOR2XBUHDV4	3.360	8.960
NOR2XBUHDV6	3.360	11.760
NOR2XBUHDV8	3.360	15.120

Pin Power (uW/MHz)

Pin	V0P4	V0P7	V1	V2	V3	V4	V6	V8
A1	0.00706	0.00910	0.01071	0.01943	0.02771	0.03716	0.05438	0.07356
B1	0.00241	0.00313	0.00365	0.00619	0.00991	0.01352	0.01940	0.02488

Pin Capacitance (pf)

Pin	V0P4	V0P7	V1	V2	V3	V4	V6	V8
A1	0.00290	0.00312	0.00332	0.00441	0.00467	0.00670	0.00838	0.01239
B1	0.00236	0.00320	0.00370	0.00702	0.01020	0.01366	0.02003	0.02665

Max Leakage Power (uW)

V0P4	V0P7	V1	V2	V3	V4	V6	V8
0.00004053	0.00005126	0.00005942	0.00012610	0.00018946	0.00025837	0.00039225	0.00053171

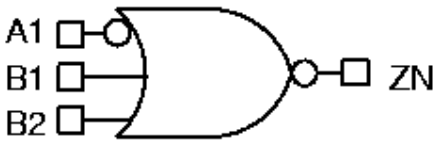
Delay Table (ns)

Description	V0P4	V0P7	V1	V2	V3	V4	V6	V8
A1→ZN_FALL	0.08917	0.08763	0.08579	0.08510	0.09111	0.08541	0.08713	0.08334
A1→ZN_RISE	0.11967	0.09907	0.09685	0.09340	0.10273	0.09427	0.09588	0.09304
B1→ZN_FALL	0.03437	0.02687	0.02495	0.02050	0.02055	0.02055	0.01954	0.01898
B1→ZN_RISE	0.07904	0.06232	0.05598	0.04723	0.04792	0.04656	0.04467	0.04330

NOR3BUHD

Cell Description

NOR3B
ZN=(!((!A1)|B1|B2))



Function Table

A1	B1	B2	ZN
0	X	X	0
1	0	0	1
1	0	1	0
1	1	X	0

Cell Size

CellName	Height(um)	Width(um)
NOR3BUHDV0P7	3.360	3.920
NOR3BUHDV1	3.360	3.920
NOR3BUHDV2	3.360	6.160
NOR3BUHDV3	3.360	8.960
NOR3BUHDV4	3.360	12.320

Pin Power (uW/MHz)

Pin	V0P7	V1	V2	V3	V4
A1	0.00948	0.01091	0.01821	0.02568	0.03223
B1	0.00536	0.00640	0.01191	0.01878	0.02424
B2	0.00663	0.00804	0.01527	0.02422	0.03190

Pin Capacitance (pf)

Pin	V0P7	V1	V2	V3	V4
A1	0.00325	0.00338	0.00437	0.00459	0.00641
B1	0.00327	0.00392	0.00773	0.01084	0.01439
B2	0.00337	0.00390	0.00851	0.01107	0.01463

Max Leakage Power (uW)

V0P7	V1	V2	V3	V4
0.00007595	0.00008888	0.00018787	0.00027890	0.00038291

Delay Table (ns)

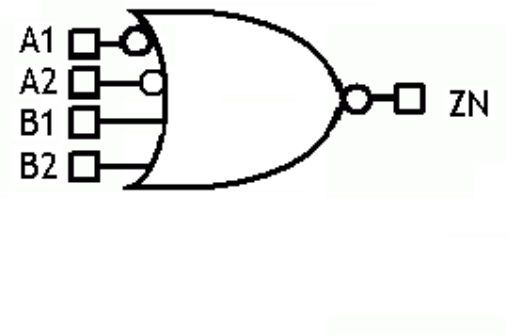
Description	V0P7	V1	V2	V3	V4
A1→ZN_FALL	0.09317	0.08979	0.08181	0.08906	0.08679
A1→ZN_RISE	0.12775	0.12003	0.10978	0.10780	0.09412
B1→ZN_FALL	0.03261	0.03102	0.02756	0.02703	0.02595
B1→ZN_RISE	0.12409	0.11391	0.10415	0.10444	0.09883
B2→ZN_FALL	0.03287	0.03115	0.02832	0.02693	0.02578
B2→ZN_RISE	0.13459	0.12419	0.11667	0.11595	0.11148

NOR4XXBBUHD

Cell Description

NOR4XXBB

ZN=(!((!A1)|(!A2)|B1|B2))



Function Table

A1	A2	B1	B2	ZN
0	0	0	0	0
1	0	0	0	0
0	1	0	0	0
1	1	0	0	1
0	0	1	0	0
1	0	1	0	0
0	1	1	0	0
1	1	1	0	0
0	0	0	1	0
1	0	0	1	0
0	1	0	1	0
1	1	0	1	0
0	0	1	1	0
1	0	1	1	0
0	1	1	1	0
1	1	1	1	0

Cell Size

CellName	Height(um)	Width(um)
NOR4XXBBUHDV0P7	3.360	4.480
NOR4XXBBUHDV1	3.360	4.480
NOR4XXBBUHDV2	3.360	7.280
NOR4XXBBUHDV3	3.360	8.960
NOR4XXBBUHDV4	3.360	13.440

Pin Power (uW/MHz)

Pin	V0P7	V1	V2	V3	V4
A1	0.01213	0.01415	0.02623	0.03712	0.04984
A2	0.01287	0.01488	0.02722	0.03829	0.05158
B1	0.00545	0.00650	0.01204	0.01859	0.02466
B2	0.00417	0.00488	0.00842	0.01244	0.01573

Pin Capacitance (pf)

Pin	V0P7	V1	V2	V3	V4
A1	0.00296	0.00310	0.00405	0.00415	0.00633
A2	0.00304	0.00318	0.00423	0.00437	0.00700
B1	0.00323	0.00391	0.00784	0.01027	0.01363
B2	0.00327	0.00376	0.00695	0.01023	0.01358

Max Leakage Power (uW)

V0P7	V1	V2	V3	V4
0.00008391	0.00009815	0.00020235	0.00029835	0.00038730

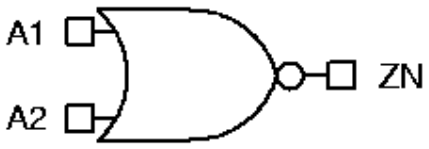
Delay Table (ns)

Description	V0P7	V1	V2	V3	V4
A1→ZN_FALL	0.10059	0.09638	0.09133	0.10134	0.09739
A1→ZN_RISE	0.18099	0.17444	0.17086	0.17804	0.16880
A2→ZN_FALL	0.11213	0.10644	0.09972	0.11085	0.10481
A2→ZN_RISE	0.18346	0.17691	0.17319	0.18070	0.17149
B1→ZN_FALL	0.03332	0.03173	0.02871	0.02738	0.02674
B1→ZN_RISE	0.12498	0.11446	0.10035	0.10189	0.09873
B2→ZN_FALL	0.03085	0.02876	0.02405	0.02352	0.02238
B2→ZN_RISE	0.10152	0.09048	0.07202	0.06934	0.06390

NOR2UHD

Cell Description

2-Input NOR
ZN=(!(A1|A2))



Function Table

A1	A2	ZN
0	0	1
0	1	0
1	X	0

Cell Size

CellName	Height(um)	Width(um)
NOR2UHDV0P4	3.360	2.240
NOR2UHDV0P7	3.360	2.240
NOR2UHDV1	3.360	2.240
NOR2UHDV2	3.360	3.920
NOR2UHDV3	3.360	5.600
NOR2UHDV4	3.360	6.720
NOR2UHDV6	3.360	10.080
NOR2UHDV8	3.360	12.880

Pin Power (uW/MHz)

Pin	V0P4	V0P7	V1	V2	V3	V4	V6	V8
A1	0.00237	0.00314	0.00368	0.00663	0.01034	0.01319	0.01979	0.02617
A2	0.00313	0.00435	0.00522	0.00987	0.01525	0.01951	0.02959	0.03937

Pin Capacitance (pf)

Pin	V0P4	V0P7	V1	V2	V3	V4	V6	V8
A1	0.00230	0.00311	0.00372	0.00706	0.01122	0.01460	0.02214	0.02957
A2	0.00223	0.00318	0.00390	0.00824	0.01152	0.01575	0.02351	0.03104

Max Leakage Power (uW)

V0P4	V0P7	V1	V2	V3	V4	V6	V8
0.00002994	0.00004228	0.00005000	0.00010934	0.00016899	0.00023317	0.00035829	0.00048339

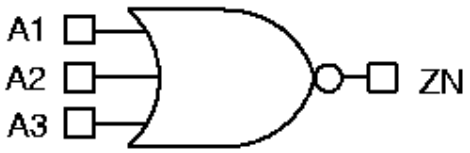
Delay Table (ns)

Description	V0P4	V0P7	V1	V2	V3	V4	V6	V8
A1→ZN_FALL	0.03442	0.02705	0.02512	0.02127	0.02159	0.02020	0.01992	0.01967
A1→ZN_RISE	0.07733	0.06233	0.05631	0.04881	0.04928	0.04766	0.04703	0.04641
A2→ZN_FALL	0.03660	0.02945	0.02795	0.02533	0.02478	0.02391	0.02349	0.02322
A2→ZN_RISE	0.08589	0.07140	0.06564	0.06008	0.06008	0.05944	0.05867	0.05811

NOR3UHD

Cell Description

3-Input NOR
ZN=(!(A1|A2|A3))



Function Table

A1	A2	A3	ZN
0	0	0	1
0	0	1	0
0	1	X	0
1	X	X	0

Cell Size

CellName	Height(um)	Width(um)
NOR3UHDV0P4	3.360	3.360
NOR3UHDV0P7	3.360	2.800
NOR3UHDV1	3.360	3.360
NOR3UHDV2	3.360	5.600
NOR3UHDV3	3.360	7.840
NOR3UHDV4	3.360	10.080

Pin Power (uW/MHz)

Pin	V0P4	V0P7	V1	V2	V3	V4
A1	0.00313	0.00364	0.00490	0.00815	0.01314	0.01630
A2	0.00395	0.00494	0.00652	0.01168	0.01839	0.02329
A3	0.00467	0.00608	0.00818	0.01594	0.02381	0.03145

Pin Capacitance (pf)

Pin	V0P4	V0P7	V1	V2	V3	V4
A1	0.00231	0.00299	0.00381	0.00736	0.01106	0.01487
A2	0.00236	0.00313	0.00382	0.00775	0.01120	0.01530
A3	0.00229	0.00310	0.00397	0.00747	0.01125	0.01473

Max Leakage Power (uW)

V0P4	V0P7	V1	V2	V3	V4
0.00004833	0.00005819	0.00007890	0.00017048	0.00026429	0.00035835

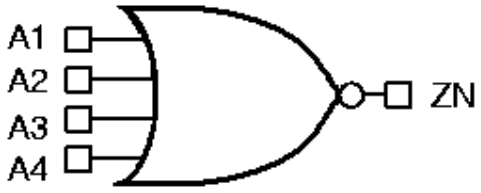
Delay Table (ns)

Description	V0P4	V0P7	V1	V2	V3	V4
A1→ZN_FALL	0.03828	0.03208	0.02888	0.02385	0.02440	0.02299
A1→ZN_RISE	0.12535	0.09049	0.08993	0.07171	0.07426	0.06879
A2→ZN_FALL	0.04136	0.03556	0.03173	0.02808	0.02818	0.02690
A2→ZN_RISE	0.14907	0.11448	0.11375	0.10022	0.10169	0.09620
A3→ZN_FALL	0.04152	0.03589	0.03215	0.02771	0.02787	0.02646
A3→ZN_RISE	0.15626	0.12252	0.12452	0.11431	0.11303	0.10966

NOR4UHD

Cell Description

4-Input NOR
ZN=(!(A1|A2|A3|A4))



Function Table

A1	A2	A3	A4	ZN
0	0	0	0	1
0	0	0	1	0
0	0	1	X	0
0	1	X	X	0
1	X	X	X	0

Cell Size

CellName	Height(um)	Width(um)
NOR4UHDV0P7	3.360	3.360
NOR4UHDV1	3.360	3.920
NOR4UHDV2	3.360	6.720
NOR4UHDV3	3.360	10.080

Pin Power (uW/MHz)

Pin	V0P7	V1	V2	V3
A1	0.00399	0.00538	0.00981	0.01519
A2	0.00529	0.00704	0.01342	0.02083
A3	0.00669	0.00878	0.01855	0.02680
A4	0.00798	0.01035	0.02143	0.03124

Pin Capacitance (pf)

Pin	V0P7	V1	V2	V3
A1	0.00303	0.00378	0.00708	0.01094
A2	0.00306	0.00384	0.00771	0.01125
A3	0.00301	0.00379	0.00790	0.01135

A4	0.00302	0.00383	0.00754	0.01152

Max Leakage Power (uW)

V0P7	V1	V2	V3
0.00008001	0.00010872	0.00023294	0.00035802

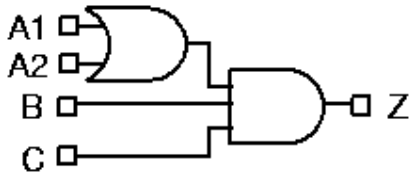
Delay Table (ns)

Description	V0P7	V1	V2	V3
A1→ZN_FALL	0.03349	0.03011	0.02629	0.02642
A1→ZN_RISE	0.11634	0.11613	0.09513	0.09619
A2→ZN_FALL	0.03680	0.03316	0.03053	0.03044
A2→ZN_RISE	0.15512	0.15584	0.14058	0.14336
A3→ZN_FALL	0.03768	0.03364	0.03091	0.03044
A3→ZN_RISE	0.18123	0.18123	0.18119	0.17399
A4→ZN_FALL	0.03668	0.03247	0.02930	0.02920
A4→ZN_RISE	0.19099	0.18931	0.18854	0.18214

OA112UHD

Cell Description

1-1-2 OA
Z=((A1|A2)&B&C)



Function Table

A1	A2	B	C	Z
0	0	X	X	0
0	1	0	X	0
0	1	1	0	0
0	1	1	1	1
1	X	0	X	0
1	X	1	0	0
1	X	1	1	1

Cell Size

CellName	Height(um)	Width(um)
OA112UHDV0P4	3.360	4.480
OA112UHDV0P7	3.360	4.480
OA112UHDV1	3.360	4.480
OA112UHDV2	3.360	5.040
OA112UHDV3	3.360	6.160

Pin Power (uW/MHz)

Pin	V0P4	V0P7	V1	V2	V3
A1	0.00820	0.01040	0.01212	0.01983	0.02914
A2	0.00906	0.01128	0.01313	0.02136	0.03073
B	0.00987	0.01208	0.01370	0.02095	0.02908
C	0.01039	0.01278	0.01440	0.02196	0.03000

Pin Capacitance (pf)

Pin	V0P4	V0P7	V1	V2	V3

A1	0.00236	0.00252	0.00267	0.00377	0.00387
A2	0.00256	0.00273	0.00288	0.00385	0.00392
B	0.00258	0.00282	0.00296	0.00389	0.00403
C	0.00269	0.00292	0.00307	0.00403	0.00425

Max Leakage Power (uW)

V0P4	V0P7	V1	V2	V3
0.00004292	0.00004935	0.00005232	0.00009248	0.00012406

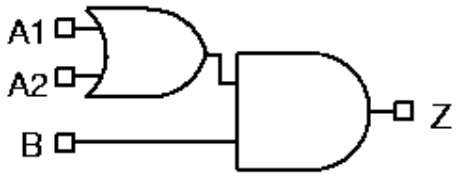
Delay Table (ns)

Description	V0P4	V0P7	V1	V2	V3
A1→Z_FALL	0.15881	0.16323	0.15728	0.14631	0.17360
A1→Z_RISE	0.13570	0.11659	0.12187	0.11491	0.12217
A2→Z_FALL	0.17129	0.17575	0.16943	0.15690	0.18410
A2→Z_RISE	0.14803	0.12591	0.13238	0.12475	0.13069
B→Z_FALL	0.12570	0.12743	0.12026	0.10501	0.12147
B→Z_RISE	0.15597	0.13324	0.13827	0.12589	0.13267
C→Z_FALL	0.13178	0.13514	0.12679	0.10833	0.11920
C→Z_RISE	0.15931	0.13637	0.14141	0.12865	0.13543

OA12UHD

Cell Description

1-2 OA
Z=((A1|A2)&B)



Function Table

A1	A2	B	Z
0	0	X	0
0	1	0	0
0	1	1	1
1	X	0	0
1	X	1	1

Cell Size

CellName	Height(um)	Width(um)
OA12UHDV0P4	3.360	4.480
OA12UHDV0P7	3.360	4.480
OA12UHDV1	3.360	4.480
OA12UHDV2	3.360	4.480
OA12UHDV3	3.360	5.600
OA12UHDV4	3.360	8.960

Pin Power (uW/MHz)

Pin	V0P4	V0P7	V1	V2	V3	V4
A1	0.00727	0.00927	0.01073	0.01756	0.02623	0.03511
A2	0.00807	0.01007	0.01167	0.01917	0.02769	0.03822
B	0.00872	0.01083	0.01219	0.01886	0.02634	0.03761

Pin Capacitance (pf)

Pin	V0P4	V0P7	V1	V2	V3	V4
A1	0.00242	0.00280	0.00293	0.00381	0.00392	0.00702
A2	0.00237	0.00261	0.00274	0.00366	0.00378	0.00776

B	0.00275	0.00300	0.00314	0.00407	0.00420	0.00760

Max Leakage Power (uW)

V0P4	V0P7	V1	V2	V3	V4
0.00004196	0.00005112	0.00005434	0.00007900	0.00010992	0.00016047

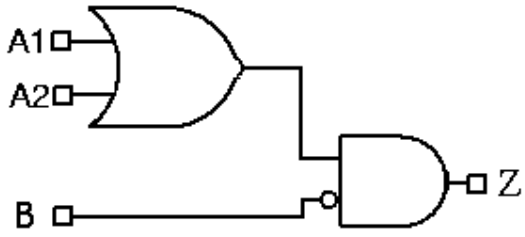
Delay Table (ns)

Description	V0P4	V0P7	V1	V2	V3	V4
A1→Z_FALL	0.14089	0.14574	0.14033	0.13223	0.15919	0.12973
A1→Z_RISE	0.10711	0.08687	0.08895	0.08624	0.09230	0.08367
A2→Z_FALL	0.15063	0.15574	0.15011	0.14279	0.16752	0.14122
A2→Z_RISE	0.11356	0.09245	0.09551	0.09420	0.09857	0.09173
B→Z_FALL	0.11330	0.11676	0.10967	0.09763	0.11353	0.09594
B→Z_RISE	0.11824	0.09607	0.09790	0.09265	0.09762	0.09023

OA21BUHD

Cell Description

OA21B
Z=(A1|A2)&(!B)



Function Table

A1	A2	B	Z
0	0	0	0
1	0	0	1
0	1	0	1
1	1	0	1
0	0	1	0
1	0	1	0
0	1	1	0
1	1	1	0

Cell Size

CellName	Height(um)	Width(um)
OA21BUHDV0P4	3.360	3.920
OA21BUHDV0P7	3.360	3.920
OA21BUHDV1	3.360	3.920
OA21BUHDV2	3.360	5.040
OA21BUHDV3	3.360	6.720

Pin Power (uW/MHz)

Pin	V0P4	V0P7	V1	V2	V3
A1	0.00781	0.01023	0.01143	0.02102	0.03063
A2	0.00859	0.01113	0.01242	0.02202	0.03219
B	0.00247	0.00327	0.00370	0.00631	0.00983

Pin Capacitance (pf)

Pin	V0P4	V0P7	V1	V2	V3

A1	0.00295	0.00303	0.00305	0.00293	0.00420
A2	0.00273	0.00323	0.00325	0.00317	0.00442
B	0.00270	0.00356	0.00382	0.00734	0.01052

Max Leakage Power (uW)

V0P4	V0P7	V1	V2	V3
0.00004659	0.00005493	0.00006076	0.00012018	0.00019084

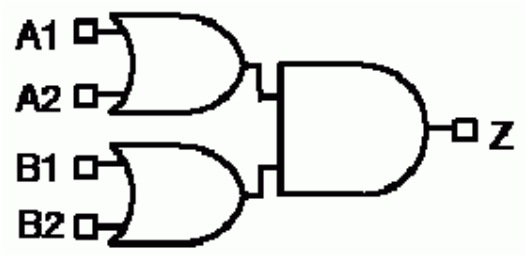
Delay Table (ns)

Description	V0P4	V0P7	V1	V2	V3
A1→Z_FALL	0.12598	0.13968	0.13561	0.18389	0.15170
A1→Z_RISE	0.11393	0.10151	0.09975	0.10851	0.10527
A2→Z_FALL	0.13500	0.15346	0.14912	0.19741	0.16376
A2→Z_RISE	0.11637	0.10510	0.10414	0.11287	0.10956
B→Z_FALL	0.02818	0.02619	0.02507	0.02078	0.02056
B→Z_RISE	0.07781	0.06342	0.05675	0.04794	0.04695

OA22UHD

Cell Description

2-2 OA with Simple Gates
Z=((A1|A2)&(B1|B2))



Function Table

A1	A2	B1	B2	Z
0	0	X	X	0
0	1	0	0	0
0	1	0	1	1
0	1	1	X	1
1	X	0	0	0
1	X	0	1	1
1	X	1	X	1

Cell Size

CellName	Height(um)	Width(um)
OA22UHDV0P4	3.360	5.040
OA22UHDV0P7	3.360	5.040
OA22UHDV1	3.360	5.040
OA22UHDV2	3.360	6.160
OA22UHDV3	3.360	10.080
OA22UHDV4	3.360	10.640
OA22UHDV6	3.360	17.360

Pin Power (uW/MHz)

Pin	V0P4	V0P7	V1	V2	V3	V4	V6
A1	0.00781	0.00971	0.01089	0.01903	0.02979	0.03691	0.05680
A2	0.00869	0.01059	0.01198	0.02064	0.03269	0.04004	0.06265
B1	0.01001	0.01249	0.01360	0.02225	0.03527	0.04270	0.06688
B2	0.01085	0.01335	0.01461	0.02373	0.03828	0.04604	0.07262

Pin Capacitance (pf)

Pin	V0P4	V0P7	V1	V2	V3	V4	V6
A1	0.00257	0.00285	0.00290	0.00390	0.00694	0.00718	0.01412
A2	0.00270	0.00298	0.00309	0.00428	0.00767	0.00793	0.01485
B1	0.00226	0.00255	0.00263	0.00380	0.00680	0.00742	0.01370
B2	0.00235	0.00263	0.00270	0.00379	0.00773	0.00831	0.01433

Max Leakage Power (uW)

V0P4	V0P7	V1	V2	V3	V4	V6
0.00004244	0.00005051	0.00005175	0.00007807	0.00014192	0.00015994	0.00026799

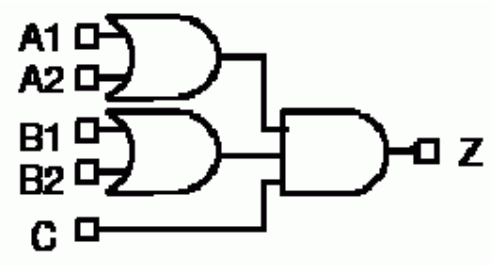
Delay Table (ns)

Description	V0P4	V0P7	V1	V2	V3	V4	V6
A1→Z_FALL	0.15066	0.15360	0.14147	0.14041	0.12450	0.13120	0.11663
A1→Z_RISE	0.10726	0.08705	0.09185	0.08896	0.08326	0.08598	0.08027
A2→Z_FALL	0.16451	0.16723	0.15624	0.15357	0.13630	0.14282	0.12850
A2→Z_RISE	0.11701	0.09384	0.10124	0.09965	0.09119	0.09382	0.08846
B1→Z_FALL	0.19812	0.20848	0.18739	0.17220	0.15888	0.15942	0.14409
B1→Z_RISE	0.12399	0.10098	0.10672	0.10033	0.09343	0.09504	0.08992
B2→Z_FALL	0.20889	0.21939	0.19881	0.18194	0.17163	0.17162	0.15490
B2→Z_RISE	0.13220	0.10680	0.11445	0.10755	0.10157	0.10328	0.09741

OA221UHD

Cell Description

2-2-1 OA
Z=((A1|A2)&(B1|B2)&C)



Function Table

A1	A2	B1	B2	C	Z
0	0	X	X	X	0
0	1	0	0	X	0
0	1	0	1	0	0
0	1	0	1	1	1
0	1	1	X	0	0
0	1	1	X	1	1
1	X	0	0	X	0
1	X	0	1	0	0
1	X	0	1	1	1
1	X	1	X	0	0
1	X	1	X	1	1

Cell Size

CellName	Height(um)	Width(um)
OA221UHDV0P4	3.360	5.600
OA221UHDV0P7	3.360	6.160
OA221UHDV1	3.360	6.160
OA221UHDV2	3.360	6.720
OA221UHDV3	3.360	11.200

Pin Power (uW/MHz)

Pin	V0P4	V0P7	V1	V2	V3
A1	0.01140	0.01531	0.01728	0.02570	0.04043
A2	0.01223	0.01618	0.01829	0.02727	0.04351
B1	0.00965	0.01318	0.01507	0.02266	0.03561
B2	0.01047	0.01402	0.01602	0.02419	0.03827

C	0.00824	0.01075	0.01244	0.01879	0.02922

Pin Capacitance (pf)

Pin	V0P4	V0P7	V1	V2	V3
A1	0.00253	0.00288	0.00299	0.00390	0.00695
A2	0.00249	0.00292	0.00310	0.00401	0.00793
B1	0.00243	0.00258	0.00278	0.00377	0.00641
B2	0.00245	0.00268	0.00285	0.00384	0.00720
C	0.00258	0.00285	0.00298	0.00397	0.00724

Max Leakage Power (uW)

V0P4	V0P7	V1	V2	V3
0.00003958	0.00004453	0.00004907	0.00009225	0.00015254

Delay Table (ns)

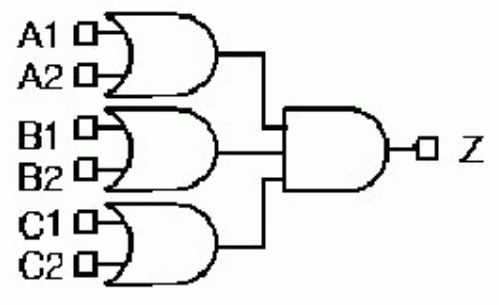
Description	V0P4	V0P7	V1	V2	V3
A1→Z_FALL	0.22225	0.25618	0.24008	0.19892	0.18431
A1→Z_RISE	0.16610	0.14620	0.15075	0.13872	0.12118
A2→Z_FALL	0.23334	0.26832	0.25252	0.21017	0.19712
A2→Z_RISE	0.17770	0.15467	0.16056	0.14899	0.13218
B1→Z_FALL	0.18674	0.21417	0.20311	0.16940	0.16988
B1→Z_RISE	0.15036	0.13453	0.13854	0.12693	0.11175
B2→Z_FALL	0.19710	0.22536	0.21362	0.17925	0.18177
B2→Z_RISE	0.16179	0.14234	0.14717	0.13734	0.12106
C→Z_FALL	0.10144	0.10587	0.10192	0.08773	0.07911
C→Z_RISE	0.13128	0.11487	0.11933	0.11142	0.09711

OA222UHD

Cell Description

2-2-2 OA

Z=((A1|A2)&(B1|B2)&(C1|C2))



Function Table

A1	A2	B1	B2	C1	C2	Z
0	0	X	X	X	X	0
0	1	0	0	X	X	0
0	1	0	1	0	0	0
0	1	0	1	0	1	1
0	1	0	1	1	X	1
0	1	1	X	0	0	0
0	1	1	X	0	1	1
0	1	1	X	1	X	1
1	X	0	0	X	X	0
1	X	0	1	0	0	0
1	X	0	1	0	1	1
1	X	0	1	1	X	1
1	X	1	X	0	0	0
1	X	1	X	0	1	1
1	X	1	X	1	X	1

Cell Size

CellName	Height(um)	Width(um)
OA222UHDV0P4	3.360	6.720
OA222UHDV0P7	3.360	6.720
OA222UHDV1	3.360	6.720
OA222UHDV2	3.360	7.840
OA222UHDV3	3.360	13.440

Pin Power (uW/MHz)

Pin	V0P4	V0P7	V1	V2	V3

A1	0.01030	0.01235	0.01411	0.02326	0.03712
A2	0.00953	0.01156	0.01317	0.02173	0.03415
B1	0.01192	0.01452	0.01611	0.02533	0.04007
B2	0.01274	0.01537	0.01710	0.02689	0.04313
C1	0.01445	0.01745	0.01915	0.02962	0.04878
C2	0.01360	0.01659	0.01815	0.02795	0.04569

Pin Capacitance (pf)

Pin	V0P4	V0P7	V1	V2	V3
A1	0.00241	0.00263	0.00281	0.00381	0.00775
A2	0.00256	0.00276	0.00286	0.00387	0.00690
B1	0.00235	0.00257	0.00268	0.00376	0.00617
B2	0.00248	0.00271	0.00286	0.00382	0.00727
C1	0.00258	0.00279	0.00297	0.00414	0.00757
C2	0.00247	0.00266	0.00286	0.00405	0.00616

Max Leakage Power (uW)

V0P4	V0P7	V1	V2	V3
0.00004608	0.00005260	0.00005477	0.00009412	0.00014409

Delay Table (ns)

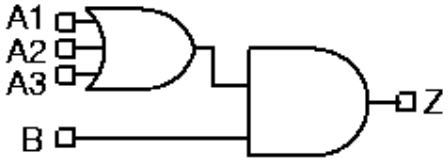
Description	V0P4	V0P7	V1	V2	V3
A1→Z_FALL	0.18012	0.18012	0.17151	0.15718	0.14823
A1→Z_RISE	0.15304	0.12505	0.13212	0.12788	0.12246
A2→Z_FALL	0.17092	0.17076	0.16179	0.14773	0.13642
A2→Z_RISE	0.14335	0.11774	0.12306	0.11806	0.11106
B1→Z_FALL	0.22437	0.23039	0.21179	0.18334	0.17918
B1→Z_RISE	0.17142	0.14181	0.14651	0.13615	0.13037
B2→Z_FALL	0.23540	0.24135	0.22257	0.19297	0.19184
B2→Z_RISE	0.18281	0.15048	0.15665	0.14619	0.13658
C1→Z_FALL	0.27001	0.28047	0.25501	0.21051	0.22390
C1→Z_RISE	0.19737	0.16273	0.16688	0.15629	0.14871
C2→Z_FALL	0.25784	0.26828	0.24316	0.20007	0.21064
C2→Z_RISE	0.18647	0.15455	0.15733	0.14619	0.14302

OA31UHD

Cell Description

3-1 OA

Z=((A1|A2|A3)&B)



Function Table

A1	A2	A3	B	Z
0	0	0	X	0
0	0	1	0	0
0	0	1	1	1
0	1	X	0	0
0	1	X	1	1
1	X	X	0	0
1	X	X	1	1

Cell Size

CellName	Height(um)	Width(um)
OA31UHDV0P4	3.360	4.480
OA31UHDV0P7	3.360	4.480
OA31UHDV1	3.360	4.480
OA31UHDV2	3.360	5.600

Pin Power (uW/MHz)

Pin	V0P4	V0P7	V1	V2
A1	0.00923	0.01107	0.01334	0.02230
A2	0.01011	0.01181	0.01454	0.02420
A3	0.01100	0.01259	0.01549	0.02572
B	0.00761	0.00849	0.01049	0.01695

Pin Capacitance (pf)

Pin	V0P4	V0P7	V1	V2
A1	0.00236	0.00219	0.00289	0.00396

A2	0.00242	0.00228	0.00291	0.00394
A3	0.00241	0.00228	0.00299	0.00408
B	0.00257	0.00246	0.00302	0.00424

Max Leakage Power (uW)

V0P4	V0P7	V1	V2
0.00005107	0.00005420	0.00006693	0.00010102

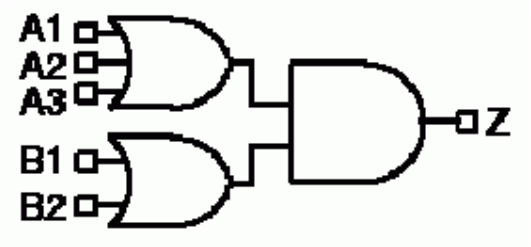
Delay Table (ns)

Description	V0P4	V0P7	V1	V2
A1→Z_FALL	0.24243	0.28158	0.23944	0.21976
A1→Z_RISE	0.11880	0.11117	0.09652	0.08947
A2→Z_FALL	0.26893	0.30818	0.26971	0.24925
A2→Z_RISE	0.12826	0.11854	0.10463	0.09786
A3→Z_FALL	0.28078	0.32050	0.28101	0.25978
A3→Z_RISE	0.13408	0.12294	0.10842	0.10171
B→Z_FALL	0.09520	0.10116	0.08843	0.08038
B→Z_RISE	0.10214	0.09439	0.08330	0.07799

OA32UHD

Cell Description

3-2 OA
Z=((A1|A2|A3)&(B1|B2))



Function Table

A1	A2	A3	B1	B2	Z
0	0	0	X	X	0
0	0	1	0	0	0
0	0	1	0	1	1
0	0	1	1	X	1
0	1	X	0	0	0
0	1	X	0	1	1
0	1	X	1	X	1
1	X	X	0	0	0
1	X	X	0	1	1
1	X	X	1	X	1

Cell Size

CellName	Height(um)	Width(um)
OA32UHDV0P7	3.360	6.160
OA32UHDV1	3.360	6.160
OA32UHDV2	3.360	6.720
OA32UHDV3	3.360	7.280
OA32UHDV4	3.360	11.760

Pin Power (uW/MHz)

Pin	V0P7	V1	V2	V3	V4
A1	0.01109	0.01279	0.02146	0.03267	0.04317
A2	0.01201	0.01410	0.02336	0.03469	0.04667
A3	0.01285	0.01504	0.02508	0.03665	0.04945
B1	0.01334	0.01498	0.02371	0.03351	0.04670
B2	0.01413	0.01597	0.02530	0.03514	0.04937

Pin Capacitance (pf)

Pin	V0P7	V1	V2	V3	V4
A1	0.00283	0.00277	0.00370	0.00379	0.00619
A2	0.00287	0.00298	0.00397	0.00404	0.00691
A3	0.00293	0.00307	0.00408	0.00432	0.00787
B1	0.00276	0.00278	0.00379	0.00406	0.00604
B2	0.00272	0.00277	0.00377	0.00414	0.00715

Max Leakage Power (uW)

V0P7	V1	V2	V3	V4
0.00007332	0.00007636	0.00010547	0.00012660	0.00020160

Delay Table (ns)

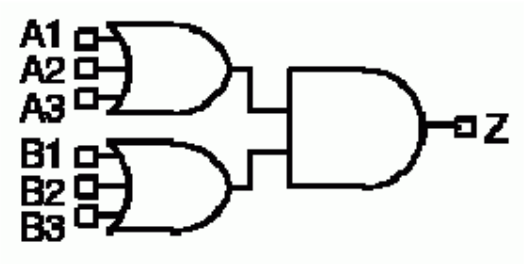
Description	V0P7	V1	V2	V3	V4
A1→Z_FALL	0.22431	0.20957	0.19534	0.23643	0.21458
A1→Z_RISE	0.09097	0.09257	0.09136	0.09784	0.09311
A2→Z_FALL	0.25295	0.24616	0.22785	0.26929	0.24954
A2→Z_RISE	0.09757	0.10213	0.10126	0.10690	0.10253
A3→Z_FALL	0.26343	0.25483	0.23871	0.28161	0.26445
A3→Z_RISE	0.10104	0.10547	0.10623	0.11224	0.10836
B1→Z_FALL	0.22054	0.20441	0.17957	0.20155	0.20071
B1→Z_RISE	0.10194	0.10394	0.10144	0.10736	0.10304
B2→Z_FALL	0.23028	0.21542	0.18996	0.21130	0.21372
B2→Z_RISE	0.10687	0.11023	0.10867	0.11405	0.11030

OA33UHD

Cell Description

3-3 OA

Z=((A1|A2|A3)&(B1|B2|B3))



Function Table

A1	A2	A3	B1	B2	B3	Z
0	0	0	X	X	X	0
0	0	1	0	0	0	0
0	0	1	0	0	1	1
0	0	1	0	1	X	1
0	0	1	1	X	X	1
0	1	X	0	0	0	0
0	1	X	0	0	1	1
0	1	X	0	1	X	1
0	1	X	1	X	X	1
1	X	X	0	0	0	0
1	X	X	0	0	1	1
1	X	X	0	1	X	1
1	X	X	1	X	X	1

Cell Size

CellName	Height(um)	Width(um)
OA33UHDV0P7	3.360	6.160
OA33UHDV1	3.360	6.160
OA33UHDV2	3.360	6.720
OA33UHDV3	3.360	7.840
OA33UHDV4	3.360	13.440

Pin Power (uW/MHz)

Pin	V0P7	V1	V2	V3	V4
A1	0.01181	0.01399	0.02265	0.03358	0.04468
A2	0.01286	0.01520	0.02449	0.03545	0.04816

A3	0.01364	0.01620	0.02615	0.03738	0.05095
B1	0.01523	0.01736	0.02738	0.03945	0.05392
B2	0.01617	0.01852	0.02927	0.04148	0.05727
B3	0.01710	0.01949	0.03077	0.04337	0.05999

Pin Capacitance (pf)

Pin	V0P7	V1	V2	V3	V4
A1	0.00276	0.00285	0.00376	0.00383	0.00630
A2	0.00294	0.00294	0.00379	0.00389	0.00699
A3	0.00290	0.00297	0.00390	0.00409	0.00791
B1	0.00272	0.00295	0.00383	0.00392	0.00651
B2	0.00284	0.00290	0.00390	0.00416	0.00680
B3	0.00281	0.00303	0.00399	0.00422	0.00765

Max Leakage Power (uW)

V0P7	V1	V2	V3	V4
0.00007569	0.00007813	0.00010780	0.00012973	0.00020334

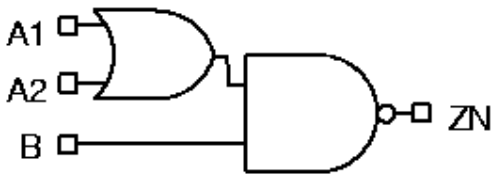
Delay Table (ns)

Description	V0P7	V1	V2	V3	V4
A1→Z_FALL	0.22934	0.22282	0.19930	0.23622	0.21689
A1→Z_RISE	0.09126	0.09559	0.09199	0.09641	0.09252
A2→Z_FALL	0.26341	0.25590	0.22910	0.26532	0.25196
A2→Z_RISE	0.09799	0.10395	0.10077	0.10427	0.10147
A3→Z_FALL	0.27125	0.26604	0.23948	0.27668	0.26693
A3→Z_RISE	0.10047	0.10761	0.10544	0.10929	0.10694
B1→Z_FALL	0.32817	0.30658	0.26609	0.30475	0.28947
B1→Z_RISE	0.10638	0.11011	0.10499	0.10937	0.10695
B2→Z_FALL	0.35790	0.33677	0.29635	0.33528	0.32105
B2→Z_RISE	0.11274	0.11739	0.11353	0.11745	0.11500
B3→Z_FALL	0.36874	0.34890	0.30637	0.34768	0.33566
B3→Z_RISE	0.11563	0.12130	0.11751	0.12179	0.12007

OAI21UHD

Cell Description

2-1 OAI provides the logical inverted AND of one OR group and an additional input.
ZN=(!((A1|A2)&B))



Function Table

A1	A2	B	ZN
0	0	X	1
0	1	0	1
0	1	1	0
1	X	0	1
1	X	1	0

Cell Size

CellName	Height(um)	Width(um)
OAI21UHDV0P4	3.360	2.800
OAI21UHDV0P7	3.360	3.360
OAI21UHDV1	3.360	3.360
OAI21UHDV2	3.360	5.600
OAI21UHDV3	3.360	7.840
OAI21UHDV4	3.360	10.080
OAI21UHDV6	3.360	13.440

Pin Power (uW/MHz)

Pin	V0P4	V0P7	V1	V2	V3	V4	V6
A1	0.00384	0.00516	0.00618	0.01146	0.01692	0.02240	0.03241
A2	0.00465	0.00641	0.00776	0.01486	0.02207	0.02973	0.04296
B	0.00269	0.00369	0.00444	0.00804	0.01195	0.01558	0.02289

Pin Capacitance (pf)

Pin	V0P4	V0P7	V1	V2	V3	V4	V6
A1	0.00230	0.00330	0.00402	0.00717	0.01130	0.01491	0.02253

A2	0.00222	0.00330	0.00397	0.00831	0.01166	0.01596	0.02420
B	0.00233	0.00326	0.00387	0.00708	0.00978	0.01217	0.01758

Max Leakage Power (uW)

V0P4	V0P7	V1	V2	V3	V4	V6
0.00002649	0.00003740	0.00004427	0.00009589	0.00014861	0.00020160	0.00030561

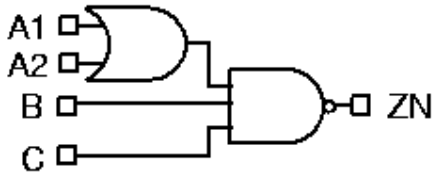
Delay Table (ns)

Description	V0P4	V0P7	V1	V2	V3	V4	V6
A1→ZN_FALL	0.05548	0.04330	0.04097	0.03645	0.03482	0.03405	0.03372
A1→ZN_RISE	0.10998	0.09176	0.08519	0.07653	0.07519	0.07493	0.07159
A2→ZN_FALL	0.06180	0.04845	0.04610	0.04237	0.03995	0.03946	0.03939
A2→ZN_RISE	0.12034	0.10169	0.09486	0.08846	0.08701	0.08848	0.08439
B→ZN_FALL	0.04462	0.03523	0.03333	0.02889	0.02697	0.02567	0.02638
B→ZN_RISE	0.04871	0.04083	0.03817	0.03545	0.03883	0.03956	0.03703

OAI211UHD

Cell Description

2-1-1 OAI provides the logical inverted AND of one OR group and two additional inputs.
ZN=(!((A1|A2)&B&C))



Function Table

A1	A2	B	C	ZN
0	0	X	X	1
0	1	0	X	1
0	1	1	0	1
0	1	1	1	0
1	X	0	X	1
1	X	1	0	1
1	X	1	1	0

Cell Size

CellName	Height(um)	Width(um)
OAI211UHDV0P4	3.360	3.360
OAI211UHDV0P7	3.360	3.920
OAI211UHDV1	3.360	3.360
OAI211UHDV2	3.360	6.720
OAI211UHDV3	3.360	8.960

Pin Power (uW/MHz)

Pin	V0P4	V0P7	V1	V2	V3
A1	0.00515	0.00690	0.00895	0.01567	0.02235
A2	0.00589	0.00815	0.01049	0.01928	0.02773
B	0.00350	0.00441	0.00623	0.00978	0.01402
C	0.00393	0.00527	0.00729	0.01234	0.01773

Pin Capacitance (pf)

Pin	V0P4	V0P7	V1	V2	V3

A1	0.00215	0.00327	0.00383	0.00713	0.01128
A2	0.00210	0.00326	0.00397	0.00825	0.01199
B	0.00230	0.00283	0.00389	0.00666	0.00816
C	0.00229	0.00282	0.00389	0.00709	0.00939

Max Leakage Power (uW)

V0P4	V0P7	V1	V2	V3
0.00002472	0.00003777	0.00004496	0.00009681	0.00014870

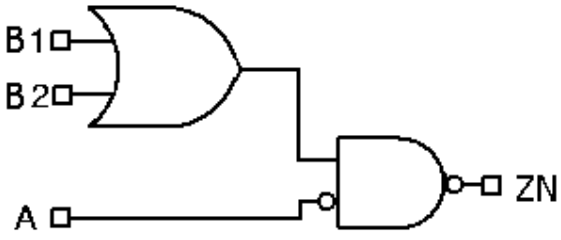
Delay Table (ns)

Description	V0P4	V0P7	V1	V2	V3
A1→ZN_FALL	0.08295	0.06250	0.06272	0.05238	0.05042
A1→ZN_RISE	0.13662	0.11213	0.11081	0.09845	0.09380
A2→ZN_FALL	0.09096	0.07132	0.07052	0.06094	0.05832
A2→ZN_RISE	0.14547	0.12173	0.12033	0.11124	0.10546
B→ZN_FALL	0.06537	0.04724	0.04987	0.03771	0.03631
B→ZN_RISE	0.05677	0.05879	0.04600	0.04612	0.05887
C→ZN_FALL	0.06794	0.05107	0.05378	0.04376	0.04174
C→ZN_RISE	0.06215	0.06912	0.05289	0.05653	0.06003

OAI21BUHD

Cell Description

OAI21B
ZN=!((B1|B2)&!A)



Function Table

B1	B2	A	ZN
0	0	0	1
1	0	0	0
0	1	0	0
1	1	0	0
0	0	1	1
1	0	1	1
0	1	1	1
1	1	1	1

Cell Size

CellName	Height(um)	Width(um)
OAI21BUHDV0P4	3.360	4.480
OAI21BUHDV0P7	3.360	4.480
OAI21BUHDV1	3.360	4.480
OAI21BUHDV2	3.360	6.720

Pin Power (uW/MHz)

Pin	V0P4	V0P7	V1	V2
A	0.00743	0.00898	0.01036	0.01723
B1	0.00426	0.00531	0.00635	0.01160
B2	0.00502	0.00653	0.00791	0.01497

Pin Capacitance (pf)

Pin	V0P4	V0P7	V1	V2
A	0.00298	0.00298	0.00313	0.00412

B1	0.00260	0.00319	0.00381	0.00723
B2	0.00260	0.00322	0.00389	0.00796

Max Leakage Power (uW)

V0P4	V0P7	V1	V2
0.00004844	0.00005401	0.00006091	0.00011463

Delay Table (ns)

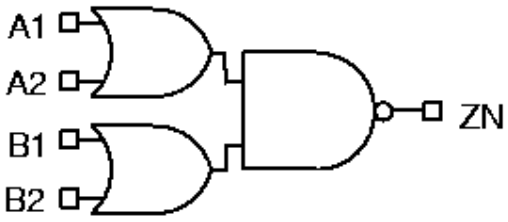
Description	V0P4	V0P7	V1	V2
A→ZN_FALL	0.09261	0.09648	0.09233	0.08252
A→ZN_RISE	0.07694	0.07001	0.06976	0.06846
B1→ZN_FALL	0.04811	0.04607	0.04356	0.03917
B1→ZN_RISE	0.12129	0.09395	0.08665	0.07649
B2→ZN_FALL	0.05150	0.05094	0.04872	0.04514
B2→ZN_RISE	0.12920	0.10233	0.09528	0.08846

OAI22UHD

Cell Description

2-2 OAI provides the logical inverted AND of two OR groups.

ZN=(!((A1|A2)&(B1|B2)))



Function Table

A1	A2	B1	B2	ZN
0	0	X	X	1
0	1	0	0	1
0	1	0	1	0
0	1	1	X	0
1	X	0	0	1
1	X	0	1	0
1	X	1	X	0

Cell Size

CellName	Height(um)	Width(um)
OAI22UHDV0P4	3.360	3.360
OAI22UHDV0P7	3.360	3.920
OAI22UHDV1	3.360	3.920
OAI22UHDV2	3.360	7.280
OAI22UHDV3	3.360	10.080
OAI22UHDV4	3.360	13.440
OAI22UHDV6	3.360	19.040

Pin Power (uW/MHz)

Pin	V0P4	V0P7	V1	V2	V3	V4	V6
A1	0.00515	0.00696	0.00827	0.01568	0.02342	0.03097	0.04607
A2	0.00595	0.00823	0.00990	0.01873	0.02785	0.03827	0.05672
B1	0.00328	0.00435	0.00521	0.00989	0.01504	0.01989	0.02991
B2	0.00417	0.00565	0.00668	0.01263	0.01965	0.02628	0.03935

Pin Capacitance (pf)

Pin	V0P4	V0P7	V1	V2	V3	V4	V6
A1	0.00236	0.00343	0.00399	0.00767	0.01163	0.01409	0.02123
A2	0.00237	0.00329	0.00391	0.00808	0.01086	0.01639	0.02388
B1	0.00223	0.00313	0.00361	0.00654	0.01032	0.01364	0.02048
B2	0.00244	0.00326	0.00376	0.00750	0.01124	0.01579	0.02355

Max Leakage Power (uW)

V0P4	V0P7	V1	V2	V3	V4	V6
0.00003216	0.00004754	0.00005594	0.00012359	0.00018304	0.00026048	0.00039543

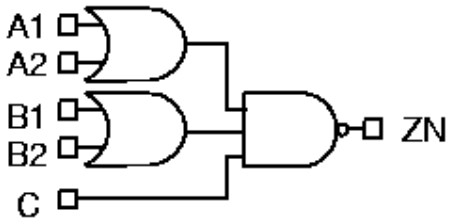
Delay Table (ns)

Description	V0P4	V0P7	V1	V2	V3	V4	V6
A1→ZN_FALL	0.06485	0.04989	0.04679	0.04194	0.04171	0.03979	0.03927
A1→ZN_RISE	0.13204	0.11157	0.10241	0.09837	0.10246	0.09895	0.09842
A2→ZN_FALL	0.07084	0.05458	0.05179	0.04649	0.04562	0.04512	0.04423
A2→ZN_RISE	0.14232	0.12130	0.11243	0.10898	0.11405	0.11277	0.11176
B1→ZN_FALL	0.04926	0.03802	0.03595	0.03115	0.03199	0.03005	0.02987
B1→ZN_RISE	0.09049	0.07252	0.07215	0.07194	0.06655	0.06661	0.06606
B2→ZN_FALL	0.05913	0.04323	0.04053	0.03586	0.03649	0.03460	0.03430
B2→ZN_RISE	0.10368	0.08392	0.08327	0.08386	0.07850	0.07957	0.07867

OAI221UHD

Cell Description

2-2-1 OAI provides the logical inverted AND of two OR groups and an additional input.
ZN=(!((A1|A2)&(B1|B2)&C))



Function Table

A1	A2	B1	B2	C	ZN
0	0	X	X	X	1
0	1	0	0	X	1
0	1	0	1	0	1
0	1	0	1	1	0
0	1	1	X	0	1
0	1	1	X	1	0
1	X	0	0	X	1
1	X	0	1	0	1
1	X	0	1	1	0
1	X	1	X	0	1
1	X	1	X	1	0

Cell Size

CellName	Height(um)	Width(um)
OAI221UHDV0P4	3.360	5.040
OAI221UHDV0P7	3.360	5.040
OAI221UHDV1	3.360	5.600
OAI221UHDV2	3.360	8.960
OAI221UHDV3	3.360	12.320
OAI221UHDV4	3.360	17.360

Pin Power (uW/MHz)

Pin	V0P4	V0P7	V1	V2	V3	V4
A1	0.00822	0.00905	0.01142	0.02104	0.03153	0.04426
A2	0.00898	0.01031	0.01299	0.02437	0.03628	0.05034
B1	0.00620	0.00665	0.00862	0.01543	0.02301	0.03300

B2	0.00709	0.00785	0.01008	0.01869	0.02744	0.03982
C	0.00523	0.00512	0.00669	0.01156	0.01760	0.02613

Pin Capacitance (pf)

Pin	V0P4	V0P7	V1	V2	V3	V4
A1	0.00229	0.00322	0.00386	0.00650	0.01050	0.01554
A2	0.00221	0.00327	0.00397	0.00816	0.01191	0.01612
B1	0.00227	0.00316	0.00371	0.00737	0.01094	0.01542
B2	0.00224	0.00314	0.00397	0.00779	0.01101	0.01620
C	0.00234	0.00289	0.00382	0.00709	0.01057	0.01475

Max Leakage Power (uW)

V0P4	V0P7	V1	V2	V3	V4
0.00002959	0.00003822	0.00004657	0.00010437	0.00017023	0.00020977

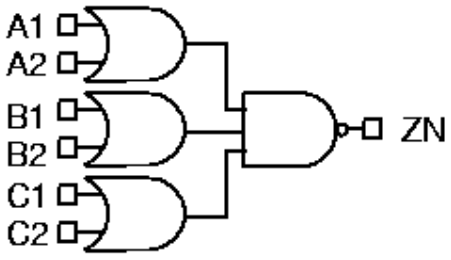
Delay Table (ns)

Description	V0P4	V0P7	V1	V2	V3	V4
A1→ZN_FALL	0.11437	0.07610	0.07306	0.06307	0.06150	0.06507
A1→ZN_RISE	0.18699	0.13587	0.13127	0.13789	0.12972	0.12634
A2→ZN_FALL	0.12340	0.08383	0.08086	0.07048	0.06828	0.07131
A2→ZN_RISE	0.19696	0.14547	0.14130	0.14988	0.14016	0.13567
B1→ZN_FALL	0.09584	0.06219	0.06208	0.05174	0.04891	0.05367
B1→ZN_RISE	0.14842	0.10490	0.11288	0.10237	0.10469	0.09412
B2→ZN_FALL	0.10652	0.07415	0.06839	0.05904	0.05546	0.06164
B2→ZN_RISE	0.16187	0.11494	0.12444	0.11648	0.11923	0.10677
C→ZN_FALL	0.08027	0.05005	0.04898	0.03942	0.03881	0.04261
C→ZN_RISE	0.06825	0.06099	0.04879	0.04139	0.04138	0.04164

OAI222UHD

Cell Description

2-2-2 OAI
ZN=(!((A1|A2)&(B1|B2)&(C1|C2)))



Function Table

A1	A2	B1	B2	C1	C2	ZN
0	0	X	X	X	X	1
0	1	0	0	X	X	1
0	1	0	1	0	0	1
0	1	0	1	0	1	0
0	1	0	1	1	X	0
0	1	1	X	0	0	1
0	1	1	X	0	1	0
0	1	1	X	1	X	0
1	X	0	0	X	X	1
1	X	0	1	0	0	1
1	X	0	1	0	1	0
1	X	0	1	1	X	0
1	X	1	X	0	0	1
1	X	1	X	0	1	0
1	X	1	X	1	X	0

Cell Size

CellName	Height(um)	Width(um)
OAI222UHDV0P4	3.360	5.600
OAI222UHDV0P7	3.360	5.600
OAI222UHDV1	3.360	6.160
OAI222UHDV2	3.360	10.640
OAI222UHDV3	3.360	15.120

Pin Power (uW/MHz)

Pin	V0P4	V0P7	V1	V2	V3

A1	0.00852	0.01038	0.01303	0.02535	0.03886
A2	0.00918	0.01150	0.01443	0.02850	0.04343
B1	0.00684	0.00851	0.01080	0.01958	0.03047
B2	0.00762	0.00983	0.01217	0.02266	0.03483
C1	0.00463	0.00595	0.00760	0.01370	0.02193
C2	0.00564	0.00715	0.00904	0.01639	0.02627

Pin Capacitance (pf)

Pin	V0P4	V0P7	V1	V2	V3
A1	0.00235	0.00294	0.00332	0.00684	0.01106
A2	0.00230	0.00291	0.00335	0.00803	0.01136
B1	0.00222	0.00309	0.00365	0.00668	0.01045
B2	0.00236	0.00310	0.00375	0.00774	0.01121
C1	0.00228	0.00282	0.00367	0.00659	0.01082
C2	0.00223	0.00295	0.00366	0.00770	0.01068

Max Leakage Power (uW)

V0P4	V0P7	V1	V2	V3
0.00003724	0.00003938	0.00005891	0.00011775	0.00018669

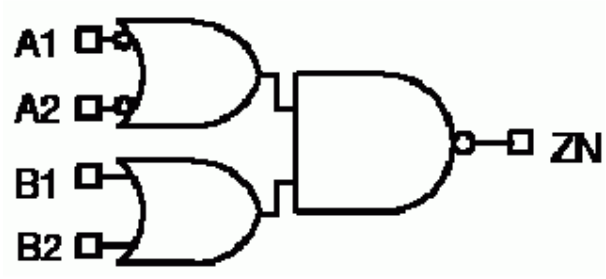
Delay Table (ns)

Description	V0P4	V0P7	V1	V2	V3
A1→ZN_FALL	0.11390	0.10190	0.09751	0.06988	0.07131
A1→ZN_RISE	0.18990	0.14259	0.14143	0.14988	0.14565
A2→ZN_FALL	0.11981	0.11010	0.10520	0.07678	0.07791
A2→ZN_RISE	0.19563	0.15027	0.14898	0.16101	0.15715
B1→ZN_FALL	0.09783	0.08807	0.07727	0.05780	0.05959
B1→ZN_RISE	0.15803	0.12297	0.13371	0.12560	0.12523
B2→ZN_FALL	0.10677	0.09861	0.08677	0.06438	0.06582
B2→ZN_RISE	0.16875	0.13421	0.14352	0.13838	0.13585
C1→ZN_FALL	0.07104	0.06632	0.05540	0.04372	0.04555
C1→ZN_RISE	0.10481	0.08433	0.09124	0.08365	0.08243
C2→ZN_FALL	0.08179	0.07717	0.06490	0.04915	0.05161
C2→ZN_RISE	0.11873	0.09476	0.10173	0.09562	0.09407

OAI22BBUHD

Cell Description

OAI22BB
ZN=(!(((!A1)|(!A2))&(B1|B2)))



Function Table

B1	B2	A1	A2	ZN
0	0	X	X	1
0	1	0	X	0
0	1	1	0	0
0	1	1	1	1
1	X	0	X	0
1	X	1	0	0
1	X	1	1	1

Cell Size

CellName	Height(um)	Width(um)
OAI22BBUHDV0P4	3.360	5.040
OAI22BBUHDV0P7	3.360	5.040
OAI22BBUHDV1	3.360	5.040
OAI22BBUHDV2	3.360	7.280

Pin Power (uW/MHz)

Pin	V0P4	V0P7	V1	V2
A1	0.00755	0.00940	0.01083	0.01858
A2	0.00794	0.01001	0.01144	0.01944
B1	0.00404	0.00514	0.00628	0.01188
B2	0.00480	0.00635	0.00785	0.01531

Pin Capacitance (pf)

Pin	V0P4	V0P7	V1	V2
A1	0.00272	0.00297	0.00309	0.00419

A2	0.00237	0.00263	0.00280	0.00387
B1	0.00233	0.00297	0.00382	0.00740
B2	0.00234	0.00302	0.00388	0.00802

Max Leakage Power (uW)

V0P4	V0P7	V1	V2
0.00004419	0.00005078	0.00006304	0.00011715

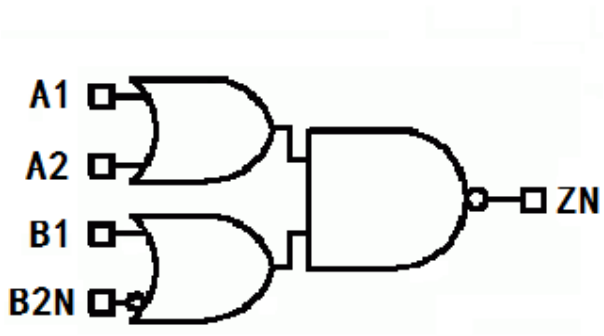
Delay Table (ns)

Description	V0P4	V0P7	V1	V2
A1→ZN_FALL	0.10763	0.10527	0.09831	0.09072
A1→ZN_RISE	0.10721	0.08845	0.08965	0.09330
A2→ZN_FALL	0.11083	0.11106	0.10309	0.09461
A2→ZN_RISE	0.10649	0.08861	0.08983	0.09382
B1→ZN_FALL	0.05995	0.05060	0.04284	0.03875
B1→ZN_RISE	0.11567	0.09158	0.08594	0.07849
B2→ZN_FALL	0.06509	0.05631	0.04802	0.04436
B2→ZN_RISE	0.12357	0.09998	0.09491	0.09052

OAI22XBUHD

Cell Description

OAI22XB
Function ZN= (!((!B2N)|B1)&(A1|A2)))



Function Table

B2N	B1	A1	A2	ZN
0	0	0	0	1
1	0	0	0	1
0	1	0	0	1
1	1	0	0	1
0	0	1	0	0
1	0	1	0	1
0	1	1	0	0
1	1	1	0	0
0	0	0	1	0
1	0	0	1	1
0	1	0	1	0
1	1	0	1	0
0	0	1	1	0
1	0	1	1	1
0	1	1	1	0
1	1	1	1	0

Cell Size

CellName	Height(um)	Width(um)
OAI22XBUHDV0P4	3.360	5.040
OAI22XBUHDV0P7	3.360	5.600
OAI22XBUHDV1	3.360	5.600
OAI22XBUHDV2	3.360	8.400
OAI22XBUHDV4	3.360	15.120

Pin Power (uW/MHz)

Pin	V0P4	V0P7	V1	V2	V4
A1	0.00510	0.00627	0.00794	0.01568	0.03054
A2	0.00581	0.00748	0.00964	0.01889	0.03700
B1	0.00291	0.00395	0.00495	0.01016	0.01959
B2N	0.00690	0.00902	0.01116	0.02219	0.04274

Pin Capacitance (pf)

Pin	V0P4	V0P7	V1	V2	V4
A1	0.00218	0.00305	0.00380	0.00713	0.01490
A2	0.00206	0.00300	0.00388	0.00812	0.01621
B1	0.00202	0.00291	0.00366	0.00678	0.01351
B2N	0.00201	0.00203	0.00234	0.00360	0.00690

Max Leakage Power (uW)

V0P4	V0P7	V1	V2	V4
0.00004330	0.00005120	0.00006299	0.00013102	0.00026985

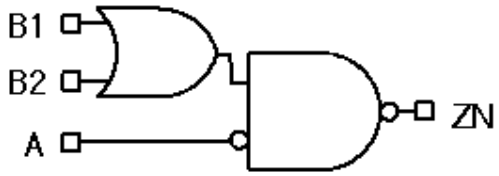
Delay Table (ns)

Description	V0P4	V0P7	V1	V2	V4
A1→ZN_FALL	0.06309	0.05140	0.04652	0.04350	0.04147
A1→ZN_RISE	0.15920	0.11254	0.10190	0.09657	0.09297
A2→ZN_FALL	0.06744	0.05651	0.05177	0.04894	0.04667
A2→ZN_RISE	0.16964	0.12335	0.11259	0.10809	0.10445
B1→ZN_FALL	0.04439	0.03875	0.03498	0.03295	0.03107
B1→ZN_RISE	0.09772	0.07388	0.06695	0.06455	0.06573
B2N→ZN_FALL	0.12032	0.11923	0.10556	0.10107	0.09592
B2N→ZN_RISE	0.13736	0.11623	0.11151	0.11272	0.11159

OAI2XB1UHD

Cell Description

OAI2XB1
ZN=(!((B1|B2)&(!A)))



Function Table

A	B1	B2	ZN
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

Cell Size

CellName	Height(um)	Width(um)
OAI2XB1UHDV0P4	3.360	4.480
OAI2XB1UHDV0P7	3.360	4.480
OAI2XB1UHDV1	3.360	4.480
OAI2XB1UHDV2	3.360	6.720
OAI2XB1UHDV4	3.360	11.760

Pin Power (uW/MHz)

Pin	V0P4	V0P7	V1	V2	V4
A	0.00255	0.00336	0.00444	0.00802	0.01614
B1	0.00368	0.00470	0.00611	0.01157	0.02301
B2	0.00764	0.00978	0.01253	0.02418	0.04660

Pin Capacitance (pf)

Pin	V0P4	V0P7	V1	V2	V4

A	0.00202	0.00286	0.00368	0.00677	0.01387
B1	0.00203	0.00291	0.00375	0.00704	0.01439
B2	0.00200	0.00203	0.00234	0.00359	0.00685

Max Leakage Power (uW)

V0P4	V0P7	V1	V2	V4
0.00003329	0.00004088	0.00005151	0.00010778	0.00022477

Delay Table (ns)

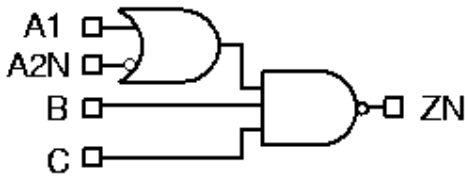
Description	V0P4	V0P7	V1	V2	V4
A→ZN_FALL	0.04224	0.03593	0.03328	0.02885	0.02624
A→ZN_RISE	0.05438	0.04181	0.03783	0.03476	0.03426
B1→ZN_FALL	0.05330	0.04392	0.04050	0.03671	0.03439
B1→ZN_RISE	0.12679	0.09348	0.08391	0.07667	0.07635
B2→ZN_FALL	0.12805	0.12341	0.11207	0.10610	0.09916
B2→ZN_RISE	0.16614	0.13678	0.12974	0.12646	0.12246

OAI2XB11UHD

Cell Description

OAI2XB11

Function ZN= (!((A1|!A2N)&B&C))



Function Table

A1	A2N	B	C	ZN
0	0	0	0	1
1	0	0	0	1
0	1	0	0	1
1	1	0	0	1
0	0	1	0	1
1	0	1	0	1
0	1	1	0	1
1	1	1	0	1
0	0	0	1	1
1	0	0	1	1
0	1	0	1	1
1	1	0	1	1
0	0	1	1	0
1	0	1	1	0
0	1	1	1	1
1	1	1	1	0

Cell Size

CellName	Height(um)	Width(um)
OAI2XB11UHDV0P4	3.360	5.040
OAI2XB11UHDV0P7	3.360	5.040
OAI2XB11UHDV1	3.360	5.040
OAI2XB11UHDV2	3.360	7.840

Pin Power (uW/MHz)

Pin	V0P4	V0P7	V1	V2

A1	0.00511	0.00665	0.00864	0.01658
A2N	0.00903	0.01169	0.01499	0.02900
B	0.00400	0.00537	0.00701	0.01322
C	0.00353	0.00459	0.00592	0.01083

Pin Capacitance (pf)

Pin	V0P4	V0P7	V1	V2
A1	0.00207	0.00296	0.00383	0.00719
A2N	0.00200	0.00203	0.00234	0.00360
B	0.00212	0.00300	0.00389	0.00819
C	0.00216	0.00299	0.00384	0.00716

Max Leakage Power (uW)

V0P4	V0P7	V1	V2
0.00003359	0.00004241	0.00005365	0.00010825

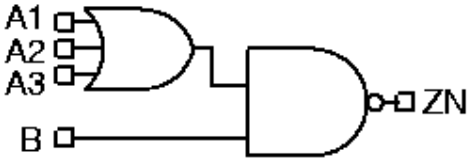
Delay Table (ns)

Description	V0P4	V0P7	V1	V2
A1→ZN_FALL	0.08002	0.06646	0.06114	0.05575
A1→ZN_RISE	0.15947	0.12000	0.10780	0.10049
A2N→ZN_FALL	0.15626	0.14755	0.13452	0.12701
A2N→ZN_RISE	0.19781	0.16264	0.15315	0.14971
B→ZN_FALL	0.06727	0.05687	0.05236	0.04742
B→ZN_RISE	0.07315	0.05700	0.05152	0.04735
C→ZN_FALL	0.06401	0.05299	0.04827	0.04179
C→ZN_RISE	0.06581	0.04982	0.04451	0.04182

OAI31UHD

Cell Description

3-1 OAI
ZN=(!((A1|A2|A3)&B))



Function Table

A1	A2	A3	B	ZN
0	0	0	X	1
0	0	1	0	1
0	0	1	1	0
0	1	X	0	1
0	1	X	1	0
1	X	X	0	1
1	X	X	1	0

Cell Size

CellName	Height(um)	Width(um)
OAI31UHDV0P4	3.360	3.360
OAI31UHDV0P7	3.360	3.920
OAI31UHDV1	3.360	3.920
OAI31UHDV2	3.360	7.280
OAI31UHDV3	3.360	9.520

Pin Power (uW/MHz)

Pin	V0P4	V0P7	V1	V2	V3
A1	0.00417	0.00545	0.00660	0.01257	0.01864
A2	0.00495	0.00673	0.00826	0.01610	0.02503
A3	0.00582	0.00805	0.00991	0.01936	0.03047
B	0.00292	0.00414	0.00495	0.00884	0.01414

Pin Capacitance (pf)

Pin	V0P4	V0P7	V1	V2	V3

A1	0.00253	0.00331	0.00388	0.00633	0.01059
A2	0.00225	0.00325	0.00393	0.00773	0.01070
A3	0.00211	0.00319	0.00390	0.00852	0.01108
B	0.00231	0.00340	0.00407	0.00747	0.01104

Max Leakage Power (uW)

V0P4	V0P7	V1	V2	V3
0.00004166	0.00005776	0.00006824	0.00014666	0.00022438

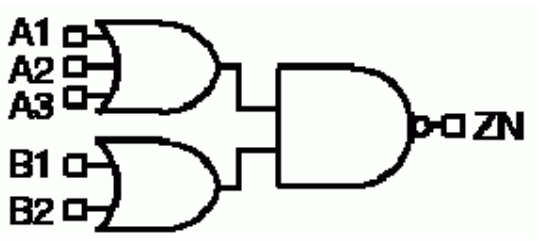
Delay Table (ns)

Description	V0P4	V0P7	V1	V2	V3
A1→ZN_FALL	0.05149	0.04529	0.04304	0.03766	0.03734
A1→ZN_RISE	0.16842	0.13503	0.12526	0.13266	0.10945
A2→ZN_FALL	0.06439	0.05014	0.04828	0.04280	0.04344
A2→ZN_RISE	0.18825	0.15717	0.14813	0.16228	0.14188
A3→ZN_FALL	0.06870	0.05132	0.04949	0.04365	0.04377
A3→ZN_RISE	0.19932	0.16734	0.15815	0.17519	0.15356
B→ZN_FALL	0.04324	0.03526	0.03330	0.02715	0.02781
B→ZN_RISE	0.04832	0.04149	0.03837	0.03553	0.03512

OAI32UHD

Cell Description

3-2 OAI
ZN=(!((A1|A2|A3)&(B1|B2)))



Function Table

A1	A2	A3	B1	B2	ZN
0	0	0	X	X	1
0	0	1	0	0	1
0	0	1	0	1	0
0	0	1	1	X	0
0	1	X	0	0	1
0	1	X	0	1	0
0	1	X	1	X	0
1	X	X	0	0	1
1	X	X	0	1	0
1	X	X	1	X	0

Cell Size

CellName	Height(um)	Width(um)
OAI32UHDV0P4	3.360	4.480
OAI32UHDV0P7	3.360	4.480
OAI32UHDV1	3.360	4.480
OAI32UHDV2	3.360	8.400
OAI32UHDV3	3.360	11.760

Pin Power (uW/MHz)

Pin	V0P4	V0P7	V1	V2	V3
A1	0.00540	0.00734	0.00855	0.01682	0.02434
A2	0.00625	0.00862	0.01018	0.01999	0.03057
A3	0.00701	0.00993	0.01182	0.02348	0.03601
B1	0.00334	0.00478	0.00554	0.01108	0.01640
B2	0.00412	0.00615	0.00716	0.01420	0.02159

Pin Capacitance (pf)

Pin	V0P4	V0P7	V1	V2	V3
A1	0.00220	0.00329	0.00390	0.00641	0.01040
A2	0.00225	0.00333	0.00389	0.00781	0.01064
A3	0.00227	0.00325	0.00388	0.00858	0.01098
B1	0.00241	0.00330	0.00374	0.00692	0.01039
B2	0.00243	0.00335	0.00387	0.00811	0.01083

Max Leakage Power (uW)

V0P4	V0P7	V1	V2	V3
0.00004411	0.00005985	0.00007089	0.00015038	0.00022927

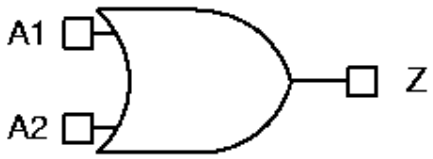
Delay Table (ns)

Description	V0P4	V0P7	V1	V2	V3
A1→ZN_FALL	0.06375	0.05133	0.04778	0.04416	0.04265
A1→ZN_RISE	0.19820	0.16459	0.14848	0.16257	0.13173
A2→ZN_FALL	0.07001	0.05650	0.05300	0.04915	0.04887
A2→ZN_RISE	0.22306	0.18845	0.17214	0.18828	0.16391
A3→ZN_FALL	0.07222	0.05798	0.05439	0.05038	0.04966
A3→ZN_RISE	0.23190	0.19834	0.18205	0.20148	0.17555
B1→ZN_FALL	0.04644	0.03812	0.03531	0.03253	0.03151
B1→ZN_RISE	0.08861	0.07379	0.06903	0.06753	0.05978
B2→ZN_FALL	0.05159	0.04323	0.04018	0.03745	0.03643
B2→ZN_RISE	0.09910	0.08595	0.08098	0.07971	0.07323

OR2UHD

Cell Description

2-Input OR
Z=(A1|A2)



Function Table

A1	A2	Z
0	0	0
0	1	1
1	X	1

Cell Size

CellName	Height(um)	Width(um)
OR2UHDV0P4	3.360	3.360
OR2UHDV0P7	3.360	2.800
OR2UHDV1	3.360	3.360
OR2UHDV2	3.360	3.920
OR2UHDV3	3.360	4.480
OR2UHDV4	3.360	6.720
OR2UHDV6	3.360	8.400
OR2UHDV8	3.360	11.200

Pin Power (uW/MHz)

Pin	V0P4	V0P7	V1	V2	V3	V4	V6	V8
A1	0.00630	0.00820	0.00952	0.01628	0.02462	0.03254	0.04714	0.06329
A2	0.00710	0.00907	0.01050	0.01772	0.02626	0.03515	0.05011	0.06835

Pin Capacitance (pf)

Pin	V0P4	V0P7	V1	V2	V3	V4	V6	V8
A1	0.00242	0.00265	0.00279	0.00369	0.00410	0.00629	0.00742	0.01219
A2	0.00256	0.00286	0.00295	0.00394	0.00430	0.00713	0.00802	0.01240

Max Leakage Power (uW)

V0P4	V0P7	V1	V2	V3	V4	V6	V8
0.00004052	0.00004647	0.00005240	0.00007756	0.00009828	0.00014975	0.00020266	0.00028692

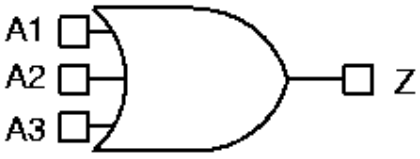
Delay Table (ns)

Description	V0P4	V0P7	V1	V2	V3	V4	V6	V8
A1→Z_FALL	0.12985	0.13072	0.12593	0.12652	0.14145	0.13048	0.14489	0.12960
A1→Z_RISE	0.07674	0.06536	0.06608	0.06405	0.07028	0.06399	0.06395	0.06316
A2→Z_FALL	0.14308	0.14440	0.13865	0.13870	0.15286	0.14374	0.15656	0.14173
A2→Z_RISE	0.08189	0.06964	0.07057	0.06847	0.07454	0.06917	0.06830	0.06763

OR3UHD

Cell Description

3-Input OR
Z=(A1|A2|A3)



Function Table

A1	A2	A3	Z
0	0	0	0
0	0	1	1
0	1	X	1
1	X	X	1

Cell Size

CellName	Height(um)	Width(um)
OR3UHDV0P7	3.360	3.920
OR3UHDV1	3.360	3.920
OR3UHDV2	3.360	4.480
OR3UHDV3	3.360	5.040
OR3UHDV4	3.360	8.400

Pin Power (uW/MHz)

Pin	V0P7	V1	V2	V3	V4
A1	0.00950	0.01084	0.01908	0.02963	0.03776
A2	0.01038	0.01181	0.02077	0.03158	0.04184
A3	0.01120	0.01290	0.02231	0.03335	0.04455

Pin Capacitance (pf)

Pin	V0P7	V1	V2	V3	V4
A1	0.00278	0.00286	0.00373	0.00401	0.00557
A2	0.00277	0.00286	0.00354	0.00395	0.00569
A3	0.00280	0.00299	0.00380	0.00423	0.00596

Max Leakage Power (uW)

V0P7	V1	V2	V3	V4
0.00007031	0.00007330	0.00010458	0.00012652	0.00019322

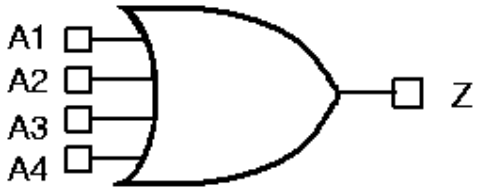
Delay Table (ns)

Description	V0P7	V1	V2	V3	V4
A1→Z_FALL	0.19360	0.18257	0.18219	0.20676	0.19243
A1→Z_RISE	0.06985	0.06996	0.06736	0.07420	0.06718
A2→Z_FALL	0.22039	0.20776	0.21186	0.23642	0.23989
A2→Z_RISE	0.07353	0.07385	0.07210	0.07920	0.07414
A3→Z_FALL	0.22754	0.21894	0.22418	0.24811	0.25267
A3→Z_RISE	0.07422	0.07551	0.07410	0.08154	0.07542

OR4UHD

Cell Description

4-Input OR
Z=(A1|A2|A3|A4)



Function Table

A1	A2	A3	A4	Z
0	0	0	0	0
0	0	0	1	1
0	0	1	X	1
0	1	X	X	1
1	X	X	X	1

Cell Size

CellName	Height(um)	Width(um)
OR4UHDV0P7	3.360	4.480
OR4UHDV1	3.360	4.480
OR4UHDV2	3.360	5.040

Pin Power (uW/MHz)

Pin	V0P7	V1	V2
A1	0.01035	0.01231	0.02238
A2	0.01127	0.01337	0.02390
A3	0.01215	0.01445	0.02551
A4	0.01316	0.01565	0.02683

Pin Capacitance (pf)

Pin	V0P7	V1	V2
A1	0.00263	0.00270	0.00369
A2	0.00261	0.00275	0.00367
A3	0.00254	0.00283	0.00377
A4	0.00277	0.00289	0.00389

Max Leakage Power (uW)

V0P7	V1	V2
0.00009117	0.00009418	0.00014263

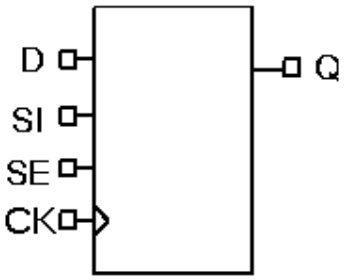
Delay Table (ns)

Description	V0P7	V1	V2
A1→Z_FALL	0.24164	0.23611	0.24325
A1→Z_RISE	0.07051	0.07237	0.06615
A2→Z_FALL	0.28627	0.28145	0.28557
A2→Z_RISE	0.07438	0.07723	0.06986
A3→Z_FALL	0.31011	0.30901	0.31340
A3→Z_RISE	0.07551	0.07945	0.07175
A4→Z_FALL	0.32483	0.32089	0.32382
A4→Z_RISE	0.07589	0.07909	0.07164

SDQUHD

Cell Description

A positive edge-triggered, static D-type flip-flop with scan input (SI) and active-high scan enable (SE). The cell has a single output (Q).
Q = rising (CK) ? (SE&SI | !SE&D) : pre_Q



Function Table

CK<1>	CK	SE	D	SI	Q
0	0	X	X	X	Q<1>
0	1	0	0	X	0
0	1	0	1	X	1
0	1	1	X	0	0
0	1	1	X	1	1
1	X	X	X	X	Q<1>

Cell Size

CellName	Height(um)	Width(um)
SDQUHDV0P7	3.360	16.800
SDQUHDV1	3.360	16.800
SDQUHDV2	3.360	17.360
SDQUHDV3	3.360	17.920

Pin Power (uW/MHz)

Pin	V0P7	V1	V2	V3
CK	0.01661	0.01661	0.01663	0.01665
D	0.00544	0.00540	0.00545	0.00543
Q	0.01926	0.02047	0.02762	0.03726
SE	0.01161	0.01156	0.01161	0.01159
SI	0.00677	0.00673	0.00678	0.00675

Pin Capacitance (pf)

Pin	V0P7	V1	V2	V3
CK	0.00253	0.00253	0.00253	0.00254

D	0.00329	0.00327	0.00328	0.00328
SE	0.00735	0.00736	0.00736	0.00735
SI	0.00300	0.00300	0.00300	0.00300

Max Leakage Power (uW)

V0P7	V1	V2	V3
0.00014386	0.00014650	0.00017489	0.00020433

Delay Table (ns)

Description	V0P7	V1	V2	V3
CK→Q_FALL	0.16870	0.17120	0.18790	0.21250
CK→Q_RISE	0.25970	0.25900	0.26800	0.28360

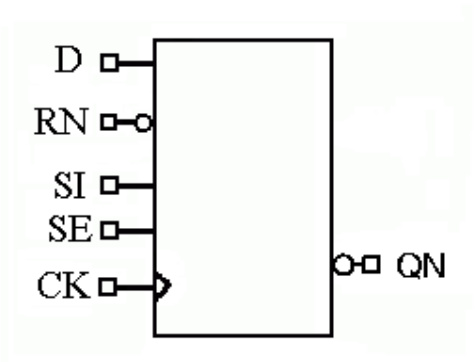
Timing Constraints (ns)

Pin	Requirement	V0P7	V1	V2	V3
D	hold_FALL→CK	-0.11560	-0.11560	-0.11560	-0.11560
D	hold_RISE→CK	-0.07980	-0.07580	-0.07980	-0.07980
D	setup_FALL→CK	0.23530	0.23130	0.23530	0.23130
D	setup_RISE→CK	0.09170	0.09180	0.09170	0.09170
SE	hold_FALL→CK	-0.11560	-0.11160	-0.11560	-0.11560
SE	hold_RISE→CK	-0.07970	-0.07970	-0.07970	-0.07970
SE	setup_FALL→CK	0.23920	0.23530	0.23930	0.23530
SE	setup_RISE→CK	0.09970	0.09570	0.09970	0.09570
SI	hold_FALL→CK	-0.15150	-0.15150	-0.15550	-0.15550
SI	hold_RISE→CK	-0.09570	-0.09570	-0.09570	-0.09570
SI	setup_FALL→CK	0.28710	0.28310	0.28710	0.28310
SI	setup_RISE→CK	0.11560	0.11570	0.11560	0.11560
CK	minpwh	0.10070	0.10070	0.10070	0.10500
CK	minpwl	0.28030	0.27770	0.28030	0.27760

SDGRNQNUHD

Cell Description

Scan D Flip-Flop with Sync Clear with a single output (QN)
QN = rising (CK) ? !(SE&SI | !SE&(D&RN)) : pre_QN



Function Table

CK<1>	CK	D	SE	RN	SI	QN
0	0	X	X	X	X	QN<1>
0	1	0	0	X	X	1
0	1	0	1	X	0	1
0	1	0	1	X	1	0
0	1	1	0	0	X	1
0	1	1	0	1	X	0
0	1	1	1	X	0	1
0	1	1	1	X	1	0
1	X	X	X	X	X	QN<1>

Cell Size

CellName	Height(um)	Width(um)
SDGRNQNUHDV0P7	3.360	17.920
SDGRNQNUHDV1	3.360	17.920
SDGRNQNUHDV2	3.360	18.480

Pin Power (uW/MHz)

Pin	V0P7	V1	V2
CK	0.01545	0.01546	0.01624
D	0.00268	0.00268	0.00295
QN	0.01856	0.01986	0.02790
RN	0.00297	0.00297	0.00325
SE	0.01151	0.01152	0.01208
SI	0.00685	0.00685	0.00754

Pin Capacitance (pf)

Pin	V0P7	V1	V2
CK	0.00250	0.00250	0.00252
D	0.00240	0.00240	0.00241
RN	0.00301	0.00301	0.00301
SE	0.00763	0.00763	0.00764
SI	0.00235	0.00235	0.00237

Max Leakage Power (uW)

V0P7	V1	V2
0.00014593	0.00014876	0.00018101

Delay Table (ns)

Description	V0P7	V1	V2
CK→QN_FALL	0.18520	0.18950	0.18990
CK→QN_RISE	0.22810	0.22750	0.22840

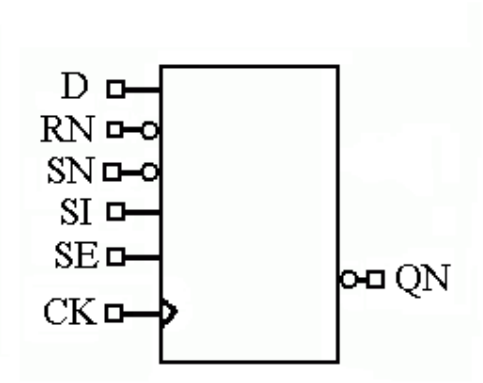
Timing Constraints (ns)

Pin	Requirement	V0P7	V1	V2
D	hold_FALL→CK	-0.06380	-0.06380	-0.06780
D	hold_RISE→CK	-0.11160	-0.11160	-0.10760
D	setup_FALL→CK	0.18740	0.19140	0.19940
D	setup_RISE→CK	0.18740	0.18740	0.16750
RN	hold_FALL→CK	-0.05980	-0.05980	-0.06380
RN	hold_RISE→CK	-0.11960	-0.11960	-0.11960
RN	setup_FALL→CK	0.22330	0.22330	0.23130
RN	setup_RISE→CK	0.19940	0.19940	0.17940
SE	hold_FALL→CK	-0.05180	-0.05180	-0.05580
SE	hold_RISE→CK	-0.11160	-0.10760	-0.10760
SE	setup_FALL→CK	0.16350	0.16750	0.16750
SE	setup_RISE→CK	0.19540	0.19540	0.17150
SI	hold_FALL→CK	-0.19540	-0.19140	-0.19940
SI	hold_RISE→CK	-0.13560	-0.13160	-0.13160
SI	setup_FALL→CK	0.39480	0.39870	0.41070
SI	setup_RISE→CK	0.21540	0.21530	0.19140
CK	minpwh	0.09650	0.09650	0.09660
CK	minpwl	0.31190	0.31190	0.32770

SDGRSNQNUHD

Cell Description

Scan D Flip-Flop with Sync Clear and Set with a single output (QN)
QN = rising (CK) ? !(SE ? SI : (!RN ? 0 : !SN ? 1 : D)) : pre_QN



Function Table

CK<1>	CK	RN	SE	SN	D	SI	QN
0	0	X	X	X	X	X	QN<1>
0	1	0	0	X	X	X	1
0	1	0	1	X	X	0	1
0	1	0	1	X	X	1	0
0	1	1	0	0	X	X	0
0	1	1	0	1	0	X	1
0	1	1	0	1	1	X	0
0	1	1	1	X	X	0	1
0	1	1	1	X	X	1	0
1	X	X	X	X	X	X	QN<1>

Cell Size

CellName	Height(um)	Width(um)
SDGRSNQNUHDV0P7	3.360	20.720
SDGRSNQNUHDV1	3.360	20.720
SDGRSNQNUHDV2	3.360	21.280

Pin Power (uW/MHz)

Pin	V0P7	V1	V2
CK	0.01534	0.01534	0.01558
D	0.00158	0.00158	0.00173
QN	0.01850	0.01995	0.02717
RN	0.00460	0.00460	0.00507
SE	0.01186	0.01288	0.01354
SI	0.00752	0.00752	0.00824
SN	0.00633	0.00634	0.00649

Pin Capacitance (pf)

Pin	V0P7	V1	V2
CK	0.00251	0.00251	0.00250
D	0.00243	0.00244	0.00243
RN	0.00268	0.00268	0.00268
SE	0.00664	0.00835	0.00835
SI	0.00234	0.00234	0.00234
SN	0.00269	0.00268	0.00268

Max Leakage Power (uW)

V0P7	V1	V2
0.00015682	0.00016767	0.00019988

Delay Table (ns)

Description	V0P7	V1	V2
CK→QN_FALL	0.18840	0.19280	0.18440
CK→QN_RISE	0.22860	0.22780	0.22410

Timing Constraints (ns)

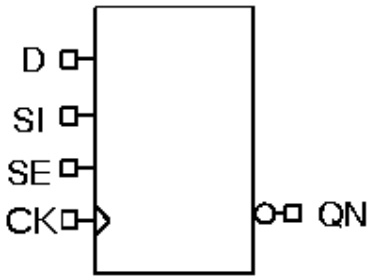
Pin	Requirement	V0P7	V1	V2
D	hold_FALL→CK	-0.12760	-0.12760	-0.13560
D	hold_RISE→CK	-0.11170	-0.11170	-0.11170
D	setup_FALL→CK	0.30710	0.30700	0.31900
D	setup_RISE→CK	0.18740	0.18740	0.17550
RN	hold_FALL→CK	-0.13960	-0.13960	-0.14750
RN	hold_RISE→CK	-0.14360	-0.14360	-0.14750
RN	setup_FALL→CK	0.34690	0.34690	0.35890
RN	setup_RISE→CK	0.22730	0.22730	0.21930
SE	hold_FALL→CK	-0.14750	-0.14750	-0.15550
SE	hold_RISE→CK	-0.13160	-0.13160	-0.13560
SE	setup_FALL→CK	0.35890	0.36290	0.37090
SE	setup_RISE→CK	0.21530	0.21530	0.20340
SI	hold_FALL→CK	-0.24720	-0.24320	-0.25120
SI	hold_RISE→CK	-0.14750	-0.14750	-0.14750
SI	setup_FALL→CK	0.51040	0.51040	0.52240
SI	setup_RISE→CK	0.23130	0.23130	0.21930
SN	hold_FALL→CK	-0.19940	-0.19940	-0.19940
SN	hold_RISE→CK	-0.19140	-0.19140	-0.19940
SN	setup_FALL→CK	0.27910	0.27910	0.27110

SN	setup_RISE→CK	0.37090	0.37480	0.38680
CK	minpwh	0.09660	0.09650	0.09650
CK	minpwl	0.42500	0.42770	0.44080

SDQNUHD

Cell Description

Scan D Flip-Flop, Single Output QN
QN = rising (CK) ? !(SE&SI | !SE&D) : pre_QN



Function Table

CK<1>	CK	SE	SI	D	QN
0	0	X	X	X	QN<1>
0	1	0	X	0	1
0	1	0	X	1	0
0	1	1	0	X	1
0	1	1	1	X	0
1	X	X	X	X	QN<1>

Cell Size

CellName	Height(um)	Width(um)
SDQNUHDV0P7	3.360	15.680
SDQNUHDV1	3.360	15.680
SDQNUHDV2	3.360	16.240

Pin Power (uW/MHz)

Pin	V0P7	V1	V2
CK	0.01535	0.01558	0.01615
D	0.00461	0.00460	0.00535
QN	0.01868	0.02035	0.02773
SE	0.01029	0.01028	0.01150
SI	0.00564	0.00563	0.00669

Pin Capacitance (pf)

Pin	V0P7	V1	V2
CK	0.00252	0.00252	0.00252
D	0.00271	0.00271	0.00328

SE	0.00697	0.00697	0.00733
SI	0.00251	0.00250	0.00298

Max Leakage Power (uW)

V0P7	V1	V2
0.00014120	0.00014403	0.00018261

Delay Table (ns)

Description	V0P7	V1	V2
CK→QN_FALL	0.19060	0.19860	0.18810
CK→QN_RISE	0.23140	0.23250	0.22730

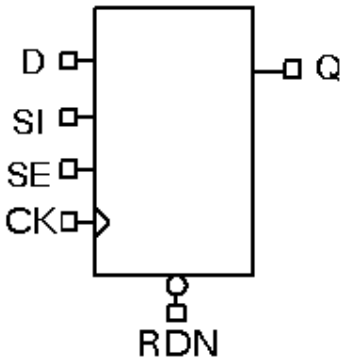
Timing Constraints (ns)

Pin	Requirement	V0P7	V1	V2
D	hold_FALL→CK	-0.09170	-0.08770	-0.05980
D	hold_RISE→CK	-0.08370	-0.08370	-0.07980
D	setup_FALL→CK	0.24320	0.24320	0.19540
D	setup_RISE→CK	0.15550	0.15550	0.13160
SE	hold_FALL→CK	-0.09170	-0.08770	-0.05980
SE	hold_RISE→CK	-0.08770	-0.08770	-0.07970
SE	setup_FALL→CK	0.24720	0.24330	0.19540
SE	setup_RISE→CK	0.15950	0.15950	0.13560
SI	hold_FALL→CK	-0.12360	-0.11960	-0.08770
SI	hold_RISE→CK	-0.10370	-0.10370	-0.09970
SI	setup_FALL→CK	0.29910	0.29510	0.24320
SI	setup_RISE→CK	0.17950	0.17540	0.15550
CK	minpwh	0.09650	0.09650	0.09650
CK	minpwl	0.39870	0.40140	0.36980

SDRNQUHD

Cell Description

Scan D Flip-Flop with Async Clear
Q = !RDN ? 0 : rising (CK) ? (SE&SI | !SE&D) : pre_Q



Function Table

RDN	CK<1>	CK	SE	D	SI	Q
0	X	X	X	X	X	0
1	0	0	X	X	X	Q<1>
1	0	1	0	0	X	0
1	0	1	0	1	X	1
1	0	1	1	X	0	0
1	0	1	1	X	1	1
1	1	X	X	X	X	Q<1>

Cell Size

CellName	Height(um)	Width(um)
SDRNQUHDV0P7	3.360	17.360
SDRNQUHDV1	3.360	17.360
SDRNQUHDV2	3.360	17.920
SDRNQUHDV3	3.360	19.040

Pin Power (uW/MHz)

Pin	V0P7	V1	V2	V3
CK	0.01785	0.01785	0.01788	0.01799
D	0.00654	0.00652	0.00653	0.00654
Q	0.02847	0.02950	0.03523	0.04304
RDN	0.00136	0.00136	0.00137	0.00137
SE	0.01115	0.01113	0.01114	0.01115
SI	0.00773	0.00771	0.00772	0.00772

Pin Capacitance (pf)

Pin	V0P7	V1	V2	V3
CK	0.00252	0.00252	0.00253	0.00253
D	0.00262	0.00262	0.00262	0.00262
RDN	0.00730	0.00735	0.00738	0.00725
SE	0.00505	0.00506	0.00505	0.00505
SI	0.00247	0.00247	0.00247	0.00247

Max Leakage Power (uW)

V0P7	V1	V2	V3
0.00018399	0.00018525	0.00019915	0.00021271

Delay Table (ns)

Description	V0P7	V1	V2	V3
CK→Q_FALL	0.26200	0.26410	0.27180	0.28540
CK→Q_RISE	0.27800	0.27900	0.29470	0.31810
RDN→Q_FALL	0.07715	0.07815	0.08367	0.09875

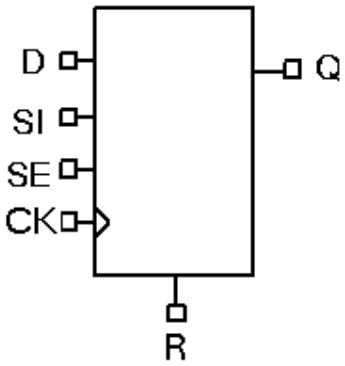
Timing Constraints (ns)

Pin	Requirement	V0P7	V1	V2	V3
D	hold_FALL→CK	-0.13560	-0.13560	-0.13560	-0.13960
D	hold_RISE→CK	-0.08770	-0.08770	-0.08770	-0.08770
D	setup_FALL→CK	0.25520	0.25520	0.25520	0.25520
D	setup_RISE→CK	0.15950	0.15950	0.15950	0.15550
RDN	setup_RISE→CK	-0.09972	-0.09571	-0.09570	-0.09573
RDN	hold_RISE→CK	0.12364	0.12359	0.12361	0.12361
SE	hold_FALL→CK	-0.13560	-0.13560	-0.13560	-0.13960
SE	hold_RISE→CK	-0.09170	-0.09170	-0.09170	-0.09170
SE	setup_FALL→CK	0.25520	0.25520	0.25520	0.25520
SE	setup_RISE→CK	0.16350	0.16350	0.16350	0.16350
SI	hold_FALL→CK	-0.16350	-0.16350	-0.16740	-0.16740
SI	hold_RISE→CK	-0.10360	-0.10360	-0.10360	-0.10360
SI	setup_FALL→CK	0.29910	0.29910	0.29900	0.29900
SI	setup_RISE→CK	0.17540	0.17540	0.17550	0.17550
CK	minpwh	0.11760	0.11760	0.13030	0.13860
CK	minpwl	0.25920	0.25920	0.25920	0.25920
RDN	minpwl	0.08390	0.08810	0.10500	0.12180

SDRQUHD

Cell Description

Scan D Flip-Flop with Async Clear
Q = R ? 0 : rising (CK) ? (SE&SI | !SE&D) : pre_Q



Function Table

R	CK<1>	CK	SE	D	SI	Q
1	X	X	X	X	X	0
0	0	0	X	X	X	Q<1>
0	0	1	0	0	X	0
0	0	1	0	1	X	1
0	0	1	1	X	0	0
0	0	1	1	X	1	1
0	1	X	X	X	X	Q<1>

Cell Size

CellName	Height(um)	Width(um)
SDRQUHDV0P7	3.360	17.360
SDRQUHDV1	3.360	17.360
SDRQUHDV2	3.360	18.480
SDRQUHDV3	3.360	19.040

Pin Power (uW/MHz)

Pin	V0P7	V1	V2	V3
CK	0.01679	0.01679	0.01679	0.01679
D	0.00371	0.00371	0.00371	0.00371
Q	0.02189	0.02415	0.02975	0.03702
RD	0.00170	0.00170	0.00170	0.00170
SE	0.00941	0.00941	0.00941	0.00941
SI	0.00452	0.00452	0.00452	0.00452

Pin Capacitance (pf)

Pin	V0P7	V1	V2	V3
CK	0.00261	0.00261	0.00261	0.00261
D	0.00329	0.00329	0.00329	0.00329
RD	0.00453	0.00452	0.00453	0.00453
SE	0.00728	0.00728	0.00728	0.00728
SI	0.00227	0.00227	0.00227	0.00227

Max Leakage Power (uW)

V0P7	V1	V2	V3
0.00015881	0.00016489	0.00018326	0.00021256

Delay Table (ns)

Description	V0P7	V1	V2	V3
CK→Q_FALL	0.26160	0.25890	0.26750	0.28040
CK→Q_RISE	0.27100	0.27510	0.28510	0.30080
RD→Q_FALL	0.12988	0.12630	0.13424	0.14676

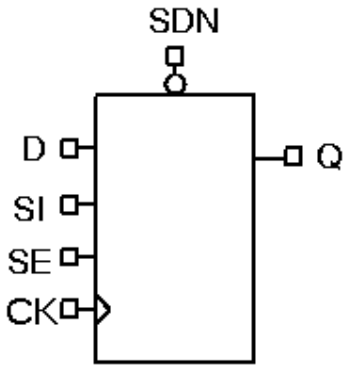
Timing Constraints (ns)

Pin	Requirement	V0P7	V1	V2	V3
D	hold_FALL→CK	-0.07580	-0.07580	-0.07580	-0.07580
D	hold_RISE→CK	-0.07180	-0.07180	-0.07180	-0.07180
D	setup_FALL→CK	0.17550	0.17550	0.17550	0.17550
D	setup_RISE→CK	0.23530	0.23530	0.23530	0.23530
RD	setup_FALL→CK	0.15151	0.15151	0.15151	0.14754
RD	hold_FALL→CK	0.00400	0.00400	0.00400	0.00400
SE	hold_FALL→CK	-0.07970	-0.07970	-0.07970	-0.07980
SE	hold_RISE→CK	-0.09170	-0.09170	-0.09170	-0.09170
SE	setup_FALL→CK	0.17950	0.17950	0.17950	0.17950
SE	setup_RISE→CK	0.26320	0.26320	0.26320	0.25920
SI	hold_FALL→CK	-0.22730	-0.22330	-0.22330	-0.22330
SI	hold_RISE→CK	-0.10370	-0.10370	-0.10370	-0.10370
SI	setup_FALL→CK	0.37480	0.37480	0.37480	0.37480
SI	setup_RISE→CK	0.27510	0.27510	0.27510	0.27120
CK	minpwh	0.13440	0.14290	0.15130	0.15970
CK	minpwl	0.37760	0.37760	0.37760	0.37500
RD	minpwh	0.07550	0.07970	0.08390	0.08390

SDSNQUHD

Cell Description

Scan D Flip-Flop with Async Set
Q = !SDN ? 1 : rising (CK) ? (SE&SI | !SE&D) : pre_Q



Function Table

SDN	CK<1>	CK	SE	SI	D	Q
0	X	X	X	X	X	1
1	0	0	X	X	X	Q<1>
1	0	1	0	X	0	0
1	0	1	0	X	1	1
1	0	1	1	0	X	0
1	0	1	1	1	X	1
1	1	X	X	X	X	Q<1>

Cell Size

CellName	Height(um)	Width(um)
SDSNQUHDV0P7	3.360	16.800
SDSNQUHDV1	3.360	16.800
SDSNQUHDV2	3.360	17.360
SDSNQUHDV3	3.360	18.480

Pin Power (uW/MHz)

Pin	V0P7	V1	V2	V3
CK	0.01645	0.01643	0.01642	0.01642
D	0.00554	0.00554	0.00554	0.00554
Q	0.02962	0.03112	0.03641	0.04360
SDN	0.00278	0.00278	0.00278	0.00278
SE	0.01014	0.01014	0.01014	0.01014
SI	0.00670	0.00670	0.00670	0.00670

Pin Capacitance (pf)

Pin	V0P7	V1	V2	V3
CK	0.00251	0.00249	0.00249	0.00249
D	0.00263	0.00263	0.00263	0.00263
SDN	0.00622	0.00622	0.00622	0.00622
SE	0.00506	0.00506	0.00506	0.00506
SI	0.00247	0.00247	0.00247	0.00247

Max Leakage Power (uW)

V0P7	V1	V2	V3
0.00020373	0.00020651	0.00023449	0.00026369

Delay Table (ns)

Description	V0P7	V1	V2	V3
CK→Q_FALL	0.26760	0.27090	0.28060	0.29530
CK→Q_RISE	0.22170	0.22060	0.22940	0.24410
SDN→Q_RISE	0.21939	0.21845	0.22730	0.24164

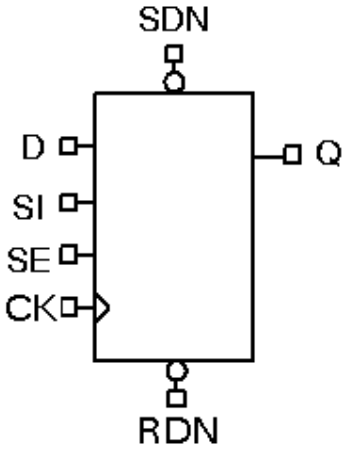
Timing Constraints (ns)

Pin	Requirement	V0P7	V1	V2	V3
D	hold_FALL→CK	-0.13160	-0.13160	-0.13160	-0.13160
D	hold_RISE→CK	-0.08370	-0.08370	-0.08370	-0.08370
D	setup_FALL→CK	0.28710	0.28710	0.28710	0.28710
D	setup_RISE→CK	0.17150	0.17150	0.17150	0.17150
SDN	setup_RISE→CK	-0.00798	-0.00800	-0.00799	-0.00799
SDN	hold_RISE→CK	0.03189	0.03189	0.03189	0.03189
SE	hold_FALL→CK	-0.13560	-0.13160	-0.13160	-0.13560
SE	hold_RISE→CK	-0.08770	-0.08770	-0.08770	-0.08770
SE	setup_FALL→CK	0.28710	0.28710	0.28710	0.28710
SE	setup_RISE→CK	0.17940	0.17940	0.17940	0.17550
SI	hold_FALL→CK	-0.16350	-0.15950	-0.15950	-0.16350
SI	hold_RISE→CK	-0.09970	-0.09970	-0.09970	-0.09970
SI	setup_FALL→CK	0.33100	0.33100	0.33100	0.33100
SI	setup_RISE→CK	0.19140	0.19140	0.19140	0.19140
CK	minpwh	0.09230	0.09230	0.09650	0.10070
CK	minpwl	0.26970	0.26970	0.26970	0.26970
SDN	minpwl	0.10500	0.10920	0.11340	0.12180

SDSRNQUHD

Cell Description

Scan D Flip-Flop with Async Clear and Set
Q = !RDN ? 0 : !SDN ? 1 : rising (CK) ? (SE&SI | !SE&D) : pre_Q



Function Table

RDN	SDN	CK<1>	CK	SE	D	SI	Q
0	0	X	X	X	X	X	0
0	1	X	X	X	X	X	0
1	0	X	X	X	X	X	1
1	1	0	0	X	X	X	Q<1>
1	1	0	1	0	0	X	0
1	1	0	1	0	1	X	1
1	1	0	1	1	X	0	0
1	1	0	1	1	X	1	1
1	1	1	X	X	X	X	Q<1>

Cell Size

CellName	Height(um)	Width(um)
SDSRNQUHDV1	3.360	19.040
SDSRNQUHDV2	3.360	20.160

Pin Power (uW/MHz)

Pin	V1	V2
CK	0.01797	0.01809
D	0.00541	0.00542
Q	0.02577	0.03302
RDN	0.00023	0.00023
SDN	0.00213	0.00212
SE	0.01029	0.01030
SI	0.00651	0.00651

Pin Capacitance (pf)

Pin	V1	V2
CK	0.00260	0.00263
D	0.00301	0.00301
RDN	0.00712	0.00710
SDN	0.00537	0.00537
SE	0.00613	0.00613
SI	0.00219	0.00218

Max Leakage Power (uW)

V1	V2
0.00018567	0.00021469

Delay Table (ns)

Description	V1	V2
CK→Q_FALL	0.29510	0.31730
CK→Q_RISE	0.24820	0.26210
RDN→Q_FALL	0.12803	0.14939
RDN→Q_RISE	0.08700	0.09644
SDN→Q_RISE	0.29497	0.30853

Timing Constraints (ns)

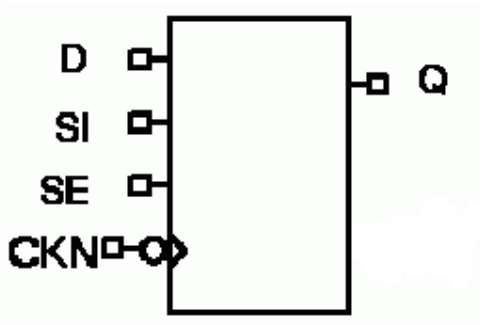
Pin	Requirement	V1	V2
D	hold_FALL→CK	-0.06780	-0.06380
D	hold_RISE→CK	-0.09170	-0.09170
D	setup_FALL→CK	0.16350	0.15950
D	setup_RISE→CK	0.20730	0.20730
RDN	setup_RISE→CK	-0.13957	-0.13957
RDN	hold_RISE→CK	0.17146	0.17148
SDN	setup_RISE→CK	-0.05579	-0.05979
SDN	hold_RISE→CK	0.11562	0.11563
SDN	non_seq_hold_RISE→RDN	0.00798	0.01993
SDN	non_seq_setup_RISE→RDN	0.01198	0.00000
SE	hold_FALL→CK	-0.07180	-0.07180
SE	hold_RISE→CK	-0.09970	-0.09970
SE	setup_FALL→CK	0.16750	0.16750
SE	setup_RISE→CK	0.21930	0.21530
SI	hold_FALL→CK	-0.16350	-0.15950
SI	hold_RISE→CK	-0.10760	-0.10760
SI	setup_FALL→CK	0.34300	0.33890
SI	setup_RISE→CK	0.22730	0.22330
CK	minpwh	0.10920	0.11760
CK	minpwl	0.29870	0.29870

RDN	minpwl	0.15130	0.18920
SDN	minpwl	0.21020	0.22290

SNDQUHD

Cell Description

Negative Edge Trigger Scan D Flip-Flop with a single output (Q)
Q = falling (CKN) ? (SE&SI | !SE&D) : pre_Q



Function Table

CKN<1>	CKN	SE	SI	D	Q
0	X	X	X	X	Q<1>
1	0	0	X	0	0
1	0	0	X	1	1
1	0	1	0	X	0
1	0	1	1	X	1
1	1	X	X	X	Q<1>

Cell Size

CellName	Height(um)	Width(um)
SNDQUHDV0P7	3.360	16.800
SNDQUHDV1	3.360	16.800
SNDQUHDV2	3.360	17.920
SNDQUHDV3	3.360	19.040

Pin Power (uW/MHz)

Pin	V0P7	V1	V2	V3
CKN	0.01396	0.01400	0.01628	0.01626
D	0.00498	0.00499	0.00599	0.00599
Q	0.01908	0.02079	0.02790	0.03821
SE	0.01075	0.01076	0.01207	0.01207
SI	0.00506	0.00507	0.00614	0.00613

Pin Capacitance (pf)

Pin	V0P7	V1	V2	V3
CKN	0.00235	0.00239	0.00238	0.00238

D	0.00259	0.00259	0.00308	0.00308
SE	0.00738	0.00738	0.00793	0.00793
SI	0.00225	0.00226	0.00267	0.00266

Max Leakage Power (uW)

V0P7	V1	V2	V3
0.00013413	0.00013723	0.00017333	0.00020227

Delay Table (ns)

Description	V0P7	V1	V2	V3
CKN→Q_FALL	0.31240	0.31910	0.30630	0.32940
CKN→Q_RISE	0.22490	0.22710	0.25500	0.27730

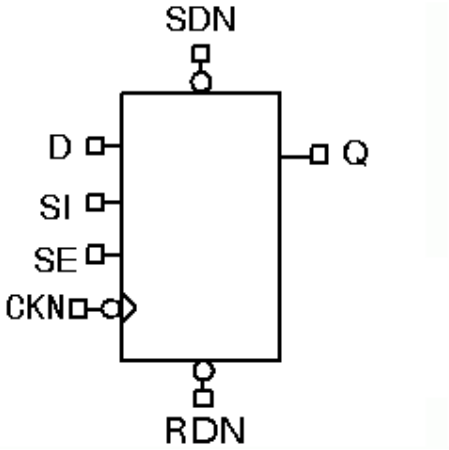
Timing Constraints (ns)

Pin	Requirement	V0P7	V1	V2	V3
D	hold_FALL→CKN	-0.23530	-0.23130	-0.19540	-0.19540
D	hold_RISE→CKN	0.02390	0.02390	0.03990	0.03990
D	setup_FALL→CKN	0.26320	0.26320	0.21930	0.21930
D	setup_RISE→CKN	0.08380	0.08380	0.06380	0.05980
SE	hold_FALL→CKN	-0.24720	-0.24320	-0.20740	-0.20740
SE	hold_RISE→CKN	0.02390	0.02390	0.03590	0.03590
SE	setup_FALL→CKN	0.27510	0.27510	0.23130	0.23130
SE	setup_RISE→CKN	0.08380	0.08380	0.06780	0.06380
SI	hold_FALL→CKN	-0.23130	-0.23130	-0.22330	-0.22330
SI	hold_RISE→CKN	0.01990	0.01990	0.03590	0.03590
SI	setup_FALL→CKN	0.26320	0.25920	0.25120	0.25120
SI	setup_RISE→CKN	0.08370	0.08380	0.06780	0.06380
CKN	minpwh	0.26180	0.26180	0.28820	0.28550
CKN	minpwl	0.17660	0.18080	0.21870	0.23970

SNDSRNQUHD

Cell Description

Negative Edge Trigger Scan D Flip-Flop with Async Clear and Set
Q = !RDN ? 0 : !SDN ? 1 : falling (CKN) ? (SE&SI | !SE&D) : pre_Q



Function Table

RDN	SDN	CKN<1>	CKN	SE	D	SI	Q
0	0	X	X	X	X	X	0
0	1	X	X	X	X	X	0
1	0	X	X	X	X	X	1
1	1	0	X	X	X	X	Q<1>
1	1	1	0	0	0	X	0
1	1	1	0	0	1	X	1
1	1	1	0	1	X	0	0
1	1	1	0	1	X	1	1
1	1	1	1	X	X	X	Q<1>

Cell Size

CellName	Height(um)	Width(um)
SNDSRNQUHDV1	3.360	19.040
SNDSRNQUHDV2	3.360	20.160

Pin Power (uW/MHz)

Pin	V1	V2
CKN	0.01807	0.01840
D	0.00541	0.00550
Q	0.02592	0.03316
RDN	0.00023	0.00023
SDN	0.00213	0.00212
SE	0.01029	0.01038
SI	0.00651	0.00660

Pin Capacitance (pf)

Pin	V1	V2
CKN	0.00242	0.00242
D	0.00312	0.00312
RDN	0.00712	0.00711
SDN	0.00525	0.00526
SE	0.00613	0.00613
SI	0.00220	0.00220

Max Leakage Power (uW)

V1	V2
0.00018547	0.00021317

Delay Table (ns)

Description	V1	V2
CKN→Q_FALL	0.29020	0.31280
CKN→Q_RISE	0.31950	0.33430
RDN→Q_FALL	0.12794	0.14977
RDN→Q_RISE	0.08696	0.09596
SDN→Q_RISE	0.29471	0.30780

Timing Constraints (ns)

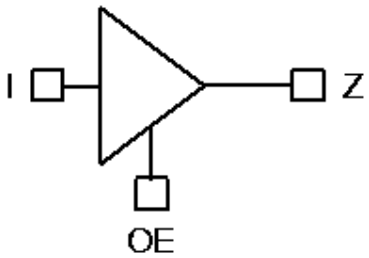
Pin	Requirement	V1	V2
D	hold_FALL→CKN	-0.09970	-0.09970
D	hold_RISE→CKN	0.02390	0.02390
D	setup_FALL→CKN	0.18740	0.18740
D	setup_RISE→CKN	0.09570	0.09970
RDN	setup_RISE→CKN	-0.23924	-0.24322
RDN	hold_RISE→CKN	0.29107	0.30304
SDN	setup_RISE→CKN	-0.03587	-0.03987
SDN	hold_RISE→CKN	0.09569	0.09967
SDN	non_seq_hold_RISE→RDN	-0.00000	0.00398
SDN	non_seq_setup_RISE→RDN	0.02393	0.01597
SE	hold_FALL→CKN	-0.10370	-0.10370
SE	hold_RISE→CKN	0.01990	0.01590
SE	setup_FALL→CKN	0.19140	0.19140
SE	setup_RISE→CKN	0.10770	0.11170
SI	hold_FALL→CKN	-0.23930	-0.23930
SI	hold_RISE→CKN	0.00800	0.00800
SI	setup_FALL→CKN	0.38280	0.38280
SI	setup_RISE→CKN	0.11570	0.11960
CKN	minpwh	0.20920	0.21450
CKN	minpwl	0.17230	0.18080

RDN	minpwl	0.23550	0.24400
SDN	minpwl	0.21020	0.21450

TBUFUHD

Cell Description

3-State Buffer with High Enable
Z=!OE ? I:(1'bZ)



Function Table

OE	I	Z
0	X	Z
1	0	0
1	1	1

Cell Size

CellName	Height(um)	Width(um)
TBUFUHDV0P7	3.360	6.720
TBUFUHDV1	3.360	6.720
TBUFUHDV2	3.360	7.840
TBUFUHDV3	3.360	8.400
TBUFUHDV4	3.360	10.080
TBUFUHDV6	3.360	11.200
TBUFUHDV8	3.360	13.440
TBUFUHDV12	3.360	16.800
TBUFUHDV16	3.360	21.280
TBUFUHDV24	3.360	30.240

Pin Power (uW/MHz)

Pin	V0P7	V1	V2	V3	V4	V6	V8	V12
I	0.01410	0.01449	0.02058	0.02646	0.03123	0.04195	0.05541	0.07712
OE	0.01036	0.01066	0.01591	0.02107	0.02510	0.03434	0.04566	0.06381

Pin	V16	V24
I	0.10163	0.15175
OE	0.08432	0.12755

Pin Capacitance (pf)

Pin	V0P7	V1	V2	V3	V4	V6	V8	V12
I	0.00291	0.00307	0.00398	0.00434	0.00637	0.00795	0.01182	0.01597
OE	0.00562	0.00558	0.00567	0.00556	0.00563	0.00555	0.00589	0.00634

Pin	V16	V24
I	0.02357	0.03119
OE	0.00628	0.00722

Max Leakage Power (uW)

V0P7	V1	V2	V3	V4	V6	V8	V12
0.00005779	0.00006000	0.00007756	0.00010595	0.00014118	0.00020633	0.00027829	0.00041240

V16	V24
0.00055524	0.00081770

Delay Table (ns)

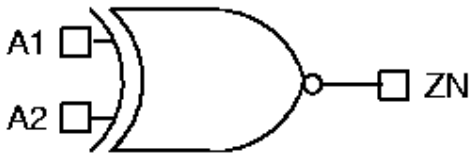
Description	V0P7	V1	V2	V3	V4	V6	V8	V12
I→Z_FALL	0.15466	0.14639	0.12516	0.13017	0.11709	0.11814	0.11466	0.12453
I→Z_RISE	0.11398	0.11124	0.10665	0.11224	0.10431	0.11156	0.11059	0.12738
OE→Z_FALL	0.09850	0.09867	0.10412	0.11371	0.12268	0.13955	0.15005	0.14280
OE→Z_RISE	0.09193	0.09040	0.09674	0.10247	0.10627	0.11706	0.12138	0.13748

Description	V16	V24
I→Z_FALL	0.13235	0.11813
I→Z_RISE	0.14554	0.11362
OE→Z_FALL	0.17301	0.21618
OE→Z_RISE	0.15335	0.16528

XNOR2UHD

Cell Description

2-Input Exclusive NOR
ZN=(!(A1^A2))



Function Table

A2	A1	ZN
0	0	1
0	1	0
1	0	0
1	1	1

Cell Size

CellName	Height(um)	Width(um)
XNOR2UHDV0P4	3.360	4.480
XNOR2UHDV0P7	3.360	5.040
XNOR2UHDV1	3.360	5.040
XNOR2UHDV2	3.360	7.280
XNOR2UHDV4	3.360	14.560

Pin Power (uW/MHz)

Pin	V0P4	V0P7	V1	V2	V4
A1	0.00698	0.00999	0.01116	0.01321	0.03337
A2	0.00807	0.01231	0.01389	0.02091	0.04756

Pin Capacitance (pf)

Pin	V0P4	V0P7	V1	V2	V4
A1	0.00464	0.00694	0.00715	0.01141	0.02647
A2	0.00247	0.00349	0.00329	0.00843	0.01634

Max Leakage Power (uW)

V0P4	V0P7	V1	V2	V4
0.00005441	0.00007426	0.00008766	0.00015825	0.00037075

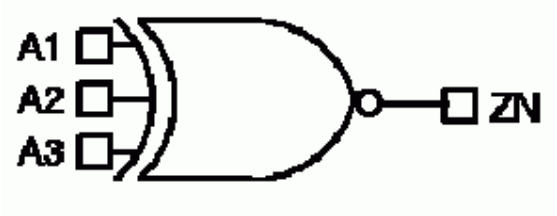
Delay Table (ns)

Description	V0P4	V0P7	V1	V2	V4
A1→ZN_FALL	0.06220	0.05460	0.04876	0.04063	0.04504
A1→ZN_RISE	0.09735	0.08632	0.08138	0.04920	0.06914
A2→ZN_FALL	0.09590	0.08654	0.09142	0.06786	0.08911
A2→ZN_RISE	0.12612	0.11541	0.12980	0.08138	0.11901

XNOR3UHD

Cell Description

3-Input Exclusive NOR
ZN=(!(A1^A2^A3))



Function Table

A2	A1	A3	ZN
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

Cell Size

CellName	Height(um)	Width(um)
XNOR3UHDV0P7	3.360	10.080
XNOR3UHDV1	3.360	10.080
XNOR3UHDV2	3.360	12.320

Pin Power (uW/MHz)

Pin	V0P7	V1	V2
A1	0.03160	0.03404	0.05273
A2	0.02629	0.02855	0.04348
A3	0.01422	0.01555	0.02499

Pin Capacitance (pf)

Pin	V0P7	V1	V2
A1	0.00273	0.00288	0.00425
A2	0.00526	0.00552	0.00690

A3	0.00513	0.00535	0.00716

Max Leakage Power (uW)

V0P7	V1	V2
0.00014988	0.00015671	0.00024125

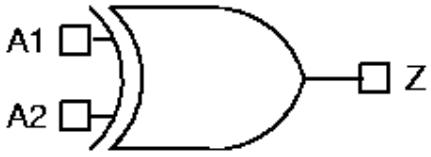
Delay Table (ns)

Description	V0P7	V1	V2
A1→ZN_FALL	0.28448	0.27492	0.24824
A1→ZN_RISE	0.26454	0.26053	0.24168
A2→ZN_FALL	0.22863	0.22116	0.19840
A2→ZN_RISE	0.20900	0.20670	0.19136
A3→ZN_FALL	0.12358	0.11966	0.11072
A3→ZN_RISE	0.10868	0.10582	0.10005

XOR2UHD

Cell Description

2-Input Exclusive OR
Z=(A1^A2)



Function Table

A2	A1	Z
0	0	0
0	1	1
1	0	1
1	1	0

Cell Size

CellName	Height(um)	Width(um)
XOR2UHDV0P4	3.360	5.040
XOR2UHDV0P7	3.360	5.600
XOR2UHDV1	3.360	6.160
XOR2UHDV2	3.360	7.280
XOR2UHDV4	3.360	14.560

Pin Power (uW/MHz)

Pin	V0P4	V0P7	V1	V2	V4
A1	0.00734	0.01093	0.01246	0.01377	0.03349
A2	0.00844	0.01243	0.01627	0.02115	0.04736

Pin Capacitance (pf)

Pin	V0P4	V0P7	V1	V2	V4
A1	0.00470	0.00629	0.00755	0.01145	0.02566
A2	0.00249	0.00340	0.00440	0.00853	0.01657

Max Leakage Power (uW)

V0P4	V0P7	V1	V2	V4
0.00006154	0.00008420	0.00010433	0.00015379	0.00036849

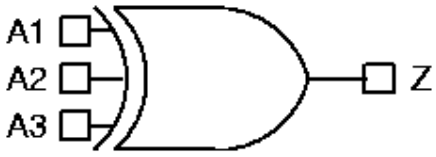
Delay Table (ns)

Description	V0P4	V0P7	V1	V2	V4
A1→Z_FALL	0.07448	0.06524	0.05781	0.04188	0.04945
A1→Z_RISE	0.07863	0.06801	0.06273	0.04719	0.05463
A2→Z_FALL	0.09908	0.08538	0.08622	0.06801	0.08841
A2→Z_RISE	0.13139	0.11747	0.11652	0.08156	0.11866

XOR3UHD

Cell Description

3-Input Exclusive OR
Z=(A1^A2^A3)



Function Table

A2	A1	A3	Z
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Cell Size

CellName	Height(um)	Width(um)
XOR3UHDV0P7T	3.360	10.080
XOR3UHDV1T	3.360	10.080
XOR3UHDV2T	3.360	12.320

Pin Power (uW/MHz)

Pin	V0P7T	V1T	V2T
A1	0.03155	0.03396	0.05237
A2	0.02625	0.02847	0.04328
A3	0.01371	0.01507	0.02438

Pin Capacitance (pf)

Pin	V0P7T	V1T	V2T
A1	0.00273	0.00288	0.00436
A2	0.00526	0.00552	0.00690

A3	0.00517	0.00542	0.00690

Max Leakage Power (uW)

V0P7T	V1T	V2T
0.00015835	0.00016443	0.00025372

Delay Table (ns)

Description	V0P7T	V1T	V2T
A1→Z_FALL	0.28613	0.27802	0.24926
A1→Z_RISE	0.26547	0.26358	0.24232
A2→Z_FALL	0.23009	0.22434	0.19962
A2→Z_RISE	0.20985	0.20963	0.19229
A3→Z_FALL	0.11980	0.11497	0.10852
A3→Z_RISE	0.10947	0.10958	0.10250