



Semiconductor Manufacturing International (Shanghai) Corporation

**SMIC 0.18 μm
I/O Cell Library (*SP018*)
Data Book**

Version 1.3

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Semiconductor Manufacturing International Corporation



Semiconductor Manufacturing International (Shanghai) Corporation

SMIC 0.18 μm

I/O cell Library (*SP018*)

Data Book

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Semiconductor Manufacturing International (Shanghai) Corporation
No 18 Zhangjiang Road
Pudong New Area
Shanghai 201203
The People's Republic of China
E-mail: Design_Services@smics.com
URL: www.smics.com



Document Revision History

VERSION	EFFECTIVE DATE	NOTE AND CHANGE
		DESCRIPTION
0.13	2 April 2003	Initial version of data book
1.0	9 July 2003	<ul style="list-style-type: none">● DC specification: R_{PU}, R_{PD}, V_{T+}, V_{T-}, I_{OL} & I_{OH} (2, 4, 8, 12, 16 and 24mA)● Appendix A (Maximum Allowable Current)● Update design tools
1.1	23 July 2003	<ul style="list-style-type: none">● Describe FP pin in I/O Layout Configuration section● Update design tools● Power, ground cells and PCI cell description in detail● Appendix B: Maximum Allowable Current for Analog power and ground cells
	31 October 2003	<ul style="list-style-type: none">● Description of IP usage statement on page iii● Add new analog power/ground cells in cell categories● Appendix A and B
1.2	1 December 2003	<ul style="list-style-type: none">● Add three cells: PANA3AP, PVDD1ANP, PVSS1ANP● Add bonding pad: PADI65, PADI60, PADI55, PADI50, PADI45● Update description of analog cells● Add ESD description and one Characterization Condition in Chapter 5● Update DC specification● Update Appendix A and B
1.3	29 July 2004	<ul style="list-style-type: none">● Add three cells: PANA3AP, PVDD1ANP, PVSS1ANP● Add bonding pad: PADI65, PADI60, PADI55, PADI50, PADI45● Update description of analog cells● Add ESD description and one Characterization Condition in Chapter 5● Update DC specification● Update Appendix A and B



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1. Introduction

This data book provides general technical information and property of SMIC 0.18μm logic I/O Library (*SP018*). Where *S* stands for SMIC, *P* is pad and 0.18μm technology process. All I/O pads are matched with the design requirement of SMIC 0.18μm Logic 1P6M Salicide 1.8V/3.3V Design Rules (TD-L018-DR-2001). Table 1 describes the process and physical specification of the Library. It should be noted that *SP018* support design with four, five or six layers of metal applications. I/O application criteria are listed as shown in Table 2.

Table 1 Physical Specification

Items	Contents
Process	SMIC 0.18μm Logic 1P6M Salicide 1.8V/3.3V Process
Metal Layers	Suitable for 4,5 and 6 layers application
Cell Size (Width * height)	40 um * 200 um without bonding pads

Table 2 I/O application table

I/O Type	Option and possible Combination
Standard I/O interface pads	3V/5V input tolerance, 3.3V output Schmitt trigger input LVCMS / LVTTL level Tri-State Slew rate controlled (Low noise) Pull-Up Tr. Resistor Range: 39-116 (Kohm) Pull-Down Tr. Resistor Range: 40-108(Kohm) 2, 4, 8,12, 16, 24 mA driving strength per I/O pads
High Drive clock buffer	(NOT Ready YET) Pad in core out, core in core out
Crystal I/O pads	Different frequencies
Special I/O pads	PCI (3.3V, 33/66MHz)

1.1. Outline Of the Document

The materials in this data book also covered the **Design Tools Support**, **I/O Layout Configuration**, **Cell Categories**, **DC and AC Specification** about SMIC *SP018* I/O Library and **Data Sheet** that contain the cell information and characteristics of each I/O pad in the Library.



2. Design Tools Support

SMIC I/O library (*SP018*) design views support the following popular industry design tools:

Front end

- Verilog models
- VHDL models
- Synopsys synthesis models
- Cadence place-and route
- Synopsys place-and route

Back end

- GDSII
- LVS Netlist

SP018 I/O library models will comply with the following file formats and versions. The CAD tools and version that are used and supported the *SP018* I/O library design flow are also listed in Table 3.

Table 3. Design tools facility

Design Phase	Tool and Vendor	Tool Version	Files Format
Verilog Simulation	NC-Verilog (Cadence)	2003.4	.v
	Verilog-XL (Cadence)	3.40.S002	.v
	VCS (Synopsys)	6.2R16	.v
VHDL/Vital Simulation	NC-VHDL (Cadence)	3.4	.vhd
Synthesis	Design Compiler (Synopsys)	2003.06	.lib, .slib, .db, .sdb
	Physical Compiler (Synopsys)	2003.06	.plib, .pdb
	BuildGates/PKS (Cadence)	5.09-s043+2	.tlf
Static timing / Delay calculation	PrimeTime (Synopsys)	2002.09-SP1	.lib, .db
	Pearl (Cadence)	5.1-s068	.tlf
	Design Compiler (Synopsys)	2003.06	.lib, .db
Schematic simulation	HSPICE (Avant!)	2002.2.2	.sp
	Eldo (Mentor)	V6.2_1.1	.cir
Power Estimation/Optimum	Power Compiler (Synopsys)	2003.06	.lib, .db
Place-and Route	Silicon Ensemble (Cadence)	5.4	
	Apollo-II (Avant!)	U2003.03	
Back end Verification (DRC and LVS)	Layout: Virtuoso (Cadence)	V5.0.0	GDSII
	Layout: Laker (Silicon Canvas, Inc.)	V2.3	
	Layout: Mentor: IC Station DRC:	8.9_11.1	



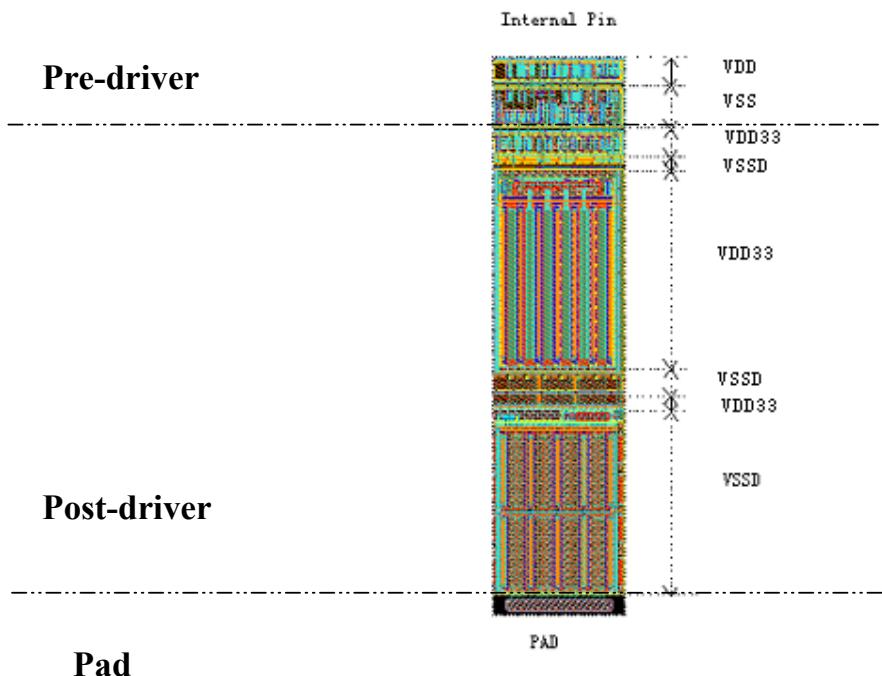
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	Dracula (Cadence);	Rev.1.2	
	Hercules (Avant!)	Rev.1.3	CDL netlist
	Calibre (Mentor)	V9.3_4.7	
LVS:			
	Dracula (Cadence);	4.9.03-2003	
	Hercules (Avant!)	U-2003.03.0052	
	Calibre (Mentor)	V9.3_4.7	



3. I/O Layout Configuration

In this section I/O layout sample, the detail of the I/O layout configuration and structure of power supplies are presented. SMIC I/O structure is constructed by pre-driver and post-driver section as shown in the layout sample below. Each section has its own function. Pre-driver provides logic operation for I/O circuit, and post-driver provides large driving capability and ESD protection ability.



The pre-driver section contains VDD and VSS ports. In which VDD is connecting to the 1.8V power ring of pre-driver and VSS is connecting to the ground of pre-driver respectively. The post-driver section contains various ports and their functions are connecting to the 3.3V power and ground ring of post-driver, and connecting to various guard ring for latch-up and ESD protection purposes.

Note that SMIC SP018 I/O uses both 1.8V (VDD) and 3.3V (VDD33) power supplies to adept its 1.8V input of core logic and 3.3V output signal with 5V tolerant. 5V tolerant means maximum supply voltage can be handled by the I/O is up to 5V. For noise immunity consideration, ground power supplies separated into two parts where VSS for pre-driver section and VSSD for post-driver section.



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FP is stand for ‘From Power Pad’ and FP pin is for global signal. Under normal condition, FP is activated by PVDD2 to ‘HIGH’ (3.3V). FP rail will be automatically connected while joining with other digital I/O cells.

4. Cell Categories

Cell categories of digital and analog I/O cells and their functions description are listed in Table 4. The suffix of cell means the drive strength and x can be 2, 4, 8, 12, 16 and 24. For examples, PB2 means the drive strength is 2mA and PB24 mean the drive strength is 24mA.

Table 4. Cell categories

Cells	Function Description of Digital I/O Cells
Name	
PCKHI1	High drive, internal CMOS clock buffer (Not Ready)
PCKHI2	High drive, internal CMOS clock buffer (Not Ready)
PCKHI3	High drive, internal CMOS clock buffer (Not Ready)
PCKHIS1	High drive, with internal Schmitt trigger clock buffer (Not Ready)
PCKHIS2	High drive, with internal Schmitt trigger clock buffer (Not Ready)
PCKHIS3	High drive, with internal Schmitt trigger clock buffer (Not Ready)
PCKI1	Very fast, internal clock buffer (Not Ready)
PCKI2	Very fast, internal clock buffer (Not Ready)
PCKI3	Very fast, internal clock buffer (Not Ready)
PCKI4	Very fast, internal clock buffer (Not Ready)
PCKI5	Very fast, internal clock buffer (Not Ready)
PCKI6	Very fast, internal clock buffer (Not Ready)
PCKHP1	High drive, CMOS input clock Pad (Not Ready)
PCKHP2	High drive, CMOS input clock Pad (Not Ready)
PCKHP3	High drive, CMOS input clock Pad (Not Ready)
PCKHPS1	High drive, Schmitt trigger input clock pad (Not Ready)
PCKHPS2	High drive, Schmitt trigger input clock pad (Not Ready)
PCKHPS3	High drive, Schmitt trigger input clock pad (Not Ready)
PID	Input pad with pull down
PISD	Schmitt trigger input pad with pull down
PICD	Input pad with enable controlled pull down



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PI	Input pad
PIS	Schmitt trigger input pad
PIU	Input pad with pull-up
PISU	Schmitt trigger input pad with pull-up
PICU	Input pad with enable controlled pull-up
PXWE1	Crystal oscillator with high enable
PXWE2	Crystal oscillator with high enable
PXWE3	Crystal oscillator with high enable
PX1	Crystal oscillator
PX2	Crystal oscillator
PX3	Crystal oscillator
PXWER1	Crystal oscillator with high enable and feedback resister (Not Ready)
PXWER2	Crystal oscillator with high enable and feedback resister (Not Ready)
PXWER3	Crystal oscillator with high enable and feedback resister (Not Ready)
PXWR1	Crystal oscillator with feedback resister (Not Ready)
PXWR2	Crystal oscillator with feedback resister (Not Ready)
PXWR3	Crystal oscillator with feedback resister (Not Ready)
PVDD1	Vdd power pad for I/O pre-driver & core
PVDD2	Vdd power pad for I/O post-driver
PVSS1	Vss ground pad for I/O pre-driver & core
PVSS2	Vss ground pad for I/O post-driver
PVSS3	Vss ground pad for ALL (I/O pre-driver, post-driver & core)

SMIC PCI is complies with PCI Local Bus Specification, Revision 2.2. PCI3B has same functionality as PCI6B, however PCI3B will consume more power and slower than PCI6B. In addition, please note that, a 66 MHz PCI device operates as a 33MHz PCI device when it is connected to a 33MHz PCI bus. Similarly, if any 33 MHz PCI devices are connected to a 66 MHz PCI bus, the 66 MHz PCI bus will operate as a 33 MHz PCI bus. Thus right choice of PCI pads is totally depend on user's specific implement.

Cells	Function Description of Digital Bi-input I/O Cells
Name	
PCI3B	3-state, output 33Mhz,pci buffer pad with input and limited slew rate
PCI3BS	3-state, output 33Mhz,pci buffer pad with Schmitt trigger input and limited slew rate
PCI6B	3-state, output 66Mhz,pci buffer pad with input and limited slew rate
PCI6BS	3-state, output 66Mhz,pci buffer pad with Schmitt trigger input and limited slew rate



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PB2	CMOS 3-state output pad with input
PB4	CMOS 3-state output pad with input
PB8	CMOS 3-state output pad with input
PB12	CMOS 3-state output pad with input
PB16	CMOS 3-state output pad with input
PB24	CMOS 3-state output pad with input
PBS2	CMOS 3-state output pad with Schmitt trigger input
PBS4	CMOS 3-state output pad with Schmitt trigger input
PBS8	CMOS 3-state output pad with Schmitt trigger input
PBS12	CMOS 3-state output pad with Schmitt trigger input
PBS16	CMOS 3-state output pad with Schmitt trigger input
PBS24	CMOS 3-state output pad with Schmitt trigger input
PBCD2	3-state output pad with input and enable controlled pull down
PBCD4	3-state output pad with input and enable controlled pull down
PBCD8	3-state output pad with input and enable controlled pull down
PBCD12	3-state output pad with input and enable controlled pull down
PBCD16	3-state output pad with input and enable controlled pull down
PBCD24	3-state output pad with input and enable controlled pull down
PBD2	CMOS 3-state output pad with input and pull down
PBD4	CMOS 3-state output pad with input and pull down
PBD8	CMOS 3-state output pad with input and pull down
PBD12	CMOS 3-state output pad with input and pull down
PBD16	CMOS 3-state output pad with input and pull down
PBD24	CMOS 3-state output pad with input and pull down
PBSD2	CMOS 3-state output pad with Schmitt trigger input and pull down
PBSD4	CMOS 3-state output pad with Schmitt trigger input and pull down
PBSD8	CMOS 3-state output pad with Schmitt trigger input and pull down
PBSD12	CMOS 3-state output pad with Schmitt trigger input and pull down
PBSD16	CMOS 3-state output pad with Schmitt trigger input and pull down
PBSD24	CMOS 3-state output pad with Schmitt trigger input and pull down
PO2	CMOS output pad
PO4	CMOS output pad
PO8	CMOS output pad
PO12	CMOS output pad
PO16	CMOS output pad
PO24	CMOS output pad
POT2	CMOS 3-state output pad
POT4	CMOS 3-state output pad
POT8	CMOS 3-state output pad
POT12	CMOS 3-state output pad



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POT16	CMOS 3-state output pad
POT24	CMOS 3-state output pad
PBCU2	3-state output pad with input and enable controlled pull-up
PBCU4	3-state output pad with input and enable controlled pull-up
PBCU8	3-state output pad with input and enable controlled pull-up
PBCU12	3-state output pad with input and enable controlled pull-up
PBCU16	3-state output pad with input and enable controlled pull-up
PBCU24	3-state output pad with input and enable controlled pull-up
PBU2	CMOS 3-state output pad with input and pull-up
PBU4	CMOS 3-state output pad with input and pull-up
PBU8	CMOS 3-state output pad with input and pull-up
PBU12	CMOS 3-state output pad with input and pull-up
PBU16	CMOS 3-state output pad with input and pull-up
PBU24	CMOS 3-state output pad with input and pull-up
PBSU2	CMOS 3-state output pad with Schmitt trigger input and pull-up
PBSU4	CMOS 3-state output pad with Schmitt trigger input and pull-up
PBSU8	CMOS 3-state output pad with Schmitt trigger input and pull-up
PBSU12	CMOS 3-state output pad with Schmitt trigger input and pull-up
PBSU16	CMOS 3-state output pad with Schmitt trigger input and pull-up
PBSU24	CMOS 3-state output pad with Schmitt trigger input and pull-up
PBL8	CMOS 3-state output pad with input and limited slew rate
PBL12	CMOS 3-state output pad with input and limited slew rate
PBL16	CMOS 3-state output pad with input and limited slew rate
PBL24	CMOS 3-state output pad with input and limited slew rate
PBSL8	CMOS 3-state output pad with Schmitt trigger input and limited slew rate
PBSL12	CMOS 3-state output pad with Schmitt trigger input and limited slew rate
PBSL16	CMOS 3-state output pad with Schmitt trigger input and limited slew rate
PBSL24	CMOS 3-state output pad with Schmitt trigger input and limited slew rate
PBCDL8	3-state output pad with input, limited slew rate and enable controlled pull down
PBCDL12	3-state output pad with input, limited slew rate and enable controlled pull down
PBCDL16	3-state output pad with input, limited slew rate and enable controlled pull down
PBCDL24	3-state output pad with input, limited slew rate and enable controlled pull down



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PBDL8	CMOS 3-state output pad with input, pull down, and limited slew rate
PBDL12	CMOS 3-state output pad with input, pull down, and limited slew rate
PBDL16	CMOS 3-state output pad with input, pull down, and limited slew rate
PBDL24	CMOS 3-state output pad with input, pull down, and limited slew rate
PBSDL8	CMOS 3-state output pad with Schmitt trigger input, pull down, and limited slew rate
PBSDL12	CMOS 3-state output pad with Schmitt trigger input, pull down, and limited slew rate
PBSDL16	CMOS 3-state output pad with Schmitt trigger input, pull down, and limited slew rate
PBSDL24	CMOS 3-state output pad with Schmitt trigger input, pull down, and limited slew rate
POL8	CMOS output pad with limited slew rate
POL12	CMOS output pad with limited slew rate
POL16	CMOS output pad with limited slew rate
POL24	CMOS output pad with limited slew rate
POTL8	CMOS 3-state output pad with limited slew rate
POTL12	CMOS 3-state output pad with limited slew rate
POTL16	CMOS 3-state output pad with limited slew rate
POTL24	CMOS 3-state output pad with limited slew rate
PBCUL8	3-state output pad with input, limited slew rate and enable controlled pull-up
PBCUL12	3-state output pad with input, limited slew rate and enable controlled pull-up
PBCUL16	3-state output pad with input, limited slew rate and enable controlled pull-up
PBCUL24	3-state output pad with input, limited slew rate and enable controlled pull-up
PBUL8	CMOS 3-state output pad with input, pull-up, and limited slew rate
PBUL12	CMOS 3-state output pad with input, pull-up, and limited slew rate
PBUL16	CMOS 3-state output pad with input, pull-up, and limited slew rate
PBUL24	CMOS 3-state output pad with input, pull-up, and limited slew rate
PBSUL8	CMOS 3-state output pad with Schmitt trigger input, pull-up, and limited slew rate
PBSUL12	CMOS 3-state output pad with Schmitt trigger input, pull-up, and limited slew rate
PBSUL16	CMOS 3-state output pad with Schmitt trigger input, pull-up, and limited slew rate
PBSUL24	CMOS 3-state output pad with Schmitt trigger input, pull-up, and limited slew rate



Note: SMIC does not recommend customers to use this library to interface with non-SMIC analog macros. Misuse of the analog library may cause damages to customer's product.

Cells Name	Function Description of Analog I/O Cells**
PANA2AP	Analog IO pad used with power-cut cell for high frequency application
PANA2AP1	Similar to PANA2AP but utilizes a different post-driver power
PANA1AP	Analog IO pad used with power-cut cell for low frequency application
PANA1AP1	Similar to PANA1AP but utilizes a different post-driver power
PDIODE	Power-Cut Cell for same voltage level between digital and analog
PDIODE8	Power-Cut Cell for High Voltage Drop for difference voltage level between digital and analog
PVDD3AP	VDD analog PAD
PVSS3AP	VSS analog PAD
PVDD1AP	VDD analog PAD
PVSS1AP	VSS analog PAD
PVDD5AP	VDD analog PAD
PVSS5AP	VSS analog PAD
PVDD1AP1	VDD analog PAD
PVSS1AP1	VSS analog PAD
PVDD4AP	VDD analog PAD
PVSS4AP	VSS analog PAD
PVDD2AP	VDD analog PAD
PVSS2AP	VSS analog PAD
PVDD1CAP	VDD analog PAD (for 1.8v)
PVDD1CAP1	VDD analog PAD (for 1.8v)
PVSS1CAP	VSS analog PAD (for 1.8v)
PVSS1CAP1	VSS analog PAD (for 1.8v)
PVSS3CAP	VSS analog PAD (for 1.8v)
PVDD3CAP	VDD analog PAD (for 1.8v)
PANA4AP	Analog IO pad used with power-cut cell for high frequency



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	application and higher maximum allowable current capability
PANA3AP	Analog IO pad used with power-cut cell for high frequency application and 5V tolerance
PVDD1ANP	VDD analog PAD within digital power domain
PVSS1ANP	VSS analog PAD within digital power domain

**Please refer to application note for more information.

Cells Name	Function Description of Filler Cells
PADI40	PAD
PAD040	PAD
PADI45	PAD
PADI50	PAD
PADI55	PAD
PADI60	PAD
PADI65	PAD
PCORNER	Corner cell
PFILL001	Filler cell
PFILL01	Filler cell
PFILL1	Filler cell
PFILL10	Filler cell
PFILL2	Filler cell
PFILL20	Filler cell
PFILL22	Filler cell
PFILL5	Filler cell
PFILL50	Filler cell
PFILL001A	Filler cell for analog IO cells
PFILL01A	Filler cell for analog IO cells
PFILL10A	Filler cell for analog IO cells
PFILL1A	Filler cell for analog IO cells
PFILL20A	Filler cell for analog IO cells
PFILL2A	Filler cell for analog IO cells
PFILL50A	Filler cell for analog IO cells
PFILL5A	Filler cell for analog IO cells



5. DC and AC Specification

This section provided DC and AC information of I/O library. It includes recommended operating conditions and the absolute maximum rating conditions for the I/O library. The device should be operated under recommended operating condition. Since, absolute maximum rating condition can either caused device reliability problem or damage the device sufficiently to cause immediate failure. ESD of SP018 library meets HBM-2KV and MM-200V.

5.1 DC Specifications

The I/O library is LVTTL/LVC MOS compatible, recommended DC operating conditions and electrical characteristics are listed in Table 5. The Absolute Maximum Ratings Condition is shown in Table 6.

Table 5. Recommended Operating Conditions

Symbol	Parameter	Min.	Norm	Max
VDD	Pre-driver supply voltage	1.62V	1.8V	1.98V
VDD33	I/O supply voltage	2.97V	3.3V	3.63V
V _{IH}	Input High Voltage	1.5V		5.5V
V _{IL}	Input Low Voltage	-0.3V		1.2V
V _T	Threshold point	1.37V	1.46V	1.58V
V _{T+}	Schmitt trig Low to High threshold point	1.44V	1.50V	1.56V
V _{T-}	Schmitt trig. High to Low threshold point	0.88V	0.94V	0.99V
T _J	Junction Temperature	0 °C	25°C	125°C
I _L	Input Leakage Current			±10uA
I _{OZ}	Tri-State output leakage current			±10uA
R _{PU}	Pull-up Resistor	39kohm	65kohm	116kohm
R _{PD}	Pull-down Resistor	40kohm	56kohm	108kohm
V _{OL}	Output low voltage @I _{OL} =2,4...24mA			0.4V
V _{OH}	Output high voltage @ I _{OH} =2,4...24mA	2.4V		
I _{OL}	Low level output current @V _{OL} =0.4V	2mA	2.3mA	4.0mA
		4mA	4.7mA	8.0mA
		8mA	9.4mA	15.8mA
		12mA	14.1mA	23.8mA
		16mA	18.8mA	31.7mA
		24mA	28.2mA	47.5mA
I _{OH}	High level output current @VOH=2.4V	2mA	2.8mA	9.3mA
		4mA	5.6mA	11.7mA
				18.6mA



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	8mA	11.1mA	23.4mA	37.3mA
	12mA	16.7mA	35.1mA	55.9mA
	16mA	22.3mA	46.8mA	74.5mA
	24mA	33.4mA	70.1mA	111.8mA

Table 6. Absolute Maximum Ratings

Parameters	Value
Input Voltage, VI	-0.5v~6v
Output Voltage, Vo	-0.5v~4.6v
Pre-driver power supply voltage	-0.5v~2.5v
Post-driver Power supply voltage	-0.5v~4.6v
Operation Temperature, T _{OPT}	-40°C~ +125°C
Storage Temperature, T _{STG}	-65°C~ +150°C

5.2 AC Specifications

AC specifications are characterized in four operating condition. Those are worst-case, typical-case, best-case and low temperature conditions. The detail of each condition is listed in the Table 7.

Table 7. AC Characterization Condition

Type	Condition
Typical case	VDD33=3.3V, VDD=1.8V temperature=25°C Process = Typical-Typical
Best case	VDD33=3.63V, VDD=1.98V temperature=0°C Process = Fast-Fast
Worst case	VDD33=2.97V, VDD=1.62V temperature=125°C Process =Slow-Slow
Low temperature	VDD33=3.63V, VDD=1.98V temperature=-40°C Process = Fast-Fast

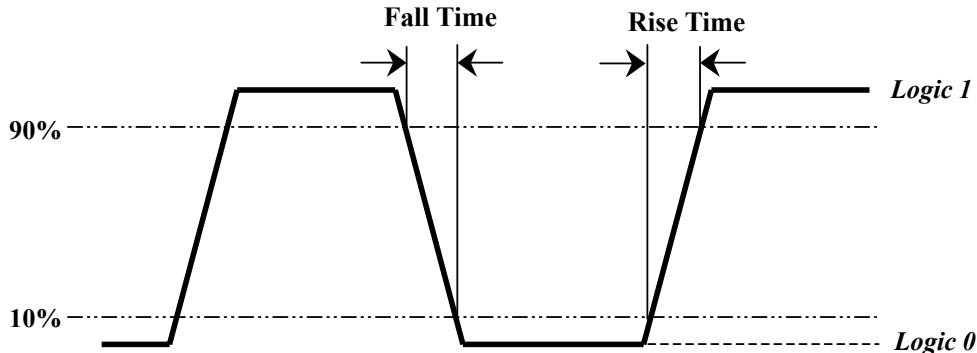
5.3 Timing Parameters

The timing parameters that are used in cell characterization are transition time (Rise/Fall) and Propagation time delay. These two important parameters are addressed in the next section.

Transition Time (Rise/Fall)

The rise time is defined as the transition time from output logic low to logic high. Conversely, the fall time, also defined as the transition time from output logic high to output logic low. This transition time is measured at specified percentages (10% ~ 90%) of the output waveform amplitude (refer to Figure 1).

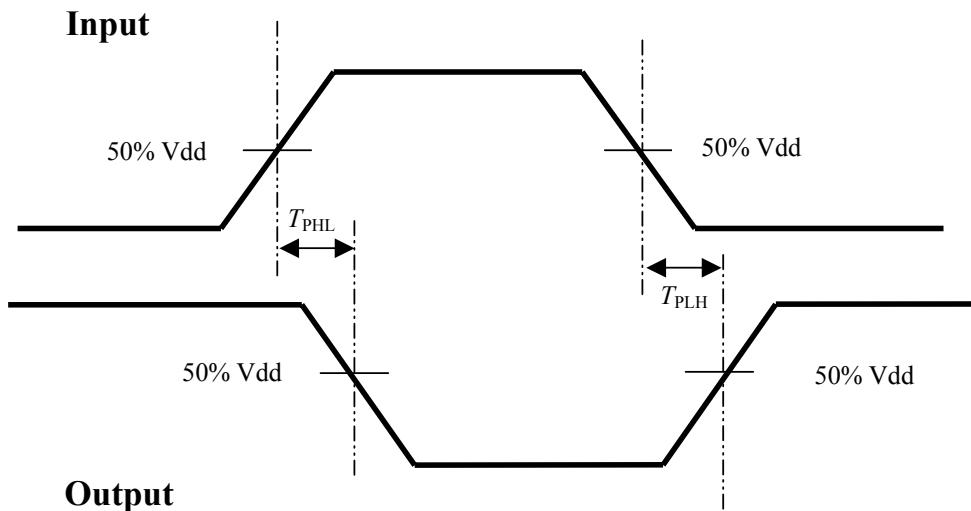
Figure 1. Rise/Fall Transition Time



Propagation Delays

Propagation delays are time delays inherent in all switching circuits. It is the minimum time required for data to be propagated from the input of the cell to the output. The propagation delay time T_{PHL} and T_{PLH} determine the input-to-output signal delay during the high-to-low and low-to-high transitions of the output, respectively. By definition, it is the time from the point where the input transition reaches 50% of the supply voltage to the point where the output transition reaches 50% of the supply voltage (Refer to Figure 2). If the input triggers the rising output, the propagation delay is referred to as a rising delay (T_{PLH}). If the input triggers the falling output, the delay is referred to as a falling delay (T_{PHL}).

Figure 2. Propagation delay of data signal at input/output of the cell





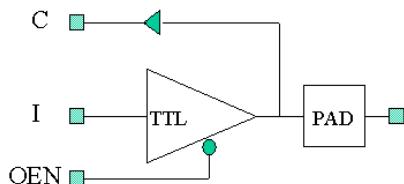
6. Data Sheet

Notice: Pin Capacitance values are NOT READY YET

PCI3B

PCI3B

3-STATE OUTPUT 33MHz PCI BUFFER PAD WITH INPUT
AND LIMITED SLEW RATE, 5V-Tolerant



● Truth Table

OEN	Input		Output	
	I	PAD	C	
1	x	0	0	
1	x	1	1	
1	x	Z	x	
0	0	0	0	
0	1	1	1	

● Cell Information

Cell Name	No.Pad Req.	Power(μ W/MHz)
PCI3B	1	384



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● Pin Capacitance (pF)

Cell Name	C	I	OEN	PAD
PCI3B				

PCI3B

*3-STATE OUTPUT 33MHz PCI BUFFER PAD WITH
INPUT AND LIMITED SLEW RATE, 5V-Tolerant*

● Propagation Delay(ns)

VDD_IO=3.3V, VDD_CORE=1.8V, temperature=25 °C , typical process, standard load=0.00699 pf, input slew time=0.06ns (measured from 10% to 90% transition)

Cell	delay_path	Sample Loads (pf)				Performance Equation
		10	30	50	125	
PCI3B	I->PAD (fall)	1. 965	2. 454	2. 866	4. 241	0. 0196*Cload+1. 828
PCI3B	I->PAD (rise)	1. 854	2. 319	2. 715	4. 089	0. 0193*Cload+1. 7068
PCI3B	OEN->PAD (fall)	1. 413	2. 091	2. 59	4. 101	0. 0230*Cload+1. 3125
PCI3B	OEN->PAD (rise)	1. 385	1. 989	2. 448	3. 934	0. 022*Cload+1. 2565

Cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PCI3B	PAD->C (fall)	0. 2653	0. 2687	0. 2749	0. 288	0. 2360*Cload+0. 2659
PCI3B	PAD->C (rise)	0. 2549	0. 257	0. 2614	0. 2714	0. 1731*Cload+0. 2551

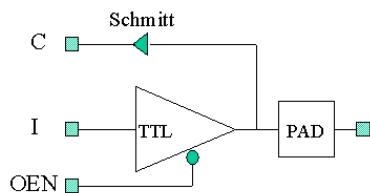


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PCI3BS

PCI3BS

*3-STATE OUTPUT 33MHz PCI BUFFER PAD WITH
INPUT AND LIMITED SLEW RATE, 5V-Tolerant*



● Truth Table

Input		Output	
OEN	I	PAD	C
1	x	0	0
1	x	1	1
1	x	Z	x
0	0	0	0
0	1	1	1

● Cell Information

Cell Name	No.Pad Req.	Power(μ W/MHz)
PCI3BS	1	392.6



Semiconductor Manufacturing International (Shanghai) Corporation

● Pin Capacitance (pF)

Cell Name	C	I	OEN	PAD
PCI3BS				

PCI3BS

*3-STATE OUTPUT 33MHz PCI BUFFER PAD WITH
INPUT AND LIMITED SLEW RATE, 5V-Tolerant*

● Propagation Delay(ns)

VDD_IO=3.3V, VDD_CORE=1.8V, temperature=25 °C , typical process, standard load=0.00699 pf, input slew time=0.06ns (measured from 10% to 90% transition)

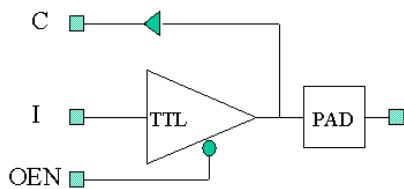
cell	delay_path	Sample Loads (pf)				Performance Equation
		10	30	50	125	
PCI3BS	I->PAD (fall)	1. 964	2. 454	2. 866	4. 241	0. 0196*Cload+1. 8277
PCI3BS	I->PAD (rise)	1. 853	2. 318	2. 714	4. 088	0. 0193*Cload+1. 7058
PCI3BS	OEN->PAD (fall)	1. 412	2. 09	2. 589	4. 101	0. 0230*Cload+1. 3117
PCI3BS	OEN->PAD (rise)	1. 384	1. 988	2. 447	3. 933	0. 022*Cload+1. 2555

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PCI3BS	PAD->C (fall)	0. 4542	0. 4565	0. 4613	0. 4722	0. 1888*Cload+0. 4544
PCI3BS	PAD->C (rise)	0. 4199	0. 4226	0. 4275	0. 4349	0. 1444*Cload+0. 4211



PCI6B

3-STATE OUTPUT 33MHz PCI BUFFER PAD WITH INPUT AND LIMITED SLEW RATE,
5V-Tolerant



● Truth Table

Input		Output	
OEN	I	PAD	C
1	x	0	0
1	x	1	1
1	x	Z	x
0	0	0	0
0	1	1	1

● Cell Information

Cell Name	No.Pad Req.	Power(μ W/MHz)
PCI6B	1	303



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● Pin Capacitance (pF)

Cell Name	C	I	OEN	PAD
PCI6B				
<i>3-STATE OUTPUT 33MHz PCI BUFFER PAD WITH INPUT AND LIMITED SLEW RATE, 5V-Tolerant</i>				

● Propagation Delay(ns)

VDD_IO=3.3V, VDD_CORE=1.8V, temperature=25 °C , typical process, standard load=0.00699 pf, input slew time=0.06ns (measured from 10% to 90% transition)

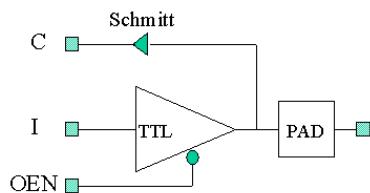
cell	delay_path	Sample Loads (pf)				Performance Equation
		10	30	50	125	
PCI6B	I->PAD (fall)	1. 641	2. 127	2. 538	3. 95	0. 0199*Cload+1. 4943
PCI6B	I->PAD (rise)	1. 532	1. 959	2. 332	3. 66	0. 0184*Cload+1. 3817
PCI6B	OEN->PAD (fall)	1. 348	1. 97	2. 434	3. 895	0. 0219*Cload+1. 2346
PCI6B	OEN->PAD (rise)	1. 23	1. 719	2. 129	3. 542	0. 0200*Cload+1. 08

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PCI6B	PAD->C (fall)	0. 2653	0. 2687	0. 2749	0. 288	0. 2360*Cload+0. 2659
PCI6B	PAD->C (rise)	0. 2549	0. 257	0. 2614	0. 2714	0. 1731*Cload+0. 2551



PCI6BS

*3-STATE OUTPUT 33MHz PCI BUFFER PAD WITH
INPUT AND LIMITED SLEW RATE, 5V-Tolerant*



● Truth Table

		Input	Output	
OEN	I	PAD	C	
1	x	0	0	
1	x	1	1	
1	x	Z	x	
0	0	0	0	
0	1	1	1	

● Cell Information

Cell Name	No.Pad Req.	Power(μ W/MHz)
PCI6BS	1	300.3



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● Pin Capacitance (pF)

Cell Name	C	I	OEN	PAD
PCI6BS				

PCI6BS

*3-STATE OUTPUT 33MHz PCI BUFFER PAD WITH
INPUT AND LIMITED SLEW RATE, 5V-Tolerant*

● Propagation Delay(ns)

VDD_IO=3.3V, VDD_CORE=1.8V, temperature=25 °C , typical process, standard load=0.00699 pf, input slew time=0.06ns (measured from 10% to 90% transition)

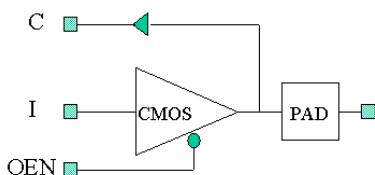
cell	delay_path	Sample Loads (pf)				Performance Equation
		10	30	50	125	
PCI6BS	I->PAD (fall)	1. 641	2. 127	2. 538	3. 95	0. 0199*Cload+1. 4943
PCI6BS	I->PAD (rise)	1. 531	1. 958	2. 331	3. 659	0. 0184*Cload+1. 3807
PCI6BS	OEN->PAD (fall)	1. 347	1. 969	2. 433	3. 895	0. 0219*Cload+1. 2338
PCI6BS	OEN->PAD (rise)	1. 229	1. 718	2. 128	3. 541	0. 0200*Cload+1. 079

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PCI6BS	PAD->C (fall)	0. 4542	0. 4565	0. 4613	0. 4722	0. 1888*Cload+0. 4544
PCI6BS	PAD->C (rise)	0. 4199	0. 4226	0. 4275	0. 4349	0. 1444*Cload+0. 4211



PBx

CMOS 3-STATE OUTPUT PAD WITH INPUT, 5V-Tolerant



● Truth Table

		Input		Output	
OEN	I	PAD	C		
1	x	0	0		
1	x	1	1		
1	x	Z	x		
0	0	0	0		
0	1	1	1		

● Cell Information

Cell Name	No.Pad Req.	Power(μ W/MHz)
PB2	1	83.7
PB4	1	96.72
PB8	1	97.99
PB12	1	110.6
PB16	1	107.2
PB24	1	121.7

Note: The suffix of cell means its drive strength, for examples, PB2 means the drive strength is 2mA and PB24 means the drive strength is 24mA.



● Pin Capacitance (pF)

Cell Name	C	I	OEN	PAD
PB2				
PB4				
PB8				
PB12				
PB16				
PB24				

● Propagation Delay(ns)

VDD_IO=3.3V, VDD_CORE=1.8V, temperature=25 °C , typical process, standard load=0.00699 pf, input slew time=0.06ns (measured from 10% to 90% transition)

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PB2	PAD->C (fall)	0.2888	0.2944	0.297	0.3081	0.2389*Cload+0.2887
	PAD->C (rise)	0.3392	0.3452	0.3515	0.3593	0.1974*Cload+0.3419
cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PB2	I->PAD (fall)	2.988	6.618	10.22	23.59	0.1789*Cload+1.2381
PB2	I->PAD (rise)	2.947	6.632	10.26	23.79	0.1812*Cload+1.1677
PB2	OEN->PAD (fall)	2.824	6.454	10.05	23.42	0.1789*Cload+1.0711
PB2	OEN->PAD (rise)	2.969	6.625	10.25	23.77	0.1808*Cload+1.1855
cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PB4	PAD->C (fall)	0.2878	0.2933	0.296	0.3071	0.2374*Cload+0.2877
	PAD->C (rise)	0.3392	0.3452	0.3515	0.3593	0.1974*Cload+0.3419
cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PB4	I->PAD (fall)	1.822	3.63	5.427	12.13	0.0895*Cload+0.9416
PB4	I->PAD (rise)	1.744	3.597	5.427	12.22	0.0910*Cload+0.8557
PB4	OEN->PAD (fall)	1.727	3.535	5.332	12.04	0.0896*Cload+0.8425
PB4	OEN->PAD (rise)	1.774	3.613	5.432	12.21	0.0907*Cload+0.8821



cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PB8	PAD->C (fall)	0.288	0.2936	0.2961	0.3073	0.2403*Cload+0.2878
PB8	PAD->C (rise)	0.3432	0.3458	0.3505	0.3632	0.2188*Cload+0.3430
cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PB8	I->PAD (fall)	1.288	2.197	3.093	6.444	0.0448*Cload+0.8475
PB8	I->PAD (rise)	1.227	2.16	3.079	6.491	0.0457*Cload+0.7828
PB8	OEN->PAD (fall)	1.239	2.144	3.041	6.391	0.0447*Cload+0.8011
PB8	OEN->PAD (rise)	1.254	2.182	3.096	6.497	0.0455*Cload+0.8116

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PB12	PAD->C (fall)	0.2878	0.2933	0.296	0.3071	0.2374*Cload+0.2877
PB12	PAD->C (rise)	0.3432	0.3458	0.3505	0.3632	0.2188*Cload+0.3430
cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PB12	I->PAD (fall)	1.131	1.74	2.338	4.571	0.0299*Cload+0.8378
PB12	I->PAD (rise)	1.085	1.718	2.333	4.613	0.0306*Cload+0.7925
PB12	OEN->PAD (fall)	1.097	1.701	2.299	4.53	0.0298*Cload+0.805
PB12	OEN->PAD (rise)	1.106	1.735	2.348	4.621	0.0305*Cload+0.8131

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PB16	PAD->C (fall)	0.288	0.2936	0.2961	0.3073	0.2403*Cload+0.2878
PB16	PAD->C (rise)	0.3432	0.3458	0.3505	0.3632	0.2188*Cload+0.3430
cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PB16	I->PAD (fall)	1.071	1.527	1.977	3.652	0.0224*Cload+0.8527
PB16	I->PAD (rise)	1.035	1.525	1.991	3.704	0.0231*Cload+0.8221
PB16	OEN->PAD (fall)	1.041	1.496	1.944	3.618	0.0224*Cload+0.8207
PB16	OEN->PAD (rise)	1.053	1.54	2.003	3.712	0.0231*Cload+0.8353

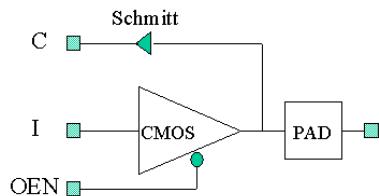


cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PB24	PAD->C (fall)	0.288	0.2906	0.2966	0.3099	$0.2274 * \text{Cload} + 0.2883$
PB24	PAD->C (rise)	0.3399	0.3422	0.3464	0.3554	$0.1616 * \text{Cload} + 0.3403$
cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PB24	I->PAD (fall)	1.131	1.45	1.752	2.87	$0.0151 * \text{Cload} + 0.9891$
PB24	I->PAD (rise)	1.094	1.453	1.774	2.925	$0.0158 * \text{Cload} + 0.9622$
PB24	OEN->PAD (fall)	1.107	1.425	1.727	2.843	$0.0150 * \text{Cload} + 0.9692$
PB24	OEN->PAD (rise)	1.1	1.456	1.775	2.923	$0.0158 * \text{Cload} + 0.9642$



PBSx

CMOS 3-STATE OUTPUT PAD WITH SCHMITT TRIGGER INPUT , 5V-Tolerant



● Truth Table

OEN	Input		Output	
	I	PAD	C	
1	x	0	0	
1	x	1	1	
1	x	Z	x	
0	0	0	0	
0	1	1	1	

● Cell Information

Cell Name	No.Pad Req.	Power(μ W/MHz)
PBS2	1	80.56
PBS4	1	89.9
PBS8	1	95.26
PBS12	1	97.35
PBS16	1	97.35
PBS24	1	123.6



● Pin Capacitance (pF)

Cell Name	C	I	OEN	PAD
PBS2				
PBS4				
PBS8				
PBS12				
PBS16				
PBS24				

● Propagation Delay(ns)

VDD_IO=3.3V, VDD_CORE=1.8V, temperature=25 °C , typical process, standard load=0.00699 pf, input slew time=0.06ns (measured from 10% to 90% transition)

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBS2	PAD->C (fall)	0.4483	0.451	0.4571	0.4704	0.2288*Cload+0.4487
PBS2	PAD->C (rise)	0.495	0.498	0.5026	0.5108	0.1602*Cload+0.4960
cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBS2	I->PAD (fall)	2.985	6.615	10.21	23.58	0.1789*Cload+1.2316
PBS2	I->PAD (rise)	2.942	6.626	10.26	23.79	0.1812*Cload+1.165
PBS2	OEN->PAD (fall)	2.821	6.451	10.05	23.42	0.1789*Cload+1.0696
PBS2	OEN->PAD (rise)	2.965	6.619	10.24	23.77	0.1808*Cload+1.1805
cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBS4	PAD->C (fall)	0.4441	0.4481	0.4572	0.4636	0.1487*Cload+0.4480
PBS4	PAD->C (rise)	0.495	0.498	0.5026	0.5108	0.1602*Cload+0.4960
cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBS4	I->PAD (fall)	1.82	3.629	5.426	12.13	0.0896*Cload+0.9352
PBS4	I->PAD (rise)	1.743	3.595	5.424	12.22	0.0910*Cload+0.8542



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PBS4	OEN->PAD (fall)	1.726	3.533	5.33	12.03 0.0895*Cload+0.8441
PBS4	OEN->PAD (rise)	1.772	3.61	5.43	12.21 0.0907*Cload+0.8803

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBS8	PAD->C (fall)	0.4508	0.4531	0.4578	0.4685 0.1859*Cload+0.4510	
PBS8	PAD->C (rise)	0.495	0.498	0.5026	0.5108 0.1602*Cload+0.4960	
cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBS8	I->PAD (fall)	1.287	2.196	3.093	6.443 0.0448*Cload+0.8467	
PBS8	I->PAD (rise)	1.226	2.159	3.078	6.49 0.0457*Cload+0.7818	
PBS8	OEN->PAD (fall)	1.238	2.144	3.04	6.39 0.0448*Cload+0.795	
PBS8	OEN->PAD (rise)	1.253	2.181	3.095	6.496 0.0455*Cload+0.8106	

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBS12	PAD->C (fall)	0.4441	0.4481	0.4572	0.4636 0.1487*Cload+0.4480	
PBS12	PAD->C (rise)	0.495	0.498	0.5026	0.5108 0.1602*Cload+0.4960	
cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBS12	I->PAD (fall)	1.13	1.739	2.338	4.57 0.0299*Cload+0.8371	
PBS12	I->PAD (rise)	1.084	1.717	2.332	4.612 0.0306*Cload+0.7915	
PBS12	OEN->PAD (fall)	1.096	1.7	2.298	4.53 0.0298*Cload+0.8042	
PBS12	OEN->PAD (rise)	1.105	1.735	2.348	4.621 0.0305*Cload+0.8128	

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBS16	PAD->C (fall)	0.4441	0.4481	0.4572	0.4636 0.1487*Cload+0.4480	
PBS16	PAD->C (rise)	0.495	0.498	0.5026	0.5108 0.1602*Cload+0.4960	
cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBS16	I->PAD (fall)	1.13	1.739	2.338	4.57 0.0299*Cload+0.8371	
PBS16	I->PAD (rise)	1.084	1.717	2.332	4.612 0.0306*Cload+0.7915	
PBS16	OEN->PAD (fall)	1.096	1.7	2.298	4.53 0.0298*Cload+0.8042	
PBS16	OEN->PAD (rise)	1.105	1.735	2.348	4.621 0.0305*Cload+0.8128	

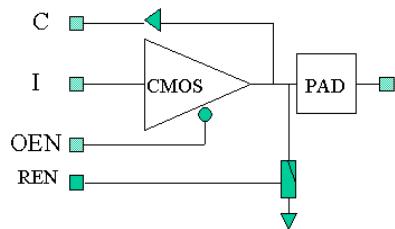


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cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBS24	PAD->C (fall)	0.4441	0.4481	0.4572	0.4636	$0.1487 * \text{Cload} + 0.4480$
PBS24	PAD->C (rise)	0.4931	0.4953	0.5001	0.5119	$0.2002 * \text{Cload} + 0.4931$
cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBS24	I->PAD (fall)	1.131	1.45	1.752	2.87	$0.0151 * \text{Cload} + 0.9891$
PBS24	I->PAD (rise)	1.094	1.453	1.773	2.925	$0.0159 * \text{Cload} + 0.9566$
PBS24	OEN->PAD (fall)	1.107	1.425	1.726	2.843	$0.0151 * \text{Cload} + 0.9636$
PBS24	OEN->PAD (rise)	1.099	1.456	1.775	2.923	$0.0158 * \text{Cload} + 0.964$

PBCDx

CMOS 3-STATE OUTPUT PAD WITH INPUT and CONTROLLABLE PULLDOWN,
5V-Tolerant



● Truth Table

Input			Output	
REN	OEN	I	PAD	C
x	1	x	0	0
x	1	x	1	1
0	1	x	pull-down	0
1	1	x	Z	x
x	0	0	0	0
x	0	1	1	1

● Cell Information

Cell Name	No.Pad Req.	Power(μ W/MHz)
PBCD2	1	75.88
PBCD4	1	89.59
PBCD8	1	96.57
PBCD12	1	103.3
PBCD16	1	106.6



PBCD24	1	122.6
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● Pin Capacitance (pF)

Cell Name	C	I	OEN	PAD
PBCD2				
PBCD4				
PBCD8				
PBCD12				
PBCD16				
PBCD24				

● Propagation Delay(ns)

VDD_IO=3.3V, VDD_CORE=1.8V, temperature=25 °C , typical process, standard load=0.00699 pf, input slew time=0.06ns (measured from 10% to 90% transition)

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBCD2	PAD->C (fall)	0.2885	0.2939	0.2968	0.3078	0.2346*Cload+0.2885
PBCD2	PAD->C (rise)	0.3432	0.3456	0.3511	0.3596	0.1559*Cload+0.3444

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBCD2	I->PAD (fall)	2.988	6.618	10.22	23.59	0.1789*Cload+1.2381
PBCD2	I->PAD (rise)	2.947	6.632	10.26	23.79	0.1812*Cload+1.1677
PBCD2	OEN->PAD (fall)	2.823	6.454	10.05	23.42	0.1789*Cload+1.0708
PBCD2	OEN->PAD (rise)	2.97	6.625	10.25	23.77	0.1807*Cload+1.1911

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBCD4	PAD->C (fall)	0.2876	0.2929	0.2958	0.3068	0.2331*Cload+0.2876

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PBCD4	PAD->C (rise)	0.3432	0.3456	0.3511	0.3596 0.1559*Cload+0.3444
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cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	

PBCD4	I->PAD (fall)	1.822	3.63	5.427	12.13 0.0895*Cload+0.9416
PBCD4	I->PAD (rise)	1.744	3.597	5.427	12.22 0.0910*Cload+0.8557
PBCD4	OEN->PAD (fall)	1.727	3.535	5.332	12.04 0.0896*Cload+0.8425
PBCD4	OEN->PAD (rise)	1.774	3.613	5.432	12.21 0.0907*Cload+0.8821

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	

PBCD8	PAD->C (fall)	0.2877	0.2931	0.2959	0.3069 0.2346*Cload+0.2877
PBCD8	PAD->C (rise)	0.3435	0.346	0.3511	0.3636 0.2145*Cload+0.3435

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	

PBCD8	I->PAD (fall)	1.288	2.197	3.093	6.444 0.0448*Cload+0.8475
PBCD8	I->PAD (rise)	1.227	2.16	3.079	6.491 0.0457*Cload+0.7828
PBCD8	OEN->PAD (fall)	1.239	2.144	3.041	6.391 0.0447*Cload+0.8011
PBCD8	OEN->PAD (rise)	1.254	2.182	3.097	6.497 0.0455*Cload+0.8118

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	

PBCD12	PAD->C (fall)	0.2876	0.2929	0.2958	0.3068 0.2331*Cload+0.2876
PBCD12	PAD->C (rise)	0.3435	0.346	0.3511	0.3636 0.2145*Cload+0.3435

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	

PBCD12	I->PAD (fall)	1.131	1.74	2.338	4.571 0.0299*Cload+0.8378
PBCD12	I->PAD (rise)	1.085	1.718	2.333	4.613 0.0306*Cload+0.7925
PBCD12	OEN->PAD (fall)	1.097	1.701	2.299	4.53 0.0298*Cload+0.805
PBCD12	OEN->PAD (rise)	1.106	1.735	2.348	4.621 0.0305*Cload+0.8131

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	

PBCD16	PAD->C (fall)	0.2877	0.2931	0.2959	0.3069 0.2346*Cload+0.2877
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PBCD16	PAD->C (rise)	0.3435	0.346	0.3511	0.3636 0.2145*Cload+0.3435
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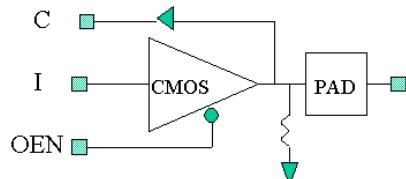
cell	delay_path	Sample Loads(pf)			Performance Equation
		10	30	50	
PBCD16	I->PAD (fall)	1.07	1.527	1.977	3.652 0.0224*Cload+0.8525
PBCD16	I->PAD (rise)	1.035	1.525	1.991	3.704 0.0231*Cload+0.8221
PBCD16	OEN->PAD (fall)	1.041	1.496	1.944	3.618 0.0224*Cload+0.8207
PBCD16	OEN->PAD (rise)	1.053	1.54	2.003	3.712 0.0231*Cload+0.8353

cell	delay_path	Standard Load			Performance Equation
		2	4	8	
PBCD24	PAD->C (fall)	0.2878	0.2904	0.2963	0.3096 0.2274*Cload+0.2880
PBCD24	PAD->C (rise)	0.3402	0.3425	0.3467	0.3557 0.1616*Cload+0.3406

cell	delay_path	Sample Loads(pf)			Performance Equation
		10	30	50	
PBCD24	I->PAD (fall)	1.131	1.45	1.752	2.87 0.0151*Cload+0.9891
PBCD24	I->PAD (rise)	1.094	1.453	1.774	2.925 0.0158*Cload+0.9622
PBCD24	OEN->PAD (fall)	1.107	1.425	1.727	2.843 0.0150*Cload+0.9692
PBCD24	OEN->PAD (rise)	1.1	1.456	1.775	2.923 0.0158*Cload+0.9642

PBDx

CMOS 3-STATE OUTPUT PAD WITH INPUT and PULLDOWN, 5V-Tolerant



● Truth Table

OEN	Input		PAD	Output	
	I	C			C
1	x		0		0
1	x		1		1
1	x		Z		0
0	0		0		0
0	1		1		1

● Cell Information

Cell Name	No.Pad Req.	Power(μ W/MHz)
PBD2	1	161.1
PBD4	1	165.4
PBD8	1	173
PBD12	1	179.5
PBD16	1	186.7
PBD24	1	197

● Pin Capacitance (pF)

Cell Name	C	I	OEN	PAD
PBD2				
PBD4				



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PBD8

PBD12

PBD16

PBD24

● Propagation Delay(ns)

VDD_IO=3.3V, VDD_CORE=1.8V, temperature=25 °C , typical process, standard load=0.00699 pf, input slew time=0.06ns (measured from 10% to 90% transition)

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBD2	PAD->C (fall)	0.2839	0.2862	0.2917	0.3045	0.2160*Cload+0.2840
PBD2	PAD->C (rise)	0.3498	0.3521	0.3577	0.3662	0.1545*Cload+0.3510

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBD2	I->PAD (fall)	2.962	6.56	10.13	23.38	0.1773*Cload+1.2281
PBD2	I->PAD (rise)	2.958	6.655	10.3	23.87	0.1817*Cload+1.1793
PBD2	OEN->PAD (fall)	2.701	6.313	9.892	23.19	0.178*Cload+0.9565
PBD2	OEN->PAD (rise)	2.98	6.647	10.28	23.85	0.1814*Cload+1.189

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBD4	PAD->C (fall)	0.2886	0.2908	0.2958	0.3076	0.2002*Cload+0.2887
PBD4	PAD->C (rise)	0.3498	0.3521	0.3577	0.3662	0.1545*Cload+0.3510

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBD4	I->PAD (fall)	1.814	3.615	5.404	12.08	0.0892*Cload+0.9337
PBD4	I->PAD (rise)	1.748	3.603	5.436	12.24	0.0911*Cload+0.8601
PBD4	OEN->PAD (fall)	1.67	3.472	5.265	11.95	0.0893*Cload+0.7893
PBD4	OEN->PAD (rise)	1.777	3.619	5.441	12.23	0.0908*Cload+0.8862



cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBD8	PAD->C (fall)	0.2841	0.2897	0.292	0.3033	0.2417*Cload+0.2838
PBD8	PAD->C (rise)	0.3498	0.3521	0.3577	0.3662	0.1545*Cload+0.3510

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBD8	I->PAD (fall)	1.286	2.192	3.087	6.43	0.0447*Cload+0.8461
PBD8	I->PAD (rise)	1.228	2.161	3.081	6.496	0.0457*Cload+0.7851
PBD8	OEN->PAD (fall)	1.211	2.115	3.01	6.356	0.0447*Cload+0.7703
PBD8	OEN->PAD (rise)	1.255	2.184	3.099	6.503	0.0456*Cload+0.8092

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBD12	PAD->C (fall)	0.2886	0.2908	0.2958	0.3076	0.2002*Cload+0.2887
PBD12	PAD->C (rise)	0.3498	0.3521	0.3577	0.3662	0.1545*Cload+0.3510

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBD12	I->PAD (fall)	1.13	1.738	2.335	4.564	0.0298*Cload+0.84
PBD12	I->PAD (rise)	1.085	1.718	2.334	4.616	0.0306*Cload+0.7935
PBD12	OEN->PAD (fall)	1.078	1.682	2.279	4.509	0.0298*Cload+0.7852
PBD12	OEN->PAD (rise)	1.106	1.736	2.35	4.624	0.0305*Cload+0.8146

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBD16	PAD->C (fall)	0.2886	0.2908	0.2958	0.3076	0.2002*Cload+0.2887
PBD16	PAD->C (rise)	0.3498	0.3521	0.3577	0.3662	0.1545*Cload+0.3510



cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBD16	I->PAD (fall)	1.07	1.526	1.976	3.648	0.0224*Cload+0.851
PBD16	I->PAD (rise)	1.035	1.526	1.991	3.706	0.0232*Cload+0.8175
PBD16	OEN->PAD (fall)	1.028	1.482	1.93	3.602	0.0223*Cload+0.8118
PBD16	OEN->PAD (rise)	1.054	1.54	2.004	3.713	0.0231*Cload+0.8361

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBD24	PAD->C (fall)	0.2886	0.2908	0.2958	0.3076	0.2002*Cload+0.2887
PBD24	PAD->C (rise)	0.3471	0.3496	0.355	0.3678	0.2188*Cload+0.3472

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBD24	I->PAD (fall)	1.13	1.449	1.752	2.868	0.0151*Cload+0.9881
PBD24	I->PAD (rise)	1.095	1.453	1.774	2.926	0.0158*Cload+0.9627
PBD24	OEN->PAD (fall)	1.097	1.416	1.717	2.833	0.0151*Cload+0.9541
PBD24	OEN->PAD (rise)	1.1	1.456	1.775	2.924	0.0158*Cload+0.9645

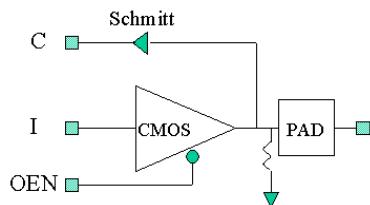


Semiconductor Manufacturing International (Shanghai) Corporation

PBSDx

PBSDx

CMOS 3-STATE OUTPUT PAD WITH SCHMITT TRIGGER INPUT and PULLDOWN,
5V-Tolerant



● Truth Table

		Input		Output	
OEN	I	PAD	C		
1	x	0	0		
1	x	1	1		
1	x	Z	0		
0	0	0	0		
0	1	1	1		

● Cell Information

Cell Name	No.Pad Req.	Power(μ W/MHz)
PBSD2	1	161.4
PBSD4	1	166.9
PBSD8	1	174.1
PBSD12	1	178.4
PBSD16	1	189
PBSD24	1	197



● Pin Capacitance (pF)

Cell Name	C	I	OEN	PAD
PBSD2				
PBSD4				
PBSD8				
PBSD12				
PBSD16				
PBSD24				

● Propagation Delay(ns)

VDD_IO=3.3V, VDD_CORE=1.8V, temperature=25 °C , typical process, standard load=0.00699 pf, input slew time=0.06ns (measured from 10% to 90% transition)

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBSD2	PAD->C (fall)	0.4509	0.4538	0.4584	0.4681	0.1802*Cload+0.4515
PBSD2	PAD->C (rise)	0.4996	0.502	0.5062	0.515	0.1602*Cload+0.5001

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBSD2	I->PAD (fall)	2.962	6.56	10.13	23.38	0.1773*Cload+1.2281
PBSD2	I->PAD (rise)	2.953	6.649	10.29	23.87	0.1818*Cload+1.1687
PBSD2	OEN->PAD (fall)	2.701	6.312	9.891	23.19	0.178*Cload+0.9560
PBSD2	OEN->PAD (rise)	2.975	6.642	10.28	23.85	0.1814*Cload+1.1865



cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBSD4	PAD->C (fall)	0.4516	0.4543	0.4588	0.4687	0.1802*Cload+0.4520
PBSD4	PAD->C (rise)	0.4996	0.502	0.5062	0.515	0.1602*Cload+0.5001

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBSD4	I->PAD (fall)	1.814	3.615	5.404	12.08	0.0892*Cload+0.9337
PBSD4	I->PAD (rise)	1.746	3.601	5.433	12.24	0.0911*Cload+0.8583
PBSD4	OEN->PAD (fall)	1.669	3.472	5.264	11.95	0.0893*Cload+0.7888
PBSD4	OEN->PAD (rise)	1.775	3.616	5.439	12.23	0.0908*Cload+0.8844

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBSD8	PAD->C (fall)	0.4552	0.4577	0.4635	0.4766	0.2231*Cload+0.4554
PBSD8	PAD->C (rise)	0.4996	0.502	0.5062	0.515	0.1602*Cload+0.5001

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBSD8	I->PAD (fall)	1.286	2.192	3.087	6.43	0.0447*Cload+0.8461
PBSD8	I->PAD (rise)	1.228	2.16	3.08	6.495	0.0457*Cload+0.7843
PBSD8	OEN->PAD (fall)	1.211	2.115	3.01	6.356	0.0447*Cload+0.7703
PBSD8	OEN->PAD (rise)	1.254	2.183	3.098	6.501	0.0456*Cload+0.808

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBSDL12	PAD->C (fall)	0.4516	0.4543	0.4588	0.4687	0.1802*Cload+0.4520
PBSDL12	PAD->C (rise)	0.4996	0.502	0.5062	0.515	0.1602*Cload+0.5001



cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBSD12	I->PAD (fall)	1.13	1.738	2.335	4.565	0.0298*Cload+0.8402
PBSD12	I->PAD (rise)	1.085	1.718	2.334	4.615	0.0306*Cload+0.7932
PBSD12	OEN->PAD (fall)	1.078	1.682	2.279	4.509	0.0298*Cload+0.7852
PBSD12	OEN->PAD (rise)	1.106	1.736	2.349	4.623	0.0305*Cload+0.8141

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBSDL16	PAD->C (fall)	0.4516	0.4543	0.4588	0.4687	0.1802*Cload+0.4520
PBSDL16	PAD->C (rise)	0.4996	0.502	0.5062	0.515	0.1602*Cload+0.5001

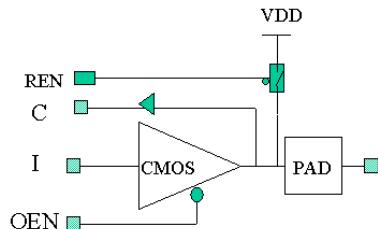
cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBSD16	I->PAD (fall)	1.07	1.526	1.976	3.648	0.0224*Cload+0.851
PBSD16	I->PAD (rise)	1.035	1.525	1.991	3.705	0.0232*Cload+0.817
PBSD16	OEN->PAD (fall)	1.027	1.481	1.93	3.602	0.0223*Cload+0.8113
PBSD16	OEN->PAD (rise)	1.053	1.54	2.003	3.713	0.0231*Cload+0.8356

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBSD24	PAD->C (fall)	0.4516	0.4543	0.4588	0.4687	0.1802*Cload+0.4520
PBSD24	PAD->C (rise)	0.4989	0.5014	0.5056	0.5143	0.1602*Cload+0.4994

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBSD24	I->PAD (fall)	1.13	1.449	1.751	2.868	0.0151*Cload+0.9878
PBSD24	I->PAD (rise)	1.094	1.453	1.774	2.925	0.0158*Cload+0.9622
PBSD24	OEN->PAD (fall)	1.097	1.415	1.717	2.833	0.0150*Cload+0.9592
PBSD24	OEN->PAD (rise)	1.099	1.456	1.775	2.923	0.0158*Cload+0.964

PBCUx

CMOS 3-STATE OUTPUT PAD WITH INPUT and CONTROLLABLE PULLUP, 5V-Tolerant



● Truth Table

Input			Output	
REN	OEN	I	PAD	C
x	1	x	0	0
x	1	x	1	1
0	1	x	pull-up	1
1	1	x	Z	x
x	0	0	0	0
x	0	1	1	1

● Cell Information

Cell Name	No.Pad Req.	Power(μ W/MHz)
PBCU2	1	86.78
PBCU4	1	85.77
PBCU8	1	95.08
PBCU12	1	100.4
PBCU16	1	112.8
PBCU24	1	125.4

● Pin Capacitance (pF)

Cell Name	C	I	OEN	PAD
PBCU2				



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PBCU4

PBCU8

PBCU12

PBCU16

PBCU24

● Propagation Delay(ns)

VDD_IO=3.3V, VDD_CORE=1.8V, temperature=25 °C , typical process, standard load=0.00699 pf, input slew time=0.06ns (measured from 10% to 90% transition)

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBCU2	PAD->C (fall)	0.2951	0.2974	0.302	0.3126	0.1845*Cload+0.2953
PBCU2	PAD->C (rise)	0.3434	0.3458	0.3513	0.3598	0.1559*Cload+0.3446

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBCU2	I->PAD (fall)	2.989	6.618	10.22	23.59	0.1789*Cload+1.2383
PBCU2	I->PAD (rise)	2.948	6.633	10.26	23.79	0.1812*Cload+1.1682
PBCU2	OEN->PAD (fall)	2.824	6.455	10.05	23.42	0.1789*Cload+1.0713
PBCU2	OEN->PAD (rise)	2.97	6.626	10.25	23.77	0.1808*Cload+1.186

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBCU4	PAD->C (fall)	0.2882	0.2914	0.298	0.311	0.2317*Cload+0.2890
PBCU4	PAD->C (rise)	0.3434	0.3458	0.3513	0.3598	0.1559*Cload+0.3446

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBCU4	I->PAD (fall)	1.822	3.63	5.427	12.13	0.0895*Cload+0.9416
PBCU4	I->PAD (rise)	1.745	3.598	5.427	12.22	0.0910*Cload+0.8562
PBCU4	OEN->PAD (fall)	1.728	3.535	5.332	12.04	0.0896*Cload+0.8427
PBCU4	OEN->PAD (rise)	1.775	3.613	5.433	12.21	0.0906*Cload+0.888



cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBCU8	PAD->C (fall)	0.2882	0.2914	0.298	0.311	0.2317*Cload+0.2890
PBCU8	PAD->C (rise)	0.3436	0.3461	0.3511	0.3636	0.2145*Cload+0.3436

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBCU8	I->PAD (fall)	1.288	2.197	3.094	6.444	0.0448*Cload+0.8477
PBCU8	I->PAD (rise)	1.227	2.16	3.079	6.491	0.0457*Cload+0.7828
PBCU8	OEN->PAD (fall)	1.239	2.144	3.041	6.391	0.0447*Cload+0.8011
PBCU8	OEN->PAD (rise)	1.254	2.182	3.097	6.498	0.0455*Cload+0.8121

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBCU12	PAD->C (fall)	0.2882	0.2914	0.298	0.311	0.2317*Cload+0.2890
PBCU12	PAD->C (rise)	0.3436	0.3461	0.3511	0.3636	0.2145*Cload+0.3436

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBCU12	I->PAD (fall)	1.131	1.74	2.338	4.571	0.0299*Cload+0.8378
PBCU12	I->PAD (rise)	1.085	1.718	2.333	4.613	0.0306*Cload+0.7925
PBCU12	OEN->PAD (fall)	1.097	1.701	2.299	4.531	0.0298*Cload+0.8052
PBCU12	OEN->PAD (rise)	1.106	1.736	2.349	4.622	0.0305*Cload+0.8138

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBCU16	PAD->C (fall)	0.2882	0.2914	0.298	0.311	0.2317*Cload+0.2890
PBCU16	PAD->C (rise)	0.3436	0.3461	0.3511	0.3636	0.2145*Cload+0.3436

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBCU16	I->PAD (fall)	1.07	1.527	1.978	3.652	0.0224*Cload+0.8527



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PBCU16	I->PAD (rise)	1.035	1.525	1.991	3.705 0.0232*Cload+0.817
PBCU16	OEN->PAD (fall)	1.041	1.496	1.945	3.618 0.0224*Cload+0.821
PBCU16	OEN->PAD (rise)	1.053	1.54	2.003	3.712 0.0231*Cload+0.8353

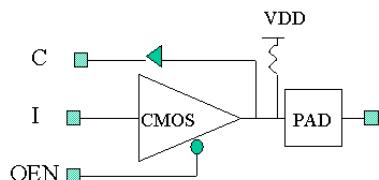
cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBCU24	PAD->C (fall)	0.2895	0.2924	0.2988	0.312	0.2303*Cload+0.2901
PBCU24	PAD->C (rise)	0.3401	0.3425	0.3467	0.3557	0.1630*Cload+0.3405

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBCU24	I->PAD (fall)	1.131	1.45	1.752	2.87	0.0151*Cload+0.9891
PBCU24	I->PAD (rise)	1.094	1.453	1.774	2.925	0.0158*Cload+0.9622
PBCU24	OEN->PAD (fall)	1.107	1.425	1.727	2.843	0.0150*Cload+0.9692
PBCU24	OEN->PAD (rise)	1.099	1.456	1.775	2.923	0.0158*Cload+0.964



PBUX

CMOS 3-STATE OUTPUT PAD WITH INPUT and PULLUP, 5V-Tolerant



● Truth Table

OEN	Input		PAD	Output	
	I	C		C	C
1	x		0	0	0
1	x		1	1	1
1	x		Z	1	1
0	0		0	0	0
0	1		1	1	1

● Cell Information

Cell Name	No.Pad Req.	Power(μ W/MHz)
PBU2	1	186.7
PBU4	1	191.9
PBU8	1	201.1
PBU12	1	206.8
PBU16	1	212
PBU24	1	229.5



● Pin Capacitance (pF)

Cell Name	C	I	OEN	PAD
PBU2				
PBU4				
PBU8				
PBU12				
PBU16				
PBU24				

● Propagation Delay(ns)

VDD_IO=3.3V, VDD_CORE=1.8V, temperature=25 °C , typical process, standard load=0.00699 pf, input slew time=0.06ns (measured from 10% to 90% transition)

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBU2	PAD->C (fall)	0.297	0.2992	0.3042	0.316	0.2002*Cload+0.2971
PBU2	PAD->C (rise)	0.339	0.3408	0.3511	0.359	0.1387*Cload+0.3426

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBU2	I->PAD (fall)	3.011	6.672	10.3	23.76	0.1802*Cload+1.25
PBU2	I->PAD (rise)	2.923	6.571	10.17	23.56	0.1793*Cload+1.1686
PBU2	OEN->PAD (fall)	2.847	6.508	10.13	23.59	0.1802*Cload+1.083
PBU2	OEN->PAD (rise)	2.883	6.516	10.11	23.55	0.1797*Cload+1.1058

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBU4	PAD->C (fall)	0.2943	0.2965	0.3014	0.3129	0.1959*Cload+0.2944
PBU4	PAD->C (rise)	0.339	0.3408	0.3511	0.359	0.1387*Cload+0.3426



cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBU4	I->PAD (fall)	1.827	3.644	5.449	12.18	0.0899*Cload+0.9428
PBU4	I->PAD (rise)	1.738	3.582	5.403	12.16	0.0905*Cload+0.8563
PBU4	OEN->PAD (fall)	1.733	3.549	5.353	12.08	0.0899*Cload+0.8466
PBU4	OEN->PAD (rise)	1.734	3.568	5.381	12.14	0.0904*Cload+0.8467

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBU8	PAD->C (fall)	0.2918	0.2945	0.3006	0.3139	0.2288*Cload+0.2922
PBU8	PAD->C (rise)	0.3427	0.3453	0.3497	0.3627	0.2231*Cload+0.3423

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBU8	I->PAD (fall)	1.289	2.2	3.099	6.456	0.0449*Cload+0.8476
PBU8	I->PAD (rise)	1.225	2.156	3.073	6.476	0.0456*Cload+0.7815
PBU8	OEN->PAD (fall)	1.24	2.148	3.046	6.403	0.0448*Cload+0.8012
PBU8	OEN->PAD (rise)	1.234	2.161	3.075	6.471	0.0455*Cload+0.7896

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBU12	PAD->C (fall)	0.29	0.2924	0.298	0.311	0.2203*Cload+0.2901
PBU12	PAD->C (rise)	0.3427	0.3453	0.3497	0.3627	0.2231*Cload+0.3423

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBU12	I->PAD (fall)	1.131	1.741	2.341	4.576	0.0299*Cload+0.8401
PBU12	I->PAD (rise)	1.084	1.716	2.33	4.607	0.0306*Cload+0.7895
PBU12	OEN->PAD (fall)	1.097	1.702	2.301	4.536	0.0298*Cload+0.8072
PBU12	OEN->PAD (rise)	1.091	1.722	2.334	4.606	0.0305*Cload+0.7988



cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBU16	PAD->C (fall)	0.29	0.2924	0.298	0.311	0.2203*Cload+0.2901
PBU16	PAD->C (rise)	0.3427	0.3453	0.3497	0.3627	0.2231*Cload+0.3423

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBU16	I->PAD (fall)	1.071	1.528	1.979	3.655	0.0224*Cload+0.8542
PBU16	I->PAD (rise)	1.034	1.524	1.989	3.701	0.0231*Cload+0.8203
PBU16	OEN->PAD (fall)	1.042	1.497	1.946	3.621	0.0224*Cload+0.8225
PBU16	OEN->PAD (rise)	1.042	1.53	1.993	3.701	0.0231*Cload+0.8248

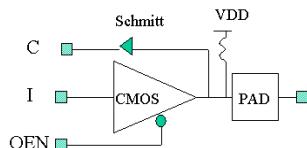
cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBU24	PAD->C (fall)	0.29	0.2924	0.298	0.311	0.2203*Cload+0.2901
PBU24	PAD->C (rise)	0.3393	0.3417	0.3459	0.3547	0.1602*Cload+0.3398

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBU24	I->PAD (fall)	1.131	1.45	1.753	2.872	0.0151*Cload+0.9898
PBU24	I->PAD (rise)	1.094	1.452	1.773	2.923	0.0158*Cload+0.9612
PBU24	OEN->PAD (fall)	1.107	1.425	1.727	2.845	0.0151*Cload+0.9643
PBU24	OEN->PAD (rise)	1.09	1.449	1.768	2.916	0.0158*Cload+0.9565



PBSUx

CMOS 3-STATE OUTPUT PAD WITH SCHMITT TRIGGER INPUT and PULLUP, 5V-Tolerant



● Truth Table

OEN	Input		Output	
	I	PAD	C	
1	x	0	0	
1	x	1	1	
1	x	Z	1	
0	0	0	0	
0	1	1	1	

● Cell Information

Cell Name	No.Pad Req.	Power(μ W/MHz)
PBSU2	1	189.6
PBSU4	1	210.4
PBSU8	1	198.2
PBSU12	1	206.6
PBSU16	1	212.7
PBSU24	1	227.9

● Pin Capacitance (pF)

Cell Name	C	I	OEN	PAD
PBSU2				
PBSU4				
PBSU8				
PBSU12				
PBSU16				



● Propagation Delay(ns)

VDD_IO=3.3V, VDD_CORE=1.8V, temperature=25 °C , typical process, standard load=0.00699 pf, input slew time=0.06ns (measured from 10% to 90% transition)

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBSU2	PAD->C (fall)	0.4561	0.459	0.4653	0.4785	0.2303*Cload+0.4566
PBSU2	PAD->C (rise)	0.4944	0.4975	0.5022	0.5104	0.1616*Cload+0.4954

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBSU2	I->PAD (fall)	3.009	6.669	10.29	23.76	0.1803*Cload+1.2408
PBSU2	I->PAD (rise)	2.918	6.565	10.16	23.56	0.1794*Cload+1.158
PBSU2	OEN->PAD (fall)	2.844	6.505	10.13	23.59	0.1802*Cload+1.0815
PBSU2	OEN->PAD (rise)	2.878	6.511	10.11	23.54	0.1796*Cload+1.1062

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBSU4	PAD->C (fall)	0.456	0.4583	0.4631	0.4742	0.1917*Cload+0.4562
PBSU4	PAD->C (rise)	0.4944	0.4975	0.5022	0.5104	0.1616*Cload+0.4954

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBSU4	I->PAD (fall)	1.826	3.642	5.447	12.18	0.0899*Cload+0.9416
PBSU4	I->PAD (rise)	1.736	3.58	5.4	12.16	0.0905*Cload+0.8546
PBSU4	OEN->PAD (fall)	1.732	3.547	5.352	12.08	0.0899*Cload+0.8456
PBSU4	OEN->PAD (rise)	1.731	3.565	5.379	12.14	0.0904*Cload+0.8447

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBSU8	PAD->C (fall)	0.4608	0.4631	0.4684	0.4811	0.2145*Cload+0.4608
PBSU8	PAD->C (rise)	0.4944	0.4975	0.5022	0.5104	0.1616*Cload+0.4954



cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBSU8	I->PAD (fall)	1.288	2.199	3.098	6.456	0.0449*Cload+0.8468
PBSU8	I->PAD (rise)	1.225	2.155	3.072	6.475	0.0456*Cload+0.7807
PBSU8	OEN->PAD (fall)	1.24	2.147	3.046	6.403	0.0448*Cload+0.801
PBSU8	OEN->PAD (rise)	1.233	2.16	3.073	6.469	0.0455*Cload+0.7881

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBSU12	PAD->C (fall)	0.4615	0.4637	0.4686	0.48	0.1945*Cload+0.4616
PBSU12	PAD->C (rise)	0.4944	0.4975	0.5022	0.5104	0.1616*Cload+0.4954

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBSU12	I->PAD (fall)	1.131	1.741	2.34	4.576	0.0299*Cload+0.8398
PBSU12	I->PAD (rise)	1.083	1.715	2.33	4.606	0.0306*Cload+0.7887
PBSU12	OEN->PAD (fall)	1.097	1.702	2.301	4.536	0.0298*Cload+0.8072
PBSU12	OEN->PAD (rise)	1.09	1.721	2.334	4.605	0.0305*Cload+0.7981

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBSU16	PAD->C (fall)	0.4615	0.4637	0.4686	0.48	0.1945*Cload+0.4616
PBSU16	PAD->C (rise)	0.4944	0.4975	0.5022	0.5104	0.1616*Cload+0.4954

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBSU16	I->PAD (fall)	1.071	1.528	1.978	3.655	0.0224*Cload+0.854
PBSU16	I->PAD (rise)	1.034	1.523	1.988	3.7	0.0231*Cload+0.8196
PBSU16	OEN->PAD (fall)	1.042	1.496	1.946	3.621	0.0224*Cload+0.8222
PBSU16	OEN->PAD (rise)	1.041	1.529	1.992	3.701	0.0231*Cload+0.8241

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBSU24	PAD->C (fall)	0.4615	0.4637	0.4686	0.48	0.1945*Cload+0.4616
PBSU24	PAD->C (rise)	0.4927	0.4949	0.4996	0.5111	0.1959*Cload+0.4927



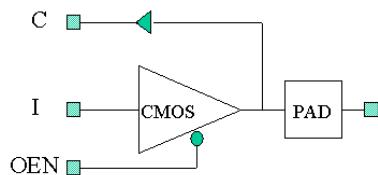
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cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBSU24	I->PAD (fall)	1.131	1.45	1.753	2.871	0.0151*Cload+0.9896
PBSU24	I->PAD (rise)	1.093	1.452	1.772	2.923	0.0158*Cload+0.9607
PBSU24	OEN->PAD (fall)	1.107	1.425	1.727	2.844	0.0151*Cload+0.9641
PBSU24	OEN->PAD (rise)	1.089	1.448	1.767	2.916	0.0158*Cload+0.9557



PBLx

CMOS 3-STATE OUTPUT WITH PAD INPUT and LIMITED SLEW RATE , 5V-Tolerant



● Truth Table

Input		Output	
OEN	I	PAD	C
1	x	0	0
1	x	1	1
1	x	Z	x
0	0	0	0
0	1	1	1

● Cell Information

Cell Name	No.Pad Req.	Power(μ W/MHz)
PBL8	1	96.32
PBL12	1	100
PBL16	1	110.7
PBL24	1	125.9

● Pin Capacitance (pF)

Cell Name	C	I	OEN	PAD
PBL8				



PBL12

PBL16

PBL24

PBLx

CMOS 3-STATE OUTPUT WITH PAD INPUT and LIMITED SLEW RATE , 5V-Tolerant

● Propagation Delay(ns)

VDD_IO=3.3V, VDD_CORE=1.8V, temperature=25 °C , typical process, standard load=0.00699 pf, input slew time=0.06ns (measured from 10% to 90% transition)

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBL8	PAD->C (fall)	0.288	0.2936	0.2961	0.3073	0.2403*Cload+0.2878
PBL8	PAD->C (rise)	0.3432	0.3458	0.3505	0.3632	0.2188*Cload+0.3430

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBL8	I->PAD (fall)	1.467	2.377	3.274	6.625	0.0448*Cload+1.0277
PBL8	I->PAD (rise)	1.421	2.355	3.275	6.687	0.0457*Cload+0.9781
PBL8	OEN->PAD (fall)	1.419	2.327	3.223	6.573	0.0448*Cload+0.9775
PBL8	OEN->PAD (rise)	1.435	2.366	3.281	6.682	0.0456*Cload+0.99

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBL12	PAD->C (fall)	0.2878	0.2933	0.296	0.3071	0.2374*Cload+0.2877
PBL12	PAD->C (rise)	0.3432	0.3458	0.3505	0.3632	0.2188*Cload+0.3430

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBL12	I->PAD (fall)	1.216	1.826	2.425	4.657	0.0299*Cload+0.9238



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PBL12	I->PAD (rise)	1.168	1.802	2.417	4.698 0.0306*Cload+0.8765
PBL12	OEN->PAD (fall)	1.18	1.787	2.385	4.617 0.0298*Cload+0.8905
PBL12	OEN->PAD (rise)	1.183	1.814	2.428	4.701 0.0305*Cload+0.8921

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	

PBL16	PAD->C (fall)	0.288	0.2936	0.2961	0.3073 0.2403*Cload+0.2878
PBL16	PAD->C (rise)	0.3432	0.3458	0.3505	0.3632 0.2188*Cload+0.3430

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	

PBL16	I->PAD (fall)	1.616	2.133	2.599	4.282 0.0231*Cload+1.4158
PBL16	I->PAD (rise)	1.552	2.076	2.55	4.269 0.0236*Cload+1.3432
PBL16	OEN->PAD (fall)	1.574	2.093	2.56	4.243 0.0231*Cload+1.3758
PBL16	OEN->PAD (rise)	1.539	2.063	2.537	4.252 0.0235*Cload+1.3346

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	

PBL24	PAD->C (fall)	0.288	0.2906	0.2966	0.3099 0.2274*Cload+0.2883
PBL24	PAD->C (rise)	0.3399	0.3422	0.3464	0.3554 0.1616*Cload+0.3403

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	

PBL24	I->PAD (fall)	1.575	1.974	2.306	3.453 0.0162*Cload+1.4562
PBL24	I->PAD (rise)	1.536	1.938	2.277	3.444 0.0165*Cload+1.4118
PBL24	OEN->PAD (fall)	1.547	1.95	2.283	3.431 0.0163*Cload+1.4266
PBL24	OEN->PAD (rise)	1.51	1.914	2.253	3.419 0.0165*Cload+1.3871

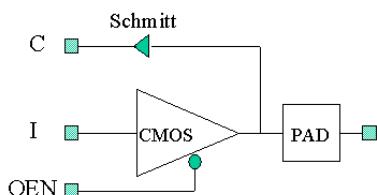


Semiconductor Manufacturing International (Shanghai) Corporation

PBSLx

PBSLx

CMOS 3-STATE OUTPUT PAD WITH SCHMITT TRIGGER INPUT and LIMITED SLEW RATE , , 5V-Toleran



● Truth Table

OEN	Input		Output	
	I	PAD	C	
1	x	0	0	
1	x	1	1	
1	x	Z	x	
0	0	0	0	
0	1	1	1	

● Cell Information

Cell Name	No.Pad Req.	Power(μ W/MHz)
PBSL8	1	99.6
PBSL12	1	101.5
PBSL16	1	115.1
PBSL24	1	125



● Pin Capacitance (pF)

Cell Name	C	I	OEN	PAD
PBSL8				
PBSL12				
PBSL16				
PBSL24				

● Propagation Delay(ns)

VDD_IO=3.3V, VDD_CORE=1.8V, temperature=25 °C , typical process, standard load=0.00699 pf, input slew time=0.06ns (measured from 10% to 90% transition)

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBSL8	PAD->C (fall)	0.4508	0.4531	0.4578	0.4685	0.1859*Cload+0.4510
PBSL8	PAD->C (rise)	0.495	0.498	0.5026	0.5108	0.1602*Cload+0.4960

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBSL8	I->PAD (fall)	1.467	2.377	3.273	6.624	0.0448*Cload+1.0272
PBSL8	I->PAD (rise)	1.42	2.354	3.274	6.686	0.0457*Cload+0.9771
PBSL8	OEN->PAD (fall)	1.418	2.326	3.222	6.573	0.0448*Cload+0.9767
PBSL8	OEN->PAD (rise)	1.434	2.364	3.28	6.681	0.0455*Cload+0.9941

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBSL12	PAD->C (fall)	0.4441	0.4481	0.4572	0.4636	0.1487*Cload+0.4480
PBSL12	PAD->C (rise)	0.495	0.498	0.5026	0.5108	0.1602*Cload+0.4960



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cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBSL12	I->PAD (fall)	1.216	1.826	2.425	4.657 0.0299*Cload+0.9238	
PBSL12	I->PAD (rise)	1.167	1.801	2.417	4.697 0.0306*Cload+0.8757	
PBSL12	OEN->PAD (fall)	1.18	1.787	2.385	4.616 0.0298*Cload+0.8902	
PBSL12	OEN->PAD (rise)	1.183	1.813	2.427	4.7 0.0305*Cload+0.8913	

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBSL16	PAD->C (fall)	0.4441	0.4481	0.4572	0.4636 0.1487*Cload+0.4480	
PBSL16	PAD->C (rise)	0.495	0.498	0.5026	0.5108 0.1602*Cload+0.4960	

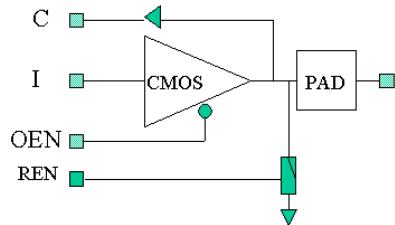
cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBSL16	I->PAD (fall)	1.616	2.132	2.598	4.282 0.0231*Cload+1.4153	
PBSL16	I->PAD (rise)	1.551	2.075	2.549	4.268 0.0236*Cload+1.3422	
PBSL16	OEN->PAD (fall)	1.574	2.093	2.559	4.243 0.0231*Cload+1.3756	
PBSL16	OEN->PAD (rise)	1.538	2.063	2.536	4.252 0.0235*Cload+1.3341	

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBSL24	PAD->C (fall)	0.4466	0.449	0.4548	0.4678 0.2203*Cload+0.4468	
PBSL24	PAD->C (rise)	0.4931	0.4953	0.5001	0.5119 0.2002*Cload+0.4931	

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBSL24	I->PAD (fall)	1.575	1.973	2.306	3.453 0.0162*Cload+1.456	
PBSL24	I->PAD (rise)	1.535	1.938	2.277	3.443 0.0165*Cload+1.4113	
PBSL24	OEN->PAD (fall)	1.547	1.95	2.283	3.43 0.0163*Cload+1.4263	
PBSL24	OEN->PAD (rise)	1.51	1.914	2.253	3.419 0.0165*Cload+1.3871	

PBCDLx

CMOS 3-STATE OUTPUT PAD WITH INPUT CONTROLLABLE PULLDOWN, and LIMITED SLEW RATE , 5V-Tolerant



● Truth Table

Input			Output	
REN	OEN	I	PAD	C
x	1	x	0	0
x	1	x	1	1
0	1	x	pull-down	0
1	1	x	Z	x
x	0	0	0	0
x	0	1	1	1

● Cell Information

Cell Name	No.Pad Req.	Power(μ W/MHz)
PBCDL8	1	93.45
PBCDL12	1	100.5
PBCDL16	1	109.2
PBCDL24	1	137.7



● Pin Capacitance (pF)

Cell Name	C	I	OEN	PAD
PBCDL8				
PBCDL12				
PBCDL16				
PBCDL24				

● Propagation Delay(ns)

VDD_IO=3.3V, VDD_CORE=1.8V, temperature=25 °C , typical process, standard load=0.00699 pf, input slew time=0.06ns (measured from 10% to 90% transition)

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBCDL8	PAD->C (fall)	0.2877	0.2931	0.2959	0.3069	0.2346*Cload+0.2877
PBCDL8	PAD->C (rise)	0.3435	0.346	0.3511	0.3636	0.2145*Cload+0.3435

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBCDL8	I->PAD (fall)	1.467	2.377	3.274	6.624	0.0448*Cload+1.0275
PBCDL8	I->PAD (rise)	1.421	2.355	3.275	6.687	0.0457*Cload+0.9781
PBCDL8	OEN->PAD (fall)	1.419	2.327	3.223	6.573	0.0448*Cload+0.9775
PBCDL8	OEN->PAD (rise)	1.435	2.366	3.281	6.682	0.0456*Cload+0.99

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBCDL12	PAD->C (fall)	0.2876	0.2929	0.2958	0.3068	0.2331*Cload+0.2876
PBCDL12	PAD->C (rise)	0.3435	0.346	0.3511	0.3636	0.2145*Cload+0.3435



cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBCDL12	I->PAD (fall)	1.216	1.826	2.425	4.657	0.0299*Cload+0.9238
PBCDL12	I->PAD (rise)	1.168	1.802	2.417	4.698	0.0306*Cload+0.8765
PBCDL12	OEN->PAD (fall)	1.18	1.787	2.385	4.617	0.0298*Cload+0.8905
PBCDL12	OEN->PAD (rise)	1.183	1.814	2.428	4.701	0.0305*Cload+0.8921

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBCDL16	PAD->C (fall)	0.2877	0.2931	0.2959	0.3069	0.2346*Cload+0.2877
PBCDL16	PAD->C (rise)	0.3435	0.346	0.3511	0.3636	0.2145*Cload+0.3435

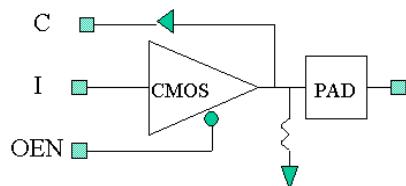
cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBCDL16	I->PAD (fall)	1.616	2.133	2.599	4.282	0.0231*Cload+1.4158
PBCDL16	I->PAD (rise)	1.552	2.076	2.55	4.269	0.0236*Cload+1.3432
PBCDL16	OEN->PAD (fall)	1.574	2.093	2.56	4.243	0.0231*Cload+1.3758
PBCDL16	OEN->PAD (rise)	1.539	2.063	2.537	4.252	0.0235*Cload+1.3346

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBCDL24	PAD->C (fall)	0.2878	0.2904	0.2963	0.3096	0.2274*Cload+0.2880
PBCDL24	PAD->C (rise)	0.3402	0.3425	0.3467	0.3557	0.1616*Cload+0.3406

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBCDL24	I->PAD (fall)	1.575	1.974	2.306	3.453	0.0162*Cload+1.4562
PBCDL24	I->PAD (rise)	1.536	1.938	2.277	3.444	0.0165*Cload+1.4118
PBCDL24	OEN->PAD (fall)	1.547	1.95	2.283	3.431	0.0163*Cload+1.4266
PBCDL24	OEN->PAD (rise)	1.51	1.914	2.253	3.419	0.0165*Cload+1.3871

PBDLx

CMOS 3-STATE OUTPUT PAD WITH INPUT PULLDOWN and LIMITED SLEW RATE ,
5V-Tolerant



● Truth Table

OEN	Input		Output	
	I	PAD	C	
1	x	0	0	
1	x	1	1	
1	x	Z	0	
0	0	0	0	
0	1	1	1	

● Cell Information

Cell Name	No.Pad Req.	Power(μ W/MHz)
PBDL8	1	169.1
PBDL12	1	175.4
PBDL16	1	183.1
PBDL24	1	192

● Pin Capacitance (pF)

Cell Name	C	I	OEN	PAD
PBDL8				
PBDL12				
PBDL16				



● Propagation Delay(ns)

VDD_IO=3.3V, VDD_CORE=1.8V, temperature=25 °C , typical process, standard load=0.00699 pf, input slew time=0.06ns (measured from 10% to 90% transition)

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBDL8	PAD->C (fall)	0.2841	0.2897	0.292	0.3033	0.2417*Cload+0.2838
PBDL8	PAD->C (rise)	0.3498	0.3521	0.3577	0.3662	0.1545*Cload+0.3510

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBDL8	I->PAD (fall)	1.465	2.373	3.267	6.611	0.0447*Cload+1.0263
PBDL8	I->PAD (rise)	1.422	2.357	3.277	6.692	0.0457*Cload+0.9806
PBDL8	OEN->PAD (fall)	1.39	2.297	3.192	6.538	0.0447*Cload+0.9516
PBDL8	OEN->PAD (rise)	1.436	2.367	3.283	6.687	0.0456*Cload+0.9922

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBDL12	PAD->C (fall)	0.2886	0.2908	0.2958	0.3076	0.2002*Cload+0.2887
PBDL12	PAD->C (rise)	0.3498	0.3521	0.3577	0.3662	0.1545*Cload+0.3510

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBDL12	I->PAD (fall)	1.215	1.824	2.422	4.651	0.0298*Cload+0.9262
PBDL12	I->PAD (rise)	1.168	1.803	2.419	4.7	0.0306*Cload+0.8777
PBDL12	OEN->PAD (fall)	1.161	1.768	2.365	4.595	0.0298*Cload+0.8705
PBDL12	OEN->PAD (rise)	1.184	1.815	2.429	4.703	0.0305*Cload+0.8933



cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBDL16	PAD->C (fall)	0.2886	0.2908	0.2958	0.3076	0.2002*Cload+0.2887
PBDL16	PAD->C (rise)	0.3498	0.3521	0.3577	0.3662	0.1545*Cload+0.3510

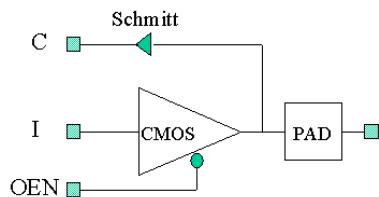
cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBDL16	I->PAD (fall)	1.616	2.131	2.596	4.278	0.0231*Cload+1.4136
PBDL16	I->PAD (rise)	1.553	2.077	2.551	4.27	0.0236*Cload+1.3442
PBDL16	OEN->PAD (fall)	1.556	2.078	2.545	4.227	0.0232*Cload+1.3545
PBDL16	OEN->PAD (rise)	1.54	2.064	2.538	4.254	0.0235*Cload+1.3358

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBDL24	PAD->C (fall)	0.2886	0.2908	0.2958	0.3076	0.2002*Cload+0.2887
PBDL24	PAD->C (rise)	0.3471	0.3496	0.355	0.3678	0.2188*Cload+0.3472

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBDL24	I->PAD (fall)	1.575	1.973	2.305	3.451	0.0162*Cload+1.4552
PBDL24	I->PAD (rise)	1.536	1.939	2.278	3.444	0.0165*Cload+1.4123
PBDL24	OEN->PAD (fall)	1.531	1.939	2.273	3.42	0.0163*Cload+1.4146
PBDL24	OEN->PAD (rise)	1.511	1.915	2.254	3.42	0.0165*Cload+1.3881

PBSDLx

CMOS 3-STATE OUTPUT PAD WITH SCHMITT TRIGGER INPUT and PULLDOWN, and LIMITED SLEW RATE , 5V-Tolerant



● Truth Table

OEN	Input		Output	
	I	PAD	C	
1	x	0	0	
1	x	1	1	
1	x	Z	0	
0	0	0	0	
0	1	1	1	

● Cell Information

Cell Name	No.Pad Req.	Power(μ W/MHz)
PBSDL8	1	170.3
PBSDL12	1	179.2
PBSDL16	1	181.2
PBSDL24	1	193.7

● Pin Capacitance (pF)

Cell Name	C	I	OEN	PAD
PBSDL8				
PBSDL12				
PBSDL16				



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PBSDL24

PBSDLx

CMOS 3-STATE OUTPUT PAD WITH SCHMITT TRIGGER INPUT and PULLDOWN, and
LIMITED SLEW RATE , 5V-Tolerant

● Propagation Delay(ns)

VDD_IO=3.3V, VDD_CORE=1.8V, temperature=25 °C , typical process, standard load=0.00699 pf, input slew time=0.06ns (measured from 10% to 90% transition)

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBSDL8	PAD->C (fall)	0.4552	0.4577	0.4635	0.4766	0.2231*Cload+0.4554
PBSDL8	PAD->C (rise)	0.4996	0.502	0.5062	0.515	0.1602*Cload+0.5001

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBSDL8	I->PAD (fall)	1.465	2.373	3.267	6.61	0.0447*Cload+1.0261
PBSDL8	I->PAD (rise)	1.421	2.356	3.276	6.691	0.0457*Cload+0.9796
PBSDL8	OEN->PAD (fall)	1.39	2.297	3.192	6.538	0.0447*Cload+0.9516
PBSDL8	OEN->PAD (rise)	1.435	2.366	3.282	6.686	0.0456*Cload+0.9912

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBSDL12	PAD->C (fall)	0.4516	0.4543	0.4588	0.4687	0.1802*Cload+0.4520
PBSDL12	PAD->C (rise)	0.4996	0.502	0.5062	0.515	0.1602*Cload+0.5001

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBSDL12	I->PAD (fall)	1.214	1.824	2.422	4.651	0.0298*Cload+0.926
PBSDL12	I->PAD (rise)	1.168	1.802	2.418	4.699	0.0306*Cload+0.877
PBSDL12	OEN->PAD (fall)	1.161	1.768	2.365	4.595	0.0298*Cload+0.8705



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PBSDL12 OEN->PAD (rise) 1.183 1.814 2.428 4.702 0.0305*Cload+0.8923

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBSDL16	PAD->C (fall)	0.4516	0.4543	0.4588	0.4687	0.1802*Cload+0.4520
PBSDL16	PAD->C (rise)	0.4996	0.502	0.5062	0.515	0.1602*Cload+0.5001

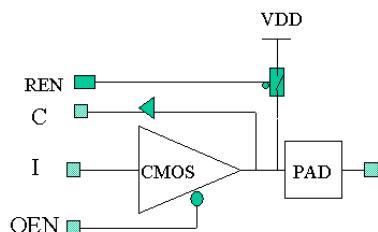
cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBSDL16	I->PAD (fall)	1.615	2.131	2.596	4.278	0.0231*Cload+1.4133
PBSDL16	I->PAD (rise)	1.552	2.076	2.55	4.27	0.0236*Cload+1.3435
PBSDL16	OEN->PAD (fall)	1.556	2.078	2.544	4.227	0.0232*Cload+1.3542
PBSDL16	OEN->PAD (rise)	1.539	2.064	2.537	4.253	0.0235*Cload+1.3351

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBSDL24	PAD->C (fall)	0.4523	0.4549	0.4594	0.4694	0.1802*Cload+0.4527
PBSDL24	PAD->C (rise)	0.4989	0.5014	0.5056	0.5143	0.1602*Cload+0.4994

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBSDL24	I->PAD (fall)	1.574	1.973	2.305	3.451	0.0162*Cload+1.455
PBSDL24	I->PAD (rise)	1.536	1.938	2.277	3.444	0.0165*Cload+1.4118
PBSDL24	OEN->PAD (fall)	1.531	1.939	2.272	3.42	0.0163*Cload+1.4143
PBSDL24	OEN->PAD (rise)	1.51	1.914	2.253	3.419	0.0165*Cload+1.3871

PBCULx

CMOS 3-STATE OUTPUT PAD WITH INPUT and CONTROLLABLE PULLUP, and LIMITED SLEW RATE , 5V-Tolerant



● Truth Table

Input			Output	
REN	OEN	I	PAD	C
x	1	x	0	0
x	1	x	1	1
0	1	x	pull-up	1
1	1	x	Z	x
x	0	0	0	0
x	0	1	1	1

● Cell Information

Cell Name	No.Pad Req.	Power(μ W/MHz)
PBCUL8	1	95.77
PBCUL12	1	96.31
PBCUL16	1	97.03
PBCUL24	1	130.3

● Pin Capacitance (pF)

Cell Name	C	I	OEN	PAD



Semiconductor Manufacturing International (Shanghai) Corporation

PBCUL8

PBCUL12

PBCUL16

PBCUL24

PBCUL

CMOS 3-STATE OUTPUT PAD WITH INPUT and CONTROLLABLE PULLUP, and LIMITED SLEW RATE , 5V-Tolerant

● Propagation Delay(ns)

VDD_IO=3.3V, VDD_CORE=1.8V, temperature=25 °C , typical process, standard load=0.00699 pf, input slew time=0.06ns (measured from 10% to 90% transition)

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBCUL8	PAD->C (fall)	0.2882	0.2914	0.298	0.311	0.2317*Cload+0.2890
PBCUL8	PAD->C (rise)	0.3436	0.3461	0.3511	0.3636	0.2145*Cload+0.3436

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBCUL8	I->PAD (fall)	1.467	2.377	3.274	6.625	0.0448*Cload+1.0277
PBCUL8	I->PAD (rise)	1.421	2.355	3.275	6.688	0.0457*Cload+0.9783
PBCUL8	OEN->PAD (fall)	1.419	2.327	3.223	6.574	0.0448*Cload+0.9777
PBCUL8	OEN->PAD (rise)	1.435	2.366	3.281	6.682	0.0456*Cload+0.99

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBCUL12	PAD->C (fall)	0.2882	0.2914	0.298	0.311	0.2317*Cload+0.2890
PBCUL12	PAD->C (rise)	0.3436	0.3461	0.3511	0.3636	0.2145*Cload+0.3436

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBCUL12	I->PAD (fall)	1.216	1.826	2.425	4.657	0.0299*Cload+0.9238

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PBCUL12 I->PAD (rise)	1.168	1.802	2.418	4.698 0.0306*Cload+0.8767
PBCUL12 OEN->PAD (fall)	1.18	1.787	2.385	4.617 0.0298*Cload+0.8905
PBCUL12 OEN->PAD (rise)	1.183	1.814	2.428	4.701 0.0305*Cload+0.8921

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBCUL16 PAD->C (fall)	0.2882	0.2914	0.298	0.311	0.2317*Cload+0.2890	
PBCUL16 PAD->C (rise)	0.3436	0.3461	0.3511	0.3636	0.2145*Cload+0.3436	

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBCUL16 I->PAD (fall)	1.616	2.133	2.599	4.283	0.0231*Cload+1.4161	
PBCUL16 I->PAD (rise)	1.552	2.076	2.55	4.269	0.0236*Cload+1.3432	
PBCUL16 OEN->PAD (fall)	1.574	2.093	2.56	4.243	0.0231*Cload+1.3758	
PBCUL16 OEN->PAD (rise)	1.539	2.063	2.537	4.252	0.0235*Cload+1.3346	

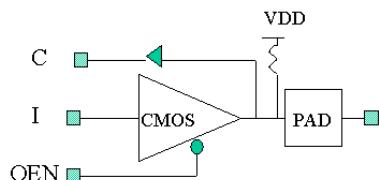
cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBCUL24 PAD->C (fall)	0.2895	0.2924	0.2988	0.312	0.2303*Cload+0.2901	
PBCUL24 PAD->C (rise)	0.3401	0.3425	0.3467	0.3557	0.1630*Cload+0.3405	

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBCUL24 I->PAD (fall)	1.575	1.974	2.306	3.453	0.0162*Cload+1.4562	
PBCUL24 I->PAD (rise)	1.536	1.938	2.277	3.444	0.0165*Cload+1.4118	
PBCUL24 OEN->PAD (fall)	1.547	1.95	2.283	3.431	0.0163*Cload+1.4266	
PBCUL24 OEN->PAD (rise)	1.51	1.914	2.253	3.419	0.0165*Cload+1.3871	



PBULx

CMOS 3-STATE OUTPUT PAD WITH INPUT and PULLUP, and SLEW RATE , 5V-Tolerant



● Truth Table

OEN	Input		PAD	Output C
	I	OEN		
1	x		0	0
1	x		1	1
1	x		Z	1
0	0		0	0
0	1		1	1

● Cell Information

Cell Name	No.Pad Req.	Power(μ W/MHz)
PBUL8	1	195.8
PBUL12	1	200.5
PBUL16	1	216
PBUL24	1	229.5

● Pin Capacitance (pF)

Cell Name	C	I	OEN	PAD
PBUL8				
PBUL12				
PBUL16				

**PBULx**CMOS 3-STATE OUTPUT PAD WITH INPUT and PULLUP, and SLEW RATE , 5V-Tolerant**● Propagation Delay(ns)**

VDD_IO=3.3V, VDD_CORE=1.8V, temperature=25 °C , typical process, standard load=0.00699 pf, input slew time=0.06ns (measured from 10% to 90% transition)

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBUL8	PAD->C (fall)	0.2918	0.2945	0.3006	0.3139	0.2288*Cload+0.2922
PBUL8	PAD->C (rise)	0.3427	0.3453	0.3497	0.3627	0.2231*Cload+0.3423

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBUL8	I->PAD (fall)	1.468	2.381	3.28	6.637	0.0449*Cload+1.0281
PBUL8	I->PAD (rise)	1.419	2.351	3.268	6.672	0.0456*Cload+0.9765
PBUL8	OEN->PAD (fall)	1.42	2.33	3.229	6.586	0.0449*Cload+0.9778
PBUL8	OEN->PAD (rise)	1.414	2.344	3.259	6.655	0.0455*Cload+0.9723

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBUL12	PAD->C (fall)	0.2943	0.2965	0.3014	0.3129	0.1959*Cload+0.2944
PBUL12	PAD->C (rise)	0.3427	0.3453	0.3497	0.3627	0.2231*Cload+0.3423

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBUL12	I->PAD (fall)	1.216	1.828	2.427	4.663	0.0299*Cload+0.9263
PBUL12	I->PAD (rise)	1.167	1.8	2.415	4.691	0.0306*Cload+0.8735
PBUL12	OEN->PAD (fall)	1.181	1.789	2.387	4.623	0.0299*Cload+0.8878
PBUL12	OEN->PAD (rise)	1.169	1.8	2.414	4.685	0.0305*Cload+0.8776



cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBUL16	PAD->C (fall)	0.29	0.2924	0.298	0.311	0.2203*Cload+0.2901
PBUL16	PAD->C (rise)	0.3427	0.3453	0.3497	0.3627	0.2231*Cload+0.3423

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBUL16	I->PAD (fall)	1.617	2.134	2.6	4.286	0.0231*Cload+1.4176
PBUL16	I->PAD (rise)	1.551	2.074	2.548	4.265	0.0235*Cload+1.3463
PBUL16	OEN->PAD (fall)	1.575	2.095	2.561	4.247	0.0232*Cload+1.3725
PBUL16	OEN->PAD (rise)	1.525	2.052	2.526	4.241	0.0236*Cload+1.3175

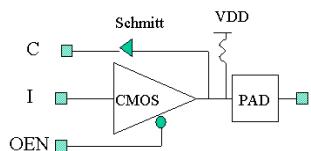
cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBUL24	PAD->C (fall)	0.29	0.2924	0.298	0.311	0.2203*Cload+0.2901
PBUL24	PAD->C (rise)	0.3393	0.3417	0.3459	0.3547	0.1602*Cload+0.3398

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBUL24	I->PAD (fall)	1.576	1.974	2.307	3.455	0.0162*Cload+1.4572
PBUL24	I->PAD (rise)	1.535	1.937	2.276	3.442	0.0165*Cload+1.4106
PBUL24	OEN->PAD (fall)	1.548	1.951	2.284	3.432	0.0163*Cload+1.4276
PBUL24	OEN->PAD (rise)	1.498	1.906	2.245	3.412	0.0165*Cload+1.3783



PBSULx

CMOS 3-STATE OUTPUT PAD WITH SCHMITT TRIGGER INPUT and PULLUP, and SLEW RATE , 5V-Tolerant



● Truth Table

OEN	Input		Output	
	I	PAD	C	
1	x	0	0	
1	x	1	1	
1	x	Z	1	
0	0	0	0	
0	1	1	1	

● Cell Information

Cell Name	No.Pad Req.	Power(μ W/MHz)
PBSUL8	1	202.9
PBSUL12	1	207.2
PBSUL16	1	211.3
PBSUL24	1	230.9

● Pin Capacitance (pF)

Cell Name	C	I	OEN	PAD
PBSUL8				



PBSUL12

PBSUL16

PBSUL24

PBSUL

CMOS 3-STATE OUTPUT PAD WITH SCHMITT TRIGGER INPUT and PULLUP, and SLEW RATE , 5V-Tolerant

● Propagation Delay(ns)

VDD_IO=3.3V, VDD_CORE=1.8V, temperature=25 °C , typical process, standard load=0.00699 pf, input slew time=0.06ns (measured from 10% to 90% transition)

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBSUL8	PAD->C (fall)	0.4608	0.4631	0.4684	0.4811	0.2145*Cload+0.4608
PBSUL8	PAD->C (rise)	0.4944	0.4975	0.5022	0.5104	0.1616*Cload+0.4954

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBSUL8	I->PAD (fall)	1.468	2.38	3.279	6.636	0.0449*Cload+1.0273
PBSUL8	I->PAD (rise)	1.418	2.35	3.267	6.671	0.0456*Cload+0.9755
PBSUL8	OEN->PAD (fall)	1.419	2.329	3.228	6.585	0.0449*Cload+0.9768
PBSUL8	OEN->PAD (rise)	1.413	2.343	3.257	6.654	0.0455*Cload+0.9711

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBSUL12	PAD->C (fall)	0.456	0.4583	0.4631	0.4742	0.1917*Cload+0.4562
PBSUL12	PAD->C (rise)	0.4944	0.4975	0.5022	0.5104	0.1616*Cload+0.4954

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBSUL12	I->PAD (fall)	1.216	1.827	2.427	4.663	0.0299*Cload+0.9261
PBSUL12	I->PAD (rise)	1.166	1.799	2.414	4.69	0.0306*Cload+0.8725



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PBSUL12	OEN->PAD (fall)	1.18	1.788	2.387	4.622 0.0299*Cload+0.8871
PBSUL12	OEN->PAD (rise)	1.168	1.8	2.413	4.684 0.0305*Cload+0.8768

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	

PBSUL16	PAD->C (fall)	0.4615	0.4637	0.4686	0.48 0.1945*Cload+0.4616
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PBSUL16	PAD->C (rise)	0.4944	0.4975	0.5022	0.5104 0.1616*Cload+0.4954
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cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	

PBSUL16	I->PAD (fall)	1.617	2.134	2.6	4.285 0.0231*Cload+1.4173
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PBSUL16	I->PAD (rise)	1.55	2.074	2.547	4.264 0.0235*Cload+1.3456
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PBSUL16	OEN->PAD (fall)	1.575	2.094	2.561	4.246 0.0232*Cload+1.372
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PBSUL16	OEN->PAD (rise)	1.524	2.052	2.525	4.24 0.0236*Cload+1.3167
---------	-----------------	-------	-------	-------	--------------------------

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	

PBSUL24	PAD->C (fall)	0.4615	0.4637	0.4686	0.48 0.1945*Cload+0.4616
---------	---------------	--------	--------	--------	--------------------------

PBSUL24	PAD->C (rise)	0.4927	0.4949	0.4996	0.511 0.1945*Cload+0.4927
---------	---------------	--------	--------	--------	---------------------------

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	

PBSUL24	I->PAD (fall)	1.576	1.974	2.306	3.455 0.0162*Cload+1.457
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PBSUL24	I->PAD (rise)	1.534	1.937	2.275	3.441 0.0165*Cload+1.4098
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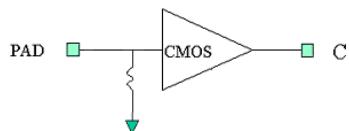
PBSUL24	OEN->PAD (fall)	1.548	1.951	2.284	3.432 0.0163*Cload+1.4276
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PBSUL24	OEN->PAD (rise)	1.498	1.905	2.245	3.411 0.0165*Cload+1.3778
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PID

Input Pad With Pulldown, 5V-Tolerant



● Truth Table

Input PAD	Output C
1	1
0	0

● Cell Information

Cell Name	No.Pad Req.	Power(μ W/MHz)
PID	1	46.15

● Pin Capacitance (pF)

Cell Name	C	PAD
PID		



PID

Input Pad With Pulldown, 5V-Tolerant

● Propagation Delay(ns)

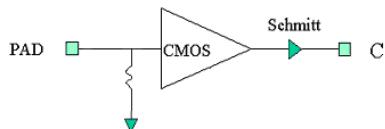
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cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PID	PAD->C (fall)	0.2886	0.2908	0.2958	0.3076	0.2002*Cload+0.2887
PID	PAD->C (rise)	0.3498	0.3521	0.3577	0.3662	0.1545*Cload+0.3510



PISD

Schmitt Trigger Input Pad, 5V-Tolerant



● Truth Table

Input PAD	Output C
1	1
0	0

● Cell Information

Cell Name	No.Pad Req.	Power(μ W/MHz)
PISD	1	47.31

● Pin Capacitance (pF)

Cell Name	C	PAD
PISD		



PISD

Schmitt Trigger Input Pad, 5V-Tolerant

● Propagation Delay(ns)

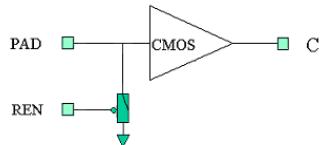
VDD_{IO}=3.3V, VDD_{CORE}=1.8V, temperature=25 °C , typical process, standard load=0.00699 pf, input slew time=0.06ns (measured from 10% to 90% transition)

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PISD	PAD->C (fall)	0.3925	0.3949	0.4005	0.4134	0.2188*Cload+0.3926
PISD	PAD->C (rise)	0.4557	0.4569	0.4649	0.4759	0.1745*Cload+0.4572



PICD

Input Pad with Controllable Pull-down , 5V-Tolerant



● Truth Table

Input		Output
REN	PAD	C
x	1	1
x	0	0
0	pull-down	0
1	z	x

● Cell Information

Cell Name	No.Pad Req.	Power(μ W/MHz)
PICD	1	887.2

● Pin Capacitance (pF)

Cell Name	C	PAD
PICD		



PICD

Input Pad with Controllable Pull-down , 5V-Tolerant

● Propagation Delay(ns)

VDD_IO=3.3V, VDD_CORE=1.8V, temperature=25°C, typical process, standard load=0.00699 pf, input slew time=0.06ns (measured from 10% to 90% transition)

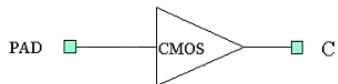
cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PICD	PAD->C (fall)	0.2876	0.2929	0.2958	0.3068	0.2331*Cload+0.2876
PICD	PAD->C (rise)	0.3432	0.3456	0.3511	0.3596	0.1559*Cload+0.3444

—



PI

Input Pad , 5V-Tolerant



● Truth Table

Input PAD	Output C
1	1
0	0

● Cell Information

Cell Name	No.Pad Req.	Power(μ W/MHz)
PI	1	50.54

● Pin Capacitance (pF)

Cell Name	C	PAD
PI		



PI

Input Pad, 5V-Tolerant

● Propagation Delay(ns)

VDD_IO=3.3V, VDD_CORE=1.8V, temperature=25 °C , typical process, standard load=0.00699 pf, input slew time=0.06ns (measured from 10% to 90% transition)

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PI	PAD->C (fall)	0.2878	0.2933	0.296	0.3071	0.2374*Cload+0.2877
PI	PAD->C (rise)	0.3392	0.3452	0.3515	0.3593	0.1974*Cload+0.3419

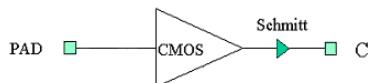


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PIS

PIS

Schmitt Trigger Input Pad, 5V-Tolerant



● Truth Table

Input PAD	Output C
1	1
0	0

● Cell Information

Cell Name	No.Pad Req.	Power(μ W/MHz)
PIS	1	46.3

● Pin Capacitance (pF)

Cell Name	C	PAD
PIS		



PIS

Schmitt Trigger Input Pad, 5V-Tolerant

● Propagation Delay(ns)

VDD_{IO}=3.3V, VDD_{CORE}=1.8V, temperature=25 °C , typical process, standard load=0.00699 pf, input slew time=0.06ns (measured from 10% to 90% transition)

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PIS	PAD->C (fall)	0.3826	0.3848	0.3901	0.4027	0.2117*Cload+0.3826
PIS	PAD->C (rise)	0.4529	0.4564	0.4613	0.4694	0.1659*Cload+0.4542

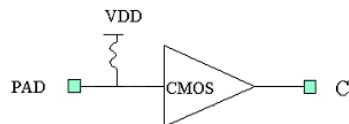


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PIU

PIU

Input Pad with Pull-up , 5V-Tolerant



● Truth Table

Input PAD	Output C
1	1
0	0

● Cell Information

Cell Name	No.Pad Req.	Power(μ W/MHz)
PIU	1	150.2

● Pin Capacitance (pF)

Cell Name	C	PAD
PIU		



PIU

Input Pad with Pull-up , 5V-Tolerant

● Propagation Delay(ns)

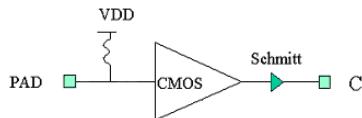
VDD_IO=3.3V, VDD_CORE=1.8V, temperature=25°C, typical process, standard load=0.00699 pf, input slew time=0.06ns (measured from 10% to 90% transition)

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PIU	PAD->C (fall)	0.2925	0.2948	0.2995	0.3104	0.1888*Cload+0.2927
PIU	PAD->C (rise)	0.339	0.3408	0.3511	0.359	0.1387*Cload+0.3426



PISU

Schmitt trigger Input Pad with Pull-up , 5V-Tolerant



● Truth Table

Input PAD	Output C
1	1
0	0

● Cell Information

Cell Name	No.Pad Req.	Power(μ W/MHz)
PISU	1	137.9

● Pin Capacitance (pF)

Cell Name	C	PAD
PISU		



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PISU

Schmitt trigger Input Pad with Pull-up , 5V-Tolerant

● Propagation Delay(ns)

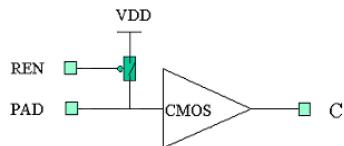
VDD_IO=3.3V, VDD_CORE=1.8V, temperature=25 °C , typical process, standard load=0.00699 pf, input slew time=0.06ns (measured from 10% to 90% transition)

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PISU	PAD->C (fall)	0.4017	0.404	0.4096	0.4225	0.2174*Cload+0.4018
PISU	PAD->C (rise)	0.4507	0.4529	0.4572	0.4664	0.1630*Cload+0.4511



PICU

Input Pad with Controllable Pull-up , 5V-Tolerant



● Truth Table

Input		Output
REN	PAD	C
x	1	1
x	0	0
0	pull-up	1
1	z	x

● Cell Information

Cell Name	No.Pad Req.	Power(μ W/MHz)
PICU	1	887.2

● Pin Capacitance (pF)

Cell Name	C	PAD
PICU		



PICU

Input Pad with Controllable Pull-up , 5V-Tolerant

● Propagation Delay(ns)

VDD_IO=3.3V, VDD_CORE=1.8V, temperature=25 °C , typical process, standard load=0.00699 pf, input slew time=0.06ns (measured from 10% to 90% transition)

cell	delay_path	Standard Load			Performance Equation
		2	4	8	
PICU	PAD->C (fall)	0.2882	0.2914	0.298	0.311 0.2317*Cload+0.2890
PICU	PAD->C (rise)	0.3434	0.3458	0.3513	0.3598 0.1559*Cload+0.3446
—					



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POx

POx

CMOS OUTPUT Only PAD , Tolerant



● Truth Table

Input I	Output Pad
1	1
0	0

● Cell Information

Cell Name	No.Pad Req.	Power(μ W/MHz)
PO2	1	71.81
PO4	1	87.25
PO8	1	92.37
PO12	1	90.65
PO16	1	101.2
PO24	1	118.5

● Pin Capacitance (pF)

Cell Name	C	PAD
PO2		
PO4		
PO8		



PO12

PO16

PO24

POxCMOS OUTPUT Only PAD , Tolerant

● Propagation Delay(ns)

VDD_IO=3.3V, VDD_CORE=1.8V, temperature=25 °C , typical process, standard load=0.00699 pf, input slew time=0.06ns (measured from 10% to 90% transition)

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PO2	I->PAD (fall)	2.971	6.601	10.2	23.57	0.1789*Cload+1.2196
PO2	I->PAD (rise)	2.914	6.598	10.23	23.76	0.1812*Cload+1.136
cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PO4	I->PAD (fall)	1.814	3.622	5.419	12.12	0.0895*Cload+0.9331
PO4	I->PAD (rise)	1.725	3.577	5.406	12.2	0.0910*Cload+0.8357
cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PO8	I->PAD (fall)	1.284	2.193	3.089	6.44	0.0448*Cload+0.8435
PO8	I->PAD (rise)	1.219	2.151	3.07	6.482	0.0457*Cload+0.7741
cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PO12	I->PAD (fall)	1.129	1.737	2.336	4.568	0.0298*Cload+0.8407
PO12	I->PAD (rise)	1.079	1.712	2.327	4.607	0.0306*Cload+0.7865
cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PO16	I->PAD (fall)	1.069	1.526	1.976	3.65	0.0224*Cload+0.8512
PO16	I->PAD (rise)	1.03	1.52	1.986	3.699	0.0231*Cload+0.8171



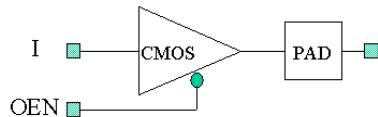
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cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PO24	I->PAD (fall)	1.13	1.449	1.751	2.869	0.0151*Cload+0.9881
PO24	I->PAD (rise)	1.092	1.451	1.772	2.923	0.0158*Cload+0.9602



POTx

CMOS 3-STATE OUTPUT PAD, 5V-Tolerant



● Truth Table

OEN	Input		Output PAD
	I	OEN	
1	x		Z
0	0		0
0	1		1

● Cell Information

Cell Name	No.Pad Req.	Power(μ W/MHz)	Drive Capability(mA)
POT2	1	72.52	
POT4	1	88.06	
POT8	1	91.44	
POT12	1	98.42	
POT16	1	99.07	
POT24	1	115.6	

● Pin Capacitance (pF)

Cell Name	C	I	OEN	PAD
POT2				
POT4				
POT8				
POT12				
POT16				

**POTx**CMOS 3-STATE OUTPUT PAD, 5V-Tolerant

● Propagation Delay(ns)

VDD_IO=3.3V, VDD_CORE=1.8V, temperature=25°C, typical process, standard load=0.00699 pf, input slew time=0.06ns (measured from 10% to 90% transition)

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
POT2	I->PAD (fall)	2.971	6.601	10.2	23.57	0.1789*Cload+1.2196
POT2	I->PAD (rise)	2.915	6.599	10.23	23.76	0.1812*Cload+1.1365
POT2	OEN->PAD (fall)	2.807	6.437	10.03	23.40	0.1789*Cload+1.0526
POT2	OEN->PAD (rise)	2.938	6.593	10.21	23.74	0.1808*Cload+1.1522

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
POT4	I->PAD (fall)	1.814	3.622	5.419	12.12	0.0895*Cload+0.9331
POT4	I->PAD (rise)	1.729	3.582	5.411	12.20	0.0909*Cload+0.8446
POT4	OEN->PAD (fall)	1.719	3.527	5.324	12.03	0.0896*Cload+0.8340
POT4	OEN->PAD (rise)	1.759	3.597	5.416	12.19	0.0906*Cload+0.8707

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
POT8	I->PAD (fall)	1.284	2.193	3.089	6.44	0.0448*Cload+0.8435
POT8	I->PAD (rise)	1.22	2.152	3.071	6.483	0.0457*Cload+0.7751
POT8	OEN->PAD (fall)	1.236	2.14	3.037	6.387	0.0447*Cload+0.7973

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POT8	OEN->PAD (rise)	1.247	2.174	3.089	6.489 0.0455*Cload+0.8041
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cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
POT12	I->PAD (fall)	1.129	1.737	2.336	4.568 0.0298*Cload+0.8407	
POT12	I->PAD (rise)	1.08	1.713	2.328	4.608 0.0306*Cload+0.7875	
POT12	OEN->PAD (fall)	1.095	1.698	2.296	4.528 0.0298*Cload+0.8025	
POT12	OEN->PAD (rise)	1.101	1.731	2.343	4.616 0.0305*Cload+0.8083	

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
POT16	I->PAD (fall)	1.069	1.526	1.976	3.65 0.0224*Cload+0.8512	
POT16	I->PAD (rise)	1.031	1.521	1.987	3.701 0.0232*Cload+0.813	
POT16	OEN->PAD (fall)	1.04	1.494	1.943	3.616 0.0223*Cload+0.8246	
POT16	OEN->PAD (rise)	1.05	1.536	1.999	3.708 0.0231*Cload+0.8316	

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
POT24	I->PAD (fall)	1.13	1.449	1.751	2.869 0.0151*Cload+0.9881	
POT24	I->PAD (rise)	1.092	1.451	1.771	2.922 0.0158*Cload+0.9597	
POT24	OEN->PAD (fall)	1.107	1.424	1.726	2.842 0.0150*Cload+0.9685	
POT24	OEN->PAD (rise)	1.097	1.454	1.772	2.921 0.0158*Cload+0.9617	



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POLx

POLx

CMOS OUTPUT Only PAD with LIMITED SLEW RATE , Tolerant



● Truth Table

Input	Output
I	Pad
1	1
0	0

● Cell Information

Cell Name	No.Pad Req.	Power(μ W/MHz)
POL8	1	83.95
POL12	1	95.45
POL16	1	106.6
POL24	1	124.2

● Pin Capacitance (pF)

Cell Name	C	PAD
POL8		
POL12		
POL16		

**POLx**CMOS OUTPUT Only PAD with LIMITED SLEW RATE , Tolerant

● Propagation Delay(ns)

VDD_IO=3.3V, VDD_CORE=1.8V, temperature=25 °C , typical process, standard load=0.00699 pf, input slew time=0.06ns (measured from 10% to 90% transition)

cell	delay_path	Sample Loads(pf)			Performance Equation
		10	30	50	
POL8	I->PAD (fall)	1.464	2.373	3.27	6.62 0.0448*Cload+1.0237
POL8	I->PAD (rise)	1.413	2.346	3.266	6.678 0.0457*Cload+0.9693

cell	delay_path	Sample Loads(pf)			Performance Equation
		10	30	50	
POL12	I->PAD (fall)	1.214	1.824	2.422	4.655 0.0299*Cload+0.9216
POL12	I->PAD (rise)	1.162	1.796	2.411	4.691 0.0306*Cload+0.8702

cell	delay_path	Sample Loads(pf)			Performance Equation
		10	30	50	
POL16	I->PAD (fall)	1.615	2.131	2.597	4.28 0.0231*Cload+1.4141
POL16	I->PAD (rise)	1.547	2.071	2.545	4.264 0.0236*Cload+1.3382

cell	delay_path	Sample Loads(pf)			Performance Equation
		10	30	50	
POL24	I->PAD (fall)	1.574	1.972	2.305	3.452 0.0162*Cload+1.455



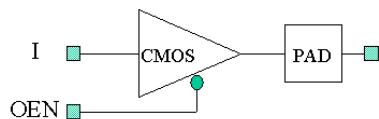
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POL24 I->PAD (rise) 1.531 1.935 2.273 3.44 0.0165*Cload+1.4078

POTLx

POTLx

CMOS 3-STATE OUTPUT PAD, with LIMITED SLEW RATE , 5V-Tolerant



● Truth Table

Input		Output	
OEN	I	PAD	
1	x	Z	
0	0	0	
0	1	1	

● Cell Information

Cell Name	No.Pad Req.	Power(μ W/MHz)	Drive Capability(mA)
POTL8	1	85.69	
POTL12	1	95.90	
POTL16	1	111.5	
POTL24	1	128.2	

● Pin Capacitance (pF)

Cell Name	C	I	OEN	PAD
POTL8				

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POTL12

POTL16

POTL24

POTLx

CMOS 3-STATE OUTPUT PAD, with LIMITED SLEW RATE , 5V-Tolerant

● Propagation Delay(ns)

VDD_{IO}=3.3V, VDD_{CORE}=1.8V, temperature=25°C, typical process, standard load=0.00699 pf, input slew time=0.06ns (measured from 10% to 90% transition)

cell	delay_path	Sample Loads(pf)			Performance Equation
		10	30	50	
POTL8	I->PAD (fall)	1.464	2.373	3.27	6.62 0.0448*Cload+1.0237
POTL8	I->PAD (rise)	1.414	2.348	3.267	6.679 0.0457*Cload+0.9706
POTL8	OEN->PAD (fall)	1.415	2.323	3.219	6.569 0.0448*Cload+0.9735
POTL8	OEN->PAD (rise)	1.428	2.358	3.273	6.674 0.0455*Cload+0.9876

cell	delay_path	Sample Loads(pf)			Performance Equation
		10	30	50	
POTL12	I->PAD (fall)	1.214	1.824	2.422	4.655 0.0299*Cload+0.9216
POTL12	I->PAD (rise)	1.163	1.797	2.412	4.692 0.0306*Cload+0.8712
POTL12	OEN->PAD (fall)	1.178	1.785	2.382	4.614 0.0298*Cload+0.888
POTL12	OEN->PAD (rise)	1.179	1.809	2.423	4.696 0.0305*Cload+0.8873

cell	delay_path	Sample Loads(pf)			Performance Equation
		10	30	50	
POTL16	I->PAD (fall)	1.615	2.131	2.597	4.28 0.0231*Cload+1.4141
POTL16	I->PAD (rise)	1.548	2.072	2.546	4.265 0.0236*Cload+1.3392
POTL16	OEN->PAD (fall)	1.572	2.092	2.558	4.241 0.0231*Cload+1.3741
POTL16	OEN->PAD (rise)	1.535	2.06	2.533	4.248 0.0235*Cload+1.3308

cell	delay_path	Sample Loads(pf)			Performance Equation
		10	30	50	
POTL24	I->PAD (fall)	1.574	1.972	2.305	3.452 0.0162*Cload+1.455
POTL24	I->PAD (rise)	1.533	1.936	2.275	3.441 0.0165*Cload+1.4093



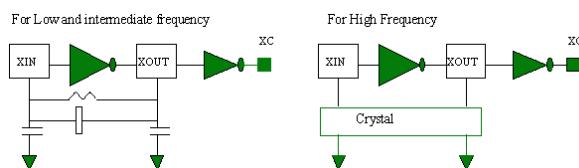
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POTL24	OEN->PAD (fall)	1.546	1.949	2.282	3.429 0.0163*Cload+1.4253
POTL24	OEN->PAD (rise)	1.507	1.912	2.251	3.416 0.0165*Cload+1.3846

PXx

PXx

Crystal Oscillator



● Truth Table

Input		Output	
XIN	XOUT	XC	
1	0	1	
0	1	0	

● Cell Information

Cell Name	No.Pad Req.	Power(μ W/MHz)
PX1	1	41.36
PX2	1	49.38
PX3	1	59.12



● Pin Capacitance (pF)

Cell Name	XC	XIN	XOUT
PX1			
PX1			
PX1			
PXx			
<i>Crystal Oscillator</i>			

● Propagation Delay(ns)

VDD_IO=3.3V, VDD_CORE=1.8V, temperature=25 °C , typical process, standard load=0.00699 pf, input slew time=0.06ns (measured from 10% to 90% transition)

cell	delay_path	Sample Loads (pf)				Performance Equation
		10	30	50	125	
PX1	XIN->XOUT (fall)	0.5512	1.199	1.843	4.254	0.0321*Cload+0.2364
PX1	XIN->XOUT (rise)	0.5512	1.199	1.843	4.254	0.0321*Cload+0.2364
cell	delay_path	Sample Loads (pf)				Performance Equation
		10	30	50	125	
PX2	XIN->XOUT (fall)	0.515	1.011	1.495	3.304	0.0242*Cload+0.2805
PX2	XIN->XOUT (rise)	0.515	1.011	1.495	3.304	0.0242*Cload+0.2805
cell	delay_path	Sample Loads (pf)				Performance Equation
		10	30	50	125	
PX3	XIN->XOUT (fall)	0.5081	0.9193	1.31	2.76	0.0195*Cload+0.3262
PX3	XIN->XOUT (rise)	0.5081	0.9193	1.31	2.76	0.0195*Cload+0.3262
cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PX1	XIN->XC (fall)	0.478	0.4792	0.4808	0.4826	0.0429*Cload+0.4786
PX1	XIN->XC (rise)	0.5041	0.506	0.5059	0.5103	0.0901*Cload+0.5034
cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PX2	XIN->XC (fall)	0.5011	0.5018	0.5051	0.509	0.0658*Cload+0.5019



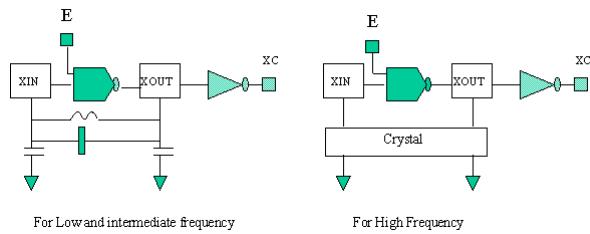
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PX2	XIN->XC (rise)	0.5308	0.5298	0.5319	0.5348	0.0271*Cload+0.5308
cell	delay_path	Standard	Load		Performance	Equation
		2	4	8	16	
PX3	XIN->XC (fall)	0.535	0.5357	0.5383	0.5375	0.5366-0.001*Cload
PX3	XIN->XC (rise)	0.5633	0.5642	0.5712	0.5712	0.0128*Cload+0.5670

PXWEx

PXWEx

Crystal Oscillator with HIGH ENABLE



● Truth Table

Input		Output	
E	XIN	XOUT	XC
1	1	0	1
1	0	1	0
0	1	1	0
0	0	1	0

● Cell Information

Cell Name	No.Pad Req.	Power(μ W/MHz)
PXWE1	1	52.63
PXWE2	1	60.76

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PXWE3	1	74.4
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● Pin Capacitance (pF)

Cell Name	XC	XIN	XOUT
PXWE1			
PXWE2			
PXWE3			
PXWEX			

Crystal Oscillator with HIGH ENABLE

● Propagation Delay(ns)

VDD_IO=3.3V, VDD_CORE=1.8V, temperature=25 °C , typical process, standard load=0.00699 pf, input slew time=0.06ns (measured from 10% to 90% transition)

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PXWE1	E->XC (rise)	0.5999	0.6017	0.6028	0.6043	0.0472*Cload+0.6005
PXWE1	E->XC (fall)	0.8411	0.8433	0.8456	0.850	0.0944*Cload+0.8417
PXWE1	XIN->XC (rise)	0.4833	0.4843	0.488	0.4909	0.0557*Cload+0.4846
PXWE1	XIN->XC (fall)	0.5578	0.5597	0.563	0.5685	0.1058*Cload+0.5585
cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PXWE2	E->XC (rise)	0.6236	0.6261	0.6281	0.6314	0.0829*Cload+0.6244
PXWE2	E->XC (fall)	0.8779	0.8795	0.881	0.8839	0.0643*Cload+0.8783
PXWE2	XIN->XC (rise)	0.5214	0.52	0.5218	0.5222	0.5218-0.014*Cload
PXWE2	XIN->XC (fall)	0.5988	0.5996	0.6016	0.6028	0.0286*Cload+0.5997
cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PXWE3	E->XC (rise)	0.6608	0.6615	0.6636	0.6654	0.0357*Cload+0.6615
PXWE3	E->XC (fall)	0.9302	0.931	0.9296	0.9328	0.0572*Cload+0.9289
PXWE3	XIN->XC (rise)	0.5549	0.5556	0.5587	0.5598	0.0257*Cload+0.5563
PXWE3	XIN->XC (fall)	0.6487	0.6495	0.6509	0.6536	0.0500*Cload+0.6489



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cell	delay_path	Sample Loads (pf)				Performance Equation
		10	30	50	125	
PXWE1	E->XOUT (rise)	1.033	1.998	2.963	6.578	0.0482*Cload+0.5522
PXWE1	E->XOUT (fall)	0.673	1.385	2.096	4.762	0.0355*Cload+0.3208
PXWE1	XIN->XOUT (rise)	0.7645	1.732	2.697	6.313	0.0482*Cload+0.2858
PXWE1	XIN->XOUT (fall)	0.7645	1.732	2.697	6.313	0.0482*Cload+0.2858
cell	delay_path	Sample Loads (pf)				Performance Equation
		10	30	50	125	
PXWE2	E->XOUT (rise)	0.926	1.568	2.21	4.62	0.0321*Cload+0.6056
PXWE2	E->XOUT (fall)	0.615	1.123	1.631	3.535	0.0253*Cload+0.3661
PXWE2	XIN->XOUT (rise)	0.6648	1.317	1.961	4.372	0.0322*Cload+0.3479
PXWE2	XIN->XOUT (fall)	0.6648	1.317	1.961	4.372	0.0322*Cload+0.3479
cell	delay_path	Sample Loads (pf)				Performance Equation
		10	30	50	125	
PXWE3	E->XOUT (rise)	0.9081	1.387	1.868	3.675	0.0240*Cload+0.6695
PXWE3	E->XOUT (fall)	0.6043	1.001	1.395	2.877	0.0197*Cload+0.4104
PXWE3	XIN->XOUT (rise)	0.6465	1.15	1.635	3.446	0.0243*Cload+0.4132
PXWE3	XIN->XOUT (fall)	0.6465	1.15	1.635	3.446	0.0243*Cload+0.4132



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PVDD1

PVDD1

Vdd Pad and Digital Power Supply Cell for 1.8V

● Cell Information

Cell Name	No. Pad Req.
PVDD1	1



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PVDD2

PVDD2

Vdd Pad and Digital Power Supply Cell for 3.3V

● Cell Information

Cell Name	No. Pad Req.
PVDD2	1



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PVSS1

PVSS1

Vss Pad and Ground for 1.8V

● Cell Information

Cell Name	No. Pad Req.	Power(µ W/MHz)
PVSS1	1	



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PVSS2

PVSS2

Vss Pad and Ground for 3.3V

● Cell Information

Cell Name	No. Pad Req.	Power(µ W/MHz)
PVSS2	1	



Appendix A (Maximum Allowable Current for Digital Power and Ground Cells)

The following table lists the maximum allowable current for the **SP018 I/O Digital** power/ground cells and bonding pads. The maximum allowable current for the different metal layer is provided. The power/ground cells and bonding pads will limit the maximum safety current for metal electro-migration consideration (EM).

The power cell, ground cell and the bonding pad determine the maximum allowable current. Whichever is smaller will be applied. For examples, if I/O cell PVSS3 + PADO40 pad and Metal 6 tape-out are used, the maximum current is 83mA in which limited by PADO40.

If PVDD2 + PADI40 and Metal 4 tape-out are used, the current is 39mA (limited by PVDD2).

Maximum Allowable Current Of Digital I/O Power/Ground Cells and Bonding Pads

	PVDD1	PVDD2	PVSS1	PVSS2	PVSS3	PADI40	PADO40
Metal 4 tape-out	42mA	39mA	42mA	101mA	101mA	140mA	63mA
Metal 5 tape-out	42mA	39mA	42mA	133mA	133mA	171mA	72mA
Metal 6 tape-out	42mA	39mA	42mA	165mA	165mA	201mA	83mA

	PADI45	PADI50	PADI55	PADI60	PADI65
Metal 4 tape-out	140mA	140mA	140mA	140mA	140mA
Metal 5 tape-out	171mA	171mA	171mA	171mA	171mA
Metal 6 tape-out	201mA	201mA	201mA	201mA	201mA

	PVDD1	PVDD2	PVSS1	PVSS2	PVSS3	BONDING PADS
Metal layer of I/O that connect to core circuit	Metal 1-6	/	Metal 1-2	/	Metal 1-2	/

Please notice the maximum allowable current in table above is corresponding to I/O power/ground cells only. The amount of current that can be provided to the core logic is related to the number of metal layer that interconnect the I/O and core logic. For an example, PVSS1 use Metal 1 and 2 to connect with the core circuit.



Appendix B (Maximum Allowable Current for Analog Power and Ground Cells)

Maximum Allowable Current Of Analog I/O Power/Ground Cells and Bonding Pads

Analog I/O Cell	Metal 4 Tapeout	Metal 5 Tapeout	Metal 6 Tapeout	Metal layer of I/O that connect to core circuit
PANA1AP	42mA	42mA	42mA	Metal 1-2
PANA1AP1	42mA	42mA	42mA	Metal 1-2
PANA2AP	11mA	11mA	11mA	Metal 2
PANA2AP1	11mA	11mA	11mA	Metal 2
PVDD1AP	42mA	42mA	42mA	Metal 1-2
PVDD1AP1	42mA	42mA	42mA	Metal 1-2
PVDD2AP	40mA	40mA	40mA	/
PVDD3AP	40mA	40mA	40mA	Metal 1-6
PVDD4AP	42mA	42mA	42mA	/
PVDD5AP	40mA	40mA	40mA	/
PVSS1AP	42mA	42mA	42mA	Metal 1-2
PVSS1AP1	42mA	42mA	42mA	Metal 1-2
PVSS2AP	101mA	133mA	165mA	/
PVSS3AP	101mA	133mA	165mA	Metal 1-2
PVSS4AP	42mA	42mA	42mA	/
PVSS5AP	101mA	133mA	165mA	/
PVDD1ANP	42mA	42mA	42mA	Metal 1-2
PVSS1ANP	42mA	42mA	42mA	Metal 1-2
PVDD1CAP	42mA	42mA	42mA	Metal 1-2
PVDD1CAP1	42mA	42mA	42mA	Metal 1-2
PVSS1CAP	42mA	42mA	42mA	Metal 1-2
PVSS1CAP1	42mA	42mA	42mA	Metal 1-2
PVDD3CAP	40mA	40mA	40mA	Metal 1-6
PVSS3CAP	101mA	133mA	165mA	Metal 1-2
PANA4AP	39mA	39mA	39mA	Metal 2-3
PANA3AP	39mA	39mA	39mA	Metal 2-3

Please notice the maximum allowable current in table above is corresponding to I/O power/ground cells only. The amount of current that can be provided to the core logic is related to the number of metal layer that interconnect the I/O and core logic. Please take notice that metal layer of PANA2AP and PANA2AP1 I/Os that connect to core logic is metal 2.