SMIC
I/O Application Check List

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Semiconductor Manufacturing International Corporation

SMIC I/O Application Check List

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Document Revision History

VERSION	*EFFECTIVE DATE*	*NOTE AND CHANGE DESCRIPTION*
0.0	May 7, 2008	Preliminary version of Application Check List
0.1	May 22, 2008	1). Update Check List 2). Add IP List of power buses information 3). Add Summary table
0.2	June 2, 2008	1). Update Check List 2). Update IP List of power buses information
0.3	October 15, 2008	1). Update Check List 2). Update IP List of power buses information 3). Add description of check items 4). Add version history
0.4	August 28, 2009	1). Update Check List item No.7
0.5	December 18, 2009	1). Update Check List item No.12
0.6	March 15, 2010	1). Add Check List item No.16

Version History)

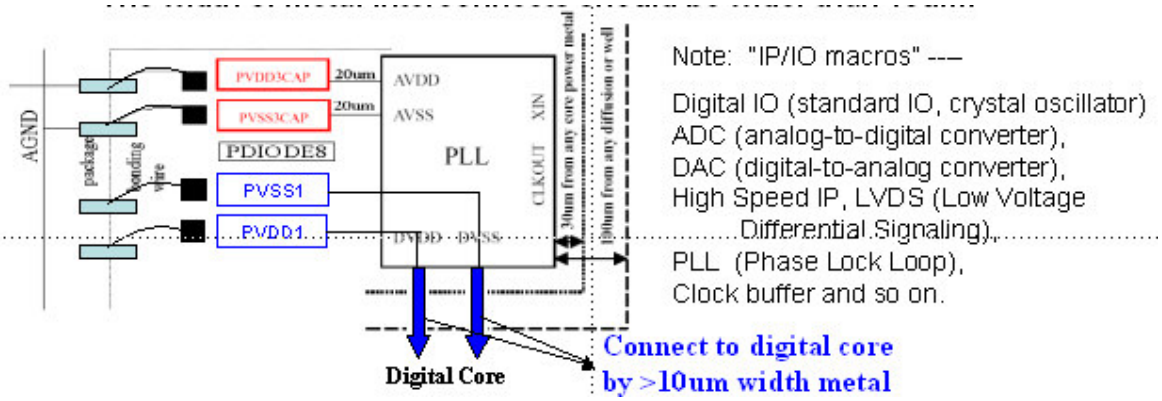
Document Version	GDS Version	Date	Total Pin Count

I/O Application Check List

(1). Check List

To ensure proper floorplan design for each chip, users should confirm that the following check items are obeyed. The page can help to verify if the design meets all check items.

No.	**Check Items** (V3.0)	Result	Violation Description
1	Please refer to the latest version of I/O Application Note regarding power/ground pad application.		
2	The ratio of I/O cell number to power/ground cell number should be consistent with SSO (Simultaneous Switching Output noise) rules.		
3	The post-driver ground bus of the I/O cells should form an unbroken ring.		
4	In one chip, the number of power domains separated by power-cut cells PDIODE, PDIODE8, P1DIODE and P1DIODE8 must be less than or equal to four. (Refer to IO application note Chapter 7.2)		
5	When ports connected to pads are higher than core voltage, PVDD1AP/PVDD1AP1/PVDD3AP should be used. (Refer to IO application note Chapter 5)		
6	When ports connected to pads are equal to or lower than core voltage, PVDD1CAP/PVDD1CAP1/PVDD3CAP should be used. (Refer to IO application note Chapter 5)		
7	**Connect power/ground pins of interface to chip's digital core in every IP/IO macros (e.g. DVDD, DVSS in a digital IO, PLL, clock buffer, ADC, DAC, LVDS and high speed IPs) to the chip's digital core area. The width of metal interconnects should be wider than 10um.** (Refer to PIC.1)		**FILL IN THE *ALL IP LIST* FORM**
8	The core power generated by the voltage regulator should be connected to the core protection device of PVDD1, PVDD1CAP or PVDD3CAP.		
9	For each side of the chip, the core must be supplied with at least two pairs of respective power/ground cells (except of PVDD1CE) for each digital or analog power domain, regardless of whether the core is already supplied by a voltage regulator.		
10	If PVDD1CE is included in I/O library, for each side of the chip, it's preferable to supply at least one PVDD1CE within each digital power domain. The PVDD1CE pin should be connected to the chip digital core area through at least 20um wide metal layer.		
11	Add dummy power/ground cells to the I/O pad ring instead of filler cells. (Refer to IO application note Chapter 7.1)		
12	ESD protection devices should be added between the digital/analog interfaces.		
13	Users must add embedded ESD resistors when using secondary ESD devices.		
14	Use a tie-high/tie-low cell to connect an I/O cell pin to power/ground rather than connecting directly. (Refer to IO application note Chapter 7.3)		
15	Any modification to SMIC I/O data is prohibited. In case modification is required, user must report to SMIC for verification.		
16	Every digital I/O power domain should be composed of I/O cell, power/ground cell (PVDD1, PVDD2, PVSS1 and PVSS2) and power cut cell. All the power buses and signal buses should be integrated. Signal buses "FP" and "FPb" should be supplied by PVDD2.		



PIC.1 Example for Item 7

(2). All IP List used in the Project

To enhance ESD performance, especially for every IP macro, users should fill the *All IP List* form with all of the IPs are used in the chip to ensure the *Item 7* in the *Check List* is obeyed. IPs should include which users owned, SMIC and 3rd licensed, etc. The page can help to verify if the design meets all check items.

(Item 1 and 2 in blue are examples of connection.)

Item	Provider	IP/Library Name	Ver.	Power/Ground Buses						
				Port Name	Description	Connection to **CORE**				Connection to I/O PAD
						NET	Coordinate	Metal		NET (I/O Cell)
								Layer	Width	
1	SMIC	Sxxx_PLL	1.1	DVDD	Digital 1.2V	VDD	(5320.25, 625.35)	M5	10u*1	VDD_PLL (PVDD1)
				DVSS	Digital ground	VSS	(5350.25, 625.35)	M5	10u*1	VSS_PLL (PVSS1)
				AVDD	Analog 1.2V					SAVDD (PVDD1CAP)
				AVSS	Analog ground					SAVSS (PVSS1CAP)
2	xxxxx	xxx_ADC	x.x	DVDDA	Digital 1.2V	VDD	(5052.50, 2685.55)	M4	8u*2	VDD_ADC (PVDD1)
				DVSSA	Digital ground	VSS	(5052.50, 2710.55)	M4	8u*2	VSS_ADC (PVSS1)
				AVDDA	Analog 1.2V					SAVDD (PVDD1CAP)
				AVSSA	Analog ground					SAVSS (PVSS1CAP)

(3). Summary: