SMIC
Standard I/O Library
Application Notes

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Semiconductor Manufacturing International Corporation

SMIC Standard I/O Library Application Notes

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1. Document Revision History

VERSION	*EFFECTIVE DATE*	*NOTE AND CHANGE DESCRIPTION*
0.1	2 April 2003	Initial version of Application Notes
1.0	30 June 2003	Minor content is revised
1.1	24 July 2003	Examples of PVDDxAPx cells to support various power separation schemes (Figure 6a and Figure 6b)
1.2	2 September 2003	Examples of Placement and Routing for PLL with I/O cells (Figure 11a and 11b)
1.3	10 September 2003	Description of crystal oscillator PXWERx and PXWRx
1.4	18 November 2003	Description of IP usage statement on page iii and statement of recommendation usage of Analog cells on page 10
1.5	1 December 2003	■ Description of Analog cells usage on page 10, 11(Figure 3), 12(Table 1 and Fig.4), 13 (Fig5, 5a), 16 and 20 ■ Page 23 Noise immunity for Oscillator I/O ■ Page 23 ~ 25 I/O bonding with PLL (Fig.11, a, & b)
1.6	24 December 2003	■ Contents are revised
1.7	21 April 2004	■ Description of ESD mask in Chapter 13
1.8	20 July 2004	■ Update Figure 6b
1.9	2 August 2004	■ Add description of Bonding PAD in chapter 4 ■ Add PVDD1ANP contents in page 5 and Table 1, add PVSS1ANP contents in page 5 ■ Annotate “>”& ”<=” core voltage notation of Table 1 ■ Add description of PANA3AP and PANA4AP in Chapter 5.1 and Table 2 ■ Modify topic of Table 4
2.0	26 August 2004	■ Add section 7.3 tie high/tie low
2.1	27 December	■ Add description of PDIODE cell usage

	2004	
2.2	11 May, 2006	■ Add one power cut cells: PDIODE8S ■ Add application description of analog cell, filler cells, power cut cells ■ Add continuity test method in Chapter 10
2.3	12 April 2007	■ Delete voltage value in chapter 3 picture ■ Add bonding pad general description in first paragraph of chapter 4 ■ Delete suggestion that not to use Type 1 analog power/ground cells group in chapter 5 ■ Revise Table 1 PVDD4AP cell in chapter 5 ■ Update digital power/ground cell and analog IO cell PANA3AP description in chapter 5 ■ Update usage of PANAxAPx cells in chapter 5.1 ■ Modify VDD guard rail to Power guard rail and VSS guard rail to Ground guard rail in chapter 7.2 ■ Delete suggestion by using metal 1 to connect guard ring in chapter 7.2 ■ Revise unit of Rf from 1MHz to 1Mohm in chapter 10 ■ Add crystal oscillator I/O description that with internal resistor in chapter 10 ■ Add information of I/O cells used with IP macros and update figure 11, 11a, 11b in chapter 11 ■ Update FP description in chapter 12
2.4	27 April 2007	■ Add the number of power/ground cells supplied to core in chapter 5 ■ Update figure 11, 11a, 11b in chapter 11 by adding connection metal width
2.5	July 2, 2007	■ Add PANA3AP tolerance description in chapter 5.1 Analog I/O cells PANAxAPx
2.6	January 14, 2008	■ Update description that power/ground cells supplied to core for circuit performance and ESD concerns in chapter 5 ■ Add Appendix A. ESD check list
2.7	March 12, 2008	■ Add P1DIODE and P1DIODE8 cells application descriptions
2.8	June 2, 2008	■ Add power cell PVDD1CE application descriptions in Chapter 5 and Chapter7.1 ■ Update Appendix A. ESD check list

2.9	July 3, 2008	■ Add Chapter 2.2: synthesis library application sequence ■ Add FPB description
3.0	October 17, 2008	■ Add descriptions of PVDD1CANP, PVSS1CANP and PVPP

2. Introduction

SMIC's *Standard I/O Library* offering provides a great deal of I/O flexibility. This document describes the application of *SMIC Standard I/O Library*. Its will provide a general application knowledge and common understanding for the user about *SMIC Standard I/O Library* application requirement.

2.1 Outline Of The Document

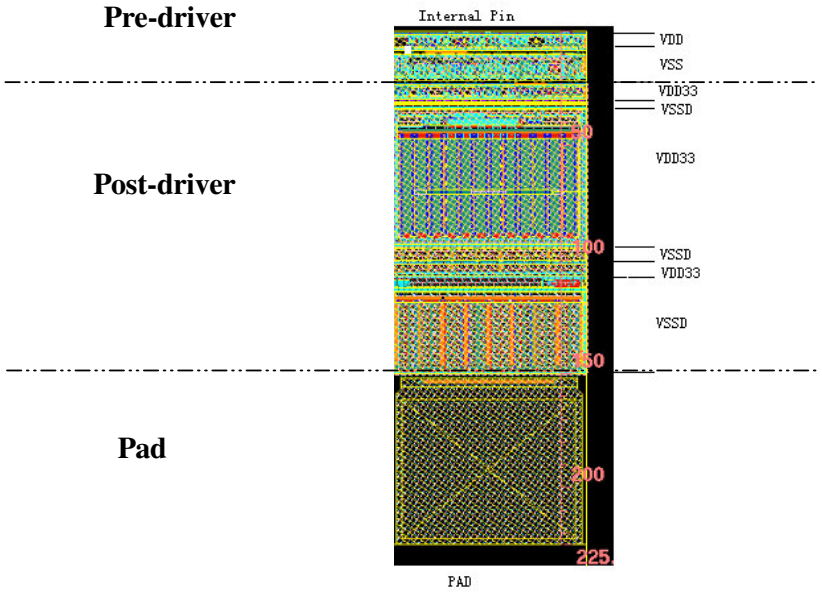
SMIC standard I/O layout configuration and structure will be discussed in Chapter 3. These include I/O power/ground rails and I/O cell layout sample.
Chapter 4 presented the bonding pad structure, such as in-line and stagger bonding pad. Bonding pad placement also addressed in detail.
The main power supply cells will be studied in Chapter 5. These include the basic concept and structure of SMIC Standard I/O's analog and digital power supply cells. Descriptions of various type analog I/O cells for low and high frequency applications are also presented.
I/O cells are very sensitive to the power up/down sequence since *SMIC Standard I/O Library* use different voltage supply for pre-driver and post driver. A perfectly good power up/down sequence is examined in Chapter 6 in order to avoid the impact of latch-up.
The ESD protection methodology on the I/O performance is discussed in Chapter 7. The function of power cut cell and dummy power/ground cell will also be discussed.
In Chapter 8 no pad I/O cell, such as I/O power/ground cell, filler and corner cell will be discussed.
Chapter 9 examines the maximum allowable currents for power I/O pad and electromigration effect consideration. Oscillator I/O cells usage and power I/O cell with IP macros especially Phase Lock Loop (PLL) is studies in Chapter 10 and Chapter 11 respectively. LVS verification will be presented in Chapter 12.
Chapter 13 will make a list of proper tape-out steps with SMIC Standard I/O Library.

2.2 Synthesis Library Application Sequence

When using different synthesis and static timing analysis tools (such as Design Compiler, RTL Compiler and PrimeTime), user maybe meets timing delay difference issue for same synthesis library. To avoid this kind of issue, SMIC recommend: when using synthesis tool, user should input Standard Cell synthesis library ***first*** then Standard I/O synthesis library.

3. I/O Layout And Power/Ground rails

In this Chapter SMIC Standard I/O cell layout sample, the detail of the I/O cell layout configuration and structure of power supplies and ground rails are presented. SMIC Standard I/O structure is constructed by pre-driver and post-driver section as shown in the layout sample below. Each section has its own function. Pre-driver provides logic operation for I/O circuit, and post-driver provides large driving capability and ESD protection ability. For more detail please refer to specific SMIC I/O Data Book.



4. Bonding PAD

Different SMIC I/O libraries provide different types of bonding pad cells. Refer to specific SMIC I/O data book to get provided bonding pads. The section is one basic introduction of bonding pad cells usage.

SMIC Standard I/O Library has provided two types of bonding pad cells: PADI40 and PADO40 for *SP018* library. Pad cells PADI35 and PADO35 for *SP018N* library. These cells can be used for inline pad and staggered pad, while the latter is for die area optimization. Stagger pad style design cannot apply to the I/O cell that have already including pad, such as *SMIC SP018W*, *SP025* and *SP035R's* I/O cell. Please notice that pad cell size of PADI40 and PADO40 is 40um × 200um. For PADI35 and PADO35, the pad cell size is 35um × 235um.

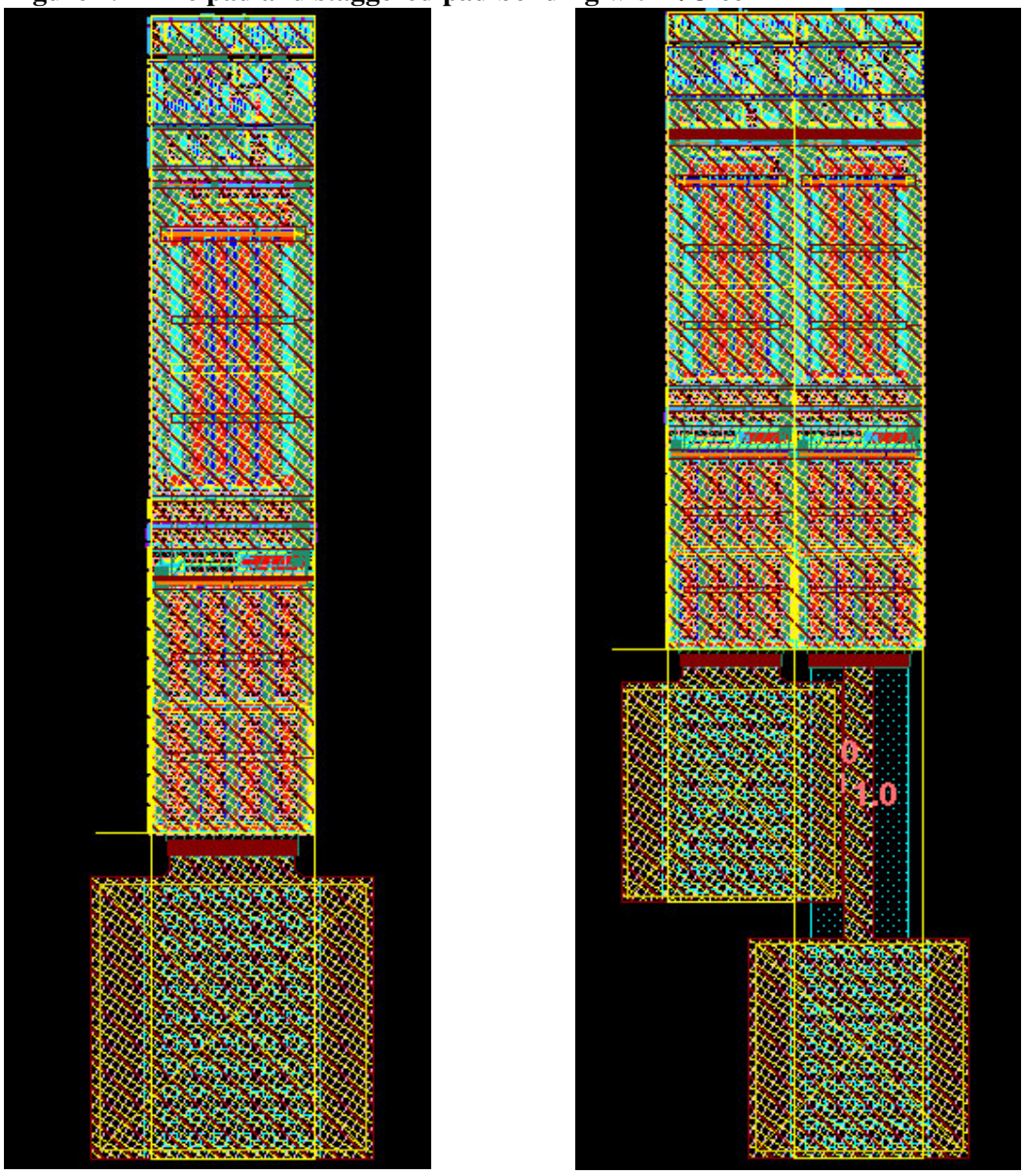
SMIC Offer different pitches IO cells such as *SP018* (40um-pitch), *SP018W* (76um-pitch) and *SP018N* (35um-pitch). In which I/O cell pitch is defined as the width of the I/O cell plus the space in between two adjacent I/O cells.

If the pad's pitch is concerned in design, SMIC will provide and design several specific special pad cells according to the customer's request: PADI45 (40um × 57um); PADI50 (43um × 57um); PADI55 (48um × 57um); PADI60 (53um × 57um); PADI65 (58um × 57um); and please notice here the size is pad opening window size (Width x height). These special pad cells have narrower in width than the other pad cell. For examples in the case of *SP018* library is applied:

1. While PAD pitch requirement is greater than 80um, use PADI40 for inline IO bonding.
2. For stagger bonding pad, use combination of both PADI40 and PADO40 pad cell (refer to Figure 1).
3. For specific special pad cells, if required PAD pitch is greater than 45um, PADI45 can be used for inline IO bonding; if required PAD pitch is greater than 50um, PADI50 can be used for inline IO bonding; if required PAD pitch is greater than 55um, PADI55 can be used for inline IO bonding; if required PAD pitch is greater than 60um, PADI60 can be used for inline IO bonding; if required PAD pitch is greater than 65um, PADI65 can be used for inline IO bonding.

Placement Application Notice: pad cells have same width of Place and Route (P&R) boundary (gds layer# 127) as the IO cells. While pad cell is bonding with I/O cell, connect them with no space left, and the pad P&R boundary is put in the same alignment with the P&R boundary of IO cell, so the pad seems as an extension of IO cell according to P&R boundary (refer to Figure 1).

Figure 1. Inline pad and staggered pad bonding with I/O cell



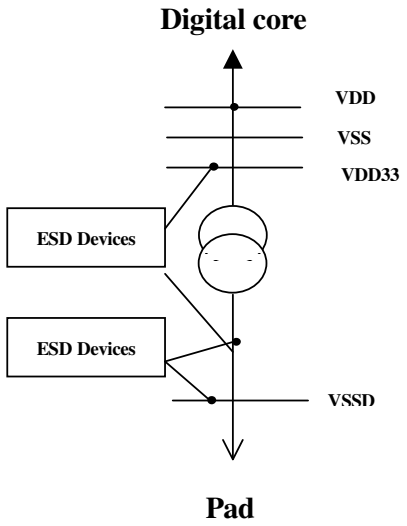
5. Analog and Digital Power Supply Cells

The basic concept and structure of SMIC Standard I/O's analog and digital power supply cells are presented in this Chapter. This includes symbolic of Digital Power Supply Cell and Analog Power Supply Cell, description and development of the power supply cells. Descriptions of various type analog I/O cells for low and high frequency applications are also presented in this chapter. ***The SMIC analog IO library is specially designed for SMIC mixed mode macros. SMIC does not recommend customers to use this library to interface with non-SMIC analog macros. Misuse of the analog library may cause damages to customer's chip.***

Due to circuit performance and ESD protection concerns, it is necessary to ensure that for each side of the chip, the core is supplied with at least two pairs of respective power/ground cells for each digital or analog power domain. This requirement stands regardless of whether the core is already supplied by a voltage regulator.

The following section list various type of SMIC Digital Power Supply Cell. **Digital power supply cells:** PVDD1, PVDD2, PVSS1, PVSS2, and PVSS3. The digital power supply cell symbolic of PVDD1 is shown in Figure 2 below.

Figure 2. Digital power supply cell (PVDD1) symbolic



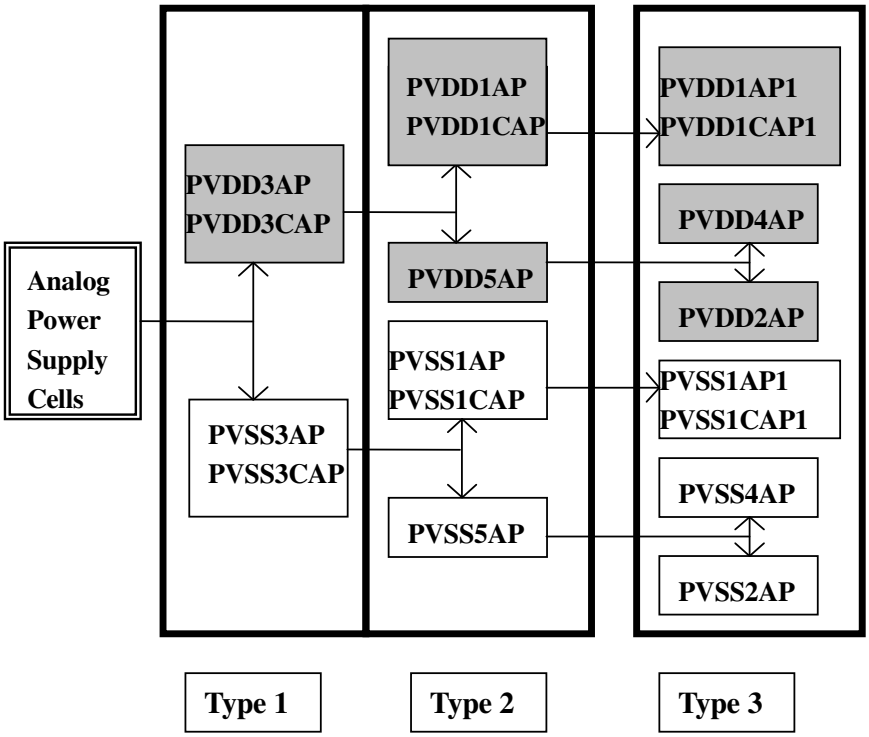
PVDD1 and PVSS1 are power and ground for pre-driver and core respectively.
PVDD2 and PVSS2 are power and ground for post-driver respectively.

PVSS3 is the combination of PVSS1 and PVSS2. In this case, power supply cell PVSS3 is connect with different VSS lines (VSS and VSSD).
PVDD1CE is one digital Vdd power cell for core ESD protection (without pad opening window). Refer to chapter 7.1 for more information.

Analog power supply cells used within digital power domain.
There are two pairs of analog cells PVDD1ANP/PVSS1ANP and PVDD1CANP/PVSS1CANP used within digital power domain.
PVDD1ANP and PVDD1CANP are VDD analog PAD within digital power domain.
PVSS1ANP and PVSS1CANP are VSS analog PAD within digital power domain.
About PVDD1ANP and PVDD1CANP please see more information in Table 1.

Analog power supply cells : PVPP , PVDDxAPx and PVSSxAPx. They should be placed in analog domain.
PVPP is Vdd power supply cell for testing pin only. PVDDxAPx and PVSSxAPx are listed in Figure 3, in which the family tree of analog power supply cells is illustrated. There are 3 types of power supply cell combination as shown in Figure 3. The purpose to develop PVDD3AP and PVSS3AP cells family tree is to diversify power in order to obtain and provide noise free power for the analog application circuit. The others analog I/O cells are called **PANAxAPx** and will be introduced in the section 5.1.

Figure 3. Analog Power Supply Cells family tree



The development concept can be revealed clearly in Figure 4. Figure 4 presents a simplified power diagram of cells PVDD3AP. Observably, PVDD3AP is used to supply all core, pre-driver and post drivers, and is equivalent to PVDD1AP + PVDD5AP. Two cells can again replace PVDD5AP. Which are PVDD4AP and PVDD2AP. Moreover, cells PVDD1AP1 is distinguished from PVDD1AP by using a different power/ground rail for ESD devices. The details description and power connection are listed in Table 1 and the power rail diagram of PVDDxAPx family is shown in Figure 5 and 5(a).
Cells PVSSxAPx are similar with PVDDxAPx.

Figure 4. A simplified power diagram of PVDD3AP and PVDD3CAP

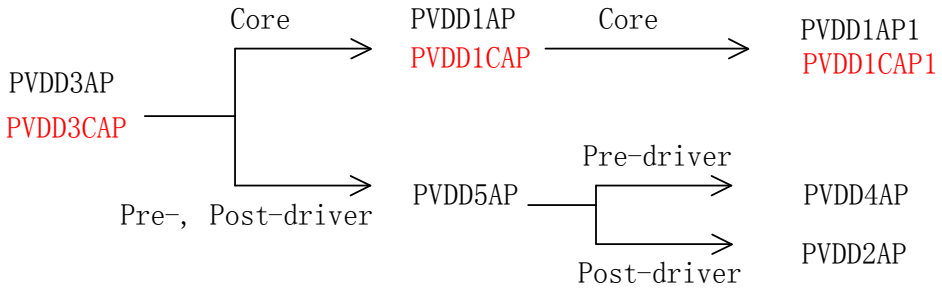


Table 1.

Cell Name	Port connected to core	Port connected to bonding pad	Pre-driver Power	Post-driver Power	Description
PVDD1AP >Core voltage	SVDD1AP	SVDD1AP	SAVDD	SAVDD	Separate power provider for core logic only
PVDD1AP1 >Core Voltage	SVDD1AP1	SVDD1AP1	SAVDD	SAVDD33	Similar duplicate of PVDD1AP but use different post-driver power
PVDD1CAP <=Core Voltage	SVDD1CAP	SVDD1CAP	SAVDD	SAVDD	Separate power provider for core logic only
PVDD1CAP1 <=Core Voltage	SVDD1CAP1	SVDD1CAP1	SAVDD	SAVDD33	Similar duplicate of PVDD1AP but use different post-driver power
PVDD2AP	(Null)	SAVDD33	SAVDD	SAVDD33	Separate power provider for post-driver rail only

PVDD3AP >Core Voltage	**SAVDD**	**SAVDD**	**SAVDD**	**SAVDD**	**Power provider for all core pro-driver and post-driver rails**
PVDD3CAP <=Core Voltage	**SAVDD**	**SAVDD**	**SAVDD**	**SAVDD**	**Power provider for all core pro-driver and post-driver rails**
PVDD4AP	**(Null)**	**SAVDD**	**SAVDD**	**SAVDD33**	**Separate power provider for pre-driver rail only**
PVDD5AP	**(Null)**	**SAVDD**	**SAVDD**	**SAVDD**	**Separate power provider for pre- and post-driver rails**
PVDD1ANP >Core voltage	**SVDD1ANP**	**SVDD1ANP**	**VDD**	**VDD33**	**Separate power provider for core logic only used within digital power domain**
PVDD1CANP <=Core voltage	**SVDD1CANP**	**SVDD1CANP**	**VDD**	**VDD33**	**Separate power provider for core logic only used within digital power domain**

Note:

">Core Voltage" means the voltage of port connected to pad is higher than core voltage, and "<=Core Voltage" means the voltage of port connected to pad is equal to or lower than core voltage. Of course, core voltage is different because different library I/O. For example 0.18μm I/O core Voltage: 1.8V, 0.15μm I/O core Voltage: 1.5V, 0.13μm Generic I/O core Voltage is 1.2V and etc.

According to Table 1, for instance, for 0.18μm I/O, which I/O core voltage is 1.8V, if the voltage of port connected to pad is higher than 1.8V, PVDD1AP should be used; if the voltage of port connected to pad is equal to or lower than 1.8V, PVDD1CAP should be used. Any random application of cell in Table 1 maybe cause unpredictable risk or danger for circuit performance, that's means, the user should care for the voltage of port connected to pad and core voltage to have a correct application. The following two kinds of application are prohibited: PVDD1AP is used when the voltage of port connected to pad is equal to or lower than 1.8V; PVDD1CAP is used when the voltage of port connected to pad is higher than1.8V.

Figure 5. The power rail diagram of PVDDxAPx family

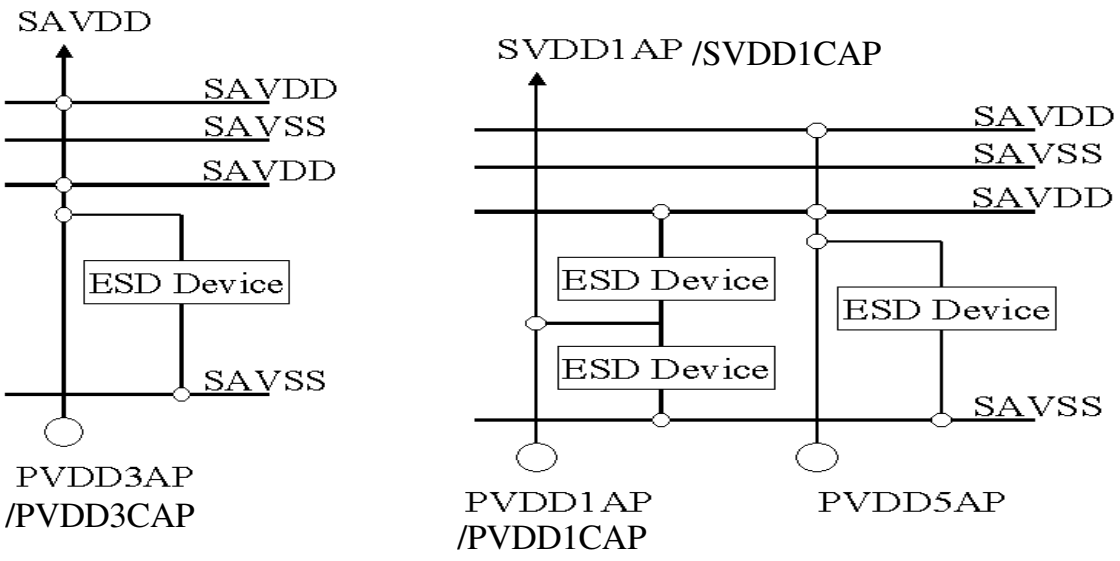
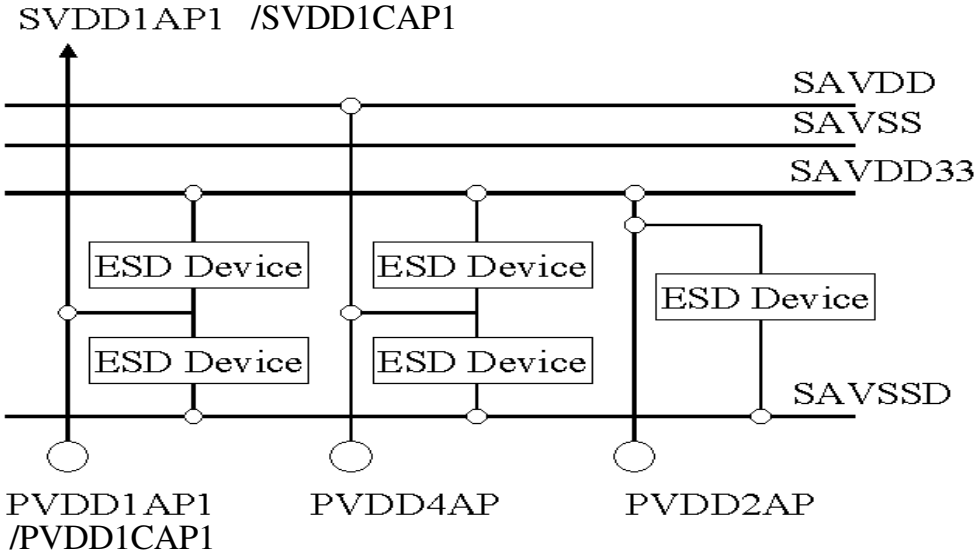


Figure 5(a). The power rail diagram of PVDDxAPx family



Notice that in Figure 5 the power rails that are labeled SAVDD and SAVDD means the pre- and post- power rails are the same voltage. It can be 1.8V, 2.5V or 3.3V. Please note PVDD5AP can be any voltage of customer's needs. However, PVDD1AP should be less than or equal to the voltage of PVDD5AP. Cells PVDDxAPx (x=1, 2) are used with power cut cells PDIODEx/P1DIODEx to support various power separation schemes, and numerous cells are offered to support separate power schemes of different

levels. For an example, cells PVDD3AP and PVSS3AP provide the power and ground of rails for pre- and post- drivers, while cell PANA1AP uses this isolated power/ground pair to sustain the power of the ESD device (Refer to Figure 6).

Another two examples of PVDDxAPx cells that are used to support various power separation schemes as shown in Figure 6a and Figure 6b. Where Figure 6a is for power supply cells (PVDD1AP, PVDD5AP, PVSS1AP and PVSS5AP) with I/O PANAxAP cell. Figure 6b illustrated power supply cells (PVDD1AP1, PVDD4AP, PVDD2AP, PVSS1AP1, PVSS2AP and PVSS4AP) with I/O PANAxAP1 cell.

Figure 6. Power supply cells (PVSS3AP and PVDD3AP) with I/O PANA1AP cell

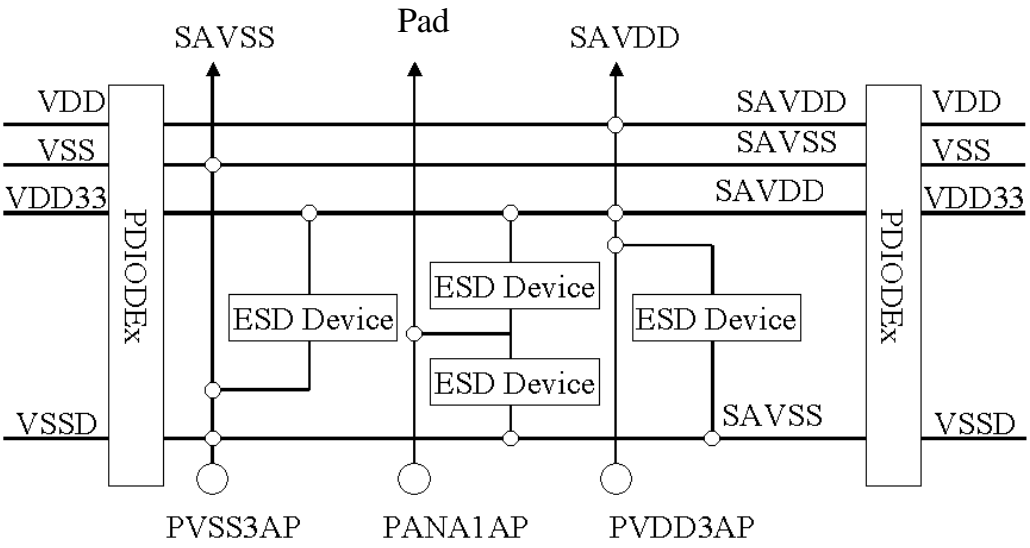


Figure 6a. Power supply cells (PVDD1AP, PVDD5AP, PVSS1AP and PVSS5AP) with I/O PANAxAP cell.

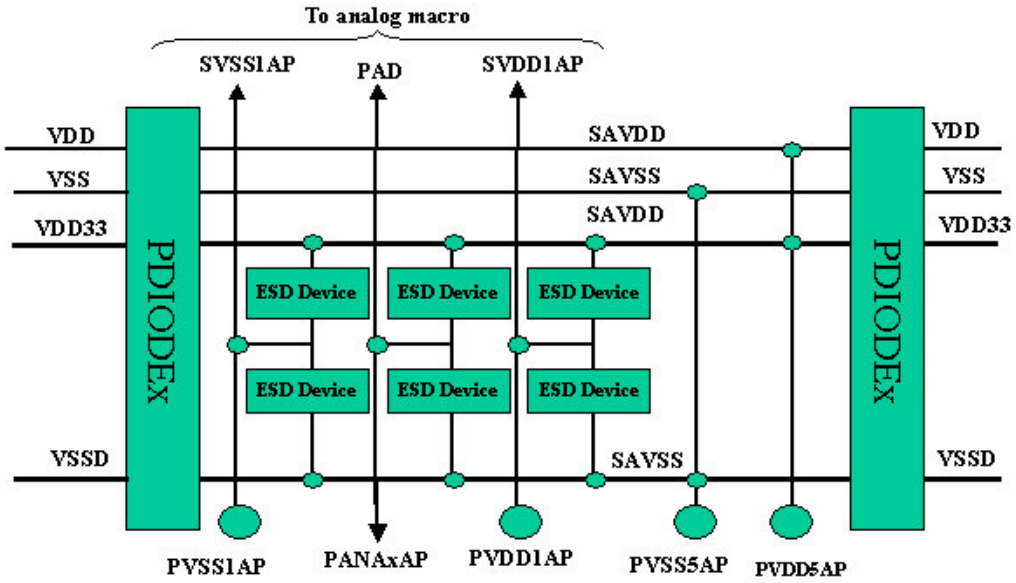
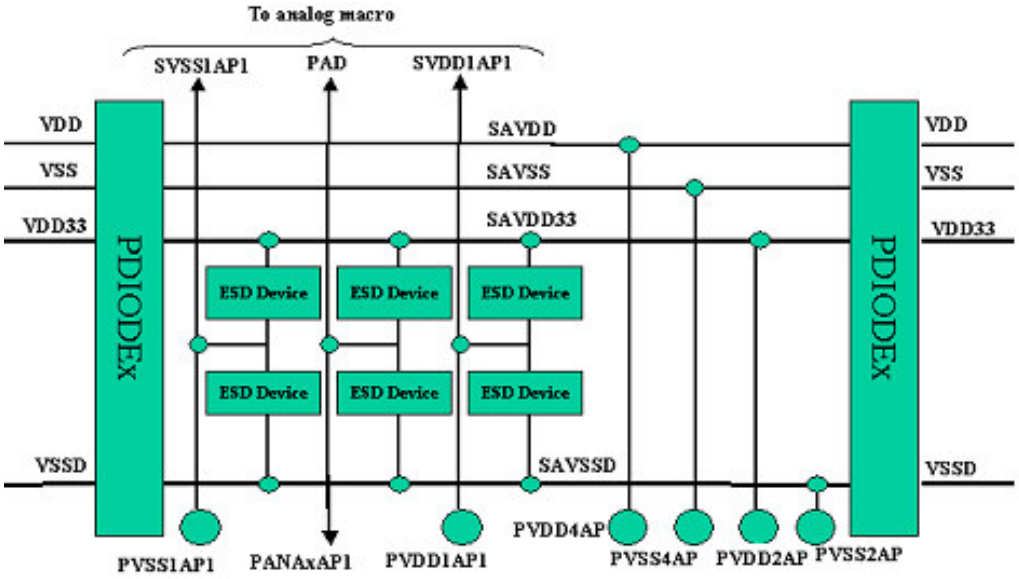


Figure 6b. Power supply cells PVDD1AP1, PVDD4AP, PVDD2AP, PVSS1AP1, PVSS2AP and PVSS4AP) with I/O PANAxAP1 cell.



Note: **SMIC does not recommend customers to use this library to interface with non-SMIC analog macros. Misuse of the analog library may cause damages to customer's product.**

5.1 Analog I/O cells PANAxAPx

SMIC Standard I/O Library provides analog I/O **PANA1AP, PANA1AP1, PANA2AP, PANA2AP1, PANA3AP and PANA4AP.** Where PANA1AP1 and PANA2AP1 cells are operate in a different post-driver power. Refer to the Table 2 below to distinguish the different between PANAxAPx cells. From test result PANA2AP has better high frequency response than PANA1AP.

Table 2. Description of analog I/O pad PANAxAPx

Analog I/O Cell Name	Description
PANA1AP (For low frequency application)	Connect to SAVDD, SAVSS and output to analog core
PANA1AP1 (For low frequency application)	Connect to SAVDD, SAVSS, SAVDD33, SAVSSD and output to analog core

PANA2AP (For high frequency application)	Connect to SAVDD, SAVSS and output to analog core
PANA2AP1 (For high frequency application)	Connect to SAVDD, SAVSS, SAVDD33, SAVSSD and output to analog core
PANA4AP (For high frequency application and higher maximum allowable current capability)	Connect to SAVDD, SAVSS and output to analog core
PANA3AP (For high frequency application and 5V (for 3.3 I/O Application) tolerance or 3.3V(for 2.5V I/O Application) tolerance)	Connect to SAVDD, SAVSS and output to analog core

Note: SAVDD and SAVSS stand for SMIC analog power/ground supply for pre-driver; SAVDD33 and SAVSSD are SMIC analog power/ground supply for post-driver.

Caution:

1). Notice that, it is important to emphasize that PANAxAPx cells are useful for analog IP macro that is designed by I/O device only.

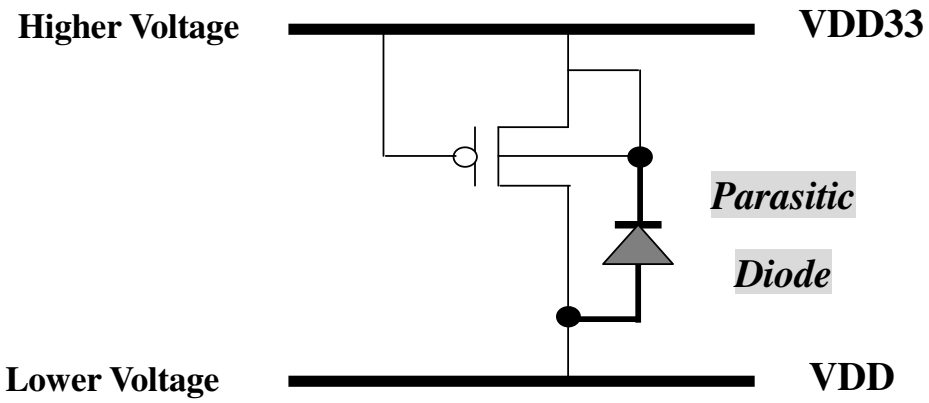
2). There is no resistor in analog I/O cells, for ESD consideration the user should add resistor in user's circuit.

3). In table 2 for PANA3AP IO cell: 5V tolerance means maximum signal voltage, **not power supply voltage** (such as USB VBus and so on), can be handled by the I/O is up to 5V; 3.3V tolerance means maximum signal voltage, **not power supply voltage,** can be handled by the I/O is up to 3.3V.

6. Power Up and Power Down Sequence

SMIC Standard I/O Library use different voltage supply for pre-driver and post driver. For full chip Electro Static Discharge (ESD) protection design, multiple voltages ESD clamping circuit has to be applied. These circuits will cause a parasitic diode in between core power rail (VDD) and I/O power rail (VDD33) as shown in Figure 7.

Figure 7. Parasitic Diode cause to exit a forward path among core and I/O power rail



A serious latch-up issue may occur, if lower voltage power rail is turn on earlier than the higher voltage without concern about it. Since parasitic diode provide a path for current to flowing through then that may activate latch-up. In order to avoid latch-up issue, one method is suggested to overcome it. This method is briefly discussed in next section.

6.1 Power Up

Method: Turn On Higher Voltage First

First turn on higher voltage power rail then lower voltage power rail. This obviously can avoid activating the parasitic diode. However, if the delay time between turn on higher voltage and lower power rail is large, some reliability issues may arise. Firstly, the un-power lower voltage rail will cause post-driver circuit in unknown state. This may cause a short circuit current in post-driver then circuit performance degradation. Secondly, power bus confliction may generate while only higher voltage power rail is turned on.

6.2 Power Down Sequence

The degradation factors such as latch-up and reliability issues are not important in power down sequence. Power down sequence mainly concern about the minimum degree of the power consumption regarding the transient current. Its can be approached by applied the power down sequence in the reversed sequence style as power up does. Please refer the example below for more detail.

An Example:

If power up sequence is ***Turn On Higher Voltage First*** then ***the power down sequence is turn off lower voltage power rail then following by higher voltage rail***.

7. Electrostatic Discharge Consideration

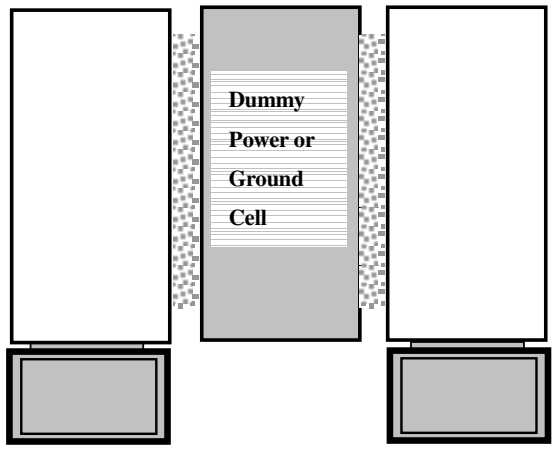
Electrostatic discharge (ESD) events can lead to failure of poorly protected circuits. For these important reasons a more methodical approach to ESD protection design is required. So fitting a proper ESD protection circuit among each power/ground cell for ESD protection is needed. These ESD issues are discussed in this Chapter.
SMIC Standard I/O Library has provided full chip ESD solution to cover all possible ESD attack conditions. It's required to pass JEDEC ESD standard of Human Body Model (HBM) and Machine Model (MM). The stress modes with respect to both power supply (VDD) and ground are include positive-to-ground (PS), negative-to-ground (NS), positive-to-VDD (PD) and negative-to-VDD (ND) modes for HBM and MM. Where, PS-mode is applied a positive discharge pulse to VSS pin relatively grounded, but the VDD pin and other pins are floating. NS-mode is applied a negative discharge pulse to VSS pin relatively grounded, but the VDD pin and other pins are floating. So as PD and ND-mode, by applied positive/negative discharge pulse to VDD pin relatively grounded, but the VSS pin and other pins are floating.

7.1 Dummy Power/Ground Cells

Although a proper ESD protection circuit among each power/ground cell has been fitted for the ESD protection. However, it is recommended to put dummy power/ground cells (PVDDx, PVSSx, PVDD1CE, PVDDxAPx and PVSSxAPx) instead of filler cells on the I/O pad ring as shown in Figure 8. Notice, this is applied only to the condition while there are extra spaces on the I/O pad ring. These dummy power/ground cells can provide a short recharge ESD path while filler cells can't. Thus, improve the ESD protection performance.

If the power pad PVDD1CE is included in I/O library, the user should notice the following points:
1). PVDD1CE is one digital Vdd power cell used in digital power domain, and it has not pad opening window.
2). It's preferred to supply at least one PVDD1CE within each digital power domain and each side of chip.
3). For good core ESD protection, it is strongly recommended to connect PVDD1CE's pin to chip digital core area using a wide metal layer.

Figure 8. Fit dummy power or ground cell instead of filler cell for better ESD protection



7.2 Power Cut Cells (PDIODEx/P1DIODEx)

In the mixed-mode application circuit the noises that generated by switches of digital circuit are undesirable to connect directly to the power/ground ports of analog circuit. The analog and digital power separation issue can be achieved by application with power cut cells (PDIODEx/**P1DIODEx**).

SMIC Standard I/O Library has provided power cut cell PDIODE and PDIODE8 to support the separate power design. **PDIODE and PDIODE8 can be used for same voltage level of VDD33 (digital) and SAVDD33 (analog), however, only PDIODE8 is used for the difference voltage level between digital and analog. Here it is strongly recommended to use PDIODE cell for the same voltage level between digital and analog power rails.**

PDIODE8S is another power cut cell, which used to connect the ground rails and disconnected power rails in both side of this cell. Cell PDIODE8S is used for different power and common ground circuit in low noise region.

P1DIODE is similar to PDIODE, but P1DIODE only includes two single diodes of opposite polarity connected in parallel. P1DIODE8 is similar to PDIODE8, but P1DIODE8 only includes two single diodes of opposite polarity connected in parallel. Therefore, P1DIODE/P1DIODE8 is weak to reduce digital power noise disturbance comparing with PDIODE/PDIODE8.

Disconnect the power rails between analog and digital can greatly reduce the digital power noise disturbance. However, this will decrease the ESD protection performance progressively. This important case can be solved by apply power cut cell. Power cut cell, which contain an appropriate number of diodes between the analog and digital power rail, is a good solution to filter out digital power noise and improve ESD protection. These features are due to the diode. By according to diode characteristic, diode can be turn-on only if the voltage drops across the diode exceeds its threshold voltage. This characteristic effectively block the digital power noise and also playing an effective cross-coupling clamp between analog and digital I/O cell by provide a discharge path through ESD device of the I/O to the power/ground rail of the adjacent I/O cell. Therefore, no excess current is couple into the core circuit when there is a high voltage stressed to the I/O cell. Thus improve ESD performance.

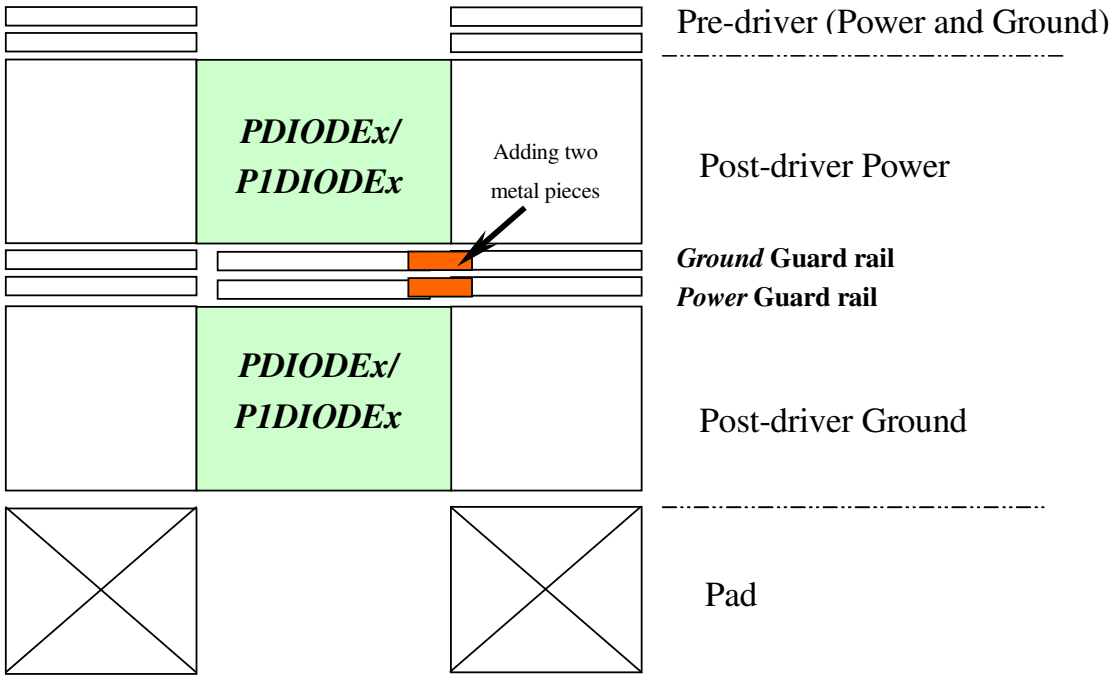


Figure 9. Layout of power cut cell among two I/O cell.

Figure 9 shows the layout of PDIODEx/P1DIODEx among two I/O cell. It should be noted that the guard bands within the PDIODEx/P1DIODEx are disconnected with the left and right sides of the cells boundary. Thus, the user should connect these gaps manually by adding two metal pieces connecting the guard rails of this cell and surrounding cell. However, notice that only ***ONE*** side of the guard rail must be connected to the neighboring guard rail (Refer Figure 9). ***The other side must be left disconnect*** to keep power across the power cut cells separate. As deciding which side to connect, practice the following rules and applied in the order of descending priority.

For the ***Power*** guard rail:

1. If there is differentiate between two sides, always connect to the side with the highest VDD voltage.
2. Always connect to the side, in which containing the most amounts of I/O cells.
3. Since Analog side is provides less noise, thus always connect with the Analog side.

For the ***Ground*** guard rail:

1. If there is differentiate between two sides, always connect to the side with the lowest VSS voltage.
2. Same as 2 above.
3. Same as 3 above.

Caution:

1) *PDIODEx/P1DIODEx* differs among applications; therefore, SPICE file must be manually modified before LVS check.

2) PDIODE8S cell can be used between digital power rails or between analog power rails. If PDIODE8S is placed between digital and analog power rails, error will occur when doing LVS check.

3) It is important to emphasize that for ESD concerns the maximum number of power domain should be equal and less four that divided by these powers cut cells in one chip. If four power domain is necessary, it's better to use at most four PDIODE/PDIODE8/P1DIODE/P1DIODE8 cells and at least PDIODE8S cell, moreover, place PDIODE8S in low noise region is necessary. Overmuch power domain or no power cut cell used in separate power domain will weak ESD performance and have risk of destroy whole circuit.

4) For PDIODE8S connect these gaps manually only by adding one metal piece to connect the power rails of this cell and surrounding cell is enough, because ground rail in the PDIODE8S cell will be automatically connected while joining with other I/O cells.

7.3 Tie high / tie low

In order to improve ESD performance, the user must use one tie-high/tie-low cell to tie IO cell pin to power/ground instead of directly to tie the pin to power/ground. Safe connections can be provided between pin and power/ground by using tie-high/tie-low cells of user's standard cell library.

8. I/O Power/Ground connection Cell

In *SMIC Standard I/O Library* there are some I/O power/ground bus connection cells. These cells neither have pad for external connection nor port for internal core circuit connection. They have no function devices as well. However, these cells are for power/ground bus rail connection. They are called I/O power/ground cell, filler and corner cell.

8.1 I/O Power/Ground Cell

The functions of the I/O power/ground cells had been discussed in Chapter 7. Please refer to Chapter 7.1 for more detail.

8.2 Filler Cell And Corner Cell

Filler cell is a power ground rail to connect up various types of I/O cells. There are two kinds of filler cells in *SMIC Standard I/O Library* design kit: **digital filler cell** (PFILLx) and **analog filler cell** (PFILLxA). In which digital filler cell has VDD, VSS, VSSD, VDD33, FP and FPB power ground rails however, analog filler cell has various types of power ground rail name. Its all depend on the I/O cell's application. The **corner cell** (PCORNER) usage is for power/ground bus edge connection.

The following regulations ought to be applied when choosing which filler cell to use for connect up I/O cells. In the cases of:

a) In between two digital I/O cells or power cut cell with digital IO cell, digital filler cell PFILLx is applied.

b) Use analog filler cell PFILLxA in between two analog I/O cells or power cut cell with analog IO cell.

c) The width of filler cell used to filling between I/O cells should be from big to small. For example, Using PFILL10/PFILL10A and PFILL2/PFILL2A are better than using six PFILL2/PFILL2A to filling.

9. Max Currents For Power I/O Pads

Electromigration (EM) can cause considerable material transport in metals. It occurs because of the enhanced and directional mobility of atoms caused by the direct influence of the electric field and the collision of electrons with atoms. In which will leads to a slow displacement of the metal. This eventually, result to a discontinuity in the current-carrying lines. Therefore, EM limits the current density flow through the metals.

SMIC Standard I/O Library has provided maximum allowable current (mA) information as shown in Appendix A of specific SMIC I/O Library Data Book. This maximum allowable current could be a guide to avoid EM in the conducting metals.

In addition, EM failure can be greatly reduced by increase the number of via and metal width at the connecting port of power/ground cells.

10. Oscillator I/O Application Note

In this Chapter oscillator I/O cells usage and application are presented. The circuit for fundamental mode oscillation also provided for reference.

There are several oscillator I/O cells in *SMIC Standard I/O Library* and they can be divided out into three groups (Refer to Table 3). These three groups oscillator I/O cells are designed to oscillate for crystal samples in the frequency range of 2MHz to 30MHz in fundamental mode. The correct way to select oscillator I/O cell is critically corresponding to the crystal specifications.

Table 3. Three groups of oscillator I/O cells

Oscillator I/O Group	Cell Name
I	PX1 / PXWE1
II	PX2 / PXWE2
III	PX3 / PXWE3

PXWEx is distinguished from PXx by the presence of an enable signal. The increasing number of suffix indicates the increasing drive strength and also the small signal gain (g_m) of the cells. Notice that in *SP015LV, SP015LVN* and *SP015LVW* libraries, PXWERx and PXWRx crystal oscillators with feedback resistor are available. In which feedback resistor is internal connected with the oscillator I/O cell. Where x can be as 1, 2 and 3. PXWERx is crystal oscillator with high enable and feedback resistor and PXWRx is crystal oscillator with feedback resistor.

To turn on the oscillator, the oscillating circuit must provide the negative resistance (-Re) at least five times the equivalent series resistance (ESR) of the crystal sample. For larger -Re value, faster turn on the crystal. Higher g_m provides larger -Re therefore cans start-up the crystal with higher ESR for the same load capacitance (CL). However, it's required higher power consumption.

There are two key parameters to turn on oscillator. Which are CL and the maximum ESR at the target frequency. By reducing the CL, the -Re can be increased thus; shorter turn on time can be achieved. However, if CL is too small, the deviation from the target frequency will increase because of the capacitance variation. So, a trade-off relationship between short turn on time and small frequency deviation in deciding CL value. The smaller ESR of the crystal sample will reduce turn on time but the price is higher. As the CL and ESR values are defined and specified, Table 4 can be a guide to select a correct oscillator I/O cell.

Table 4. Selection guide for oscillator I/O cell under typical conditions

Target Freq (Hz)	2M-3M	3M-6M	6M-10M	10M-20M	20M-30M
CL (pf)	25	20	16	12	8
Maximum ESR (ohm)	1K	400	100	80	40
Oscillator I/O Group	I	I	I	II	III

For other Target Frequencies range that are not in Table 4 above, for examples 32K Herz and the other etc, please contact SMIC Design Service for more information.

10.1 Oscillating Circuits

Figure 10. Oscillating circuit for fundamental mode

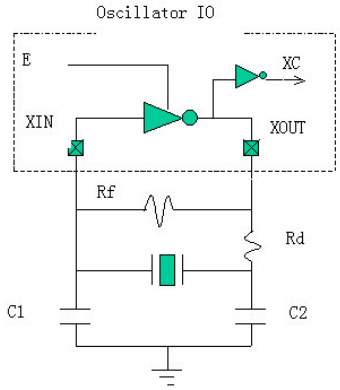


Figure 10 shows the oscillating circuit is connected with the oscillator I/O cell. Components feedback resistor (Rf), damping resistor (Rd), C1 and C2 are used to adjust the turn on time, keep stability and accurate of the oscillator.

R*f* is used to bias the inverter in the high gain region. It cannot be too low or the loop may not oscillate. For mega Hertz range applications, Rf of 1Mohm is applied.

Rd is used to increase stability, low power consumption, suppress the gain in high frequency region and also reduce -Rd of the oscillator. Thus, proper Rd cannot be too large to cease the loop oscillating.

C1 and C2 are deciding regard to the crystal or resonator CL specification. In the steady state of oscillating, CL is defined as (C1*C2)/(C1+C2). Actually, the I/O ports, bond pad, and package pin all contribute the parasitic capacitance to C1 and C2. Thus, CL can be rewrite to (C1'*C2')/(C1'+C2'), where C1'=(C1+$C_{in,stray}$) and C2'=(C2+$C_{out,stray}$). In this case, the required C1 and C2 will be reduced.

Notice, this oscillating circuit is for parallel resonate but not series resonate. Because C1, C2, Rd and Rf are varying with the crystal specifications and the selected oscillator I/O cell; therefore there is no single magic number of all the applications.
In addition, if user would like to use oscillator instead of crystal to oscillator pad, XIN pins should be connect to oscillator input.

Note: In some library, such as SMIC I/O library SP90ND3, the crystal oscillator I/O cells have embedded internal resistor, so the user need not add feedback resistor (Rf) as above description. Refer to specific SMIC I/O library data book whether crystal oscillator I/O cells with internal resistor or not.

10.2 Continuity test method

In order to avoid the floating problem of the gate, the following test method is necessary: when testing the XIN, the XOUT pin is connected to ground; when testing the XOUT, the XIN pin is connected to ground.

10.3 Noise immunity for Oscillator I/O

In the case to reduce the noise disturbance, please sandwich Oscillator I/O cell in between Power and/or Ground cell.
Please note that, Oscillator output signal is feed to one of the input signal rail named Reference Clock Signal (RCK) of the PLL (XIN). This RCK signal rail should be kept as quiet as possible. Ideally the RCK should be routed with no other active signals on either adjacent levels or within 5 microns of it on the same metal level. If this cannot make it in the layout, the RCK should be routed with the PLL's VSS shielding it from any other signals. Also, if the RCK is to be used for other purpose in the chip, it should be buffered near its source and separately fed to the non-PLL locations from this buffer. The source of the RCK should be as close to the PLL as possible.

11. I/O Cell With IP macros

When SMIC I/O cells are used with IP macros, such as ADC (analog-to-digital converter), DAC (digital-to-analog converter), High Speed IP, LVDS (Low Voltage Differential Signaling), PLL (Phase Lock Loop) and so on, SMIC strongly recommend users to connect digital power and ground pins in IP macros to chip digital core area.

The following section provided some useful information regarding place and route of Phase Lock Loop (PLL) ***(SMIC PLL IP Only)*** with SMIC Standard I/O cell. Figure 11 is a placement and routing example of PLL. In this example, PDIODE8 power cut cells are inserted between power pads of PLL and other digital pads to isolate digital power noise. Double bonding is used at the power pad (AVDD, AVSS) in order to reduce the wire inductance. If possible, it is also suggested to minimize the bonding wire length of the power/ground pads.

Some practical information about placement and routing of PLL with I/O cell (Refer to Figure 11):

1. Place PLL at corner of die and PLL's power and ground pins close to the analog power I/O pads. The routing paths should keep as short as possible and far away from any other high drive or switching digital I/O pads.
   User also can place PLL on the edge rather than the corner of die, but please do remember allowing 100μm distances from other diffusion or well.

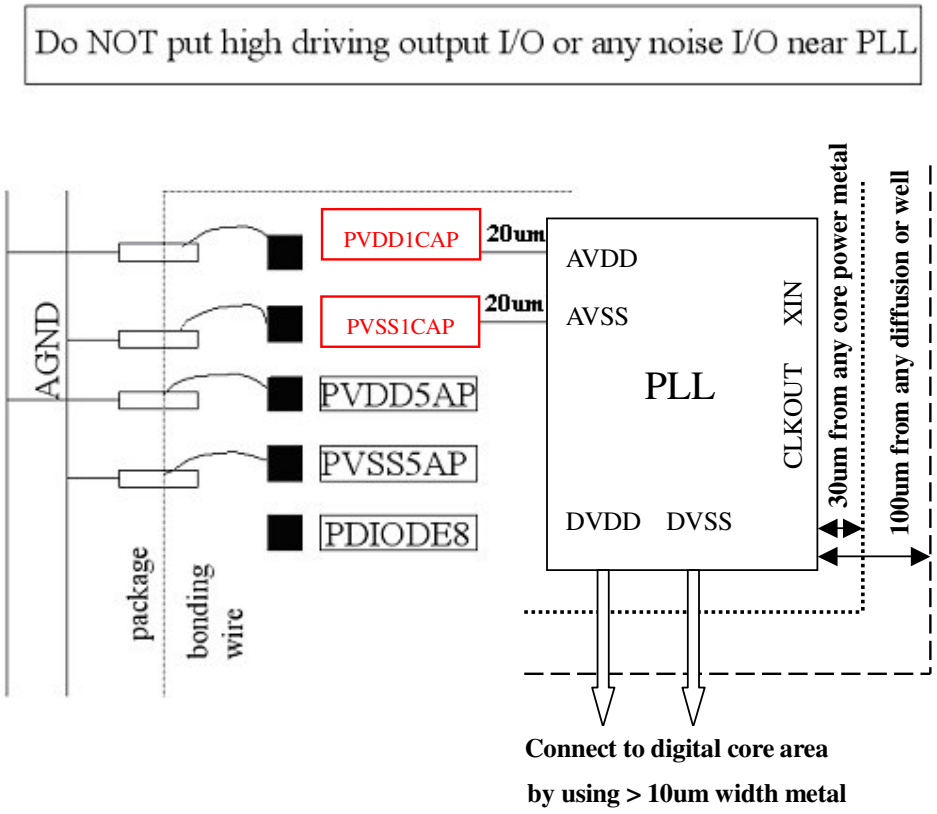
2. Avoid placement all noisy internal circuits and fast output drivers close by the PLL cell. Generally, higher frequency signals and high-power level units generate more noise than lower frequency signals and low-power level units.

3. PLL unit can't cross over by any core-logic power rail. Create dead space between the PLL internal circuit and all other internal circuit. Physical space is a good way to reduce noise transmission through the chip substrate. It is recommended that a minimum 30um space between PLL and digital core power rings and minimum 100um space between PLL and any other diffusion or well of digital core.

4. Avoid core-logic power lines and signal lines crossing over any power lines of PLL.

5. Connect PLL's digital power/ground pins (such as DVDD, DVSS) to chip digital core area. And the connection metal width should be wider than 10um.

Figure 11.Placement and Routing Consideration of PLL.



If PLL is using core power (e.g. 1.8V) only, PVDD5AP/PVSS5AP are still requiring connecting respectively for pre/post-driver. PVDD5AP can connect with either 1.8V or 3.3V power bus.

Use PVDD3CAP/PVSS3CAP power/ground cell set, if both core and pre/post driver are required (refer to Figure 11a). Figure 11b shown another type of power/ground cell set for placement and routing consideration of PLL.

User can refer to Chapter 5, Figure 6, 6a and 6b for more details in regard to power/ground rail connection and various power separation schemes issues.

Figure 11a. Placement and Routing Consideration of PLL

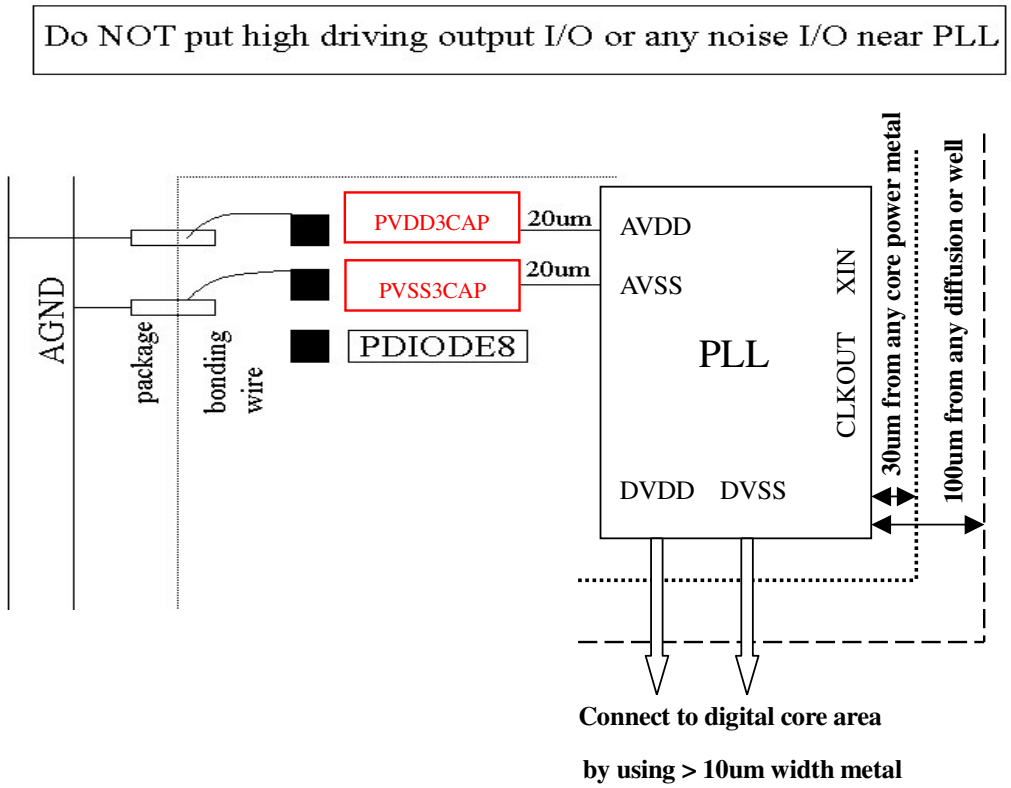
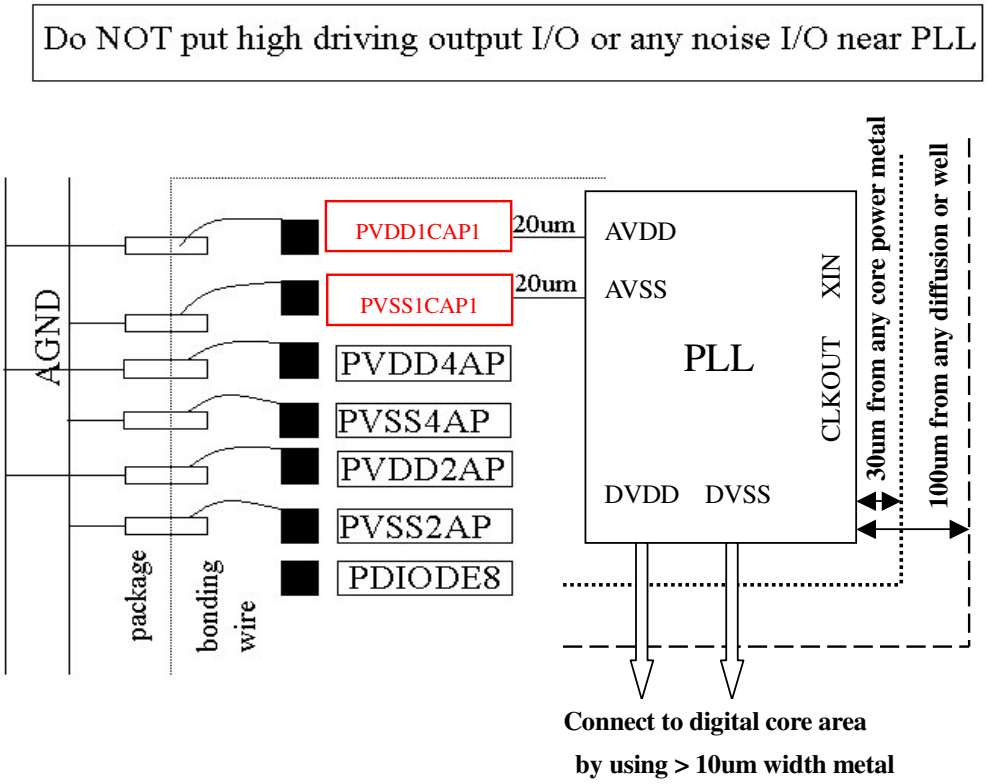


Figure 11b. Placement and Routing Consideration of PLL



12. SMIC Standard IO LVS Verification

There are floating n-channel gate without ports name in the I/O GDS layout. However, in the schematic spice netlist ports are named 'FP' and 'FPB' for LVS checking.
FP is stand for 'From Power Pad' and FP pin is for global signal. FP rail will be automatically connected while joining with other digital I/O cells. Under normal condition, FP is activated by PVDD2 to 'HIGH' voltage level.
FPB pin is for global signal. Under normal condition, FPB is activated by PVDD2 to 'Low' voltage level (0V). FPB rail will be automatically connected while joining with other digital I/O cells.
However, in some SMIC I/O library, FP and FPB are activated by PVDD1. Therefore, refer to specific SMIC I/O data book for more detail.
For Example, in SMIC I/O library SP018, FP is activated by PVDD2 to 3.3V. But in SMIC I/O library SP018EED5, FP is activated by PVDD1 to 'HIGH' (1.8V).

There will be no LVS problem encounter if only check one individual I/O cell at a time with both Hercules and Dracula runset. However, when many I/O cells are checking together, Hercules will report 'short' errors. These errors can be successfully solved by activate 'FP' and 'FPB' as two of schematic-global signals. Since, pin 'FP' and 'FPB' are global signals like VDD, VSS and etc. Thus, they must be set as global signals in the Hercules runset.

For Dracula LVS: nothing has to change in runset option.

For Hercules LVS: Add **FP and FPB** in the group of schematic global in option section of the runset file as shown in the settings below:

options {
layout_power = {VDD, VDD33……}
layout_ground = {VSS, VSSD……}
layout_global = {VDD, VSS, VDD33, VSSD……}
schematic_power = {VDD, VDD33……}
schematic_ground = {VSSD, VSS……}
schematic_global = {VDD, VSS, VSSD, VDD33, ……, **FP , FPB***}*
}

13. I/O Library Tape-out Layer Integration

I/O library tape-out layers such as GDSII layer and mask layer are important process steps to produce I/O mask for the design tape-out. If not correctly prepare, the tape-out date will be delayed. SMIC acknowledge that customer/user's time is very precious. To achieve quick tape-out cycle time and 'first-tape-out-success', tighten up I/O library tape-out layer integration with SMIC process is required.
To correctly tape-out with SMIC Standard I/O Library, user ought to check the following notes carefully before tape-out.

1. GDSII Layer Mapping Number and Mask Code

   Different libraries vendors will provide and define a different GDSII mapping number and mask code. Wrong GDSII mapping number and mask code will cause serious problems to make accurate mask layer for tape-out. Users can check the detail of SMIC GDSII layer mapping number, Mask code, Layer name and et cetera in the *Table-1: GDSII Layer Mapping of Logical / SRAM / Mask Rom / Mix-Mode* document.

2. ESD Mask

   ESD implant layer is not requiring for 0.35um process in SMIC I/O standard library since SMIC I/Os have very good ESD limitations for the process. But the layer is essential to 0.25um process and below in SMIC I/O standard library. SMIC ESD implant mask code is 110 and GDSII number is 41 (Refer to *Table-1: GDSII Layer Mapping of Logical / SRAM / Mask Rom / Mix-Mode*). Please notices that, this layer requires using the logical operation formula to generate the mask (ESD).

3. Lightly Doped Drain (LDD) Mask

   SMIC standard I/O cell library have no LDD mask layer drawn in the layout. This layer needs to do logical operation to generate the LDD mask layer.
   LDD structure is used to reduce the peak lateral electric field near the drain junction edge, thus reduce the hot carrier effects and improve the reliability of I/O.

4. Active Area (AA) Mask

SMIC used NDIFF = AA + SN and PDIFF = AA + SP to define P/N AA region in GDSII. Where the sign '+' is equal to the logical 'OR' function. The SN and SP are N+ implant and P+ implant respectively. However, there are many ways to define AA region in GDSII. For examples (1)--- DIFF; (2)--- (NDIFF + PDIFF) and (3)--- (NDIFF + PDIFF + AA). Users should notice that different libraries might use their own preference style to define AA region. Therefore, it is recommended that all AA layout styles (DIFF or PDIFF or NDIFF) have to cover the AA mask tooling, while taping-out the AA mask layer.

Appendix A: ESD Check List

To ensure proper ESD performance for each chip, users should confirm that the following guidelines are followed. The page may be printed to help verify that the design is consistent with all ESD item descriptions.

No.	ESD Check Items	Result
1	Please refer to the latest version of I/O Application Note regarding power/ground pad application.	
2	The ratio of I/O cell number to power/ground cell number should be consistent with SSO (Simultaneous Switching Output noise) rules.	
3	The post-driver ground bus of the I/O cells should form an unbroken ring.	
4	In one chip, the number of power domains separated by power-cut cells PDIODE, PDIODE8, P1DIODE and P1DIODE8 must be less than or equal to four. (Refer to I/O application note Chapter 7.2)	
5	When ports connected to pads are higher than core voltage, PVDD1AP/PVDD1AP1/PVDD3AP should be used. (Refer to I/O application note Chapter 5)	
6	When ports connected to pads are equal to or lower than core voltage, PVDD1CAP/PVDD1CAP1/PVDD3CAP should be used. (Refer to I/O application note Chapter 5)	
7	Use a tie-high/tie-low cell to connect an I/O cell pin to power/ground rather than connecting directly. (Refer to I/O application note Chapter 7.3)	
8	Power and signal lines of core-logic must not cross over power lines of IP macros.	
9	ESD protection devices should be added to metal interconnects longer than 500um at the digital/analog interface.	
10	The core power generated by the voltage regulator should be connected to the core protection device of PVDD1, PVDD1CAP or PVDD3CAP.	
11	Connect digital power/ground pins of every IP macros (e.g. DVDD, DVSS in a PLL) to the chip's digital core area. The width of metal interconnects should be wider than 10um.	
12	Add dummy power/ground cells to the I/O pad ring instead of filler cells. (Refer to I/O application note Chapter 7.1)	
13	For each side of the chip, the core must be supplied with at least two pairs of respective power/ground cells (except of PVDD1CE) for each digital or analog power domain, regardless of whether the core is already supplied by a voltage regulator.	
14	If PVDD1CE is included in I/O library, for each side of the chip, it's preferable to supply at least one PVDD1CE within each digital power domain. The	

	PVDD1CE pin should be connected to the chip digital core area using a wide metal layer.	
15	Users must add embedded ESD resistors when using secondary ESD devices.	
16	When non-SMIC analog macros are used, users must add ESD protection devices at the digital/analog interface.	
17	Any modification to SMIC I/O data is prohibited. In case modification is required, user must report to SMIC for verification.	