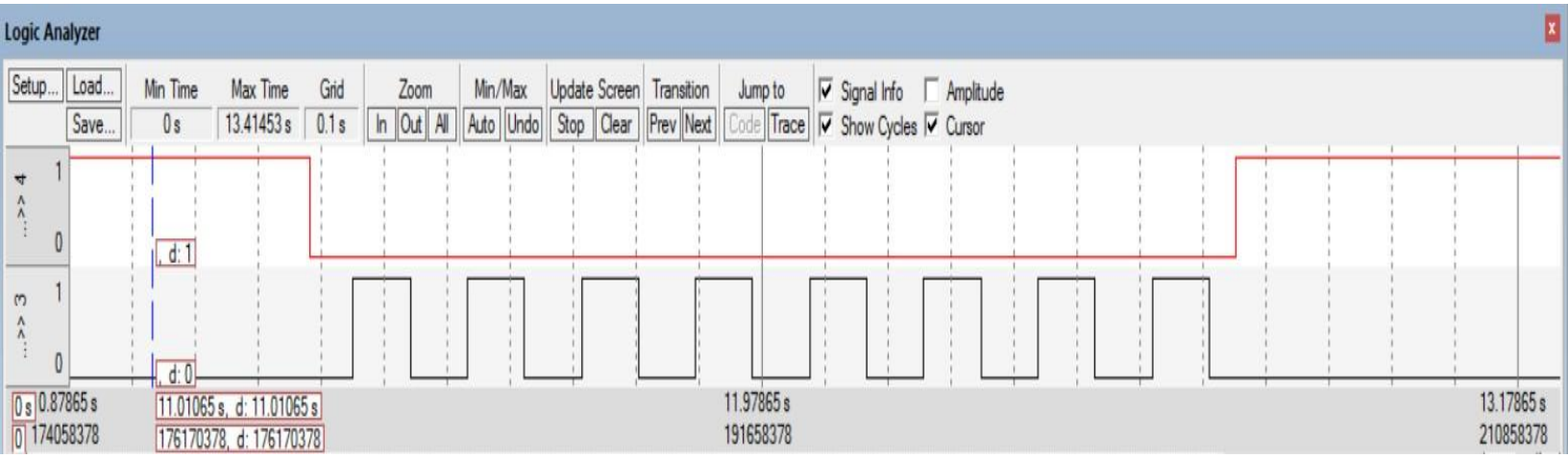
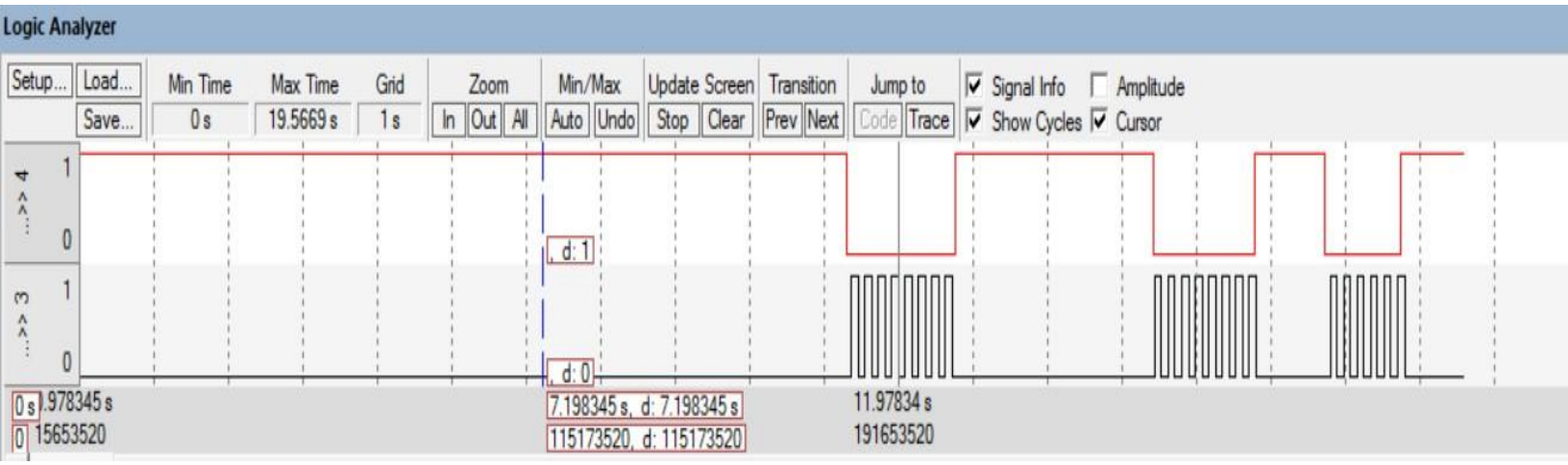
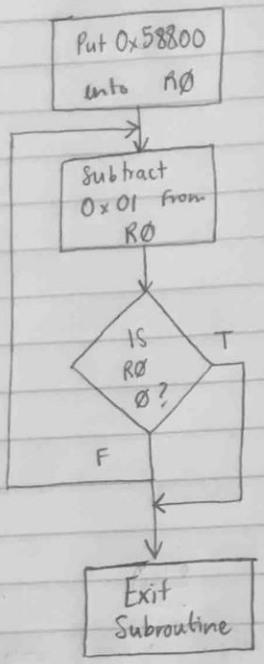

Logic Analyzer
Setup...
Load...
Save...
Min Time
0 s
Max Time
13.41453 s
Grid
0.1 s
Zoom
In
Out
All
Min/Max
Auto
Undo
Update Screen
Stop
Clear
Transition
Prev
Next
Jump to
Code
Trace
Signal Info
Amplitude
Show Cycles
Cursor
4
3
1
0
, d: 1
, d: 0
0 s
0.87865 s
0
174058378
11.01065 s, d: 11.01065 s
176170378, d: 176170378
11.97865 s
191658378
13.17865 s
210858378


Logic Analyzer
Setup...
Load...
Save...
Min Time
0 s
Max Time
19.5669 s
Grid
1 s
Zoom
In
Out
All
Min/Max
Auto
Undo
Update Screen
Stop
Clear
Transition
Prev
Next
Jump to
Code
Trace
Signal Info
Amplitude
Show Cycles
Cursor
4
3
1
0
, d: 1
, d: 0
0 s
.978345 s
0
15653520
7.198345 s, d: 7.198345 s
115173520, d: 115173520
11.97834 s
191653520

Lab 2

Part A (Delay 80-120ms)



Part A Psuedocode

```
        R0 ← 0x58800
wait    R0 ← R0 - 1
        BNE wait
        Bx  LR
```

```
;****************** main.s ***************
; Program written by: ***Your Names**update this***
; Date Created: 1/22/2016
; Last Modified: 1/22/2016
; Section ***Tuesday 1-2***update this***
; Instructor: ***Ramesh Yerraballi**update this***
; Lab number: 2
; Brief description of the program
; The overall objective of this system an interactive alarm
; Hardware connections
;  PF4 is switch input  (1 means SW1 is not pressed, 0 means SW1 is pressed)
;  PF3 is LED output (1 activates green LED)
; The specific operation of this system
;    1) Make PF3 an output and make PF4 an input (enable PUR for PF4).
;    2) The system starts with the LED OFF (make PF3 =0).
;    3) Delay for about 100 ms
;    4) If the switch is pressed (PF4 is 0), then toggle the LED once, else turn the LED OFF.
;    5) Repeat steps 3 and 4 over and over

GPIO_PORTF_DATA_R       EQU   0x400253FC
GPIO_PORTF_DIR_R        EQU   0x40025400
GPIO_PORTF_AFSEL_R      EQU   0x40025420
GPIO_PORTF_PUR_R        EQU   0x40025510
GPIO_PORTF_DEN_R        EQU   0x4002551C
GPIO_PORTF_AMSEL_R      EQU   0x40025528
GPIO_PORTF_PCTL_R       EQU   0x4002552C
SYSCTL_RCGCGPIO_R       EQU   0x400FE608
PF4                     EQU   0x40025040
PF3                     EQU   0x40025020

       AREA    |.text|, CODE, READONLY, ALIGN=2
       THUMB
       EXPORT  Start
Start  LDR R0,= SYSCTL_RCGCGPIO_R
       LDR R1,[R0]
       ORR R1,#0x20
       STR R1,[R0]

       NOP
       NOP

       LDR R0,= GPIO_PORTF_DIR_R
       LDR R1,[R0]
       BIC R1,#0x10
       ORR R1,#0x08
       STR R1,[R0]

       LDR R0,= GPIO_PORTF_AFSEL_R
       LDR R1,[R0]
       BIC R1,#0x18
       STR R1,[R0]

       LDR R0,= GPIO_PORTF_DEN_R
       LDR R1,[R0]
       ORR R1,#0x18
       STR R1,[R0]

       LDR R0,= GPIO_PORTF_PUR_R
       LDR R1,[R0]
       ORR R1,#0x10
       STR R1,[R0]

       LDR R0,= PF3
       LDR R1,[R0]
       MOV R1,#0x0
       STR R1,[R0]


loop   BL Delay


       LDR  R0,= PF4
```

```
 73          LDR  R2,= PF3
 74
 75          LDR  R1,[R0]
 76          CMP  R1,#0
 77          BEQ  Toggle
 78          BNE  Clear
 79
 80
 81    Toggle LDR  R1,[R2]
 82          EOR  R1, R1, #0xFF
 83          STR  R1,[R2]
 84          B    loop
 85
 86    Clear  LDR  R1,[R2]
 87          AND  R1, R1, #0x0
 88          STR  R1,[R2]
 89
 90
 91          B    loop
 92
 93    Delay  MOV  R8, #0x58800
 94    wait   SUBS R8, R8, #0x01
 95          BNE  wait
 96          BX   LR
 97
 98          ALIGN      ; make sure the end of this section is aligned
 99          END        ; end of file
100
```

MC Simulated Time	Real Time
3.562 sec	10 sec