

How to build an FPGA design for Aldec TySOM boards using board definition in Xilinx Vivado

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3 Introduction

TySOM is a family of development boards for embedded applications that features Xilinx® Zynq™ all programmable module combining FPGA with ARM® Cortex processor. Plethora of included peripherals makes these boards useful in various embedded applications like Automotive, IoT, Industrial automation or embedded HPC.

More information and parameters about the boards are provided on Aldec website https://www.aldec.com/en/products/emulation/tysom_boards.

One way of preparing projects for the TySOM board is using the Xilinx Vivado tool which enables to create, synthesize, perform timing analysis and implement systems for FPGA platforms. Using Vivado board definitions that have been added to a board repository allows to faster creating systems. After selecting a specific board, the project is configured with the predefined interface for that board and the Vivado design tools provide designer assistance to IP customization and creating IP integrator designs.

Using Aldec TySOM boards in Vivado tool is quite straightforward, because provided board definitions contain customized configurations of components available on the TySOM board. They describe the different operating modes supported by those components, list the signal interfaces implemented by those components, suggest the preferred IP to implement those interfaces in a design project and maps the logical ports of the interface definition to the physical ports and components pins of the Xilinx device.

This document will demonstrate how to build a Vivado design using TySOM Vivado board definition provided by Aldec. In case of any additional questions visit Aldec website www.aldec.com or create a support case in a customer-only portal https://www.aldec.com/en/support/customer_portal/cases.

This flow requires using TySOM Vivado board definition from Aldec [GitHub](#) so a TySOM user does not have to build a Vivado project from the scratch.

4 Requirements

Hardware

- Aldec TySOM board:
 - [TySOM-3A-ZU19EG](#)
 - [TySOM-3-ZU7EV](#)
 - [TySOM-2-7Z100](#)
 - [TySOM-2-7Z045](#)
 - [TySOM-2A-7Z030](#)
 - [TySOM-1-7Z030](#)
 - [TySOM-1A-7Z010](#)
- Aldec FMC daughter card:
 - [FMC-ADAS](#)

Software

- Xilinx Vivado tool 2018.2 or newer

5 Available TySOM board definitions

All board definitions for Aldec TySOM boards are freely available on Aldec [GitHub](#). Therefore, a user does not have to prepare all necessary files for TySOM board to use the board with the Vivado tool. All of them are provided and are ready to use with Vivado tool.

Every board definition includes the following files:

1. board.xml
2. preset.xml
3. part0_pins.xml
4. Board image
5. preset.tcl

According to the selected TySOM board, the user need to choose one of the available definitions:

1. **TySOM-3A-ZU19EG**
2. **TySOM-3-ZU7EV**
3. **TySOM-2-7Z100**
4. **TySOM-2-7Z045**
5. **TySOM-2A-7Z030**
6. **TySOM-1-7Z030**
7. **TySOM-1A-7Z010**

Also FMC daughter cards are available:

1. **FMC-ADAS**

6 How to add board definitions to Vivado

Adding custom board definition files to Vivado can be done in two ways:

1. By special initial file for Vivado.

Create *Vivado_init.tcl* file in a local user folder:

- for Windows 7 - %APPDATA%/Xilinx/Vivado/Vivado_init.tcl
- for Linux - \$HOME/.Xilinx/Vivado/Vivado_init.tcl

This file should contain a command like that:

```
set_param board.repoPaths [list <path1> <path2> <path3>]
```

Where *<pathx>* is the path to a directory containing TySOM or FMC board definition.

2. By copying files into Vivado installation folder.

Is it also possible to copy all board files to Vivado installation folder. The path to this folder in Vivado is `<VIVADO_PATH>/data/boards/board_files`.

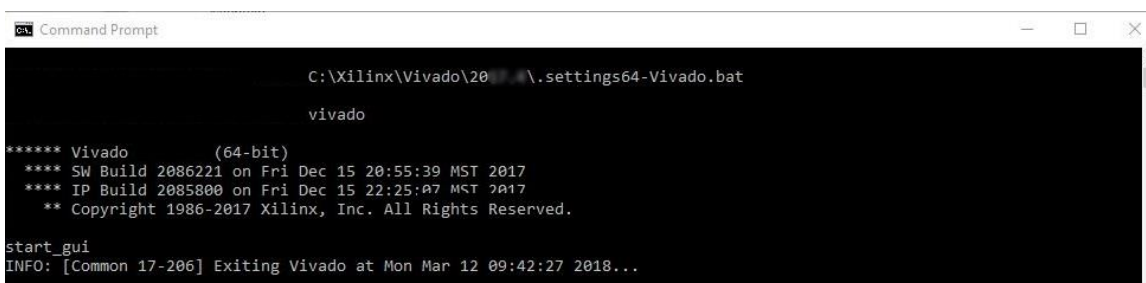
7 How to use TySOM board definition in Vivado

This chapter describes step by step how to create a Vivado project for the selected TySOM board using the TySOM Vivado board definition.

1. Create a working directory and start the Vivado from that directory.

- **for Windows:**

After creating the directory, open the Windows command line and run the `<PATH_TO_VIVADO>/settings64-Vivado.bat`. Then, run Vivado from the same path by typing `vivado` in the command line and pressing Enter.



```
Command Prompt

C:\Xilinx\Vivado\2017.3>.settings64-Vivado.bat

vivado

***** Vivado (64-bit)
***** SW Build 2086221 on Fri Dec 15 20:55:39 MST 2017
***** IP Build 2085800 on Fri Dec 15 22:25:07 MST 2017
***** Copyright 1986-2017 Xilinx, Inc. All Rights Reserved.

start_gui
INFO: [Common 17-206] Exiting Vivado at Mon Mar 12 09:42:27 2018...
```

Figure 1: How to start Vivado on Windows.

- **for Linux:**

Create a working directory and “cd” to that folder. Next source environment settings from Vivado tool by command `source <PATH_TO_VIVADO>/settings64.sh` and start Vivado tool by calling `vivado`.

2. Create a Vivado project.

- Click **Create Project**.

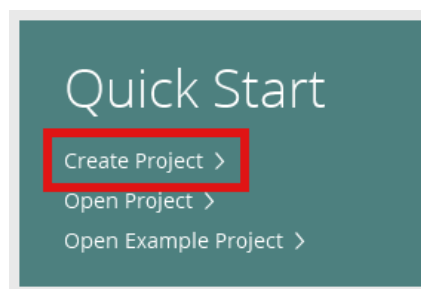


Figure 2: Create project in Vivado.

- Click **Next**.
- Provide a project name and choose previously created directory as project location (it is just set as default). Click **Next**.

- Select **RTL Project** and click **Next**.

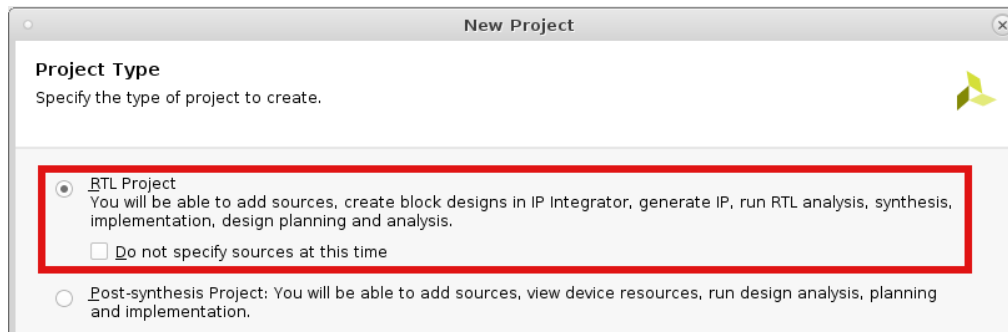


Figure 3: Select Vivado project type.

- Two times click **Next**.
- Select a target board. Boards added to Vivado board repository in step 1 should be visible here.

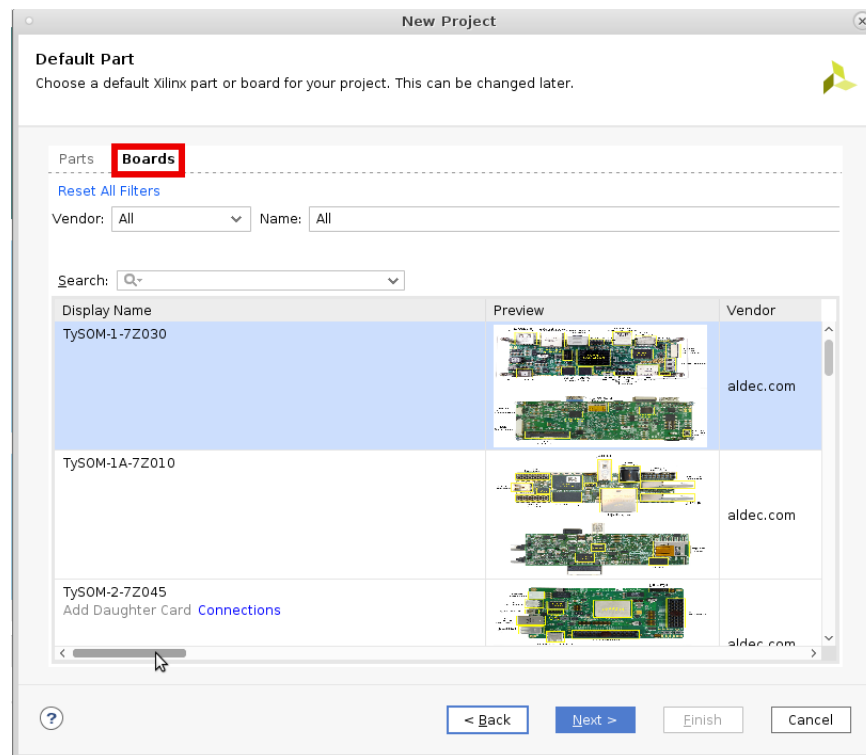


Figure 4: Select a target board.

- Some of TySOM boards have FMC connectors. Board connections can be added by selecting a FMC daughter card as shown in Figure 5 and Figure 6.

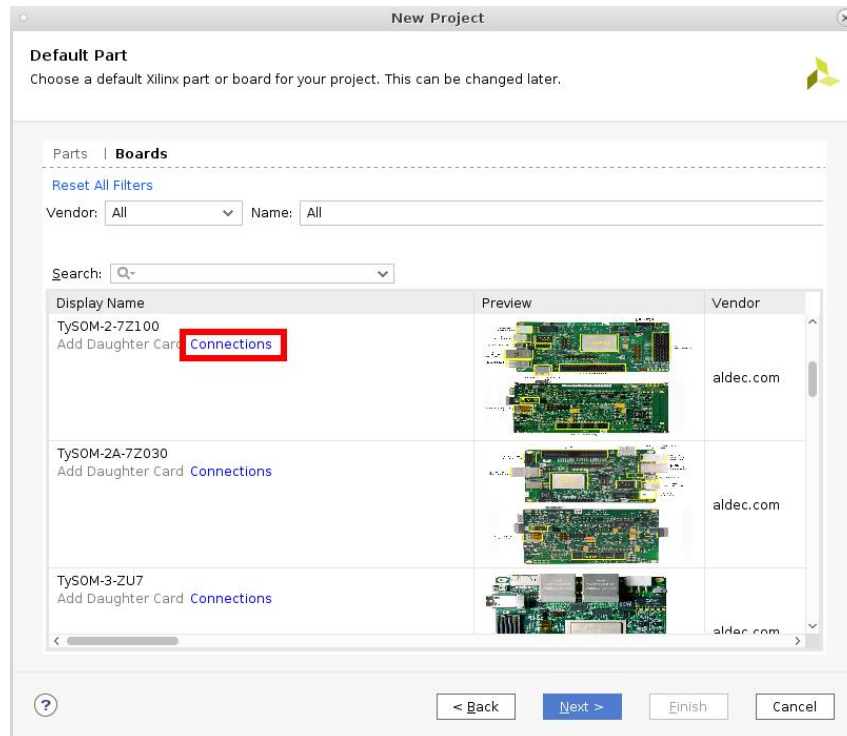


Figure 5: Add a daughter card connections.

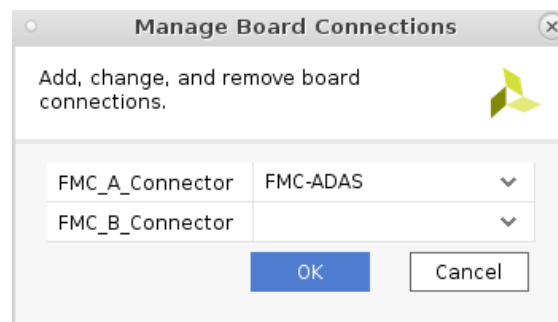


Figure 6: Select a daughter card.

- Then click **Next**.
 - Click **Finish**.
3. Add repository with custom IPs and interfaces.
 - Unzip a provided *ip_repo.zip* file for the selected TySOM board definition.
 - Select **Tools** → **Settings**.
 - Go to **Project Settings** → **IP** → **Repository**.
 - Add a file path to directory where the *ip_repo.zip* file was unpacked.
 - Click **OK**.

4. Create a Block Design by clicking **Create Block Design** from **Flow Navigator**.

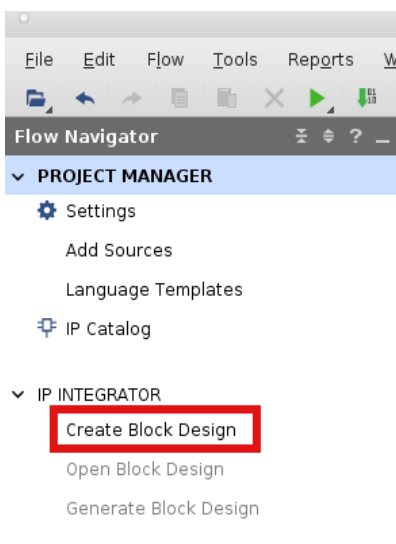


Figure 7: Create a Block Design.

5. Add customized board components to the design canvas. The components available for selected board are listed in the window **Board**, as shown in the Figure 8.

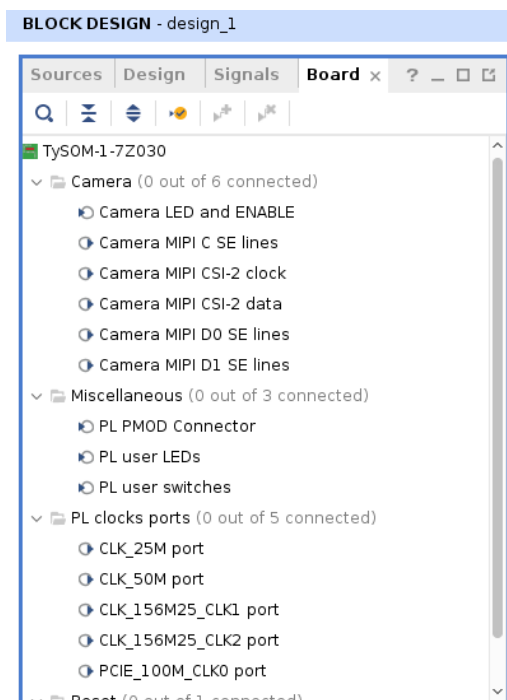


Figure 8: Window with board components.

6. You can add own IP cores if it is needed.
7. To complete connections you can use Designer Assistance by clicking **Run Block Automation** and

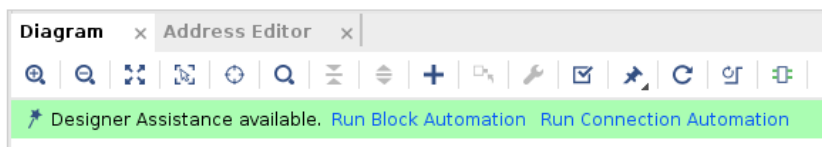
Run Connection Automation.

Figure 9: Designer Assistance.

8. The Zynq can be configured with default settings from the Vivado board definition.

- Click **Run Block Automation**.
- Select **zynq_ultra_ps_e_0** and **Apply Board Preset**, as shown in the Figure 10.
- Click **OK**.

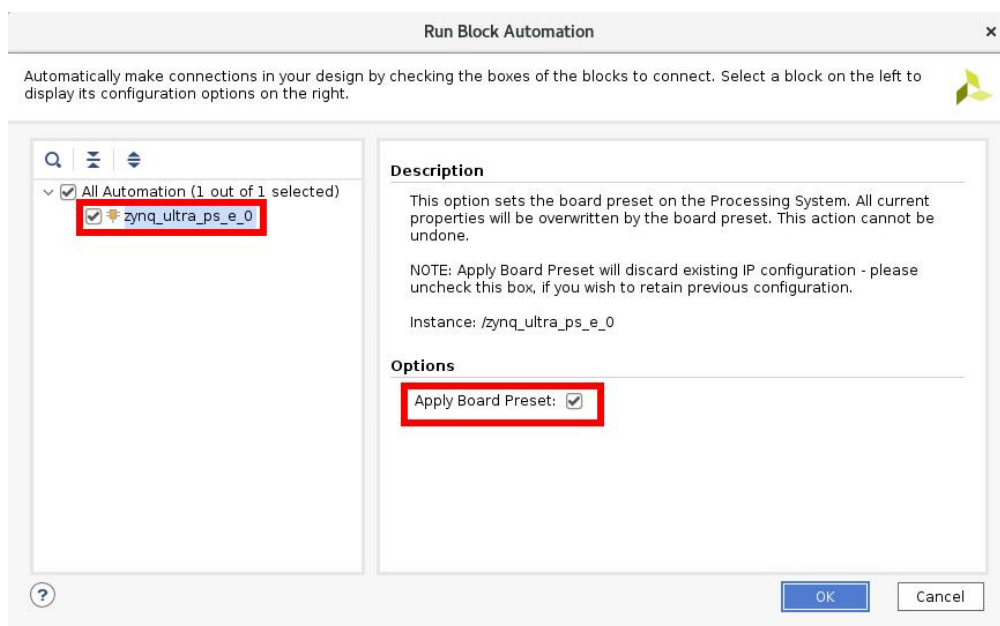


Figure 10: Applying Zynq preset by running block automation.

Another way to configure the Zynq is by using tcl script from the Vivado board definition.

- Double click on the Zynq block.
- Click **Presets** and next **Apply Configuration....**

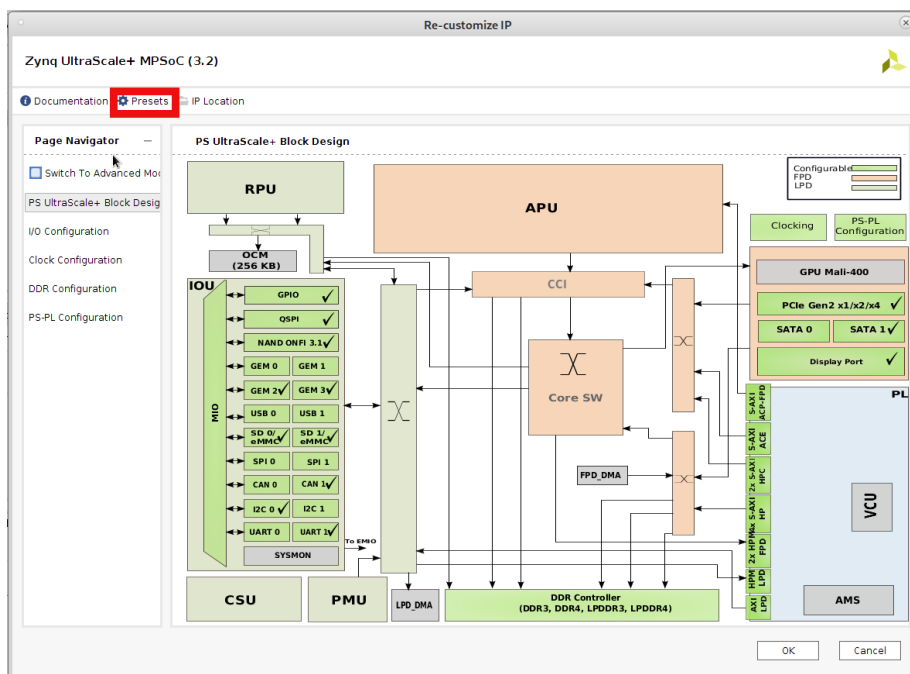


Figure 11: Applying Zynq preset by using tcl script.

- Select the tcl script from Vivado board files and click **OK**.
9. Then you can run implementation and generate a bitstream for the design.

About Aldec, Inc.

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