Modeling and Implementation of Wave Digital Filters

Sound Analysis, Synthesis and Processing
Module 2 - Sound Synthesis and Spatial Processing

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Outline

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Circuit Theory

- In its long history and evolution, Circuit Theory has had a formidable impact in nearly all fields of engineering
- Various lumped linear and nonlinear systems can be represented using equivalent electrical networks
- The model of an electrical circuit is made of
  - Equations describing the network topology called:
    - *Kirchhoff Voltage Laws* (KVL)
    - *Kirchhoff Current Laws* (KCL)
  - Constitutive equations of circuit elements such as:
    - *One-port elements* (e.g., sources, resistors, capacitors, inductors, diodes)
    - *Multi-port elements* (e.g., opamps, transformers, gyrators, transistors, vacuum tubes)

Circuit Simulation in the Kirchhoff Domain

- Kirchhoff descriptions of circuits are characterized by multivariate systems of Ordinary Differential Equations (ODEs)
- In order to numerically simulate a circuit, suitable discretization methods are needed for approximating time derivatives in the discrete-time domain
- **Computability problem**: when implicit discretization methods are used, the resulting system of discrete-time equations is implicit
    - Constitutive equations and topological information are merged

Circuit Simulation in the Kirchhoff Domain

- **Widely Adopted Solution**: using multivariate iterative solvers, such as Newton-Raphson solvers, whose dimensionality roughly equals the number of nodes (or loops) in the circuit
- Such a solution is *adopted in all the mainstream simulation methods* formulated in the Kirchhoff domain, such as:
  - Modified Nodal Analysis (MNA) method (SPICE-like software)
  - Sparse-Tableau method
  - State-Space methods
  - Port-Hamiltonian methods

Wave Digital Filters and Circuit Emulation

- Wave Digital Filter (WDF) theory developed by A. Fettweis during the 70s was *originally conceived as a methodology for modeling digital filters by discretizing reference analog circuits*
- WDF theory poses the basis for completely *new methods for emulating linear and nonlinear circuits* in the Wave Digital (WD) domain

Figure: Photo of Alfred Fettweis.

General Considerations on WDFs

- A WDF is derived discretizing a *reference analog circuit*
- Circuit elements and circuit topology are modeled separately
- One-port circuit elements are modeled as *input-output blocks* characterized by scattering relations
- Topological interconnections of elements are modeled using multi-input-multi-output *junctions* characterized by scattering matrices
- Elements and junctions are modeled in a *port-wise fashion*
- Each port of an element or junction is characterized by a pair of port variables called *wave variables*
- One introduced *free parameter* per port

Outline

Definition of Voltage Waves

- Kirchhoff variables at port n (of a generic port element or junction) are
  - the port voltage v_n
  - the port current i_n
- Wave variables (voltage waves) are defined as [1]

$$a_n = v_n + Z_n i_n \qquad b_n = v_n - Z_n i_n \tag{1}$$

  - a_n is the incident wave
  - b_n is the reflected wave
  - $Z_n \neq 0$ is a scalar free parameter called *reference port resistance*
- Inverse mapping

$$v_n = \frac{a_n + b_n}{2} \qquad i_n = \frac{a_n - b_n}{2Z_n} \tag{2}$$

Definition of Wave Variables in Vector Form

- Kirchhoff-to-Wave linear transformation

$$\begin{bmatrix} a_n \\ b_n \end{bmatrix} = \begin{bmatrix} 1 & Z_n \\ 1 & -Z_n \end{bmatrix} \begin{bmatrix} v_n \\ i_n \end{bmatrix} \tag{3}$$

- Wave-to-Kirchhoff linear transformation

$$\begin{bmatrix} v_n \\ i_n \end{bmatrix} = \frac{1}{2} \begin{bmatrix} 1 & 1 \\ 1/Z_n & -1/Z_n \end{bmatrix} \begin{bmatrix} a_n \\ b_n \end{bmatrix} \tag{4}$$

Outline

Constitutive Equations of One-Port Elements

- In the continuous-time domain (t is the time variable)

$$h\left(v(t), i(t)\right) = 0 \tag{5}$$

  - $v(t)$ is the port voltage and $i(t)$ is the port current
  - h is a (linear or nonlinear) dynamic or instantaneous function

- In the discrete-time domain

$$\widetilde{h}\left(v[k], i[k]\right) = 0 \tag{6}$$

  - $v[k] = v(kT_\mathsf{s})$ and $v[k] = v(kT_\mathsf{s})$, where k is the sampling index and $F_\mathsf{s} = 1/T_\mathsf{s}$ is the sampling frequency
  - if the element is memoryless we have that $\widetilde{h}(x, y) = h(x, y)$, otherwise $\widetilde{h}(x, y) \neq h(x, y)$

Linear One-Port Elements

- The majority of linear one-port elements in the discrete-time domain is characterized by a *constitutive equation* in the form

$$v[k] = R_{\mathsf{e}}[k]i[k] + V_{\mathsf{e}}[k] \tag{7}$$

  - $R_{\mathsf{e}}[k]$ is a resistance parameter
  - $V_{\mathsf{e}}[k]$ is a voltage bias parameter

Linear Resistor

- In the continuous-time domain the *constitutive equation* of a linear resistor with resistance R is

$$v(t) = Ri(t) \tag{8}$$

- In the discrete-time domain we get

$$v[k] = Ri[k] \tag{9}$$

- Eq. (9) is a special case of eq. (7) in which:
  - $R_{\mathsf{e}}[k] = R$
  - $V_{\mathsf{e}}[k] = 0$

Linear Resistive Voltage Generator

- In the continuous-time domain the *constitutive equation* of a linear resistive voltage source with source signal $V_{\text{g}}(t)$ and internal series resistance R_{g} is

$$v(t) = R_{\text{g}} i(t) + V_{\text{g}}(t) \tag{10}$$

- In the discrete-time domain we get

$$v[k] = R_{\text{g}} i[k] + V_{\text{g}}[k] \tag{11}$$

- Eq. (11) is a special case of eq. (7) in which:
  - $R_{\text{e}}[k] = R_{\text{g}}$
  - $V_{\text{e}}[k] = V_{\text{g}}[k] = V_{\text{g}}(kT_{\text{s}})$

Linear Dynamic Elements

- In the continuous-time domain the *constitutive equation* of a linear dynamic element (capacitor or inductor) is

$$y(t) = \mu \frac{\mathrm{d}x(t)}{\mathrm{d}t} \tag{12}$$

  - $x(t)$ is a port voltage or port current
  - $y(t)$ is a port current or port voltage
  - μ is a (capacitative or inductive) real coefficient

- In the Laplace domain, where s is the complex frequency variable, (12) is written as

$$Y(s) = s\mu X(s) \tag{13}$$

Possible Time Derivative Approximations

Mappings from the Laplace domain with complex frequency variable s to the Z-domain with complex variable $z = e^{sT_\mathsf{s}}$

- Backward Euler Method

$$s \leftarrow \frac{1 - z^{-1}}{T_\mathsf{s}} \tag{14}$$

- Trapezoidal Rule (a.k.a. bilinear transform or Tustin's method)

$$s \leftarrow \frac{2}{T_\mathsf{s}} \frac{1 - z^{-1}}{1 + z^{-1}} \tag{15}$$

- Many other discretization methods are usable (e.g., finite difference methods, Runge-Kutta methods, etc. . . .)

Trapezoidal Rule and Frequency Warping (1/2)

- According to (15), *frequencies referred to the discrete-time domain* are mapped to *frequencies referred to the continuous-time domain* by the substitution

$$j\omega \leftarrow \frac{2}{T_{\mathsf{s}}}\frac{e^{j\widetilde{\omega}T_{\mathsf{s}}}-1}{e^{j\widetilde{\omega}T_{\mathsf{s}}}+1} \tag{16}$$

  where ω satisfies $s = j\omega$ and $\widetilde{\omega}$ satisfies $z = e^{j\widetilde{\omega}T_{\mathsf{s}}}$
- After some simplifications (16) can be rewritten as

$$j\omega \leftarrow j\frac{2}{T_{\mathsf{s}}}\tan\left(\widetilde{\omega}\frac{T_{\mathsf{s}}}{2}\right) \tag{17}$$

Trapezoidal Rule and Frequency Warping (2/2)

- According to (17), it is possible to express in closed-form the reference "continuous-time frequency" ω as a function of the "discrete-time frequency" $\widetilde{\omega}$ using the warping mapping

$$\omega = \frac{2}{T_{\mathsf{s}}} \tan\left(\widetilde{\omega}\frac{T_{\mathsf{s}}}{2}\right) \tag{18}$$

- ω is really close to $\widetilde{\omega}$ at low frequencies, while they differ more and more at high frequencies
- The higher the sampling frequency $F_{\mathsf{s}} = 1/T_{\mathsf{s}}$, the more the difference between ω and $\widetilde{\omega}$ becomes negligible in the whole frequency range of interest

Linear Capacitor

- In the Laplace domain the *constitutive equation* of a linear capacitor with capacitance C is

$$I(s) = sCV(s) \tag{19}$$

- After applying the bilinear transform (15) to (19), in the discrete-time domain we get

$$v[k] = \frac{T_\mathsf{s}}{2C} i[k] + \frac{T_\mathsf{s}}{2C} i[k-1] + v[k-1] \tag{20}$$

- Eq. (20) is a special case of eq. (7) in which [2]:
  - $R_\mathsf{e}[k] = T_\mathsf{s}/(2C)$
  - $V_\mathsf{e}[k] = T_\mathsf{s} i[k-1]/(2C) + v[k-1]$

Linear Inductor

- In the Laplace domain the *constitutive equation* of a linear inductor with inductance L is

$$V(s) = sLI(s) \tag{21}$$

- After applying the bilinear transform (15) to (21), in the discrete-time domain we get

$$v[k] = \frac{2L}{T_\mathsf{s}} i[k] - \frac{2L}{T_\mathsf{s}} i[k-1] - v[k-1] \tag{22}$$

- Eq. (22) is a special case of eq. (7) in which [2]:
  - $R_\mathsf{e}[k] = 2L/T_\mathsf{s}$
  - $V_\mathsf{e}[k] = -(2Li[k-1])/T_\mathsf{s} - v[k-1]$

Linear Wave Digital One-Port Element

- Wave-to-Kirchhoff transformation in the discrete-time domain

$$v[k] = \frac{a[k]+b[k]}{2} \;, \qquad i[k] = \frac{a[k]-b[k]}{2Z[k]} \tag{23}$$

- Applying the substitution (23) in (7) and solving for $b[k]$, we get the scattering relation of a generic linear one-port element

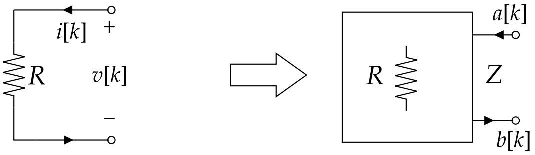
$$b[k] = \frac{R_{\mathsf{e}}[k]-Z[k]}{R_{\mathsf{e}}[k]+Z[k]}a[k] + \frac{2Z[k]}{R_{\mathsf{e}}[k]+Z[k]}V_{\mathsf{e}}[k] \tag{24}$$

- Adaptation case (the instantaneous dependency of $b[k]$ from $a[k]$ is eliminated)

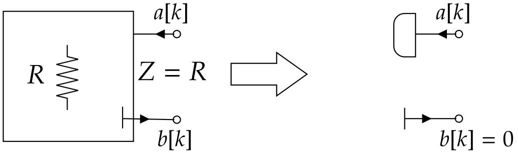
$$b[k] = V_{\mathsf{e}}[k] \;, \qquad \text{with} \qquad Z[k] = R_{\mathsf{e}}[k] \tag{25}$$

WD Resistor

$$b[k] = V_{\mathrm{e}}[k] = 0, \qquad \text{Adapation: } Z = R_{\mathrm{e}}[k] = R$$

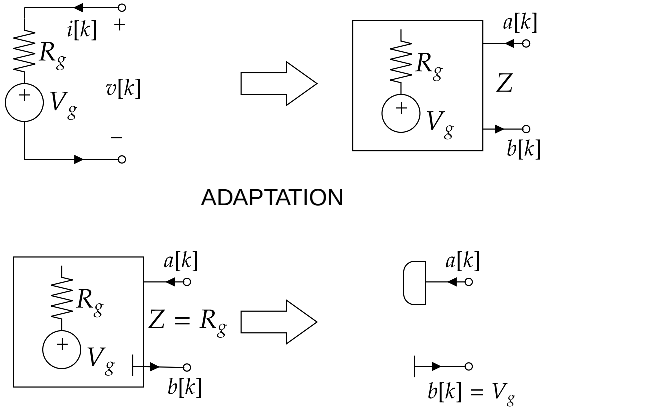


ADAPTATION



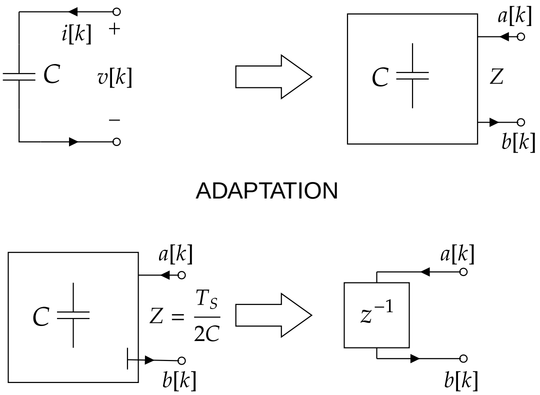
WD Resistive Voltage Source

$$b[k] = V_{\mathrm{e}}[k] = V_{\mathrm{g}}[k], \qquad \text{Adapation: } Z = R_{\mathrm{e}}[k] = R_{\mathrm{g}}$$



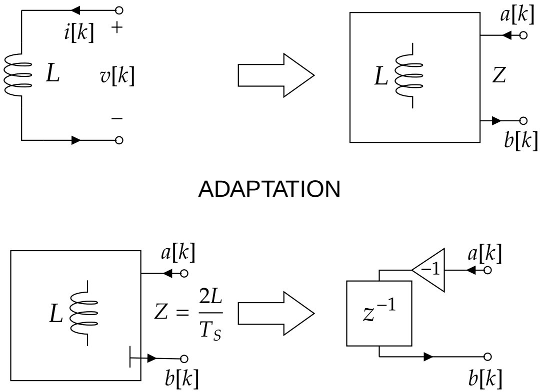
WD Capacitor

$$b[k] = V_{\mathsf{e}}[k] = \frac{T_{\mathsf{s}}}{2C} i[k-1] + v[k-1], \quad \text{Adapation: } Z = R_{\mathsf{e}}[k] = \frac{T_{\mathsf{s}}}{2C}$$



WD Inductor

$$b[k] = V_{\mathsf{e}}[k] = -\frac{2L}{T_{\mathsf{s}}} i[k-1] - v[k-1], \quad \text{Adapation: } Z = R_{\mathsf{e}}[k] = \frac{2L}{T_{\mathsf{s}}}$$



Implementation of Linear WD One-Ports

Table: *Wave mappings of common WD linear one-port elements.*

Constitutive Eq.	Wave Mapping	Adaptation Condition
$v(t) = V_{\mathrm{g}}(t) + R_{\mathrm{g}} i(t)$	$b[k] = V_{\mathrm{g}}[k]$	$Z[k] = R_{\mathrm{g}}$
$v(t) = Ri(t)$	$b[k] = 0$	$Z[k] = R$
$i(t) = C\dfrac{dv(t)}{dt}$	$b[k] = a[k-1]$	$Z[k] = \dfrac{T_{\mathrm{s}}}{2C}$
$v(t) = L\dfrac{di(t)}{dt}$	$b[k] = -a[k-1]$	$Z[k] = \dfrac{2L}{T_{\mathrm{s}}}$

Nonlinear Diode Model

- Shockley diode model for exponential p–n junction diodes

$$i(t) = I_{\mathsf{s}}\left(e^{v(t)/(\eta V_{\mathsf{th}})} - 1\right) \tag{26}$$

  - saturation current I_{s}
  - thermal voltage V_{th}
  - ideality factor η
- Eq. (26) is nonlinear and it cannot be put in the form (7)

Nonlinear WD Diode Model

- Substitute (23) into the discrete-time version of eq. (26)
- The result is a *transcendental equation* in the WD domain
- The following closed-form solution for $b[k]$ can be found [3, 4]

$$b[k] = a[k] + 2Z[k]I_{\mathsf{s}} - 2\eta V_{\mathsf{th}} \mathrm{W}\left(\frac{Z[k]I_{\mathsf{s}}}{\eta V_{\mathsf{th}}} e^{\frac{Z[k]I_{\mathsf{s}} + a[k]}{\eta V_{\mathsf{th}}}} \right) \quad (27)$$

  - $\mathrm{W}(x)$ is the *Lambert Function* implicitly defined as

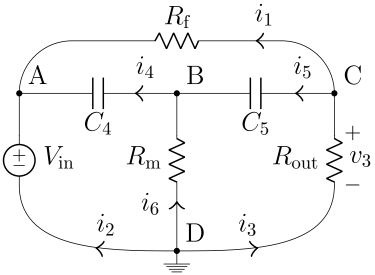
$$x = \mathrm{W}(x)e^{\mathrm{W}(x)}$$

- The nonlinear WD diode cannot be adapted!

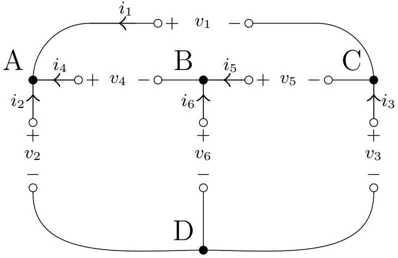
Outline

Topological Junctions or Connection Networks

- A N-port topological junction is an open interconnection network (i.e., without *electrical loads*) characterized by
  - a vector of port voltages $\mathbf{v} = [v_1, \ldots, v_N]^T$
  - a vector of port currents $\mathbf{i} = [i_1, \ldots, i_N]^T$
- Example:



(a) Reference circuit.



(b) Topological connection network.

Relations between Port Variables

- Found a *subset of independent port voltages* we have that

$$\mathbf{v} = \mathbf{Q}^T \mathbf{v}_{\mathrm{t}} \tag{28}$$

  - $\mathbf{v}_{\mathrm{t}}$ is the vector of size $q \times 1$ collecting independent port voltages
  - $\mathbf{Q}$ is the fundamental cut-set matrix of size $q \times N$
- Found a *subset of independent port currents* we have that

$$\mathbf{i} = \mathbf{B}^T \mathbf{i}_{\mathrm{l}} \tag{29}$$

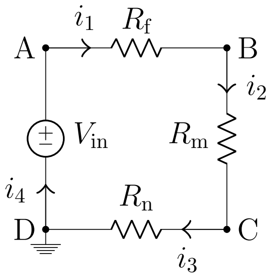
  - $\mathbf{i}_{\mathrm{l}}$ is the vector of size $p \times 1$ collecting independent port currents
  - $\mathbf{B}$ is the fundamental loop matrix of size $p \times N$
- $p + q = N$
- Orthogonality property

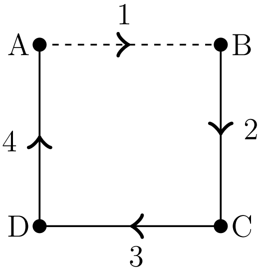
$$\mathbf{B}\mathbf{Q}^T = \mathbf{0}_{p\times q} \quad , \qquad \mathbf{Q}\mathbf{B}^T = \mathbf{0}_{q\times p} \tag{30}$$

How to find independent port variables?

- Consider the digraph $\mathcal{D}$ of the reference circuit where the *edges* represent the loads of the connection network (one per port), while the *vertices* represent the nodes of the circuit [5]
- Apply a tree-cotree decomposition to $\mathcal{D}$
  - A tree $\mathcal{T}$ of $\mathcal{D}$ is defined as *a connected acyclic subgraph of $\mathcal{D}$ containing all vertices*
  - A cotree $\mathcal{C}$ of $\mathcal{D}$ is *a subgraph of $\mathcal{D}$ containing all the edges of $\mathcal{D}$ that are not in a reference tree $\mathcal{T}$*
- Independent port voltages in $\mathbf{v}_{\mathrm{t}}$ are those *related to the edges of the tree*
- Independent port currents in $\mathbf{i}_{\mathrm{l}}$ are those *related to the edges of the cotree*

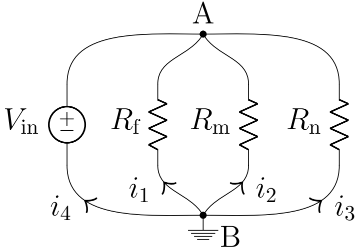
Example 1: Series Connection Network

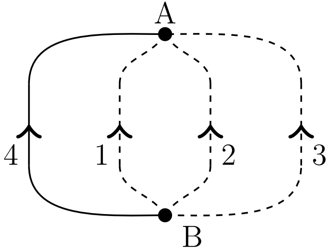




$$\mathbf{i} = \mathbf{B}^T \mathbf{i}_\mathsf{l} \quad \rightarrow \quad \begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ i_4 \end{bmatrix} = \begin{bmatrix} 1 \\ 1 \\ 1 \\ 1 \end{bmatrix} i_1 \tag{31}$$

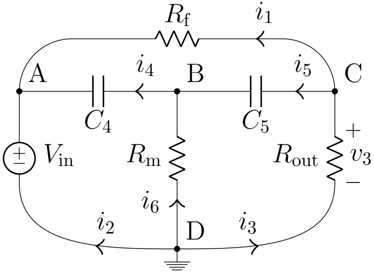
Example 2: Parallel Connection Network

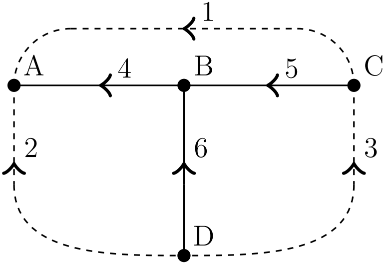




$$\mathbf{v} = \mathbf{Q}^T \mathbf{v}_{\mathsf{t}} \quad \rightarrow \quad \begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ v_4 \end{bmatrix} = \begin{bmatrix} 1 \\ 1 \\ 1 \\ 1 \end{bmatrix} v_4 \tag{32}$$

Example 3: Bridged-Tee Connection Network





$$\mathbf{i} = \mathbf{B}^T \mathbf{i}_\mathsf{l} \quad \rightarrow \quad \begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ i_4 \\ i_5 \\ i_6 \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \\ -1 & -1 & 0 \\ -1 & 0 & 1 \\ 0 & -1 & -1 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} \tag{33}$$

WD Junctions (Adaptors)

- In the WD domain a topological connection network is modeled as a WD scattering junction (also called *adaptor*)
- Kirchhoff-to-Wave mapping of port variables

$$\mathbf{a} = \mathbf{v} + \mathbf{Z}\mathbf{i} \ , \quad \mathbf{b} = \mathbf{v} - \mathbf{Z}\mathbf{i} \tag{34}$$

  - $\mathbf{a} = [a_1, \ldots, a_N]^T$ vector of waves incident to the junction
  - $\mathbf{b} = [b_1, \ldots, b_N]^T$ vector of waves reflected by the junction
  - $\mathbf{Z} = \mathrm{diag}[Z_1, \ldots, Z_N]$ is the diagonal matrix of free parameters
- Scattering relation

$$\mathbf{b} = \mathbf{S}\mathbf{a} \tag{35}$$

  - $\mathbf{S}$ is a $N \times N$ scattering matrix

Formation of the Scattering Matrix

- If $q \leq p$ use

$$\mathbf{S} = 2\mathbf{Q}^T(\mathbf{Q}\mathbf{Z}^{-1}\mathbf{Q}^T)^{-1}\mathbf{Q}\mathbf{Z}^{-1} - \mathbf{I} \tag{36}$$

    - $\mathbf{I}$ is the $N \times N$ identity matrix
    - the inversion of the $q \times q$ matrix $\mathbf{Q}\mathbf{Z}^{-1}\mathbf{Q}^T$ is required
- If $q \geq p$

$$\mathbf{S} = \mathbf{I} - 2\mathbf{Z}\mathbf{B}^T(\mathbf{B}\mathbf{Z}\mathbf{B}^T)^{-1}\mathbf{B} \tag{37}$$

    - $\mathbf{I}$ is the $N \times N$ identity matrix
    - the inversion of the $p \times p$ matrix $\mathbf{B}\mathbf{Z}\mathbf{B}^T$ is required

Reflection-Free Ports in WD Junctions

- One port of a topological WD junction can be made reflection-free (we say *the port is adapted*)
- The nth port of a WD junction is made reflection-free if the nth diagonal entry s_{nn} of $\mathbf{S}$ is imposed to be zero

$$s_{nn} = 0 \tag{38}$$

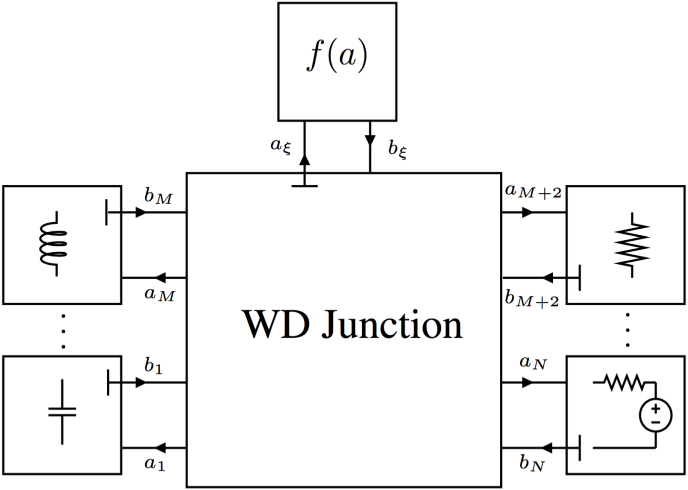
- Condition (38) can be satisfied by properly setting the free parameter Z_n
- Examples
  - The nth port of a N-port series WD junction is made reflection-free by setting $Z_n = \sum_{k \neq n} Z_k$
  - The nth port of a N-port parallel WD junction is made reflection-free by setting $Z_n^{-1} = \sum_{k \neq n} Z_k^{-1}$

Outline

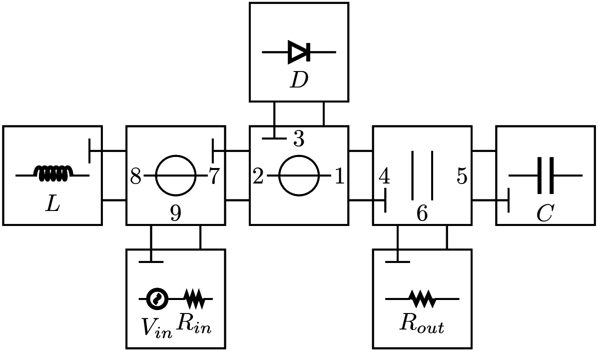
Modeling WDFs with One Nonlinearity

- The WDF is modeled as a connection tree
- *The nonlinear one-port element* is the root
- *WD topological junctions* are the nodes
  - *Ports of WD junctions either connected to other WD junctions or to the nonlinear element are made reflection-free*
- *Linear WD one-port elements* are the leaves
  - *Linear WD elements are all adapted*
- In case the topology is solely made of *series-parallel connections*, the WDF can be modeled as a Binary Connection Tree (BCT)
  - In a BCT nodes are 3-port series or parallel WD junctions [6]

Generic Connection Tree with One Node



Example of Binary Connection Tree



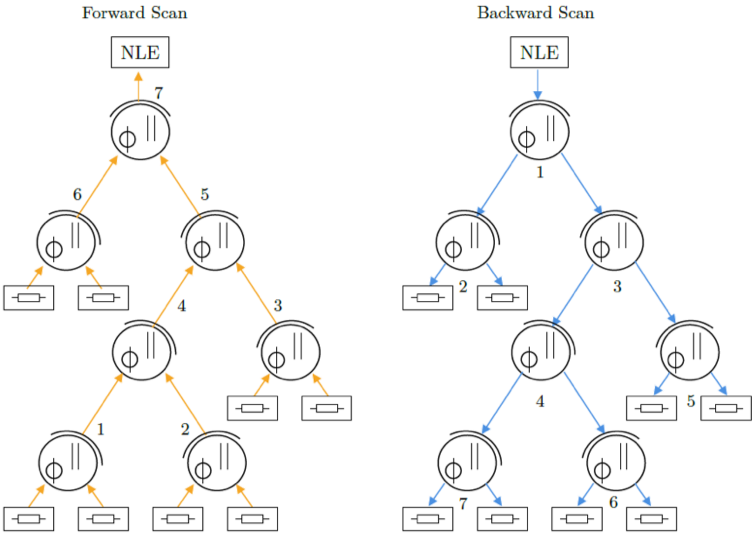
- In the BCT structure nodes are 3-port series/parallel adaptors.

Computational Flow in Connection Trees

The following process is repeated at each sampling step.

- Forward scan from the leaves to the root
  - waves reflected by the linear elements (incident to the junctions) are computed
  - waves are propagated through the junctions up to the nonlinear element
- Local nonlinear scattering stage at the root
  - given the incident wave, the wave reflected by the nonlinear element is computed
- Backward scan from the root to the leaves
  - waves are propagated through the junctions up to the linear elements
  - waves incident to the linear elements are computed

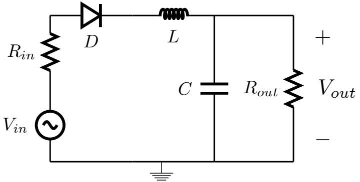
Illustration of Computational Flow in a BCT



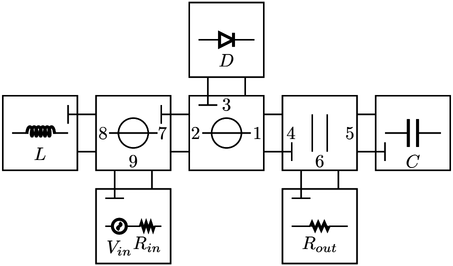
Outline

Envelope Follower Circuit and WDF Realization

- Reference circuit



- Corresponding WDF with BCT structure



WDF Structure

- The WDFs is composed of:
  - Four linear WD elements (input source V_{in} with series resistance R_{in}, inductor L, capacitor C and output resistance R_{out})
  - Three 3-port WD junctions (two series adaptors, one parallel adaptor)
  - One nonlinear WD element (the exponential diode D)
- Ports of 3-port adaptors are numbered;
  - the adaptor with ports number 4, number 5 and number 6 is a parallel adaptor
  - the other two are series adaptors

Port Connections between WD Blocks

Examples of port connections

- The port connection between port number 1 of the series adaptor and port number 4 of the parallel adaptor on the right is performed imposing the following constraints

$$a_1[k] = b_4[k] \quad , \quad a_4[k] = b_1[k] \quad , \quad Z_1 = Z_4 \tag{39}$$

- Similarly, connection between port number 2 of the series adaptor and port number 7 of the series adaptor on the left is performed imposing the following constraints

$$a_2[k] = b_7[k] \quad , \quad a_7[k] = b_2[k] \quad , \quad Z_2 = Z_7 \tag{40}$$

Adaptation Conditions

- A WD block with a *T-shaped symbol* at a port is *adapted* at that port (that port is reflection-free)
- For instance, the parallel adaptor is adapted at port number 4 and all one-port WD elements are adapted, except for the diode which cannot be adapted.
- Adaptation conditions set at *ports facing linear elements* are

$$Z_9 = R_{in} \quad , \quad Z_6 = R_{out} \quad , \quad Z_5 = T_{\mathsf{s}}/(2C) \quad , \quad Z_8 = (2L)/T_{\mathsf{s}} \tag{41}$$

- Adaptation conditions set at *ports facing other adaptors* are

$$Z_1 = Z_4 = \frac{Z_5 Z_6}{Z_5 + Z_6} \quad , \quad Z_2 = Z_7 = Z_8 + Z_9 \quad , \quad Z_3 = Z_1 + Z_2 \tag{42}$$

Scattering Relations of the Elements

- Real voltage source V_{in} with series resistance R_{in}

$$a_9[k] = V_{in}[k] \tag{43}$$

- Resistor with resistance R_{out}

$$a_6[k] = 0 \tag{44}$$

- Capacitor with capacitance C

$$a_5[k] = b_5[k-1] \tag{45}$$

- Inductor with inductance L

$$a_8[k] = -b_8[k-1] \tag{46}$$

- Diode D

$$a_3[k] = b_3[k] + 2Z_3 I_{\mathsf{s}} - 2\eta V_{\mathsf{th}} \mathrm{W}\left(\frac{Z_3 I_{\mathsf{s}}}{\eta V_{\mathsf{th}}} e^{(Z_3 I_{\mathsf{s}} + b_3[k])/(\eta V_{\mathsf{th}})}\right) \tag{47}$$

Scattering Relations of WD Junctions

- Series adaptor with ports 1, 2, 3 and scattering matrix $\mathbf{S}_{\mathsf{S1}}$

$$\begin{bmatrix} b_1[k] \\ b_2[k] \\ b_3[k] \end{bmatrix} = \mathbf{S}_{\mathsf{S1}} \begin{bmatrix} a_1[k] \\ a_2[k] \\ a_3[k] \end{bmatrix} \tag{48}$$

- Series adaptor with ports 7, 8, 9 and scattering matrix $\mathbf{S}_{\mathsf{S2}}$

$$\begin{bmatrix} b_7[k] \\ b_8[k] \\ b_9[k] \end{bmatrix} = \mathbf{S}_{\mathsf{S2}} \begin{bmatrix} a_7[k] \\ a_8[k] \\ a_9[k] \end{bmatrix} \tag{49}$$

- Parallel adaptor with ports 4, 5, 6 and scattering matrix $\mathbf{S}_{\mathsf{P1}}$

$$\begin{bmatrix} b_4[k] \\ b_5[k] \\ b_6[k] \end{bmatrix} = \mathbf{S}_{\mathsf{P1}} \begin{bmatrix} a_4[k] \\ a_5[k] \\ a_6[k] \end{bmatrix} \tag{50}$$

Scattering Matrices of WD Junctions

$$\mathbf{S}_{\mathsf{S1}} = \begin{bmatrix} s_{11} & s_{12} & s_{13} \\ s_{21} & s_{22} & s_{23} \\ s_{31} & s_{32} & s_{33} \end{bmatrix} = \begin{bmatrix} \gamma_{\mathsf{S1}} & (\gamma_{\mathsf{S1}} - 1) & (\gamma_{\mathsf{S1}} - 1) \\ -\gamma_{\mathsf{S1}} & (1 - \gamma_{\mathsf{S1}}) & -\gamma_{\mathsf{S1}} \\ -1 & -1 & 0 \end{bmatrix} \quad ,$$

$$\mathbf{S}_{\mathsf{S2}} = \begin{bmatrix} s_{77} & s_{78} & s_{79} \\ s_{87} & s_{88} & s_{89} \\ s_{97} & s_{98} & s_{99} \end{bmatrix} = \begin{bmatrix} 0 & -1 & -1 \\ -\gamma_{\mathsf{S2}} & (1 - \gamma_{\mathsf{S2}}) & -\gamma_{\mathsf{S2}} \\ (\gamma_{\mathsf{S2}} - 1) & (\gamma_{\mathsf{S2}} - 1) & \gamma_{\mathsf{S2}} \end{bmatrix} \quad ,$$

where $\gamma_{\mathsf{S1}} = Z_2/(Z_1 + Z_2)$ and $\gamma_{\mathsf{S2}} = Z_8/(Z_8 + Z_9)$.

$$\mathbf{S}_{\mathsf{P1}} = \begin{bmatrix} s_{44} & s_{45} & s_{46} \\ s_{54} & s_{55} & s_{56} \\ s_{64} & s_{65} & s_{66} \end{bmatrix} = \begin{bmatrix} 0 & (1 - \gamma_{\mathsf{P1}}) & \gamma_{\mathsf{P1}} \\ 1 & -\gamma_{\mathsf{P1}} & \gamma_{\mathsf{P1}} \\ 1 & (1 - \gamma_{\mathsf{P1}}) & (\gamma_{\mathsf{P1}} - 1) \end{bmatrix} \quad ,$$

where $\gamma_{\mathsf{P1}} = Z_5/(Z_5 + Z_6)$.

Forward Scan (from leaves to root of the BCT)

- compute waves reflected from *linear elements*

$$a_9[k] = V_{in}[k] \quad , \tag{51}$$
$$a_6[k] = 0 \quad , \tag{52}$$
$$a_5[k] = b_5[k-1] \quad , \tag{53}$$
$$a_8[k] = -b_8[k-1] \tag{54}$$

- compute waves reflected from the *first layer of adaptors*

$$b_4[k] = (1-\gamma_{\mathsf{P1}})a_5[k] + \gamma_{\mathsf{P1}} a_6[k] \quad , \tag{55}$$
$$b_7[k] = -a_8[k] - a_9[k] \tag{56}$$

- compute waves reflected from the *second layer of adaptors*

$$a_1[k] = b_4[k] \quad , \tag{57}$$
$$a_2[k] = b_7[k] \quad , \tag{58}$$
$$b_3[k] = -a_1[k] - a_2[k] \tag{59}$$

Local Nonlinear Scattering Stage

- compute wave reflected by the nonlinear diode (root of the BCT)

$$a_3[k] = b_3[k] + 2Z_3 I_{\mathsf{s}} - 2\eta V_{\mathsf{th}} \mathrm{W}\left(\frac{Z_3 I_{\mathsf{s}}}{\eta V_{\mathsf{th}}} e^{(Z_3 I_{\mathsf{s}} + b_3[k])/(\eta V_{\mathsf{th}})}\right) \quad (60)$$

Backward Scan (from root to leaves of the BCT)

- compute waves reflected from the second layer of adaptors toward linear elements

$$b_1[k] = \gamma_{\mathsf{S1}} a_1[k] + (\gamma_{\mathsf{S1}} - 1) a_2[k] + (\gamma_{\mathsf{S1}} - 1) a_3[k] \quad , \tag{61}$$

$$b_2[k] = -\gamma_{\mathsf{S1}} a_1[k] + (1 - \gamma_{\mathsf{S1}}) a_2[k] + -\gamma_{\mathsf{S1}} a_3[k] \quad . \tag{62}$$

- compute waves reflected from the first layer of adaptors toward linear elements, i.e., waves incident to linear elements,

$$a_4[k] = b_1[k] \quad , \tag{63}$$

$$a_7[k] = b_2[k] \quad , \tag{64}$$

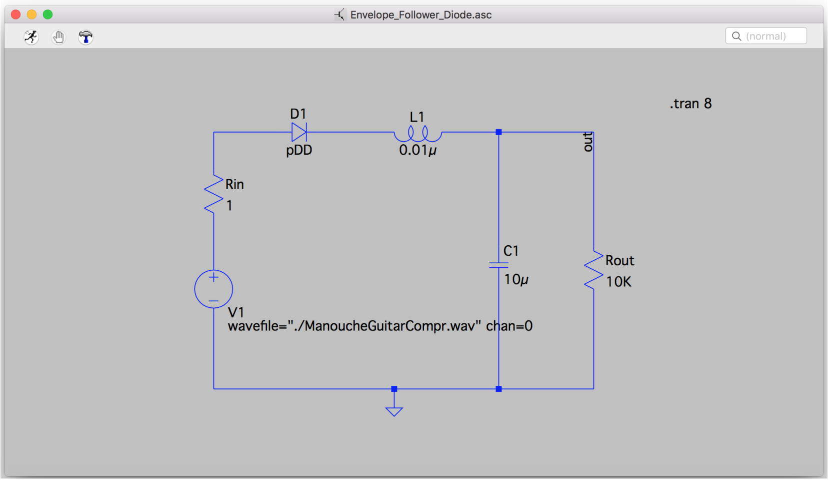
$$b_5[k] = a_4[k] - \gamma_{\mathsf{P1}} a_5[k] + \gamma_{\mathsf{P1}} a_6[k] \quad , \tag{65}$$

$$b_6[k] = a_4[k] + (1 - \gamma_{\mathsf{P1}}) a_5[k] + (\gamma_{\mathsf{P1}} - 1) a_6[k] \quad , \tag{66}$$

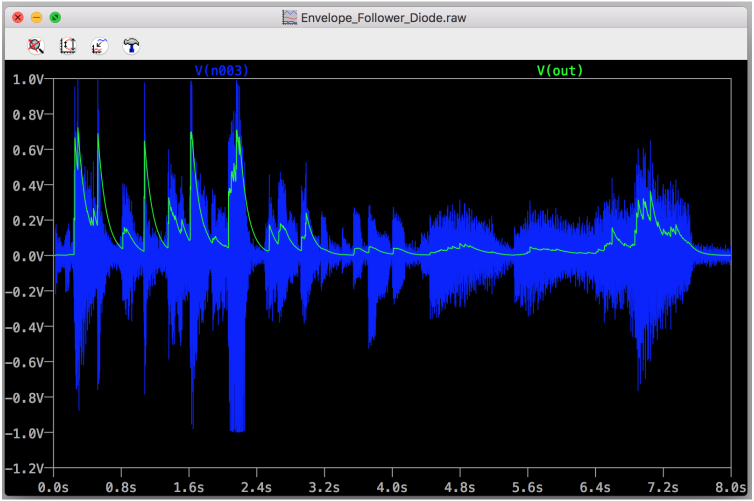
$$b_8[k] = -\gamma_{\mathsf{S2}} a_7[k] + (1 - \gamma_{\mathsf{S2}}) a_8[k] - \gamma_{\mathsf{S2}} a_9[k] \quad , \tag{67}$$

$$b_9[k] = (\gamma_{\mathsf{S2}} - 1) a_7[k] + (\gamma_{\mathsf{S2}} - 1) a_8[k] + \gamma_{\mathsf{S2}} a_9[k] \tag{68}$$

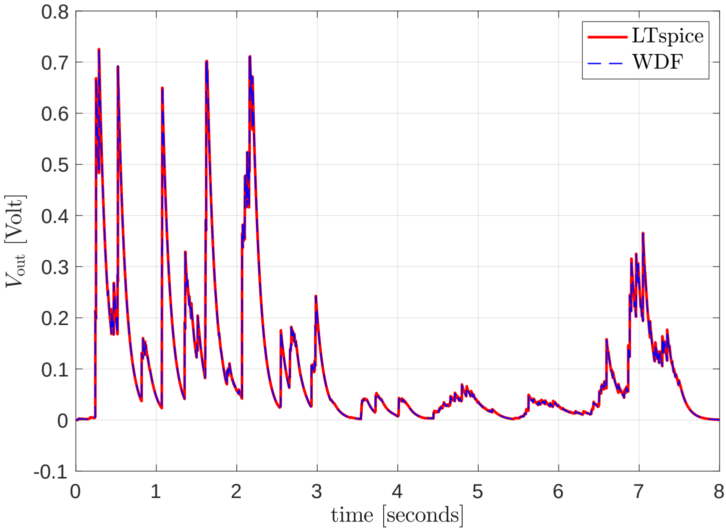
LTspice Implementation



LTspice Implementation



Comparison WDF vs LTspice



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