

Combinational Logic Circuits

Learning Outcomes

At the end of this activity, you should be able to:

1. differentiate combinational and sequential elements in a processor;
2. implement combinational logic circuit elements in VHDL;

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1 Discussion

The discussion in this handout aims only to provide an outline of what is in the video lecture. It is recommended that you watch the video in its entirety.

The computer can only execute machine language that it understands. This language is part of its architectural design or the Instruction Set Architecture (ISA). Machine language is nothing more than an encoding of bits. The computer can will do nothing unless instructions are given to it. These instructions will come from programmers. However, it is very difficult for programmers to use machine language directly. Instead, assembly language is used which is more comprehensible for humans. The assembler translates the assembly language program to machine language.

1.1 Definitions

Here are some terms worth knowing and remembering in this lab.

- *Datapath* - The component of the processor that performs arithmetic operations
- *Control* - The component of the processor that commands the datapath, memory, and I/O devices according to the instructions of the program
- *Combinational elements* - Logic elements in the datapath that operate on data values
- *State elements* - contains state, has some internal storage
- *Edge-triggered clocking* - that any values stored in a sequential logic element are updated only on a clock edge, which is a quick transition from low to high or high to low
- *Clock cycle length* - time to propagate the signal from state element 1, through the combinational element, and state element 2

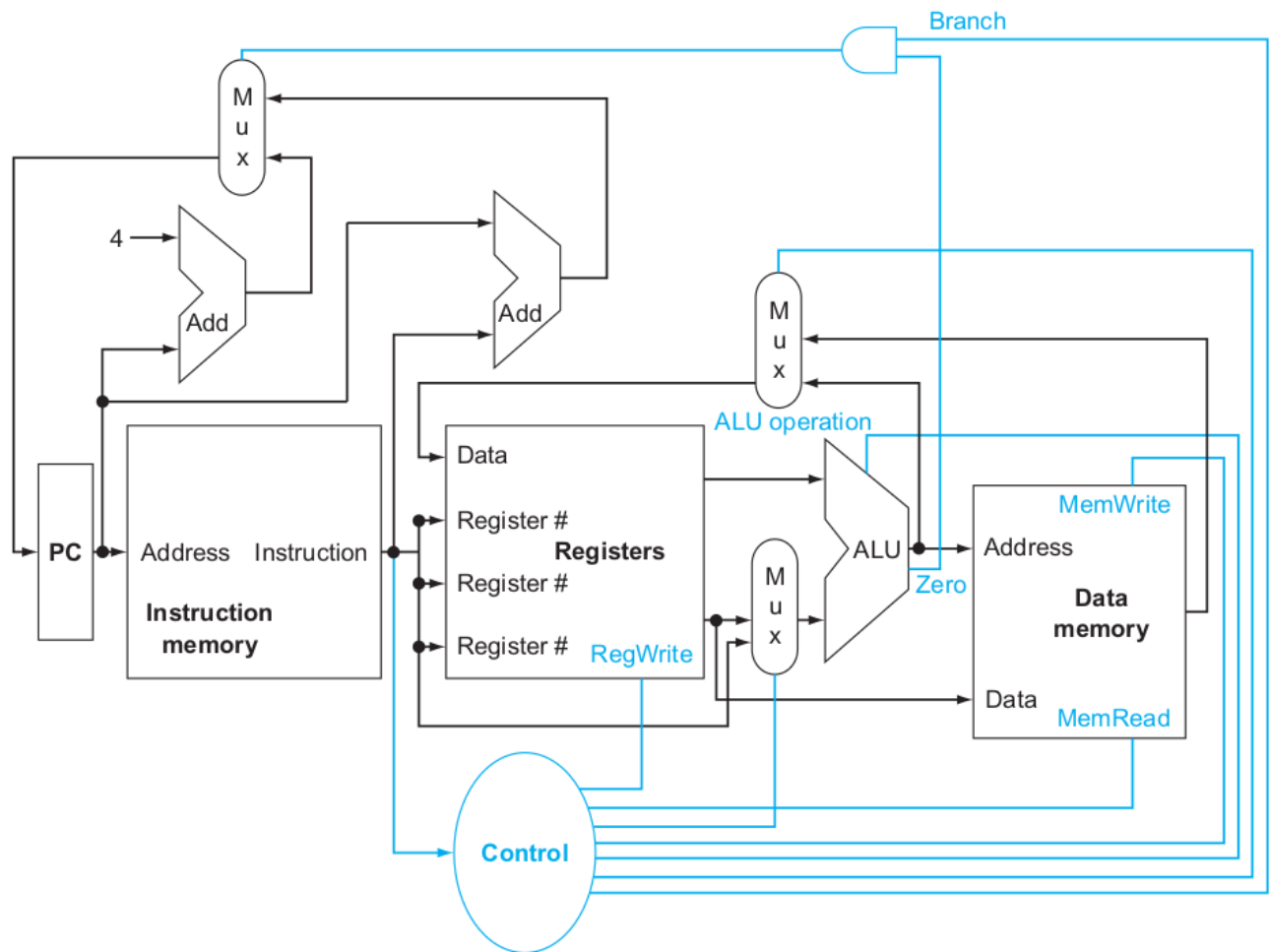


Figure 1: Single-Cycle Datapath and Control.

1.2 Single-Cycle Datapath and Control

A processor is composed of the datapath and control unit. Figure 1 shows an example of a single-cycle datapath and control. The main functional units are the following:

- *Program Counter (PC)* - holds the address of the next instruction to be executed
- *Instruction Memory (IM)*-holds the instructions/machine language
- *Register File (RF)*- fast storage
- *Arithmetic and Logic Unit (ALU)*- performs computations
- *Data Memory (DM)*- holds data used by programs
- *Control Unit (CU)*- drives the execution

The blue lines indicate control signals most of which originate from control based on the instruction being executed. You can think of the Control Unit as the 'brain' and the rest as the body parts.

Each of the above functional components are implemented using combinational and sequential logic circuits as building blocks.

Instruction execution follows the following cycle or states:

- *Instruction Fetch (IF)* - instruction is fetch from IM at address specified by PC

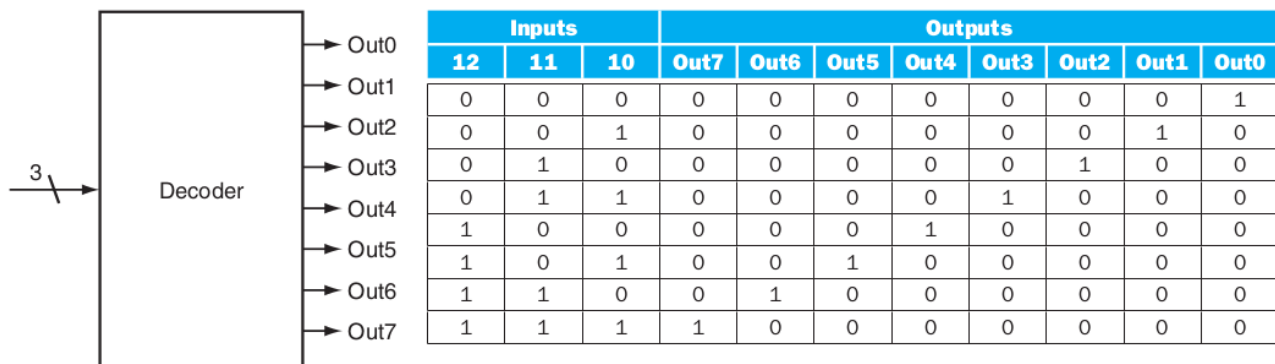


Figure 2: 3-to-8 decoder.

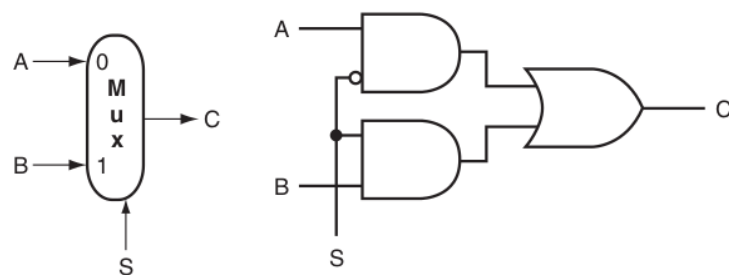


Figure 3: 2-to-1 Multiplexer.

- *Instruction Decode (ID)* - current instruction is examined for opcode and operands
- *Execute (EX)* - perform operations based on opcode
- *Memory (MEM)* - need to store data to DM
- *Writeback (WB)* - result will be used stored in register or used in the next instruction

1.3 Decoders

Decoders accepts an n -bit input and produces 2^n outputs but only one output is asserted. Figure 2 shows an example 3-to-8 decoder.

1.4 Multiplexers/Selectors

A multiplexer select which input will be allowed to pass through as output. Figure 3 show a mux with the selector S and two inputs A and B . It is implemented using two AND gates and one OR gate. To support multiple bits, this single bit multiplexer can be cascaded as an array as shown in Figure 4.

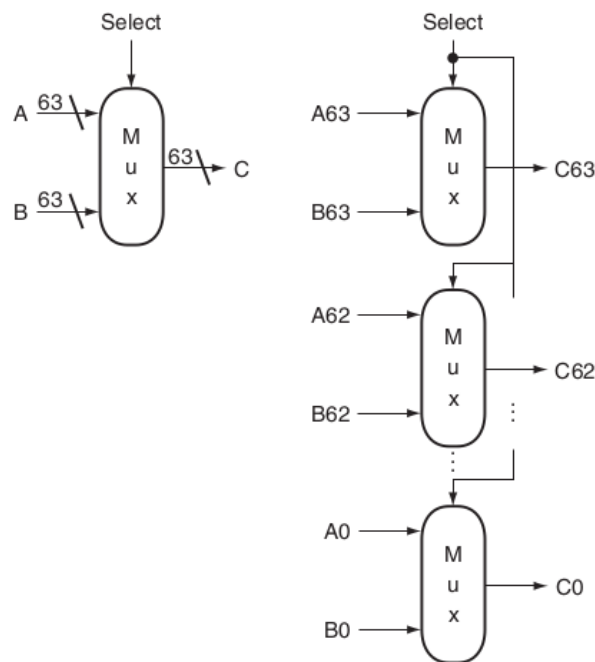


Figure 4: An array of 1-bit multiplexers to select from two 64-bit inputs.

2 Examples

3 Summary

4 Learning Activities

4.1 Self-Study Questions/Sample Problems