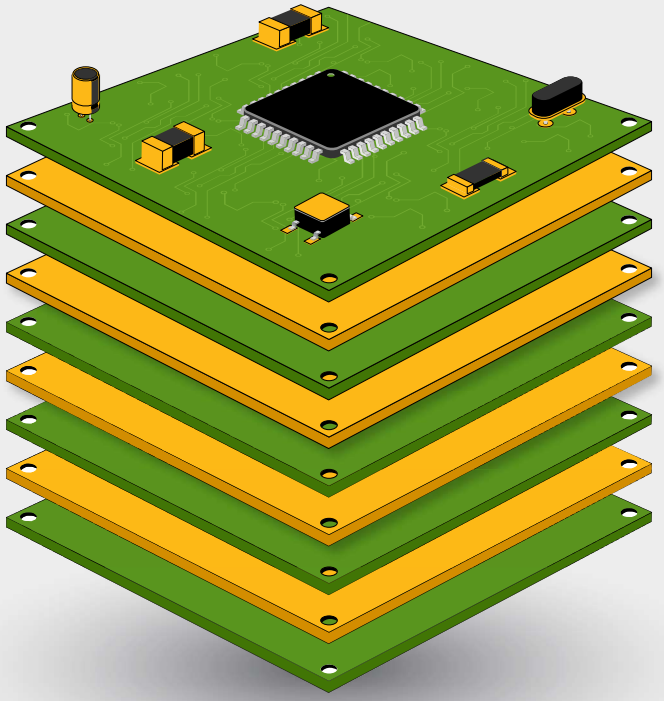
SIERRA CIRCUITS



PCB STACK-UP

DESIGN GUIDE

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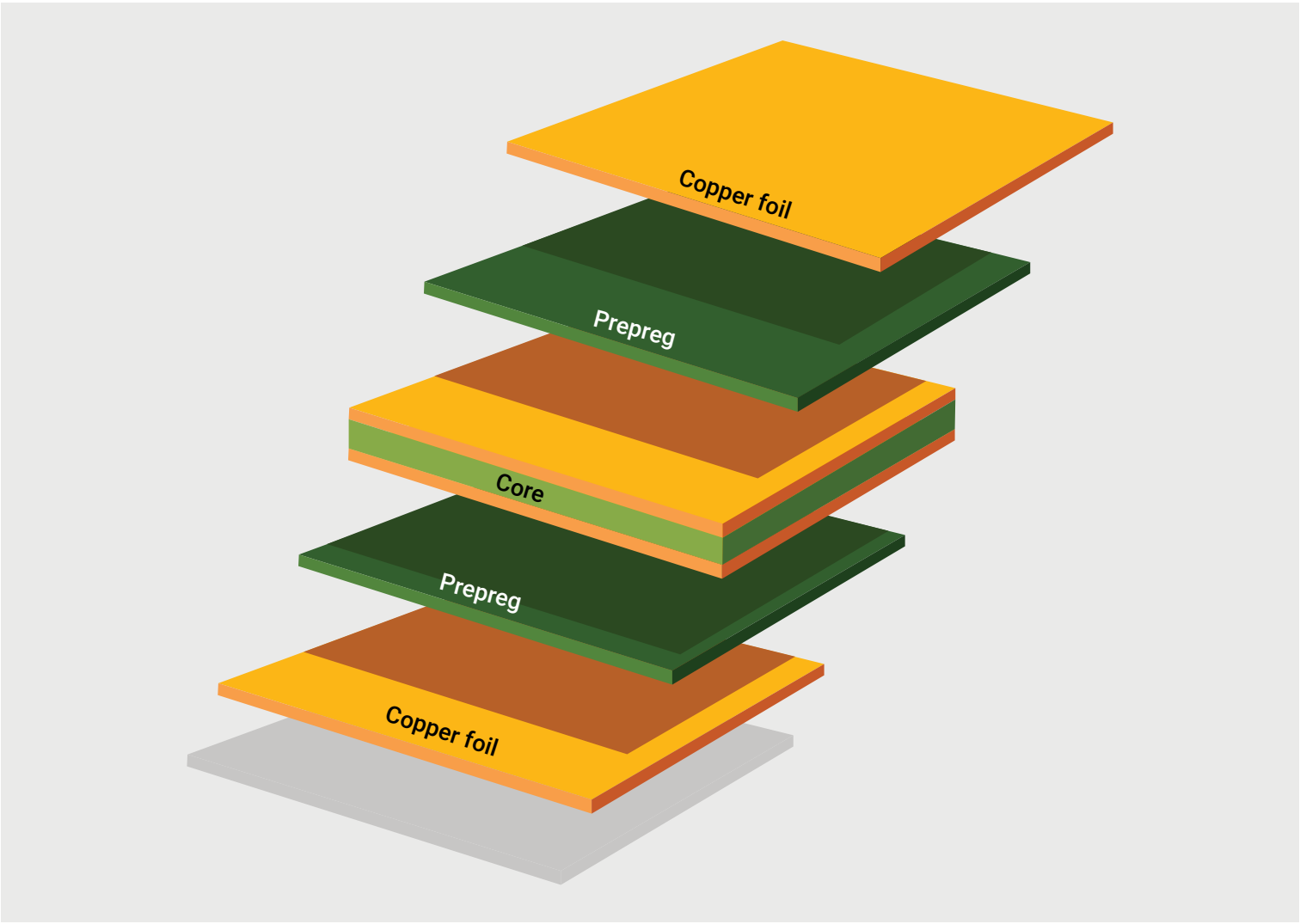


1. What is a **PCB stack-up?**

A stack-up/build-up is a sequential arrangement of copper and dielectric layers in a PCB. It describes how the layers should be arranged and provides information to the fabricator regarding material thickness, copper weights, type of prepregs to be used, overall board thickness, etc. A well-planned layer stack has lower EMI, improved signal integrity, and cost efficiency.

When you create a stack-up you need to mention:

1. Type of construction foil
2. Thickness of core and prepregs
3. Copper weight
4. Controlled impedance requirements
5. Types of layers (signal/power/ground)
6. Layer arrangement

2. What are the different layers of a PCB?

Copper foil, prepreg, and core are commonly used materials in a PCB stack-up.

2.1 Copper foil

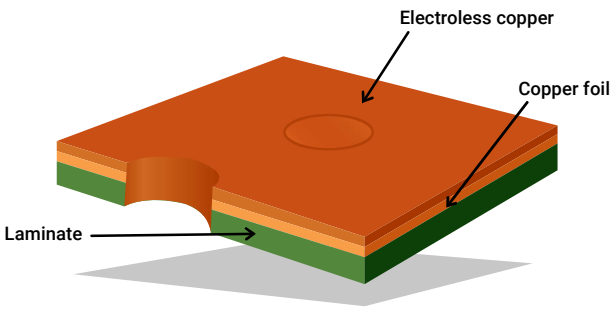
Copper layers are used to create the circuit art work such as traces, pads, and copper. This metal offers excellent electrical conductivity and eases the etching process. The thickness of the copper foil can vary depending on the specific design requirements, and it is typically measured in ounces.

For instance, if we flatten 1 ounce (28.35 grams) of copper to cover a surface area of 1 square foot (0.093 square meters), the resulting thickness would be 1.4 mils. Hence, copper weight is expressed in ounces per square foot (oz/ft²). The table below shows the relationship between copper weight and copper thickness in mils.

Copper weight (oz)	Copper thickness (mil)
1	1.4
2	2.8
3	4.2
4	5.6

2.1.1 Impact of copper foil on circuit board functionality

- Copper layer creates the desired circuitry to carry signals across the board. Due to its high conductivity, copper makes it an ideal material for this purpose. It also establishes robust interconnects between the layers, ensuring the smooth and efficient transmission of electrical signals.
- The presence of copper enhances the efficiency of power supplies, leading to more reliable and stable operation. It effectively reduces ground line impedance and voltage drop, resulting in decreased noise levels.
- In high heat-generating circuits, the copper layers (copper pours) effectively dissipate heat and prevent components from overheating.



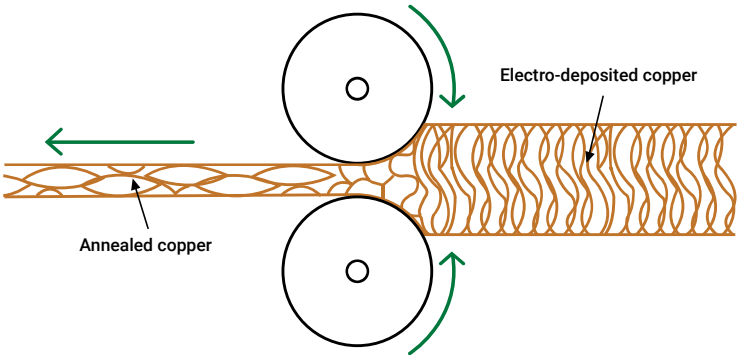
2.1.2 Different types of copper foil

Electro-deposited copper:

This type of copper does not have a smooth surface as it has a vertical grain structure. It is commonly used on rigid PCBs.

Rolled copper:

Here, the copper is made thin by placing it between heavy rollers (as shown in the image below). It is used in the production of flexible and high-speed boards. This copper has a horizontal grain structure and a smoother surface, which makes it ideal for flex circuit boards.



Rolled annealed copper

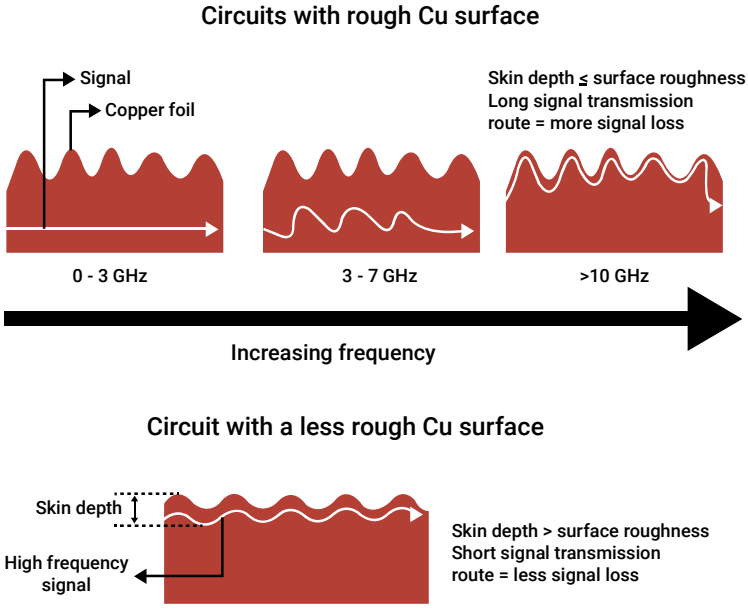
2.1.3 Selection of copper foil

The choice of copper foil mainly depends on the required copper thickness, copper purity, and copper-dielectric interface profile.

Copper thickness: The typical thickness ranges from 0.25 oz (0.3 mils) to 5 oz (7 mils). The specific copper thickness varies according to the application. For instance, if your board requires high power, you need a large copper area to support the required current.

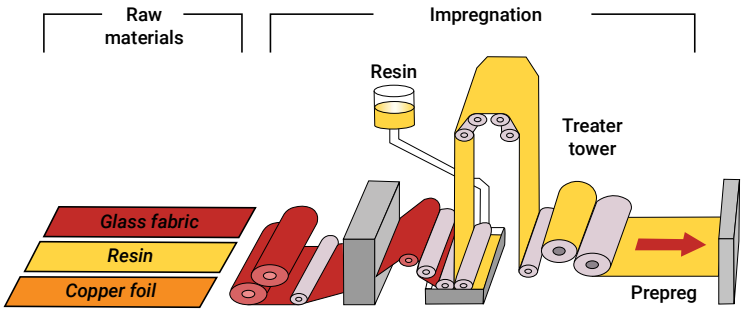
Copper purity: This refers to the percentage of copper present in a copper foil. Normally, electronic-grade copper foil will have a purity of around 99.7%.

Copper-dielectric interface profile: Low-profile (smooth surface) copper exhibits lower signal losses at high frequencies due to reduced skin effect. Therefore, it is recommended to opt for low-profile copper for high-frequency applications.



2.2 Prepreg

Prepreg, short for pre-impregnated, refers to a material composed of resin and reinforcing fibers (such as fiberglass or aramid). These are B-stage materials commonly used as an insulating layer between copper layers of a multilayer PCB stack-up. Generally, the materials used to impregnate the dielectric include epoxy-based materials or partially curedpolyimides.



Impregnation of prepreg

2.2.1 Function of prepregs

Prepreg serves as the insulation material that binds adjacent cores or cores and layers in a stack-up. Its primary functions include providing insulation, binding core layers together, and protecting the board from short circuits.

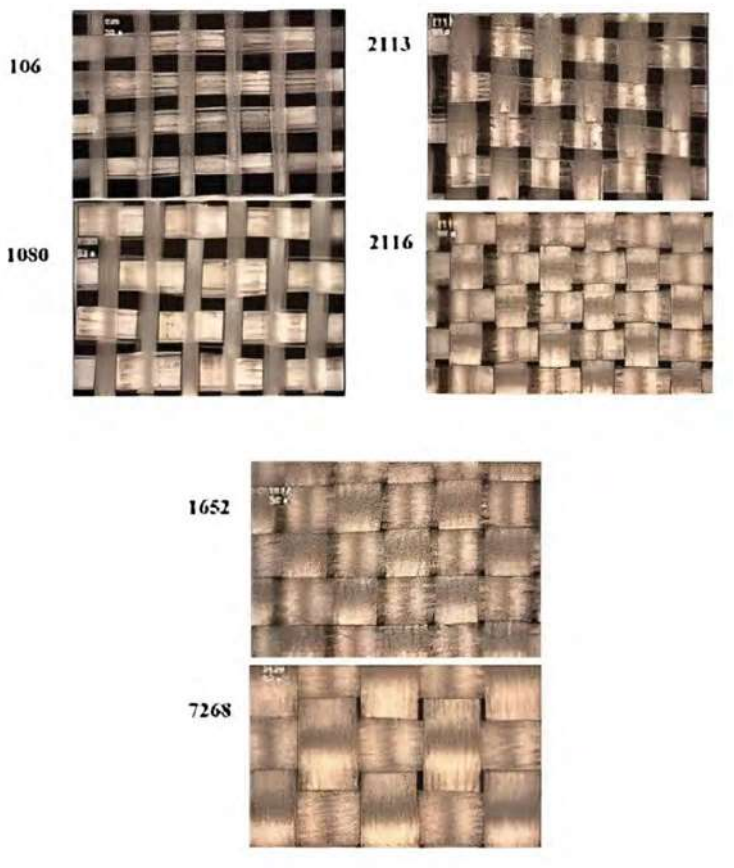
During the manufacturing process, prepreg sheets and core are layered in the PCB stack-up. Once all the layers are properly arranged, the stack-up goes through a high-temperature and high-pressure press. During this process, the prepreg softens and flows throughout the circuit board.

2.2.2 Types of prepregs

There are three main types of prepreg, categorized based on the resin content:

- High resin (HR)
- Medium resin (MR)
- Standard resin (SR)

The resin content is a critical component that significantly impacts both the final thickness and the dielectric constant. Manufacturers carefully consider these subtle variations in dielectric constants caused by resin content when modeling trace impedance.



Fiberglass weave with resin in prepreg

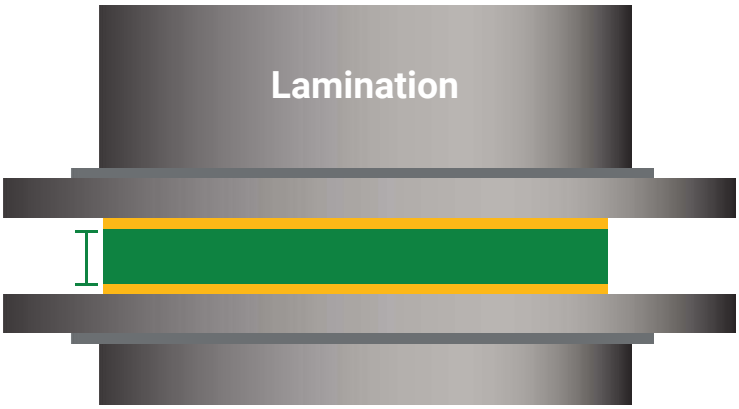
Below are the thickness and dielectric constant values for the generic prepreg glass styles of Isola 370HR material:

Prepreg style	Resin content	Nominal thickness (100% copper)	DK at 5-10 GHz
106	71%	2 mil	3.63
106	76%	2.4 mil	3.54
1067	70%	2.3 mil	3.65
1067	75%	2.7 mil	3.56
1086	63%	3 mil	3.78
1080	66%	3 mil	3.72
1080	68%	3.2 mil	3.68
1080	71%	3.6 mil	3.63
2113	59%	4.0 mil	3.86
2116	56%	4.8 mil	3.92

2.2.3 Resin flow process

Resin flow in prepreg refers to the phenomenon where the resin within the material liquefies and oozes out. This process is essential for proper lamination. The pressure applied, and the heating rate directly influences the extent of resin flow. The resin remains in a fluid state for only a limited duration, after which it turns into a gel.

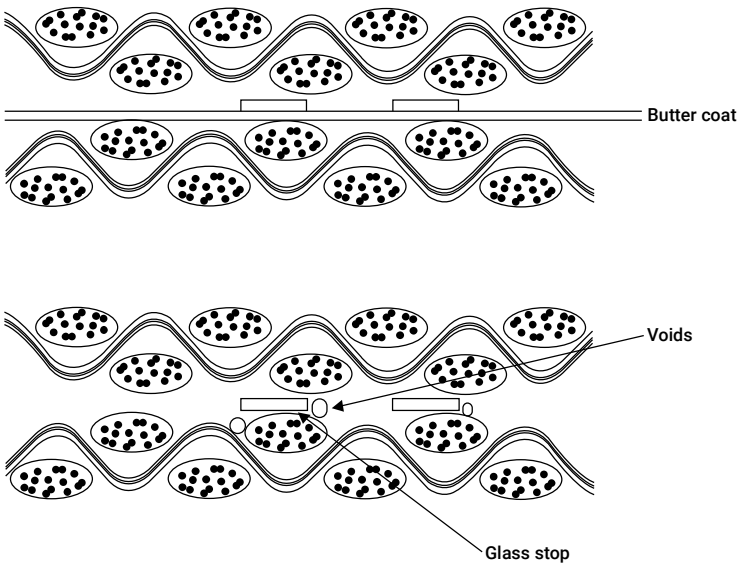
The extent of resin flow affects important properties such as the interlaminar bond strength and bond between the copper foil and prepreg. It also impacts the overall effectiveness of the prepreg as a bonding sheet.



PCB lamination under high temperature and pressure

2.2.4 Resin starvation

It is a condition where there is an inadequate amount of resin within the prepreg material during the lamination process. It occurs when the resin content in the prepreg is insufficient to fully impregnate the fiberglass or fabric reinforcement. This can lead to several issues on your PCB, such as incomplete bonding between layers, reduced mechanical strength, and compromised electrical performance.



Voids created due to resin starvation

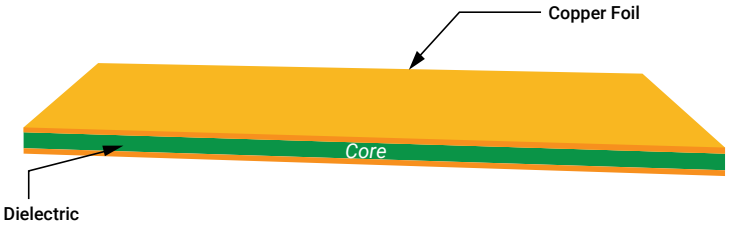
Further, resin starvation can also result in the creation of voids, air pockets, or incomplete filling of gaps between layers. This will cause poor adhesion and weak interlayer connections, resulting in poor structural integrity and reliability of the circuit board.

Resin starvation occurs due to improper resin-to-fiber ratio, inadequate resin flow, improper pressure and temperature conditions during lamination, and the use of prepreg with low resin content. It can also happen when you store the prepreg for an extended period, causing the resin to evaporate and degrade.

It is essential to use prepreg with the appropriate resin content for a specific application to prevent resin starvation. Fab houses normally perform tests and evaluations to determine the optimal resin-to-fiber ratio and ensure proper resin impregnation in the prepreg material.

2.3 Copper clad laminate (core)

The core consists of an insulating material like FR-4 with copper foil laminated on both sides. Generally, these make up the inner layers of a PCB.



Copper core laminate

2.3.1 Different types of laminates used in cores

Here are some options for laminates that are used to create high-quality copper clad laminates:

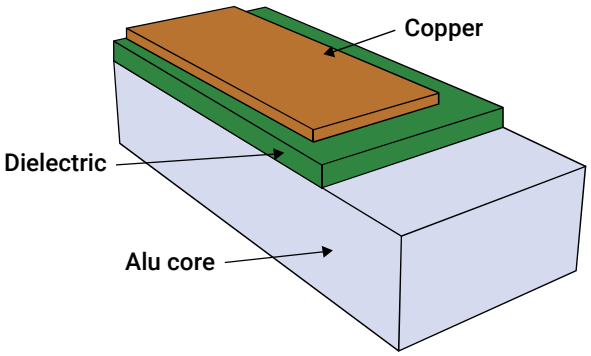
Epoxy glass fiber cloth substrate: Also known as glass epoxy copper clad boards, these laminates consist of a reinforcement layer made of electronic glass fiber cloth and an adhesive layer of epoxy resin. Key properties include:

- CTE ranging up to 55 ppm/˚C before Tg and up to 285 ppm/˚C after Tg
- UL-94V0 flammability rating
- Thermal conductivity up to 0.8 w/mK
- Dielectric constant of approximately 4.7 at 1 MHz
- Low moisture absorption rate

Paper substrate: Epoxy paper or phenolic paper is used as a substrate in copper clad laminates. The epoxy variant provides better mechanical and electrical characteristics compared to FR-4 laminates. The phenolic paper laminates are more cost-effective.

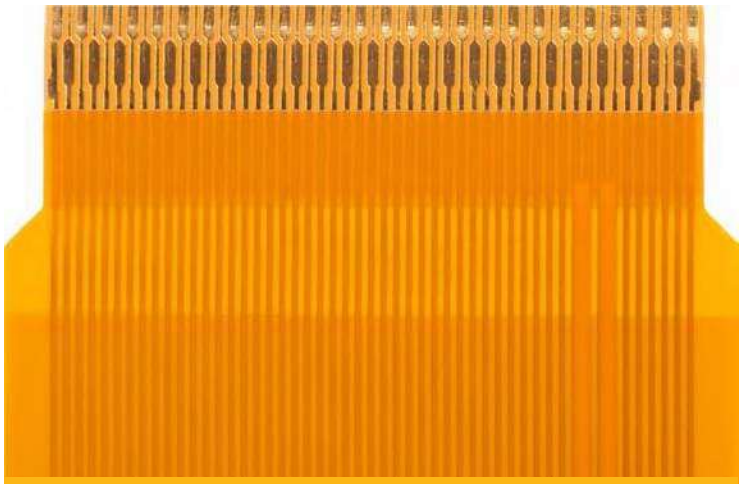
Metal base copper clad laminates: Here, aluminum is used as the base metal, which provides excellent heat dissipation and thermal conductivity. This type of laminate will have a circuit layer for higher current, a metal base for thermal conductivity, and an insulation layer that transfers heat from the copper layer to metal layer.

These substrates are for improved power output and heat dissipation. They are extensively used in hybrid integrated circuits and high-current equipment.



Metal core laminate

Polyimide (PI) flexible copper laminates: It is composed of heat-resistant, high-molecular organic polymers. Hence, they are flexible, allowing the board to fold or bend. They are also thin, lightweight, and have excellent heat resistance.



Polyimide laminate

2.3.2 Selection of core

When selecting a copper clad laminate, you need to consider its chemical composition, electrical performance, and physical attributes.

Consider the following guidelines when you select a core:

- Bending strength and peel strength (PS) of the laminates should match your application. Other physical characteristics to consider heat resistance under thermal stresses like T288, Td, and T300.
- The laminates should meet standard specifications for dimensional stability, resistance to chemical agents, flammability, and glass transition (Tg) temperature. The values depend on the type of application.
- Dk and Df values should be less than 4 for high-speed applications.
- Evaluate the water resistance rate and its ability to resist corrosion. This is crucial if your board operates in a harsh environment.

2.4 Difference between core and prepreg

The core consists of cured prepregs that are bonded to the copper foil on both sides. Therefore, the dielectric thickness of the core remains unchanged after lamination. However, prepregs, which are semi-cured materials, undergo changes in thickness after the lamination process.

Prepreg thickness before and after the lamination process

The final thickness of a prepreg material is influenced by factors such as the percentage of copper in the adjacent conducting layers and the type of prepreg employed. After the lamination process, semi-cured prepregs are transformed into fully-cured dielectric materials.

Fab houses maintain a high level of process control and integrity throughout the lamination process to ensure predictable post-lamination thicknesses. This is crucial to maintain the mechanical integrity of copper conductors.

2.5 Dielectric properties

Allan Knox, Senior PCB Design Engineer at Sierra Circuits, explains, **"Choosing the right laminate is a crucial part of stack-up preparation, as everything starts with that. It determines your signal losses, clock settings, heat management, and power handling capabilities."**

Below are the key factors to consider when choosing dielectric materials for your stack-up.

2.5.1 Electrical properties: Dk, Df

Dielectric constant (Dk): It indicates the material's ability to store electrical energy.
Typical Dk values range between 2.5 and 4.5. Dk is not consistent throughout the material and the values mentioned in the datasheet are average values. Dielectric constant is crucial for impedance control and signal integrity. Lower the Dk, lower the signal losses. Dk of 370-HR and Rogers 4350B are given in the below table.

Materials	DK
370 HR (FR-4)	3.92
Rogers 4350B	3.48

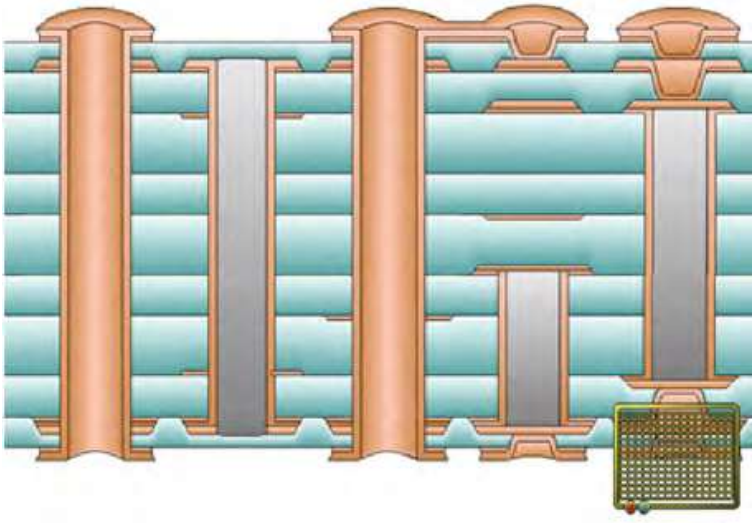
Dissipation factor (Df): It is also known as loss tangent (tan δ) and represents the tangent of the phase angle between resistive and reactive currents in the dielectric. Generally, Df values range from **0.001 to 0.030**.
Higher Df values result in greater dielectric loss.

Materials	Df
370 HR (FR-4)	0.0250
Rogers 4350B	0.0037

2.5.2 Thermal properties: CTE, Tg, Td, k

Coefficient of thermal expansion (CTE): CTE measures the change in size of an object with temperature variation. It is typically expressed in parts per million per degree Celsius. CTE is crucial during stack-up preparation as PCB materials undergo heating.

The CTE values along the X and Y axes are generally low, ranging from **10 to 20 ppm/°C**. This is due to the presence of woven glass which restricts the material's movement in the X and Y directions.



Material expansion and contraction during lamination

Even as the temperature rises beyond Tg, the CTE remains relatively stable in these directions. Therefore, the material expends in the Z direction.

It is preferable to have a low CTE along the Z-axis, ideally less than **70 ppm/°C**. However, as the material surpasses Tg, this value tends to increase. Therefore, monitoring the CTE along the Z-axis becomes crucial.

Materials	CTE (X-axis)	CTE (Y-axis)	CTE (Z-axis)
370 HR (FR-4)	13 ppm/°C	14 ppm/°C	14 ppm/°C
Rogers 4350B	10 ppm/°C	12 ppm/°C	32 ppm/°C

Glass transition temperature (Tg): Tg is the temperature at which a substrate transitions from a rigid to a molten state. Beyond Tg, the CTE value increases significantly. Tg is expressed in degrees Celsius.

Materials	Tg
370 HR (FR-4)	180°C
Rogers 4350B	280°C

Decomposition temperature (Td): Similar to Tg, Td refers to the temperature at which a substrate chemically decomposes. Decomposition temperature is expressed in degrees Celsius.

Materials	Td
370 HR (FR-4)	340°C
Rogers 4350B	390°C

Thermal conductivity (k): Thermal conductivity represents the rate at which heat dissipates from the substrate during its operation. It is measured in Watts per meter of Kelvin. A lower thermal conductivity value implies lower heat transfer, while a higher value indicates higher heat transfer. Thermal conductivity plays a crucial role in the thermal management of a circuit board and affects the temperature rise with respect to ambient temperature.

Materials	k
370 HR (FR-4)	0.4 W/mk
Rogers 4350B	0.69 W/mk

2.5.3 Chemical properties: moisture absorption, flame resistance

Moisture absorption: Dielectric materials should have low moisture absorption to prevent the absorption of moisture from the

environment. Moisture absorption can lead to changes in electrical properties, dimensional instability, and potential reliability issues.

Materials	Moisture absorption
370 HR (FR-4)	0.15%
Rogers 4350B	0.06%

Flame resistance: PCB dielectrics are often required to meet flame retardant standards to ensure safety in case of fire or high-temperature situations. Flame-resistant properties help prevent the spread of fire and minimize the release of toxic gases. Substrates are tested as per UL standards.

2.5.4 Mechanical properties: tensile strength, flexural strength

Tensile strength: Tensile strength measures the maximum stress a material can withstand before it breaks under tension. PCB dielectrics should have adequate tensile strength to withstand the forces exerted during PCB manufacturing processes such as drilling, lamination, and component mounting.

Materials	Tensile strength (length direction)	Tensile strength (length direction)
370 HR (FR-4)	55.9 ksi	35.6 ksi
Rogers 4350B	29.5 ksi	18.9 ksi

Flexural strength: Flexural strength refers to the ability of a material to withstand bending or flexing without breaking. PCB dielectrics should possess suitable flexural strength to withstand bending forces encountered during PCB handling, assembly, and operation.

Materials	Flexural strength
370 HR (FR-4)	90 ksi
Rogers 4350B	77 ksi

Stick to these guidelines when choosing dielectric materials for your PCB:

- If your design requires different kinds of materials, make sure their CTE values are equivalent. If you have substrates with different CTEs, they may expand at varying rates during the lamination process.
- For high-speed applications, select substrates with flatter and tighter weaves.

- This helps ensure a more uniform distribution of Dk.
- Avoid using FR-4 for high-frequency applications due to its high dielectric loss and the steep Dk versus frequency response curve.

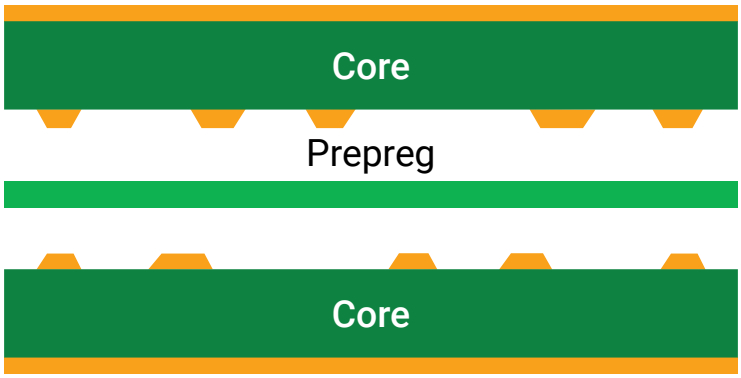
Use our material selector to choose a material that best fits your design requirements.

3. Stack-up construction

The choice between core and foil construction depends on various factors like specific design requirements, performance needs, and manufacturing cost considerations.

3.1 Core construction: Core construction is the method of building multi-layer circuit boards by using pre-made core layers. Generally, cores are rigid laminates such as FR-4 or high-speed materials.

In the core construction process, the core layers are printed with circuit layouts, etched to remove excess copper, and then bonded together using prepreg material. Here, prepreg acts as an adhesive between two core layers. The prepreg is cured using heat and pressure to create a solid multilayer circuit board. This type of four-layer (or more) stack-up is referred to as a "core build," with core material used on the outer layers.



Example of core construction

Typically, core construction is rarely used. It is mostly implemented in microwave hybrid stack-up, where low-loss laminates are stacked with low-cost laminates to achieve better performance and price.

One of the limitations of core construction is the thickness of the core and copper. The cores come in standard thicknesses. Hence it is not possible to build a stack-up with a non-standard thickness. Registration of layers is also a concern with core construction in multi-layer circuits with tight annular rings and drill-to-copper parameters.

3.2 Foil construction

Here, individual copper foil sheets and prepreg layers are laminated together sequentially with cores to create the desired stack-up.

Illustration of foil construction

This method allows more flexibility in creating different combinations of copper and prepreg thicknesses. In addition, foil construction allows you to add blind buried vias. They can be customized for specific impedance control and other design requirements. This method involves multiple press cycles to laminate the layers together and ensure proper bonding.

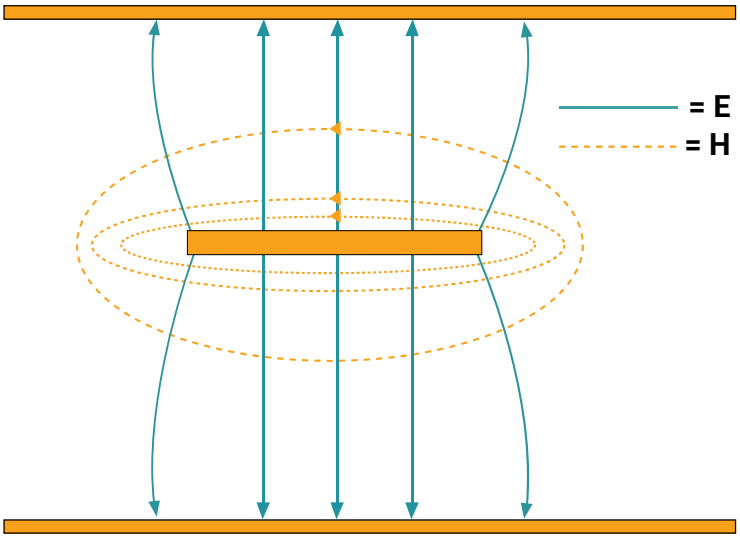
4.Impact of the stack-up on PCB functionalities

The Stack-up impacts multiple characteristics of the PCB, such as signal integrity, power distribution, and thermal management.

4.1 Signal integrity

Ensuring proper signal integrity is crucial for reliable circuit operation. Factors such as controlled impedance and managing transmission line effects should be taken into account during the stack-up design.

The main causes of signal integrity issues such as EMI, crosstalk, and signal reflection are improper grounding and trace spacing. PCB stack-up design plays a crucial role in the ground plane arrangement as well as providing spacing for routing. If the stack-up is properly planned from the initial stage, then the signal integrity problems can be reduced as much as possible.



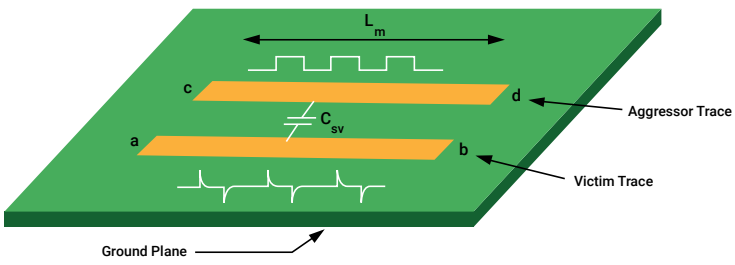
EMI generated between two fields

The stack-up determines the proximity and reference planes for signal return paths. Proper allocation of ground and power planes adjacent to signal layers helps create low-impedance return paths.

Further, to minimize EMI and susceptibility, the stack-up should include proper shielding and isolation techniques. Careful placement of sensitive components and routing of high-speed signals can help reduce EMI.

Similarly, when two traces are placed too close, instead of the energy flowing to the ground, it will couple with the secondary trace and cause a crosstalk between the signals. Crosstalk can happen between the traces placed in two different layers.

The spacing and placement of signal layers in the stack-up impact crosstalk between adjacent traces. A well-designed stack-up with appropriate spacing and signal-to-ground plane arrangements helps reduce capacitive and inductive coupling between traces, minimizing crosstalk and preserving signal integrity.

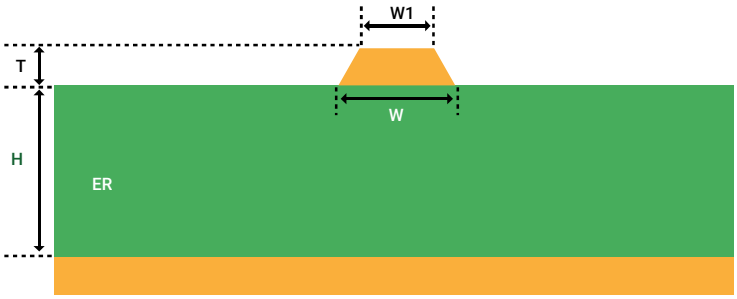


Crosstalk between two closely placed traces

If these concerns are not considered, it can lead to reworking or replacing the entire PCB.

4.2 Controlled impedance

The impedance of traces is determined by various parameters, including trace width, trace thickness, trace height from the ground plane, and material dielectric properties. Controlled impedance can be achieved through two approaches:



Controlled impedance of a trace

Controlled dielectric thickness: In this method, the designer specifies the desired dielectric thickness to the manufacturer. The focus during manufacturing is to build a board that maintains a tolerance of +/- 10% for the specified dielectric thickness from layer to layer. Impedance traces are not explicitly specified in this approach.

Impedance control: You can control the impedance by altering the dielectric thickness, trace width, and spacing. The manufacturer conducts tests using time-domain reflectometry (TDR) coupons to verify that the desired impedance can be achieved. Based on the results, adjustments are made to meet the designer's requirements. the fab house also ensures that the boards are manufactured within the specified tolerance.

Below are a few considerations that should be considered to achieve the targeted impedance:

- Limit the use of more than three different types of prepregs in the stack-up. Additionally, the dielectric thickness of each prepreg layer should be less than 10 mil to minimize variation in the final thickness.
- When multiple dielectric materials with different Dk values are placed between the signal layer and ground, it is essential to consider the effective dielectric constant of the composite material. This can be done by calculating the weighted average of the dielectric constants.

$$\text{Dk effective} = \frac{\text{Type 1: (thickness of material) x (Dk value)} + \text{Type 2: (thickness of material) x (Dk value)}}{\text{(thickness of material type 1+ type 2)}}$$

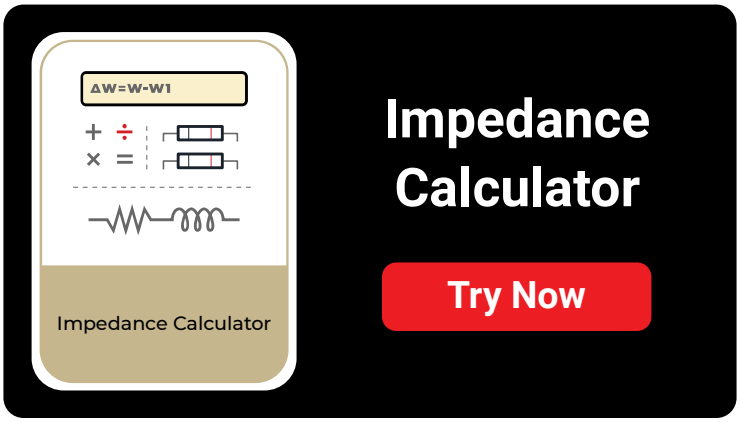
Consider the below example of 370 HR:

Signal layer	———	Foil
Prepreg	≈≈≈	2 x 106 (type of prepreg)
Core	▭	8 mil
Reference layer	———	

Thickness in mil	Dk value
2 x 2.3 = 4.6	3.22
1 x 8 = 8	3.65

$$\text{Dk effective} = \frac{(4.6 \times 3.22) + (8 \times 3.65)}{(4.6 + 8)} = \frac{(14.812) + (29.2)}{(12.6)} = 3.49$$

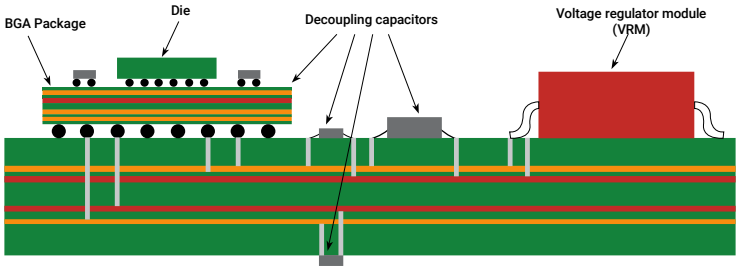
- For differential pairs, you need to keep the trace width less than twice the dielectric thickness between the target signal layer and the nearest reference layer.
- During the manufacturing process, targeted impedance is often achieved based on the actual press-out thicknesses of the prepregs rather than relying solely on the values mentioned in the data sheets. Here, the manufacturers have to consider parameters like resin content in the prepreg and the area and thickness of copper on opposing layers.



4.3 Power integrity

Efficient power distribution and management are critical to maintain steady voltage levels and minimizing noise interference. The stack-up should include dedicated power and ground planes to minimize power plane impedance and reduce power noise.

Implementing decoupling capacitors, sufficient power plane thickness, and low-inductance power delivery paths is critical for maintaining a stable power supply, reducing voltage drops, and minimizing simultaneous switching noise (SSN).



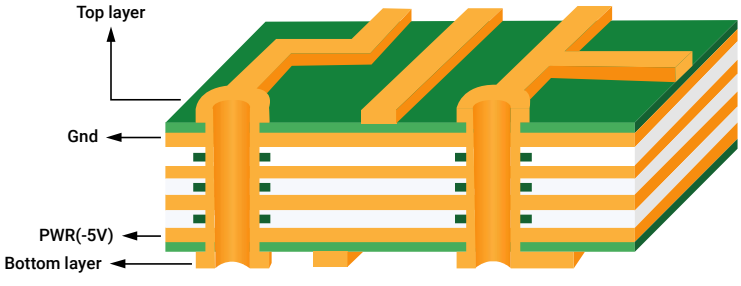
Implementing decoupling capacitors for better power integrity

5. Designing an efficient stack-up

The first step in designing the stack-up is understanding your circuit requirements and ensuring that the design stack-up is manufacturable. Each layer within a stack-up serves a unique purpose that influences the electrical characteristics of a circuit board.

Any PCB stack-up has three essential tasks to fulfill: providing power distribution, establishing ground reference planes, and creating traces for signal propagation. If the stack-up is designed without understanding the layer count requirement and its configuration, it will increase the risk of PCB functionality issues or failure.

5.1 Different types of layers in a stack-up



Different types of layers in a stack-up

5.1.1 Signal layers

These layers carry the electrical signals and traces that connect the components on the PCB. Normally, signal layers are dedicated to routing the signal traces and are sandwiched between the power and ground planes.

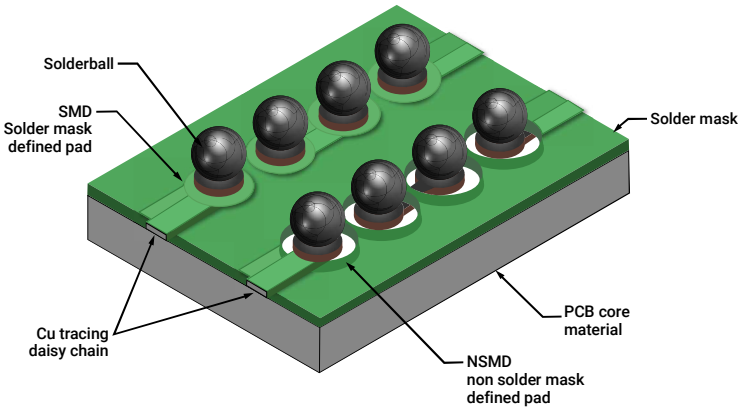
5.1.2 Power and ground layers

These are copper planes that are used to provide a stable power distribution network and serve as return paths for the signals. Additionally, they also help to minimize the DC resistance in the PDN, resulting in fewer voltage drops across devices.

By assigning a solid ground and power plane, you will have the opportunity to dedicate specific signal layers solely for routing signals. They also help to reduce noise, improve signal integrity, and provide a low-impedance path for current flow.

5.1.3 Soldermask and silkscreen layers

Soldermask is applied over the top and bottom of the PCB surface to protect the copper traces and also provide insulation. During the soldering process, they improve component placement accuracy and prevent solder bridging.



Solder mask application

A silkscreen layer is printed over the circuit board with text, symbols, and markings. They contain information such as reference designators, logos, assembly instructions, and other relevant information to aid the assembly process.

When representing the stack-up, you have to specify the material, color, and thickness of the solder mask and silkscreen layers.

5.2 Estimating the number of signal layers

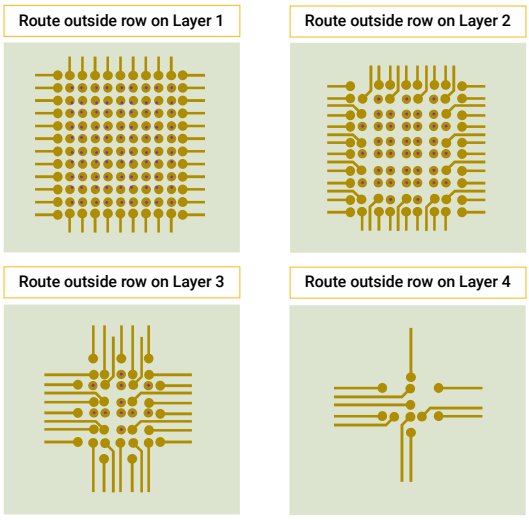
Estimating the layer count of stack-up impacts the electrical and mechanical properties of the circuit board. While deciding the number of layers, it is important to consider the signal integrity and power integrity aspects. Additionally, an increased number of layers will affect both turnaround time and cost considerations.

5.2.1 Factors that affect the layer count estimation

Even though this process is based on different application requirements, here are some general rules to follow:

- Ensure that you have sufficient space for placing all the components and the trace to route them.
- When the board dimensions get smaller, the number of signal layers increases to accommodate components and traces.
- As the BGA pin density increases, the number of layers increases.
- At least have one power layer when the circuit requires a high current for operation.
- Have enough layers to segregate and isolate the digital system, analog system, or mixed-signal circuits.
- If possible, add interleaved ground planes for every signal plane.

- Consider thermal management. An increased number of copper layers offers better heat dissipation. For instance, a multilayer board with a higher number of copper layers cools faster than a double-layered board.
- Increase the number of layers in high-speed circuits to provide proper isolation.
- For sensitive signal traces, plan to route them in a stripline configuration with ground planes on both sides for better signal integrity.
- Round up the overall layer count to an even number to maintain symmetry.
- An increased number of layers increases the final board thickness. Ensure that it remains within the minimum required limit.



BGA routing on different layers of a PCB

5.2.2 Example: Layer count estimation with a BGA

Here is an example of layer estimation considering a board with a 225-pin BGA (15 pins per row or column). By assuming that it does not have a fine pitch, you can calculate the number of layers as follows:

Signal layers = (0.5 x BGA rows) - 2

Signal layers = (0.5 x 15)-2 = 5.5 layers (even out to 6 layers)

To route this BGA, you need six signal layers. However, as most of the ICs have ground and power pins, you may not require these many signal layers. Next, you need to add alternative ground plane layers to maintain sufficient return paths.

Hence, you require five ground planes. Finally, one power layer must be added to connect all the power rails. Therefore, you will end up with a 12-layer PCB.

This is just an example; based on your application requirements, you may not need this many layers. A popular choice for PCB stack-ups is the 4-layer configuration, as it offers excellent support for high-speed, high-frequency, and mixed-signal designs, even with a reasonable component density. In cases where the signal count increases significantly, a 6-layer PCB can be suitable for many products.

Estimating the appropriate layer count is a crucial step toward achieving a successful design. As demonstrated in this section, multiple factors influence the determination of the number of layers in a circuit board.

This calculation can sometimes be difficult and time-consuming. You can use Sierra Circuits' Signal and Plane Layer Estimator tool to estimate the required layer count. It uses multiple algorithms to calculate the minimum number of layers required to accomplish all the interconnections in a PCB layout.

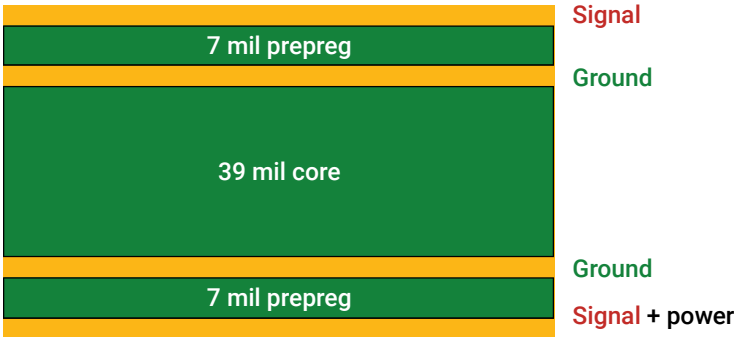
Its features include:

- Calculates the minimum number of signal and plane layers required to route all interconnections.
- Considers board dimension, component density, wiring channel width, via-in-pad, and trace width/space.
- Determines the optimum PCB area, number of nets, and net density.

5.3 Layer arrangement guidelines for a PCB

5.3.1 Add interleaved ground planes

As mentioned above, a proper return path is essential to minimize signal integrity issues. Hence, place dedicated ground planes across signal layers whenever possible. The ground planes should be continuous and cover as much area as possible to ensure effective shielding and reduce EMI in your PCB design.



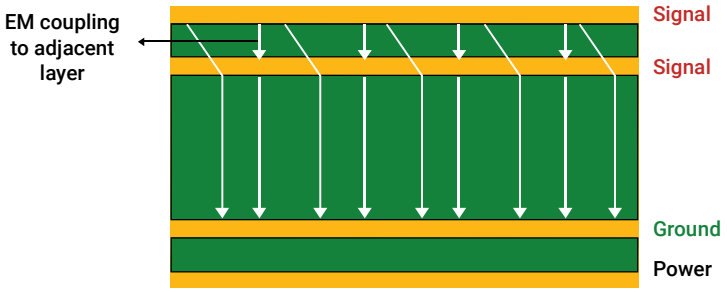
Ground plane arrangement in a stack-up

5.3.2 Use multiple power planes

Allocate separate power planes for different power domains, such as analog and digital. This helps prevent noise coupling between different power domains and reduces the risk of voltage fluctuations. Ensure adequate decoupling capacitors are placed near power pins to maintain stable power distribution.

5.3.3 Avoid placing adjacent signal layers

Avoid placing adjacent signal layers, as the EM fields from the two layers can get coupled and create common mode noise. Consider the stack-up in the below image. Here, When the EM field from layer 1 passes through layer 2 to reach the reference plane on layer 3, it gets coupled with the layer 2 EM field. This coupling can induce a common mode current, which leads to EMI.

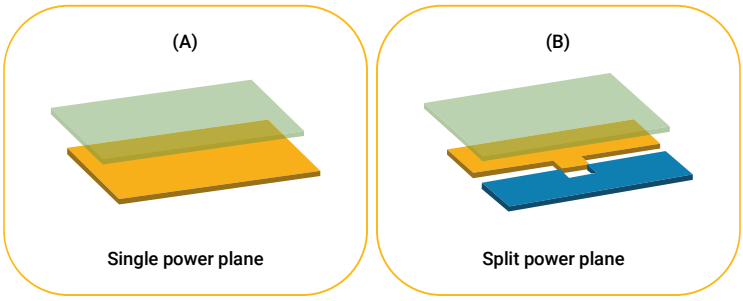


Cross-coupling in adjacent signal layers

One of the ways to reduce EMI is by routing traces orthogonally on the two layers. You can also add copper pour or ground lines on layer 1 to provide a different reference point.

5.3.4 Try not to add splits in the power plane

Using power planes as a signal reference can lead to splits in them. These splits can create impedance discontinuities, especially if there are significant differences in power levels at each end of the split. Routing signals over such splits can result in signal integrity issues.



Split in the power plane

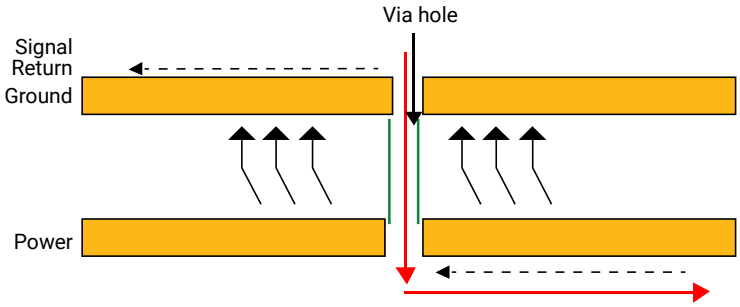
In high-speed designs, splits in the power plane can generate spikes that cause ground bounce and undesired voltage drops. These phenomena can further compromise signal integrity and lead to performance issues.

5.3.5 Place ground planes next to power planes

The close placement of power and ground planes contributes to improved signal integrity, reduced noise, and enhanced overall performance of the PCB design.

- Placing the power and ground planes in proximity (8 to 10 mil) creates a high-frequency capacitor effect. This arrangement establishes a low-impedance distribution network for power and ground connections throughout the PCB.

By keeping the power and ground planes close together, you can minimize EMI when signals transition between different layers. This proximity reduces the loop area and provides a more efficient return path for the signal currents.



Signal transition between coupled ground and power plane

5.3.6 More rules on layer arrangement

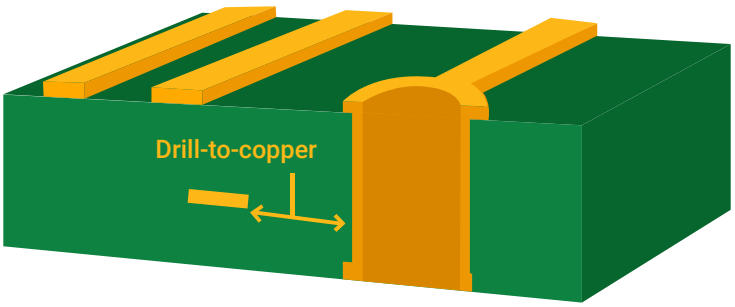
The close placement of power and ground planes contributes to improved signal integrity, reduced noise, and enhanced overall performance of the PCB design.

- Place two adjacent power planes as far apart as possible to avoid unwanted coupling. Add a reference plane near both power planes to give a low inductance path.
- Do not route the signal layer between ground and power, as it creates coupling issues.
- Aim for a balanced and symmetrical stack-up whenever possible. This helps maintain mechanical stability, reduces warping, and ensures uniform thermal expansion. Balance the copper weight between the signal layer and ground/power layer across the stack-up.

5.4 Via placement and layer transitions

Vias are the vertical interconnections that connect different layers in a stack-up. It is common to use plated through-hole (PTH) as vias.

Via type, drill size, hole placement, and annular ring size greatly impact the way you design a PCB build-up. For instance, during the sub-lamination process, you need to have larger annular rings (connections between trace and via) to reduce the risk of registration issues and maintain a good drill-to-copper distance.



Drill-to-copper distance

5.4.1 Via placement rules

Remember that specific via placement rules may vary depending on the design requirements, signal characteristics, manufacturing capabilities, and fabrication processes.

- In designs where thermal management is crucial, thermal vias are used to transfer heat away from heat-generating components or to provide thermal relief to copper

pours. These vias should be strategically placed near the thermal pads or copper areas to facilitate effective heat dissipation.

- Follow the keep_out zones, which restrict via placement near specific components or sensitive areas to avoid interference, clearance violations, or potential short circuits.

- Vias introduce their own impedance, which can cause impedance discontinuities. Hence, when routing high-speed signals or differential pairs, minimizing the size and number of vias will reduce the impedance mismatch and improve signal integrity.

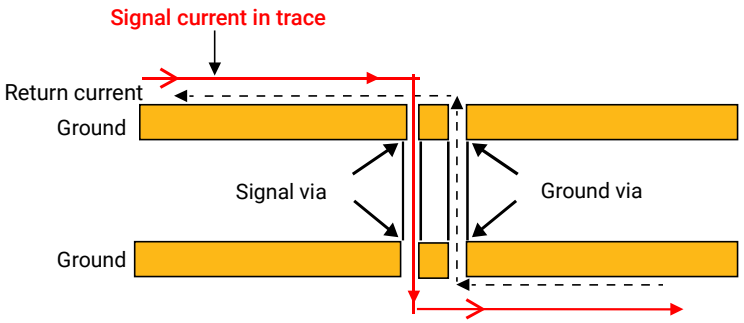
5.4.2 Via layer transition effects in a PCB stack-up

When there is a via between two reference planes, it introduces an impedance discontinuity in the signal path. The impedance mismatch can cause signal reflections and result in signal degradation, ringing, and potential signal integrity issues.

The magnitude of the impedance mismatch depends on factors such as the size and structure of the via, the dielectric materials used, and the separation between the reference planes. This also disrupts the return path for the signal current. Below are some examples of different layer transitions.

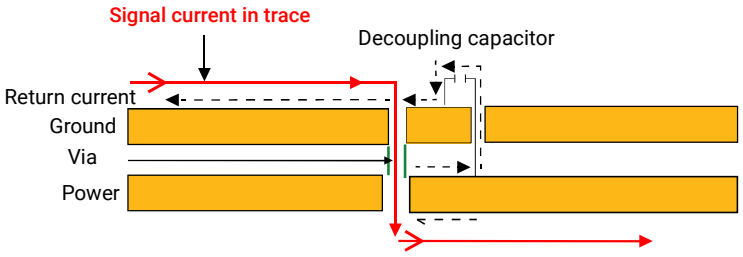
- **Case 1:** There is no issue if via transitions only one reference point (ground) and others are signal layers, as it has a clear return path.

- **Case 2:** When the via transitions between two ground planes, you need to add a ground via to create a good return path. Placing ground vias for each and every via will be ideal but not practical. Instead, you can strategically place a single ground via for multiple via connections.

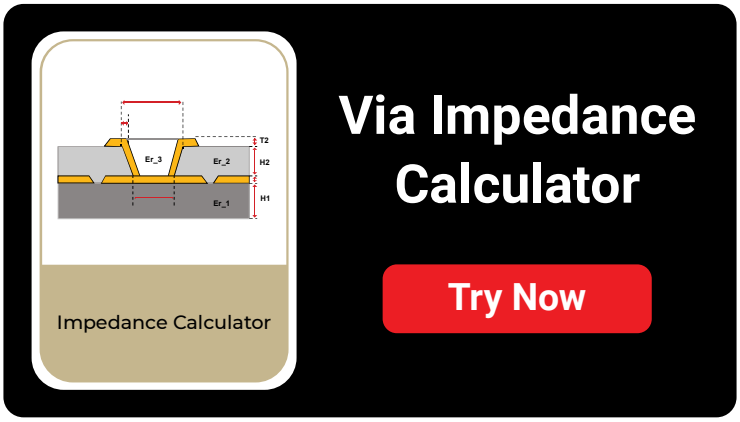


Signal transition between two ground planes

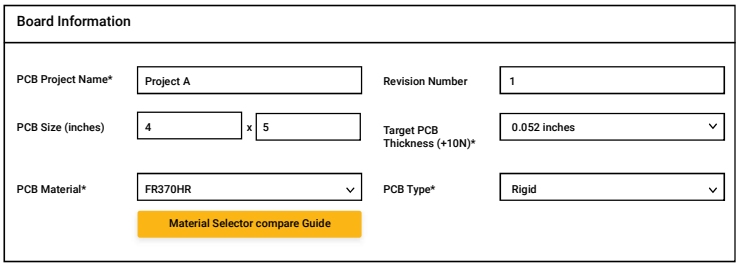
- **Case 3:** When via transitions between power and ground, the power plane can act as a reference plane. For operational frequencies below 250 MHz, you can use decoupling capacitors to improve signal propagation.

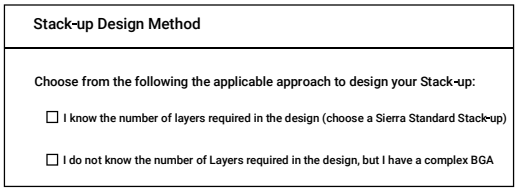


Signal transition between ground and power planes



5.5 Designing an effective stack-up using the Stackup Designer





Building a comprehensive layer stack is essential to design a successful PCB. We understand the challenges you face in achieving the right balance between cost, manufacturability and performance. To help you overcome this hurdle, we've developed the Stackup Designer, an advanced PCB design tool tailored to meet your stack-up needs.

The features of the tool include:

- **Stack-up templates based on your requirements:** Our Stackup Designer offers a library of stack-up templates, including single and sequential lamination build-ups ranging from HDI-1 to HDI-4. Whether you're working on a basic design or a complex high-density interconnect (HDI) board with multiple laminations, we've got you covered. These templates provide the foundation you need, saving you time and effort during the design phase.

- **Comprehensive material data base:** The tool comes with a material data base that includes a wide range of materials that are suitable for low-speed and high-speed designs. This ensures that your stack-up is optimized for your specific product.

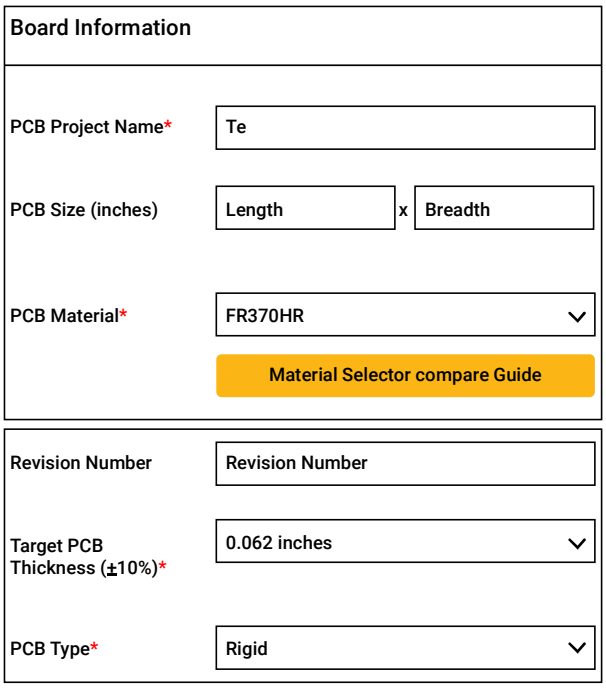
- **Simplified steps to achieve precise impedance control:** To meet the requirements of high-speed designs, the tool is linked to our 2D field solver-based impedance calculator, which allows you to design any controlled impedance traces in a go.

- **Cost index for informed decision-making:** This web application provides a cost index that offers a relative idea of the cost compared to another layer stack. This valuable feature allows you to make informed decisions, ensuring your design aligns with your budget without sacrificing the quality

5.5.1 How to use the Stackup Designer

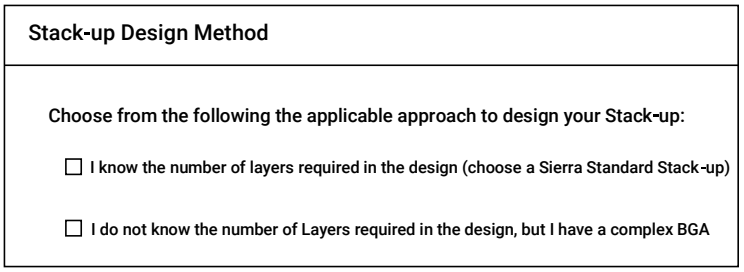
The tool has 2 input sections:

Board information:



In this section, you need to enter the project name, revision number, PCB size, target board thickness, material and board type. Click on the **material selector compare guide** to view the properties of various dielectric materials.

Stack-up design method:



After entering the board information, you can move on to the stack-up design method section. Here, you will have two options:

- I know the number of layers required in the design (Choose a Sierra Standard Stack-up)

- I do not know the number of layers required in the design, but I have a complex BGA

Choose the first option if you're aware of the number of layers in your build-up.

If you select the first option, you need to input the layer count along with the signal-plane layer combination and click on run stack-up generator.

You will be presented with Sierra Circuits' recommended solutions as shown below.

Stack-up Option	Total Layers	Signal Layers	Plane Layers	HDI/STD ⓘ	Report
Option-A	8	4	4	STD	Report
Option-B	8	4	4	HDI-0	Report
Option-C	8	4	4	HDI-1	Report
Option-D	8	4	4	HDI-2	Report
Option-E	8	4	4	HDI-3	Report

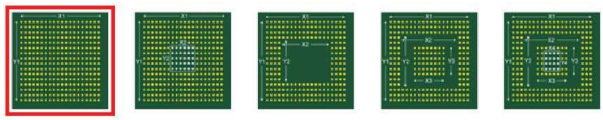
If your design has controlled impedance traces, you can use our built-in impedance calculator. This calculator allows you to add the impedance model and compute the desired trace geometry and spacing for a target impedance.

To add the impedance models, click on under the impedance calculator section and provide the following details:

- **Signal layer**
- **Target impedance**
- **Model type (single-ended/differential pair/coplanar single-ended/coplanar differential pair)**
- **Reference layers**
- **Transmission line model**
- **Trace spacing**

After providing the required impedance data, click on calculate impedance to view the required trace width, calculated impedance, and propagation delay. If you're not sure about the number of layers required in the design, and there is a complex BGA that dictates the number of layers, choose the option **I do not know the number of layers in the design, but I have a complex BGA**.

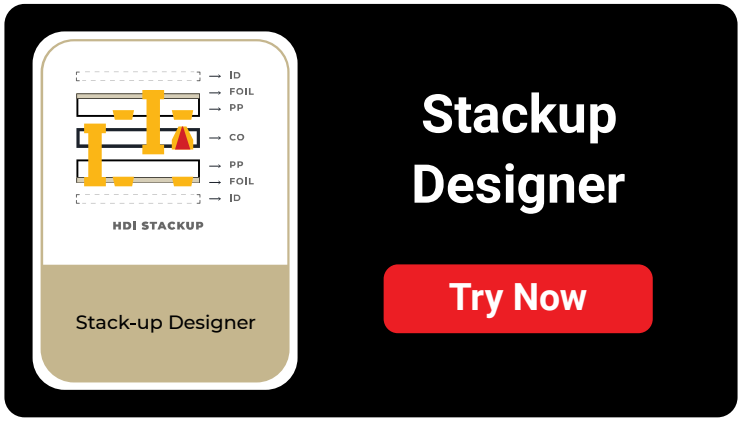
Here, you need to select the applicable BGA pattern and enter the BGA pin and pitch information. Once the required data is given, the Stackup Designer automatically calculates the total number of pins and the estimated number of signal pins. You can change the estimated number of signal pins in this section.

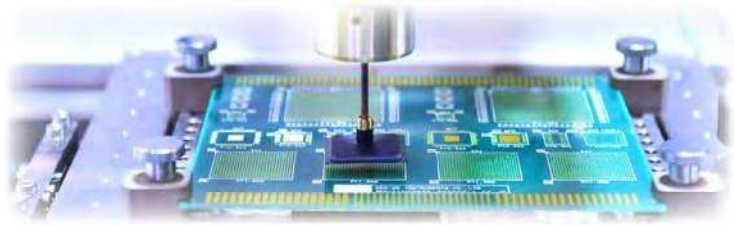


Enter Pins in	X1 Direction	Pins
Enter BGA Pitch (mm) ⓘ	Choose BGA Pitch	mm
Total number of pins		
Estimated number of signal pins	Estimated number	

After entering the BGA details, click run stack-up generator present at the bottom of the page. The tool now displays the stack-up options based on the provided input.

For a detailed demo video, visit our tool page by clicking on the banner below.





6. Different types of PCB stack-ups

There are several different types of PCB stack-ups, each designed to meet specific requirements and optimize performance for different applications. Here are some commonly used types of PCB stack-ups:

6.1 Single-sided stack-up

A single-layer stack-up consists of a copper layer on the side of the substrate with components and traces routed on them. Generally, they are implemented in simple and low-complexity circuits.

The major disadvantage is that you will have limited routing space and limited functionality compared to other types of stack-up.

6.2 Double-sided stack-up

A double-sided stack-up consists of a substrate with copper layers on either side connected by plated through holes. The circuit artwork is placed on the two copper layers. They offer more routing space and are suitable for circuits with moderate complexity.

6.3 Multilayer stack-up

A multi-layer stack-up consists of three or more copper with components and traces placed on them.

Various configurations are possible, such as 4-layer, 6-layer, 8-layer, and so on, depending on the design requirements.

They include power, ground, and signal layers. Multilayer boards have the capability to accommodate the complex circuits necessary for modern electronic devices. With multiple layers, there is more space for routing signals and providing interconnections between components. This also helps in reducing the overall size of the PCB.

These stack-ups require meticulous planning and intensive production processes.

The fabrication of multi-layer PCB stack-ups involves a single lamination cycle, resulting in reduced thermal and mechanical stress on the board. Moreover, laser drilling is not necessary, making the production process more cost-effective and faster. However, it's important to note that only through-hole vias can be implemented for interlayer connections, which may limit the utilization of space on the board.

6.4 HDI stack-up

HDI (High-Density Interconnect) circuit boards are designed to have a higher component and trace density per unit area when compared to traditional circuit boards. They incorporate features such as buried, blind, and microvias to achieve high signal performance. The benefits of HDI include:

- Reduction in the number of layers compared to traditional multi-layer boards. This helps to simplify the board structure and improve overall efficiency.
- By reducing the signal path length throughout the board, HDI technology naturally enhances signal integrity.
- Minimizes power consumption by optimizing the signal routing and reducing parasitic capacitance and resistance.
- With shorter signal paths and an optimized layout, HDI boards offer improved electrical performance, including lower crosstalk and higher speed capabilities.

6.4.1 Sequential lamination process

Sequential lamination is used to create multilayer boards with microvia structures. Here, the subsets are individually created and bonded using prepreg sheets. The number of lamination cycles required depends on the complexity of the via design.

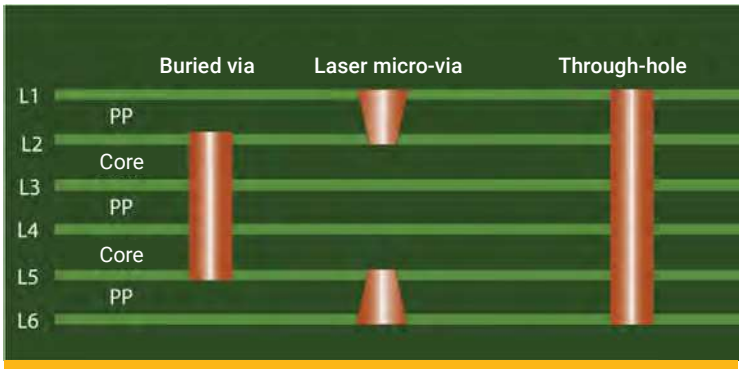


Illustration of 6 layer HDI stack-up

Consider the stack-up in the above image. Here, buried vias are created using sequential lamination. The layers that require buried vias (layers 2, 3, 4, and 5) are a subset that is fabricated in the first lamination cycle. During this process, the buried via is treated like a normal through hole via. Next, layers 1 and 6 are added to the subset, and the whole stack-up goes through a final lamination cycle. Through holes are drilled using a mechanical drill, whereas microvias are created using a laser drill.

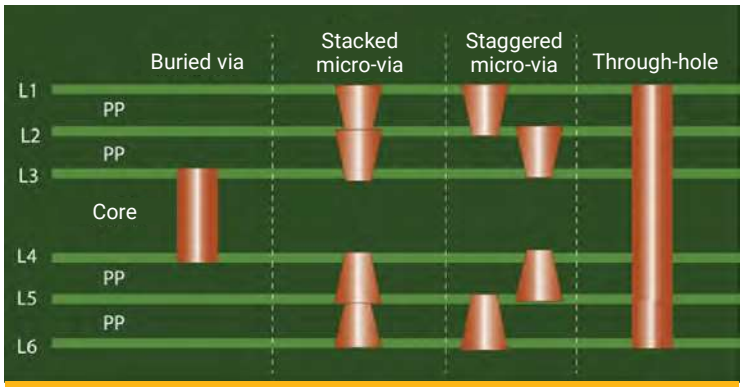


Illustration of 6-layer HDI stack-up with stacked and staggered via

If you want to establish connections between specific layers like L1 and L3 or L6 and L4, staggered or stacked vias are commonly employed.

Stacked vias are more space-efficient but tend to be less reliable and require complex manufacturing processes and filling cycles. This increases the cost of lamination. Staggered vias, on the other hand, offer a simpler process without the need to fill the laser-drilled vias with copper.

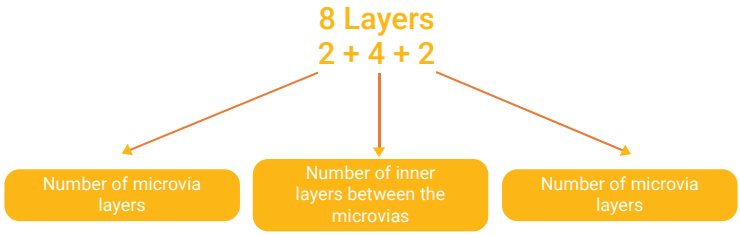
6.4.2 Design guidelines for a HDI stack-up

- During each lamination cycle, the board is subjected to heat and pressure, which will reduce the reliability of the board. Hence, it is recommended to keep the number of lamination cycles between 2 and 3.
- Due to the increased number of lamination cycles, it is crucial to address CTE-related issues such as lamination voids and copper extensions on the Z-axis. Further, using a dielectric material with a high glass transition temperature (Tg) of at least 180°C and CTE with < 70 ppm/°C, the Z-axis expansion minimizes the stress caused by CTE mismatching.
- Optimize the resin content in subsets to reduce expansion. Select dielectrics with a higher resin content to spread stress over a larger volume. The amount of resin on the copper pad depends on the material's hardness.
- Due to the higher density of the trace, the signal integrity issues become even more prominent. Hence, avoid mishaps in the stack-up layer arrangement that can lead to the creation of common-mode noise.
- As the size and number of layers are reduced in HDI stack-up, you have to pay more attention to thermal management. Therefore, implement heat sinks near the high-heat-generating components or traces.

6.4.3 Different types of HDI stack-ups

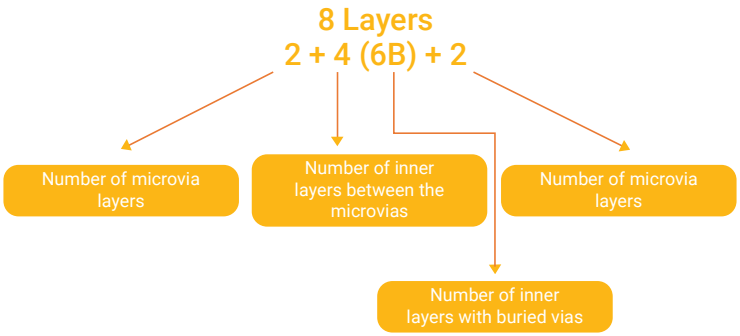
HDI stack-ups come in different configurations based on the number of sequential laminations. The stack-up notation follows the pattern of X+N+X, where "X" represents the number of sequential laminations on each side of a core/central lamination. Below are a few examples of HDI stack-up configurations.

2+4+2 stack-up: This stack-up represents an 8-layer configuration (2+4+2). Here 2 represents the number of sequential laminations and the number of layers in the core lamination.



8-layer HDI stack-up configuration without buried via

2+4(6b)+2 stack-up: This stack-up depicts an 8-layer configuration with two microvia layers on each side of the board and a buried via that connects six layers between the microvia layers.



8-layer HDI stack-up configuration with buried via

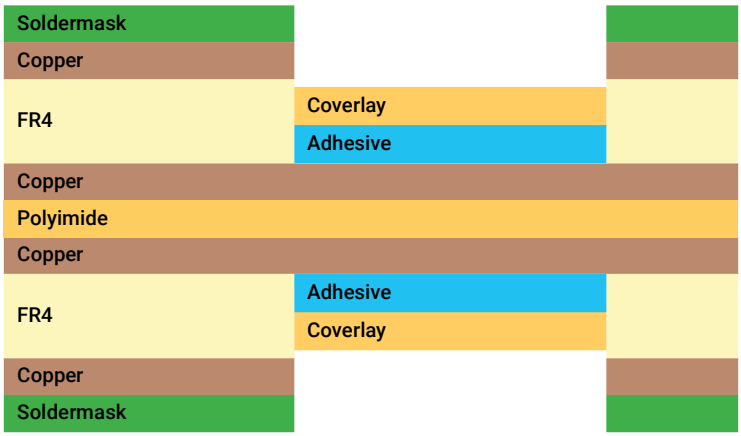
6.5 Flex and rigid-flex stack-up

Flexible PCBs are a valuable option for devices that require mechanical motion or have a complicated enclosure shape. When designing a flex stack-up, the designer must carefully select the appropriate materials and understand how they work together in the flexible layer stack-up. Some of the key benefits of using flex PCBs are:

- **Significantly lighter weight and save space in a device.**
- **Withstand flexing and bending**
- **Made from high-quality materials**
- **Withstand harsh environments**
- **Reliable and long-lasting**
- **Easy to install on devices**

Rigid-flex PCB stack-up: Usually, in a rigid-flex PCB, the flexible stack-up part is sandwiched between two rigid regions to provide structural stability. Here, the coverlay film is bonded to the prepreg during lamination so that the FR-4 stiffener regions can be assembled on the flex ribbon.

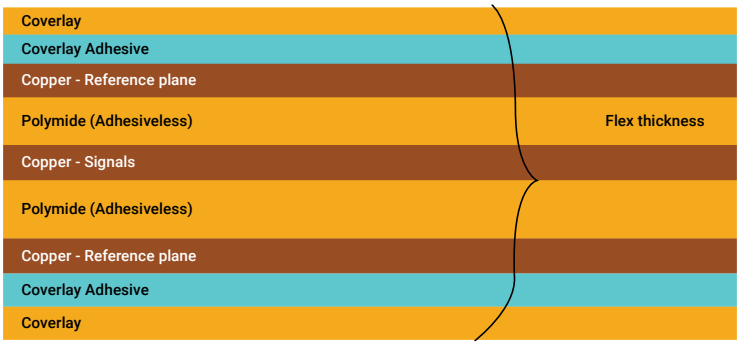
The most commonly designed rigid-flex boards usually have double-sided flexible PCBs laminated with rigid sections with layers of prepreg.



4-layer rigid-flex stack-up

In both flexible PCBs and rigid-flex PCBs, the stiffener sections use a prepreg to bond to the flex section. Multiple rigid layers can be stacked on each side of the flex region. Also, the FR-4 layers on each end can have different layer counts as these will be laid up and press laminated individually.

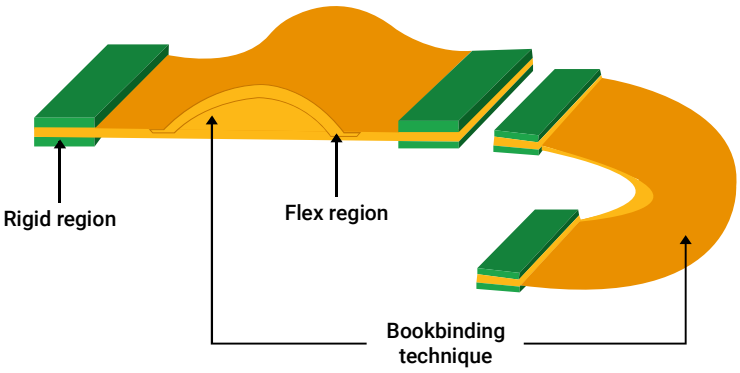
Flex PCB stack-up: Traditionally, two flexible layers are not stacked on top of each other when a flex ribbon is used as an integrated connector. However, if you are designing a multilayer flexible PCB, you can laminate multiple coverlay-substrate layers in succession to create a multilayer flexible PCB. You can also have an odd number of flex layers by bonding substrates directly and etching away one layer.



Flex stack-up illustration

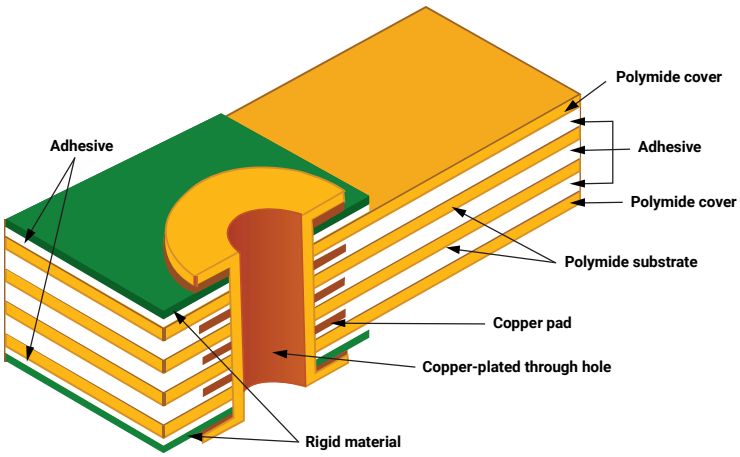
Bookbinding flex stack-up: When you have a higher layer count, bookbinding a flex stack-up will allow you to bend a small radius without any deformation. This is similar to a rigid-flex stack-up. However, two flexible layers are stacked and bonded with prepreg to create space between flex ribbons. With this method, we can elongate the flex region, and the whole stack-up can be folded without creating stress. Other advantages include:

- **Increased shelf-life**
- **Compatible with all mounting processes**
- **Prevents the inner layers from buckling at the bend radius**
- **Can perform bends of 180º**



Bookbinding technique

6.5.1 Material used in flex PCBs



Different materials used in rigid-flex design

- **Base flex material:** Polyimide or polyamide is the most common base material for flexible PCBs. Rigid-flex PCBs have an additional rigid region that contains polyimide as an inner layer. The polyimide base material gives a flexible PCB its characteristic orange color.
- **Copper conductor:** Rolled-annealed copper foil is preferred over traditional electro-deposited copper foil for flexible PCBs.
- **Coverlay:** The exposed copper circuitry of the flexible PCB is protected by a coverlay material, which also plays the same role as a solder mask on a rigid PCB. The coverlay film is also polyimide.

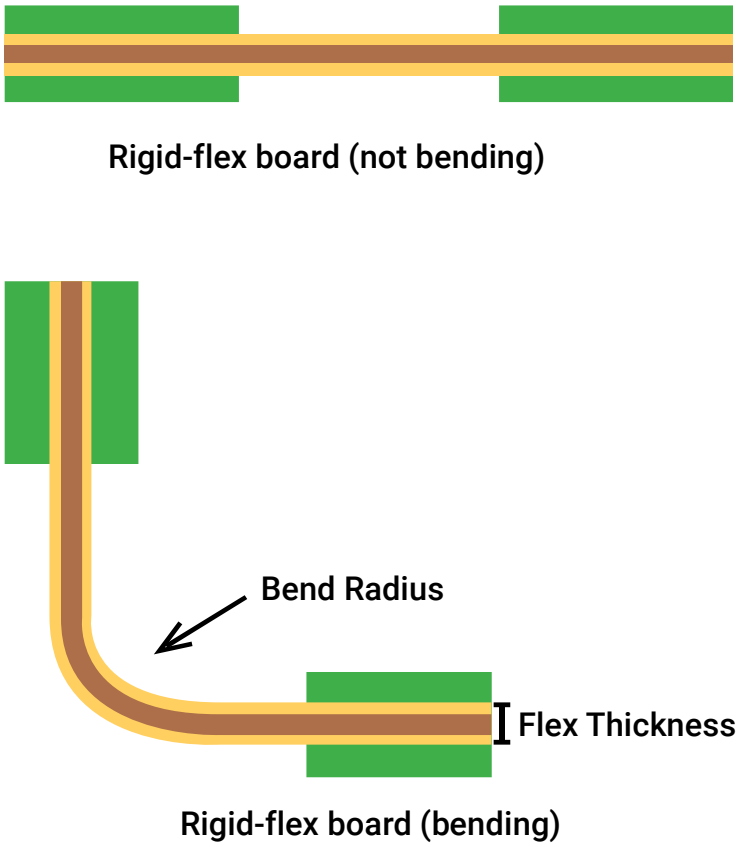
- **Adhesives:** Epoxy-based adhesives are used to bond the flex base material and coverlay onto the copper conductor. There are also processes that involve plating directly on polyimide and do not require adhesives.
- **Stiffeners:** Rigid-flex PCBs have non-flexing regions that use FR-4 or polyimide to provide rigidity. There are two methods for attaching stiffeners to the flex PCB: lamination or adhesion using a pressure-sensitive adhesive (PSA).

There are also solder mask materials available for flexible PCBs that can be used for extra environmental protection. These flex solder mask materials are specifically formulated for use on polyimide boards, and they can provide a very unique look.

6.5.2 Design guidelines for flex and rigid-flex stack-up

The stack-up design of a flex PCB is important to ensure its flexibility and durability. The following factors should be considered when designing the stack-up:

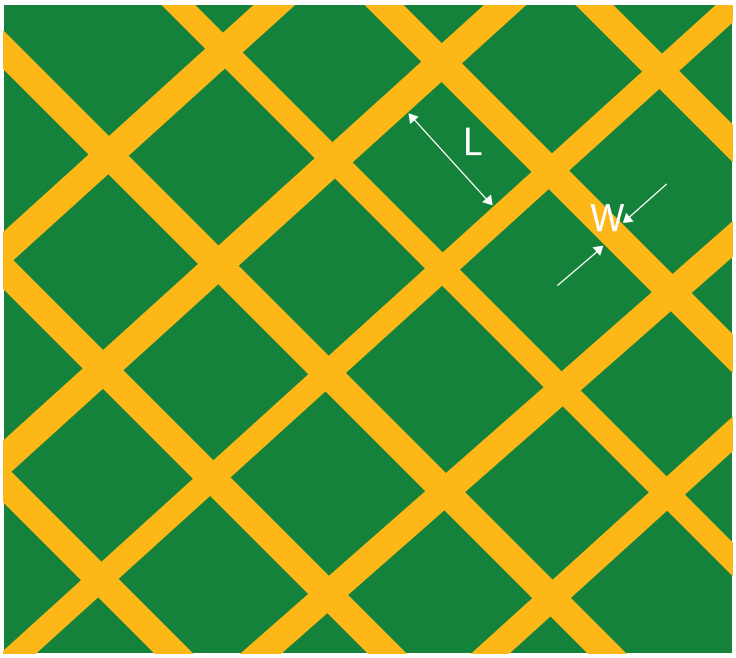
Type of application: The bend radius and overall board thickness are determined based on the application requirements. For example, a flex PCB that will be used in a dynamic application will need to have a smaller bend radius and a thinner overall thickness than a flex PCB that will be used in a static application.



Bend radius of rigid-flex PCB

Number of layers: The number of layers in a flex PCB will also affect its flexibility. A flex PCB with a larger number of layers will be less flexible than a flex PCB with a smaller number of layers.

Thickness of the copper traces: The thickness of the copper traces can also affect the flexibility of a flex PCB. Reducing the thickness of the copper traces will increase the flexibility of the PCB. You can do this by cross-hatching the ground planes on both sides of the signal layers.



Cross-hatching copper planes

In addition to these factors, follow the below-mentioned guidelines when designing a rigid-flex stack-up:

- In a rigid-flex stack-up, place the flexible layers in the middle of the stack-up. This will help prevent slippage between the flexible and rigid layers.
- Incorporate an air-gap construction method. This will eliminate the use of flex adhesives within the rigid sections, which can improve the reliability of the vias.
- Avoid 90-degree bends, as they can cause high strain on the flex region.
- Place plated through-holes and components away from the bend area. This will help prevent damage to the circuit board during bending.
- Use stiffeners in areas susceptible to excessive pressure. Stiffeners can help prevent excessive flexing of the circuit board and damage.
- Keep special copper features, vias, and plated through holes away from the transition zone. The transition zone is the area between the flexible and rigid layers of a rigid-flex PCB.

6.6 Hybrid stack-up

A hybrid stack-up has a specialized configuration where selected layers of a multilayer circuit board are built with specific materials to meet particular design requirements. The choice of materials and their arrangement depends on the specific application and desired functionality.

Advantages of a hybrid stack include:

- Each layer in a hybrid stack-up can be tailored for specific functions, enhancing performance and reliability without a significant cost increase. The use of expensive materials and complex manufacturing processes can be minimized.

- Hybrid stack-ups enable the isolation of sensitive analog or digital signals from noisy components, with careful consideration given to ground planes, power planes, and shielding layers.
- Specialized materials with enhanced heat dissipation capabilities and the incorporation of thermal planes or additional copper layers improve the board's thermal properties, which are crucial for high-power applications.
- Hybrid stack-ups facilitate effective consolidation and integration of different functionalities, such as analog and digital circuitry, RF components, sensors, and microcontrollers, reducing complexity and board size.

6.6.1 Design guidelines for a hybrid stack-up

- Select appropriate layers and materials based on design expectations, considering the dielectric constant, dissipation factor, thermal conductivity, and coefficient of thermal expansion.
- Group signal layers based on operating frequencies and sensitivity to interference, assigning layers with special materials to isolate them from the rest.
- Place RF signals on top layers with adjacent ground planes.
- Strategically plan dielectric spacing between signal, power, and ground layers to manage impedance control, crosstalk, and EMC.
- Verify stack-up performance using simulation tools.

6.6.2 Challenges in building a hybrid stack-up

- Different materials used in hybrid stack-ups have varying CTEs, which can cause registration issues during fabrication and component assembly. Proper consideration and understanding of material properties are crucial to avoiding deformation and permanent board damage.
- First article panels have to be run to confirm the scaling values. This can increase the cost of the board.

- Standard adhesives cannot be used when bonding dissimilar materials. You need to choose a bonding material with low lamination and re-melt temperatures. Typical bond materials used include fluorinated ethylene propylene (FEP), ceramic-filled PTFE, and liquid crystal polymer (LCP).

- When it comes to cost-effectiveness in hybrid stack-ups, using a single type of prepreg to bond hybrid cores is advisable. For instance, Roger 4350 and 370HR cores are bonded with 370HR prepreg. If multiple prepregs of different materials are utilized, it can significantly increase both the cost and the manufacturing time.

- The combination of different materials increases the risk of layer separation and delamination, affecting the board's structural integrity and performance. Careful lamination processes and compatible bonding materials are essential to mitigating these issues.

- Selecting optimal layer thicknesses for each material and considering the operating frequency is critical. Varying insulation and adhesion properties of materials can lead to lamination issues. Hence, collaboration with fabricators to determine suitable thicknesses is recommended.

- Different materials require specific drilling processes, and the chemicals used for hole preparation may differ. It's essential to account for these variations to ensure even and reliable plating of drilled holes.

As said above, designing an efficient stack-up is essential to maintaining good signal integrity and electrical performance. However, it is a challenging task to build an error-free stack-up design. Fortunately, there are online tools like Sierra Circuits PCB Stackup Designer. Its features include:

- Offers 3 technology levels (level I/II/III) with respect to trace geometry, drill sizes, spacing, and cost index.

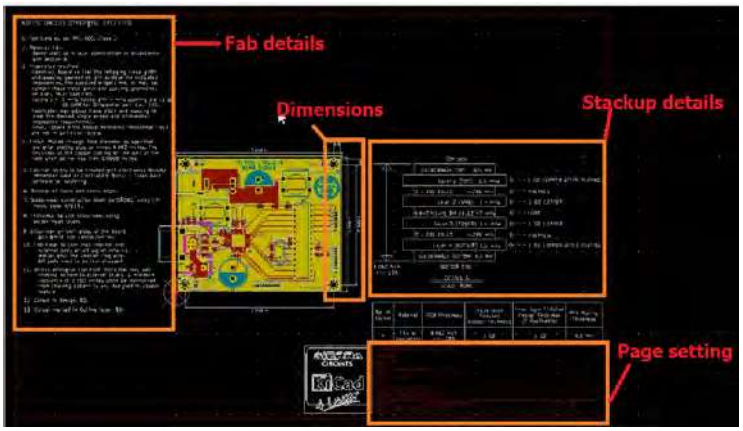
- Includes a library of single and sequential lamination stack-up templates.

- Automatically chooses the construction type (foil or core).

- Linked to our 2D field solver-based impedance calculator to design high-speed traces.

7. Stack-up representation in fabrication drawings and notes

Representing the stack-up in fabrication drawings and notes is essential for communicating the intended construction and layer arrangement of a PCB to the manufacturer. Here are some common methods for representing the stack-up in fabrication drawings and notes:



Stack-up representation in the fabrication drawing

7.1 Table with layer details

Layer Name	Type	Material	Thickness (mm)	Color	Epsilon R	Loss Tangent
F.Silkscreen	Top Silk Screen	Not specified	0 mm	Not specified	1	0
F.Paste	Top Solder Paste		0 mm		1	0
F.Mask	Top Solder Mask	Not specified	0.01 mm	Not specified	3.3	0
TOP	copper		0.035 mm		1	0
Dielectric	core	FR4	0.4716 mm		4.5	0.02
GND	copper		0.035 mm		1	0
Dielectric	prepreg	FR4	0.4716 mm		4.5	0.02
POWER	copper		0.035 mm		1	0
Dielectric	core	FR4	0.4716 mm		4.5	0.02
BOTTOM	copper		0.035 mm		1	0
B.Mask	Bottom Solder Mask	Not specified	0.01 mm	Not specified	3.3	0
B.Paste	Bottom Solder Paste		0 mm		1	0
B.Silkscreen	Bottom Silk Screen	Not specified	0 mm	Not specified	1	0

Sample of stack-up representation in table format

In the fabrication drawing, provide a clear and concise representation of the layer stacking order. Typically, this is done using a vertical column or table that lists the layers from top to bottom, along with their respective functions (e.g., signal, power, ground).

- Assign unique identifiers or names to each layer in the stack-up. These identifiers can be alphanumeric codes or descriptive labels that are used consistently throughout the fabrication drawings and notes.
- Provide material specifications for each layer in the stack-up, including the dielectric material type (FR-4, Rogers, Isola I-speed), copper weight, and any specific requirements for each layer.
- Next, indicate the thickness of the core, prepreg, and copper foil present in the stack-up.
- Add color to the solder mask and silkscreen layers.

For example, green for the solder mask and white for the silkscreen.

- Include additional details like the dielectric constant and dissipation factor.

7.2 Stack-up cross-sections

For more complex stack-ups, it may be beneficial to include cross-sectional views that illustrate the layer arrangement, material thicknesses, and any special considerations, such as controlled impedance structures or specific copper features. It is also good to include the required overall thickness of the stack-up with tolerance.

Sample of PCB stack-up cross-section

7.3 Stack-up details in fabrication notes

In the fabrication notes section, include any additional instructions or specifications related to the PCB stack-up. This includes requirements such as

- IPC class and inspection
- Dielectric material specification
- Controlled impedance requirements
- Manufacturing tolerances
- Drilling and plating details
- Surface features:
  - Solder mask and finishes
  - Silkscreen color and ink
  - Surface finishes
- RoHS compliance
- Testing and reporting requirements
- Vendor marking details and location

Sample of fabrication notes to include in the fab drawing

Remember to follow industry standards and conventions for PCB fabrication drawings and notes. It is also important to communicate directly with the manufacturer to ensure that the stack-up representation aligns with their specific requirements and capabilities.

12. About Sierra Circuits

Sierra Circuits has been serving PCB designers and engineers with the latest technologies since 1986 and has worked with over 20,000 customers since then. We specialize in manufacturing, assembly, and HDI technology. We handle all aspects of circuit board production.

We provide our customers with DFM and DFA support, which helps produce unprecedented board quality with high reliability. By choosing us, you can eliminate miscommunication between multiple vendors and delays since we provide a single point of support.

Talk to our experts

Sierra Circuits helps PCB designers plan it right! Our engineering staff has been trained on controlled impedance and can analyze the design from a holistic point of view.

Our engineering support and our stack-up team provide valuable suggestions with their knowledge of controlled impedance for high-speed designs, analog/digital, high-density board manufacturing design rules, and design for assembly guidelines. Upload your data and receive a free consultation and review of your design. Services include system-level design, schematic capture, circuit board layout, and PCB/PCBA DFM.

Our facility

Why Sierra Circuits?

Customer-oriented approach: We collaborate closely with you and tailor solutions to meet your unique design requirements.

Rapid high-tech innovation: We work in a fast-paced environment and implement cutting-edge technologies to bring your design ideas to life.

Initial collaboration: Our skilled team, comprising experts in design, manufacturing, and supply chain management, collaborates from the initial stages of your project.

Reliable class 3 PCBs: We specialize in complex products for defense and aerospace that demand high-performance and reliable PCBs to support mission-critical systems.

Sierra Circuits'
PCB manufacturing capabilities overview

Rigid PCBs

PCB highlights	Fabrication highlights	PCB classification	Quality management systems
Up to 30 layers	Routed arrays	IPC 6012, class 1, 2 and 3	AS9100D
Board thickness: .005" - .250"	Edge plating	MIL-PRF-55110	ISO 9001:2015
Max panel size: 21" x 29"	Bevels	MIL-PRF-31032/1	ISO 13485:2016
Min trace and space: .002"	Heat sinks	MIL-PRF-31032/2	
Solder mask feature tolerance: .001"			
Blind and buried vias			

HDI and microelectronics

High tech in small form	Features	Certified for your industry:
Special stack-up help / NPI review	Down to 1.5-mil trace space, 2-mil holes	Mil-spec
Up to 30 layers	Blind vias, buried vias, and other microvia techniques	Automotive
Files evaluated by engineers	Up to 5 sequential lamination cycles	Aerospace and defense
Quote sent by email within a few hours	Laser direct imaging	Medical devices
	via-in-pad technology	

Flex and rigid-flex PCBs

Surface finishes	Standard flex materials	Fabrication highlights	PCB classification
HASL	0.5 mil to 5 mil thick polyimide material	Routed array	IPC 6012, Class 1, 2 and 3
Lead-free HASL	1 mil to 5 mil thick copper clad base material	V score	ISO:9001:2015
OSP (Shikoku F2 and Entek)	Flame retardant laminate	Edge plating	ISO 13485: 2015
ENIG	UL and RoHS compliant	Edge castellation	
Immersion silver		Countersink	
Immersion white tin		Bevel	
Tin nickel		Milling	
Selective gold			

Aerospace and defense PCBs

Capabilities	Documents we provide	Ideal for
Layer count: Up to 30	Certificate of conformance	DOD product designers developing systems for mission critical functions
Minimum board thickness:10 mil	Material specifications	Contract manufacturers who need fast, predictable lead times
Thickness tolerance: 10%	Reflow profile copy (included with first article)	Purchasing teams who require pricing and supply-chin transparency
Minimum trace and space width: 3 mil	Photo requirements	Aerospace engineers looking to shore-up their supply chain troubles
Minimum drill-to-copper clearance: 6 mil	First article inspection report	
Maximum panel size: 21" x 29"	Record of calibrated tools used during manufacturing	
Controlled impedance	FPT, AOI, ionic cleanliness report	
Stacked vias		

RF and microwave PCBs

Capabilities	Certifications
Operating frequency: 10 MHz to 30 GHz	PC Manufacturers Qualification Profile (MQP)
Sodium etch hole treatment process	IPC-A-600
Full-body gold plating up to 120u"	IPC-6012 standards
Soft gold without nickel or ENEPIG surface finishes for enhanced board protection	ISO 9001:2015
Design assistance	NADCAP
	ITAR registered
	RoHS/REACH standards

Sierra Circuits PCB assembly services

We offer a diverse range of PCB assembly services tailored to meet your unique requirements. Whether you need a full turn-key assembly, consigned or partially con-signed assembly we got your covered.

Full turnkey PCB	Partially consigned assembly	Consigned assembly	Assembly capabilities
Design review	Some parts provided by the designer	Components are provided by the PCB designer	BGA, micro-BGA, QFN,CSP, lead less devices up to 0.35mm pitch, press fit components
Bare board fabrication	We will source the rest	Sierra Circuits will fully assemble your PCBs and ship them to you.	DFA
Component procurement	Supply chain resilient	Quick turn times	RoHS, leaded, indium, clean and no clean chemistry
Testing	Quick turnaround time	Fully transparent pricing	Component sizes: 0201, 01005, 08004
Quick turnaround time			Paste in-hole

To help you overcome the challenges involved in component procurement, Sierra Circuits has introduced a customer owned inventory service (COIN). It's a personalized component sourcing and stocking program.

We procure and store parts for your PCBAs. This can help you significantly reduce your product development time.

Sierra Circuits PCB design services

Whether you're beginning with a new design, or enhancing an existing one, our design experts provide the assistance you need. Our PCB design services include stack-up design, signal integrity analysis, circuit board layout optimization, schematic capture, and reverse engineering.

Our capabilities include:

- High-speed digital designs, analog designs, mixed designs, power designs, and RF designs.
- Controlled impedance with a tolerance of ±5%.
- Mechanical-constrained boards and enclosures.
- Flex, rigid, and rigid-flex designs.
- PCB designs for mobile phones.
- HDI designs with via-in-pad, blind via, buried via, microvias, via stacking, and staggering technology.
- Fine-pitch BGAs of 0.4 mm and 0.5 mm.
- Designs with high-pin count full matrix BGAs 0.4 mm pitch, PoP (package on package), with 2 mil/ 2 mil tracks/spacings.
- Design for ROHS compliance.
- Optimum impedance calculation for single-ended, differential, and coplanar-waveguide models.

Advanced PCB design tools

From material selection to impedance calculation, streamline your design process by using our comprehensive suite of cutting-edge PCB design tools. These web applications enable you to expedite your design process and make the right decisions to ensure signal integrity and reliability in your circuit board.

Sierra Circuits PCB certification and registration

IPC certified for quality standards in PCB fabrication and assembly

- IPC Manufacturers Qualification Profile (MQP) for Sierra Circuits, Sunnyvale, California.
- IPC-A-600 inspectors.

ISO-certified for military, aerospace, and medical device PCB fabrication and assembly

- ISO 9001:2015 certificate
- AS9100D - military and aerospace
- ISO 13485:2016 certificate - medical devices

Mil-Spec certified and DLA approved

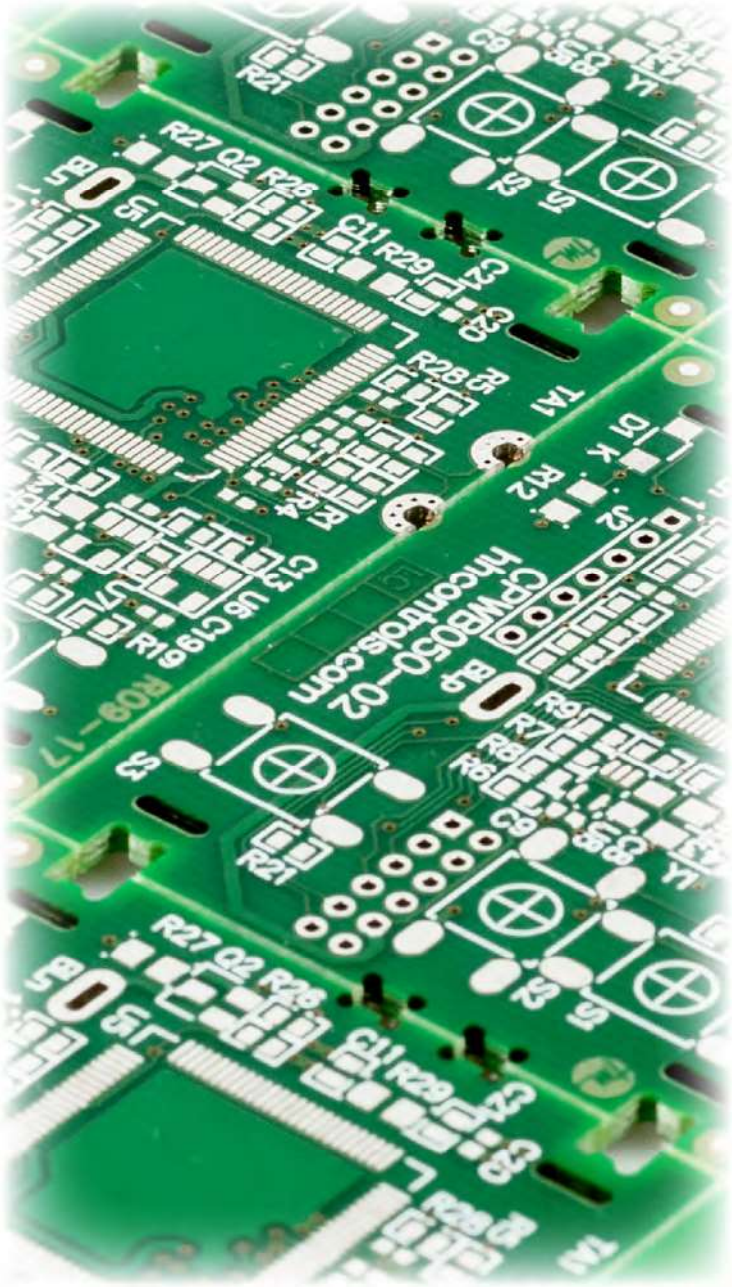
- MIL-PRF-31032/3 flex certificate
- Acc 2020 CVI VQE 035113
- JCP certification approval letter

ITAR Registered

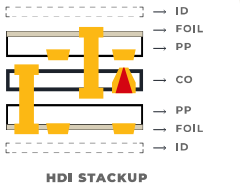
- ITAR registration letter
- Underwriters Laboratory certified
- Flex and rigid-flex PCBs
- Rigid PCBs

Exceptional material compliance and reporting

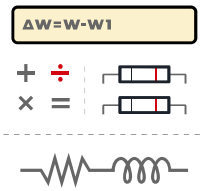
- RoHS / REACH compliance material composition declaration
- Conflict minerals reporting template
- Certified minority supplier by NMSDC
- Minority business certification



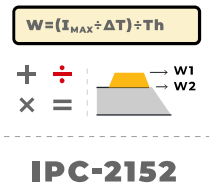
The Designer's Toolkit



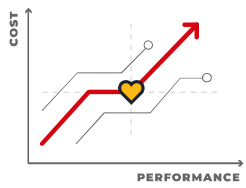
Stack-up Designer



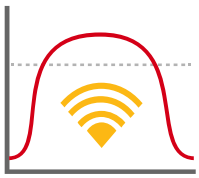
Impedance Calculator



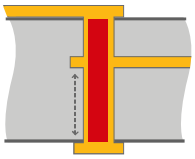
Trace Width, Current Capacity and Temperature Rise Calculator



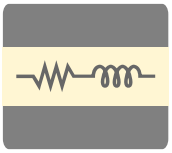
Material Selector



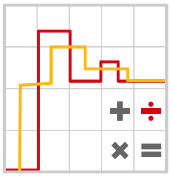
Bandwidth, Rise Time and Critical Length Calculator



Maximum Via Stub Length Calculator

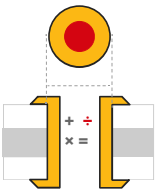


Signal Layer Estimator

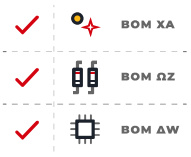


Transmission Line Reflection Calculator

RLC Resonant Frequency & Impedance Calculator

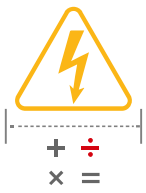


Via Current Capacity and Temperature Rise Calculator

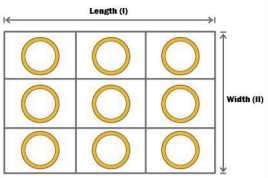


BOM Checker

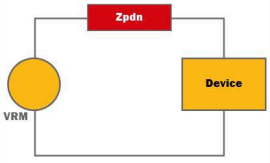
Better DFM



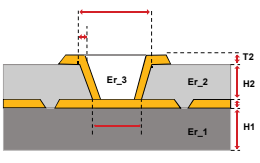
Conductor Spacing and Voltage Calculator



Via Thermal Resistance Calculator



Power Distribution Network Analyzer



Via Impedance Calculator

Try Tools