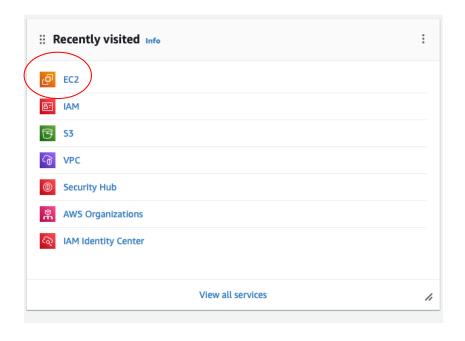
# FPGA Designs on AWS

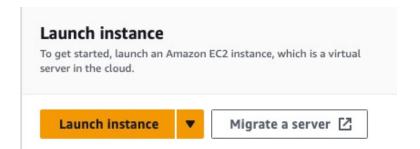
Programming FPGAs for Economics:
An Introduction to Electrical Engineering Economics

Bhagath Cheela, Alessandro Peri, André DeHon, Jesús Fernández-Villaverde

#### Steps



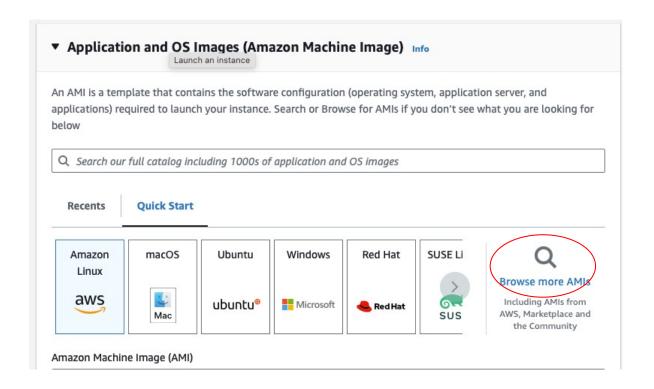
- 1. Log into your AWS account:
- 2. Navigate to the Home Console
- 3. Select EC2
- 4. Launch Instance



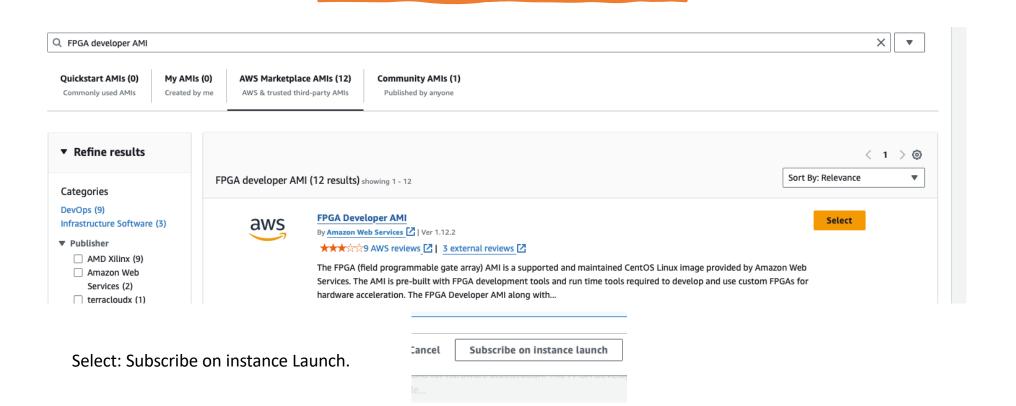
#### Steps: Name and tags

# Launch an instance Info Amazon EC2 allows you to create virtual machines, or instances, that run on the AWS Cloud. Quickly get started by following the simple steps below. Name and tags Info Name fpga-dev Add additional tags

#### Select FPGA Developer AMI: Browse more AMI



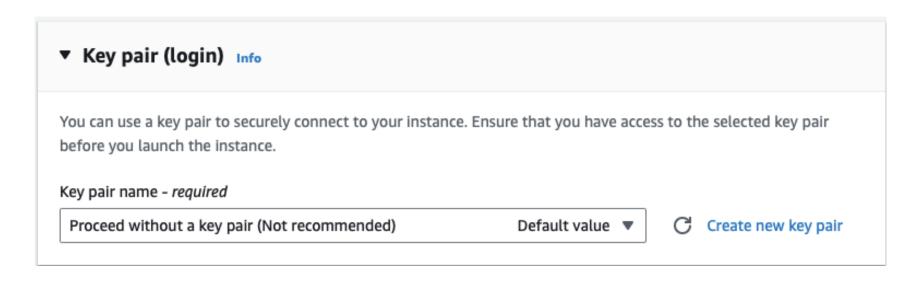
# Select FPGA Developer AMI



#### Select Build Instance

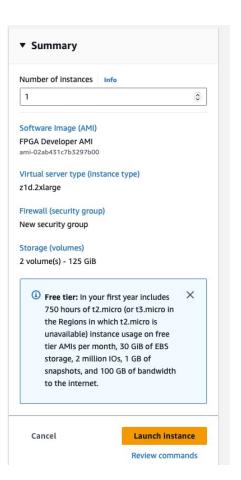


# Key pair

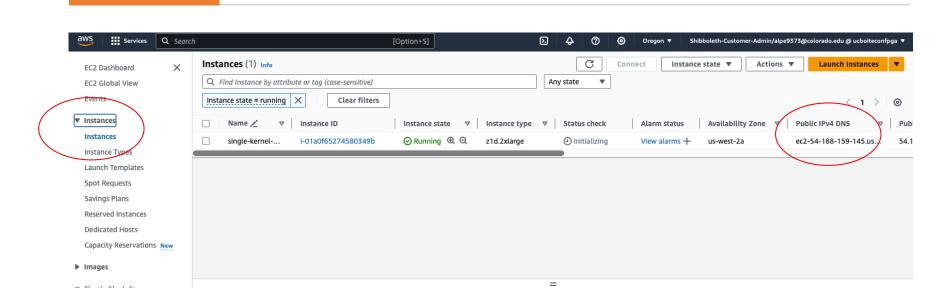


For information on how to create a new key pair go <a href="here">here</a>

#### Launch z1d.2xlarge Instance

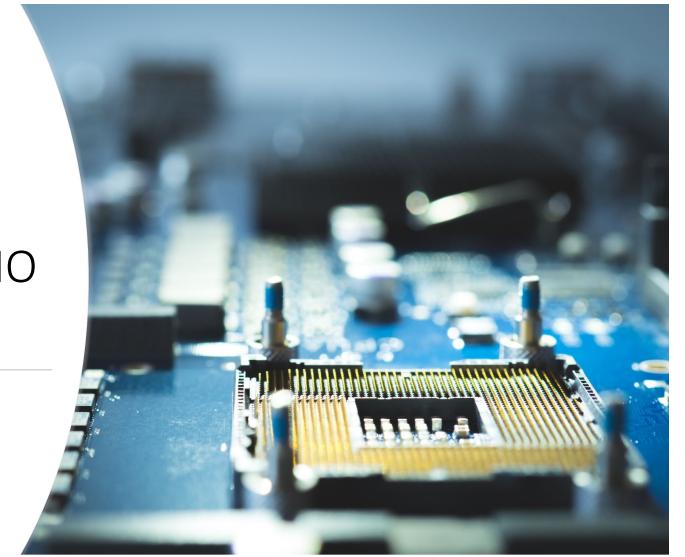


#### EC2 Instances



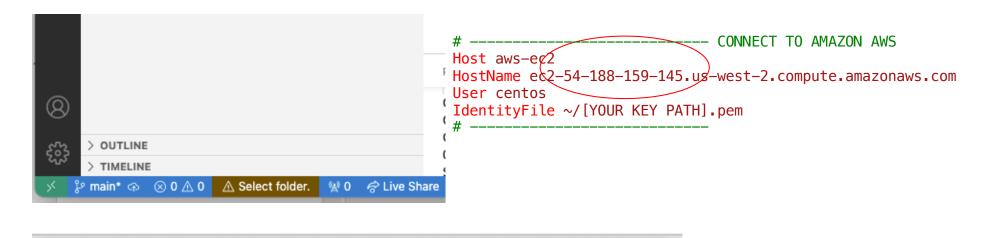
- In the top-left menu, select 'Instances'
- Copy the public IPv4 address in Visual Studio code

VISUAL STUDIO CODE



# Open a Remote Window

- On the bottom-left corner of Visual Studio Code click on the green button 'Open a Remote Window'
- · Click on Connect to Host
- Click on Configure SSH Hosts
- Copy the public IP address
- Connect to aws-ec2.
- If you receive an error try to set: User root (in place of User Centos)



Select an option to open a Remote Window

Connect to Host...

Remote-SSH

# Setup the Instance

#### Clone the Github Repos

• Clone our GitHub repository into a directory of your preference (e.g., /home/centos):

```
git clone https://github.com/aws/aws-fpga.git $AWS_FPGA_REPO_DIR
git clone https://github.com/AleP83/FPGA-Econ.git
```

#### AWS Configure

```
○ [centos@ip-10-0-1-68 ~]$ aws configure
AWS Access Key ID [None]:
```

- 1. Go to your aws account and set (one time thing):
  - AWS Access Key ID
  - -AWS Secret Access Key
- 2. Go to the terminal in visual studio and type aws configure

#### 3. Set:

- AWS Access Key ID:
- AWS Secret Access Key
- Default Region name: us-west-2 *Note:* this depends in which region you launched your instance.
- Default output format [json]: json

#### Modify the Makefile

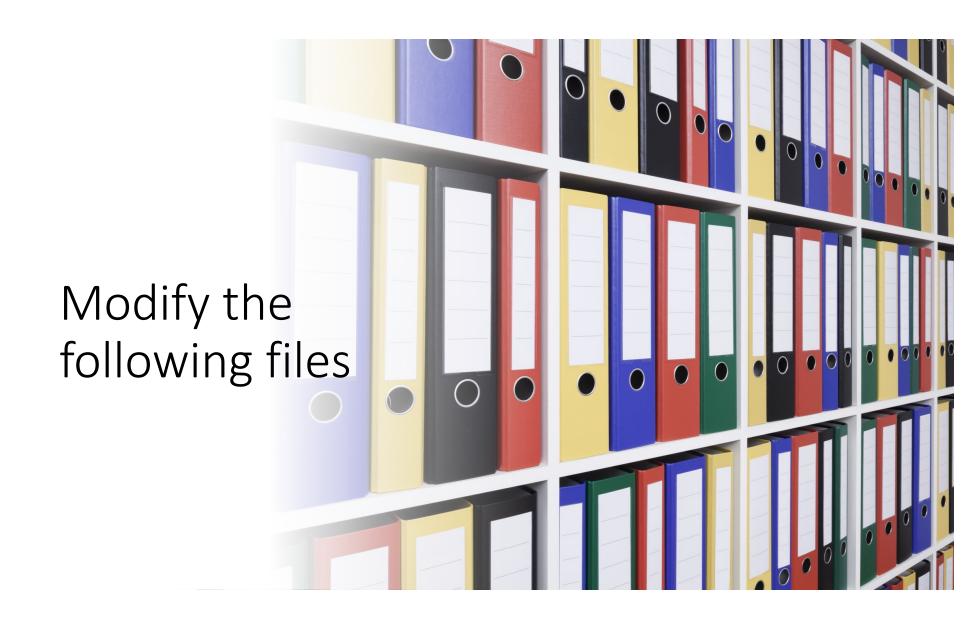
 Set the AWS S3 Bucket Name. Specify the S3 bucket name by replacing S3-NAME-GOES-HERE

```
S3_EXE_BUCKET_NAME := S3-NAME-GOES-HERE
```

Remark: The S3 bucket name must be globally unique within AWS. If an error occurs during bucket creation, it may be due to the name being already in use by another user.

Select the AWS region of the S3 bucket (default is us-west-2):

```
AWS REGION := us-west-2
```



#### 1. common/app.cpp

Line 10: Set the number of models

• #define N\_MODEL 1200 // total number of models

#### 2. common/definitions.h

#### Lines 41-42: Select the grid points

```
• /** Configure grid points.
```

- The analysis in the paper involves six distinct combinations: NKGRID={100,200,300}; NKM\_GRID={4,8}.
- \*/
- #define NKGRID 100 // grid points on individual capital grid
- #define NKM\_GRID 4 // grid points on aggregate capital grid

#### 3. common/dev options.h

```
// Select FPGA design by enabling exactty one of the following macros (setting it to one), keeping the rest to zero. For best performance, set _ACROSS_ECONOMY to 1 and rest 0

#define _BASELINE 0 // FPGA design with no HLS acceleration.

#define _PIPELINE 0 // FPGA design with only PIPELINE acceleration

#define _WITHIN_ECONOMY 0 // FPGA design with one-kernel data parallelization and pipelining

#define _ACROSS_ECONOMY 1 // FPGA design with three-kernels. Benchmark
```

#### 5. fpga/design.cfg

• Select the kernel design: three-kernel design vs single-kernel design Deafult: three-kernel design

# Create the FPGA Images

#### In Visual Studio Code

- Open the terminal
- Go to the terminal



# Follow instructions on readme from here

Build. Navigate to the directory /code. From there, execute the following instructions in the terminal to generate the host and the fpga target files on the build instance (zld.2xlarge) and upload the generated executables to AWS bucket:

```
make clean
unset XCLEMULATION MODE

//setup environment
source $AWS_FPGA_REPO_DIR/vitis_setup.sh
export PLATFORM REPO_PATHS=$(dirname $AWS_PLATFORM)
export XCLEMULATION MODE=hw
//build the target
make afi FPGA_BIN=<fpga_bin> HOST_BIN=<host_bin>
```

Example: make afi FPGA\_BIN=3ker\_100k\_4km HOST\_BIN=1200\_3ker\_100k\_4km

#### 3-kernel-100-4 (1200 Economies)

```
/common/app.cpp
                                 #define N MODEL 1200 // total number of models
                                #define NKGRID 100 // grid points on individual capital grid
/common/definitions.h
                                #define NKM_GRID 4 // grid points on aggregate capital grid
                                // Select FPGA design by enabling exactly one of the following macros, keeping the rest to zero. For best performance,
                                 set _ACROSS_ECONOMY to 1 and rest 0
/common/dev options.h
                                #define _BASELINE 0 // FPGA design with no HLS acceleration.
                                #define _PIPELINE 0 // FPGA design with only PIPELINE acceleration
                                 #define _WITHIN_ECONOMY 0 // FPGA design with one-kernel data parallelization and pipelining
                                 #define _ACROSS_ECONOMY 1 // FPGA design with three-kernels. Benchmark
/fpga/design.cfg
                                 [connectivity]
                                 nk=runOnfpga:3:runOnfpga_1.runOnfpga_2.runOnfpga_3
                                 slr=runOnfpga_1:SLR2
                                 slr=runOnfpga_2:SLR1
                                 slr=runOnfpga_3:SLR0
                                 sp=runOnfpga_1.m_axi_gmem0:DDR[1]
                                 sp=runOnfpga_2.m_axi_gmem0:DDR[0]
                                 sp=runOnfpga_3.m_axi_gmem0:DDR[3]
                                 [vivado]
                                 prop=run.impl_1.strategy=Performance_ExtraTimingOpt
                                 make clean
Terminal launch:
                                 unset XCL_EMULATION_MODE
                                 source $AWS_FPGA_REPO_DIR/vitis_setup.sh
                                 export PLATFORM_REPO_PATHS=$(dirname $AWS_PLATFORM)
                                 export XCL_EMULATION_MODE=hw
                                 make afi FPGA_BIN=3ker_100k_4km HOST_BIN=1200_3ker_100k_4km
```

#### 1-kernel-100-4 (1200 Economies)

```
/common/app.cpp
                                 #define N MODEL 1200 // total number of models
                                 #define NKGRID 100 // grid points on individual capital grid
/common/definitions.h
                                 #define NKM_GRID 4 // grid points on aggregate capital grid
                                 // Select FPGA design by enabling exactly one of the following macros, keeping the rest to zero. For best performance,
                                 set _ACROSS_ECONOMY to 1 and rest 0
/common/dev options.h
                                 #define _BASELINE 0 // FPGA design with no HLS acceleration.
                                 #define _PIPELINE 0 // FPGA design with only PIPELINE acceleration
                                 #define _WITHIN_ECONOMY 1 // FPGA design with one-kernel data parallelization and pipelining
                                 #define _ACROSS_ECONOMY 0 // FPGA design with three-kernels. Benchmark
/fpga/design.cfg
                                 #############single kernel start##############
                                 [connectivity]
                                 nk=runOnfpga:1:runOnfpga_1
                                 [vivado]
                                 prop=run.impl_1.strategy=Performance_ExtraTimingOpt
Terminal launch:
                                  tmux
                                  make clean
                                 unset XCL_EMULATION_MODE
                                  source $AWS_FPGA_REPO_DIR/vitis_setup.sh
                                  export PLATFORM_REPO_PATHS=$(dirname $AWS_PLATFORM)
                                  export XCL_EMULATION_MODE=hw
```

make afi FPGA\_BIN=1ker\_100k\_4km HOST\_BIN=1200\_1ker\_100k\_4km

#### 1-kernel-200-4 (1200 Economies)

```
/common/app.cpp
                                 #define N MODEL 1200 // total number of models
                                 #define NKGRID 200 // grid points on individual capital grid
/common/definitions.h
                                 #define NKM_GRID 4 // grid points on aggregate capital grid
                                 // Select FPGA design by enabling exactly one of the following macros, keeping the rest to zero. For best performance,
                                 set _ACROSS_ECONOMY to 1 and rest 0
/common/dev options.h
                                 #define _BASELINE 0 // FPGA design with no HLS acceleration.
                                 #define _PIPELINE 0 // FPGA design with only PIPELINE acceleration
                                 #define _WITHIN_ECONOMY 1 // FPGA design with one-kernel data parallelization and pipelining
                                 #define _ACROSS_ECONOMY 0 // FPGA design with three-kernels. Benchmark
/fpga/design.cfg
                                 #############single kernel start##############
                                 [connectivity]
                                 nk=runOnfpga:1:runOnfpga_1
                                 [vivado]
                                 prop=run.impl_1.strategy=Performance_ExtraTimingOpt
Terminal launch:
                                  tmux
                                  make clean
                                 unset XCL_EMULATION_MODE
                                  source $AWS_FPGA_REPO_DIR/vitis_setup.sh
                                  export PLATFORM_REPO_PATHS=$(dirname $AWS_PLATFORM)
                                  export XCL_EMULATION_MODE=hw
```

make afi FPGA\_BIN=1ker\_200k\_4km HOST\_BIN=1200\_1ker\_200k\_4km

#### 1-kernel-300-4 (1200 Economies)

```
/common/app.cpp
                                 #define N MODEL 1200 // total number of models
                                 #define NKGRID 300 // grid points on individual capital grid
/common/definitions.h
                                 #define NKM_GRID 4 // grid points on aggregate capital grid
                                 // Select FPGA design by enabling exactly one of the following macros, keeping the rest to zero. For best performance,
                                 set _ACROSS_ECONOMY to 1 and rest 0
/common/dev options.h
                                 #define _BASELINE 0 // FPGA design with no HLS acceleration.
                                 #define _PIPELINE 0 // FPGA design with only PIPELINE acceleration
                                 #define _WITHIN_ECONOMY 1 // FPGA design with one-kernel data parallelization and pipelining
                                 #define _ACROSS_ECONOMY 0 // FPGA design with three-kernels. Benchmark
/fpga/design.cfg
                                 #############single kernel start##############
                                 [connectivity]
                                 nk=runOnfpga:1:runOnfpga_1
                                 [vivado]
                                 prop=run.impl_1.strategy=Performance_ExtraTimingOpt
Terminal launch:
                                  tmux
                                  make clean
                                 unset XCL_EMULATION_MODE
                                  source $AWS_FPGA_REPO_DIR/vitis_setup.sh
                                  export PLATFORM_REPO_PATHS=$(dirname $AWS_PLATFORM)
                                  export XCL_EMULATION_MODE=hw
```

make afi FPGA\_BIN=1ker\_300k\_4km HOST\_BIN=1200\_1ker\_300k\_4km

#### 1-kernel-100-8 (1200 Economies)

```
/common/app.cpp
                                 #define N MODEL 1200 // total number of models
                                 #define NKGRID 100 // grid points on individual capital grid
/common/definitions.h
                                 #define NKM_GRID 8 // grid points on aggregate capital grid
                                 // Select FPGA design by enabling exactly one of the following macros, keeping the rest to zero. For best performance,
                                 set _ACROSS_ECONOMY to 1 and rest 0
/common/dev options.h
                                 #define _BASELINE 0 // FPGA design with no HLS acceleration.
                                 #define _PIPELINE 0 // FPGA design with only PIPELINE acceleration
                                 #define _WITHIN_ECONOMY 1 // FPGA design with one-kernel data parallelization and pipelining
                                 #define _ACROSS_ECONOMY 0 // FPGA design with three-kernels. Benchmark
/fpga/design.cfg
                                 #############single kernel start##############
                                 [connectivity]
                                 nk=runOnfpga:1:runOnfpga_1
                                 [vivado]
                                 prop=run.impl_1.strategy=Performance_ExtraTimingOpt
Terminal launch:
                                  tmux
                                  make clean
                                 unset XCL_EMULATION_MODE
                                  source $AWS_FPGA_REPO_DIR/vitis_setup.sh
                                  export PLATFORM_REPO_PATHS=$(dirname $AWS_PLATFORM)
                                  export XCL_EMULATION_MODE=hw
```

make afi FPGA\_BIN=1ker\_100k\_8km HOST\_BIN=1200\_1ker\_100k\_8km

#### 1-kernel-200-8 (1200 Economies)

```
/common/app.cpp
                                 #define N MODEL 1200 // total number of models
                                 #define NKGRID 200 // grid points on individual capital grid
/common/definitions.h
                                 #define NKM_GRID 8 // grid points on aggregate capital grid
                                 // Select FPGA design by enabling exactly one of the following macros, keeping the rest to zero. For best performance,
                                 set _ACROSS_ECONOMY to 1 and rest 0
/common/dev options.h
                                 #define _BASELINE 0 // FPGA design with no HLS acceleration.
                                 #define _PIPELINE 0 // FPGA design with only PIPELINE acceleration
                                 #define _WITHIN_ECONOMY 1 // FPGA design with one-kernel data parallelization and pipelining
                                 #define _ACROSS_ECONOMY 0 // FPGA design with three-kernels. Benchmark
/fpga/design.cfg
                                 #############single kernel start##############
                                 [connectivity]
                                 nk=runOnfpga:1:runOnfpga_1
                                 [vivado]
                                 prop=run.impl_1.strategy=Performance_ExtraTimingOpt
Terminal launch:
                                  tmux
                                  make clean
                                 unset XCL_EMULATION_MODE
                                  source $AWS_FPGA_REPO_DIR/vitis_setup.sh
                                  export PLATFORM_REPO_PATHS=$(dirname $AWS_PLATFORM)
                                  export XCL_EMULATION_MODE=hw
```

make afi FPGA\_BIN=1ker\_200k\_8km HOST\_BIN=1200\_1ker\_200k\_8km

#### 1-kernel-300-8 (1200 Economies)

```
/common/app.cpp
                                 #define N MODEL 1200 // total number of models
                                 #define NKGRID 300 // grid points on individual capital grid
/common/definitions.h
                                 #define NKM_GRID 8 // grid points on aggregate capital grid
                                 // Select FPGA design by enabling exactly one of the following macros, keeping the rest to zero. For best performance,
                                 set _ACROSS_ECONOMY to 1 and rest 0
/common/dev options.h
                                 #define _BASELINE 0 // FPGA design with no HLS acceleration.
                                 #define _PIPELINE 0 // FPGA design with only PIPELINE acceleration
                                 #define _WITHIN_ECONOMY 1 // FPGA design with one-kernel data parallelization and pipelining
                                 #define _ACROSS_ECONOMY 0 // FPGA design with three-kernels. Benchmark
/fpga/design.cfg
                                 #############single kernel start##############
                                 [connectivity]
                                 nk=runOnfpga:1:runOnfpga_1
                                 [vivado]
                                 prop=run.impl_1.strategy=Performance_ExtraTimingOpt
Terminal launch:
                                  tmux
                                  make clean
                                 unset XCL_EMULATION_MODE
                                  source $AWS_FPGA_REPO_DIR/vitis_setup.sh
                                  export PLATFORM_REPO_PATHS=$(dirname $AWS_PLATFORM)
                                  export XCL_EMULATION_MODE=hw
```

make afi FPGA\_BIN=1ker\_300k\_8km HOST\_BIN=1200\_1ker\_300k\_8km

#### 1-kernel-100-4-Baseline (120 Economies)

```
/common/app.cpp
                                 #define N MODEL 120 // total number of models
                                 #define NKGRID 100 // grid points on individual capital grid
/common/definitions.h
                                 #define NKM_GRID 4 // grid points on aggregate capital grid
                                 // Select FPGA design by enabling exactly one of the following macros, keeping the rest to zero. For best performance,
                                 set _ACROSS_ECONOMY to 1 and rest 0
/common/dev options.h
                                 #define _BASELINE 1 // FPGA design with no HLS acceleration.
                                 #define _PIPELINE 0 // FPGA design with only PIPELINE acceleration
                                 #define _WITHIN_ECONOMY 0 // FPGA design with one-kernel data parallelization and pipelining
                                 #define _ACROSS_ECONOMY 0 // FPGA design with three-kernels. Benchmark
/fpga/design.cfg
                                 #############single kernel start##############
                                 [connectivity]
                                 nk=run0nfpga:1:run0nfpga_1
                                 [vivado]
                                 prop=run.impl_1.strategy=Performance_ExtraTimingOpt
Terminal launch:
                                  tmux
                                  make clean
                                 unset XCL_EMULATION_MODE
                                  source $AWS_FPGA_REPO_DIR/vitis_setup.sh
                                  export PLATFORM_REPO_PATHS=$(dirname $AWS_PLATFORM)
                                  export XCL_EMULATION_MODE=hw
```

make afi FPGA\_BIN=baseline\_1ker\_100k\_4km HOST\_BIN=120\_1ker\_100k\_4km

#### 1-kernel-100-4-Pipeline (120 Economies)

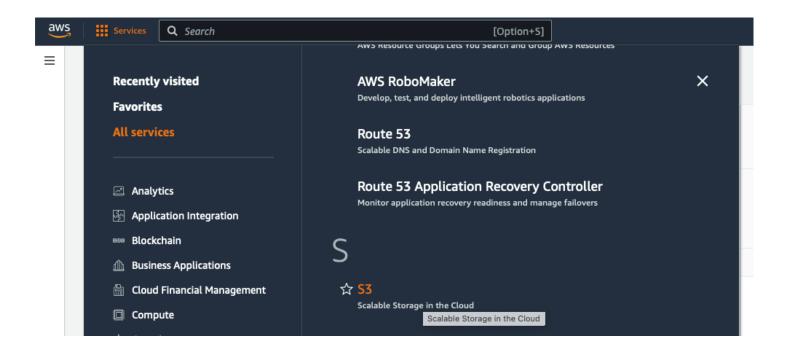
```
/common/app.cpp
                                 #define N MODEL 120 // total number of models
                                 #define NKGRID 100 // grid points on individual capital grid
/common/definitions.h
                                 #define NKM_GRID 4 // grid points on aggregate capital grid
                                 // Select FPGA design by enabling exactly one of the following macros, keeping the rest to zero. For best performance,
                                 set _ACROSS_ECONOMY to 1 and rest 0
/common/dev options.h
                                 #define _BASELINE 0 // FPGA design with no HLS acceleration.
                                 #define _PIPELINE 1 // FPGA design with only PIPELINE acceleration
                                 #define _WITHIN_ECONOMY 0 // FPGA design with one-kernel data parallelization and pipelining
                                 #define _ACROSS_ECONOMY 0 // FPGA design with three-kernels. Benchmark
/fpga/design.cfg
                                 #############single kernel start##############
                                 [connectivity]
                                 nk=run0nfpga:1:run0nfpga_1
                                 [vivado]
                                 prop=run.impl_1.strategy=Performance_ExtraTimingOpt
Terminal launch:
                                  tmux
                                  make clean
                                 unset XCL_EMULATION_MODE
                                  source $AWS_FPGA_REPO_DIR/vitis_setup.sh
                                  export PLATFORM_REPO_PATHS=$(dirname $AWS_PLATFORM)
                                  export XCL_EMULATION_MODE=hw
```

make afi FPGA\_BIN=pipeline\_1ker\_100k\_4km HOST\_BIN=120\_1ker\_100k\_4km

### Delete S3 Buckets

#### S3 Bucket

- Log in your AWS Account
- Navigate > Services > All Services > S3



# Delete the Temporary bucket

- In this example the temporary bucket is named: <u>ksfpga-613520893103</u>
- First empty the bucket and then delete it
- Follow instructions <u>here</u>

