

# Resources on AWS

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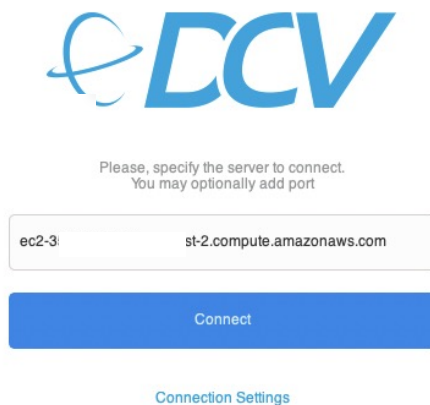
# Steps to retrieve FPGA designs' resources

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- **Step 1.** Connect to a remote development instance (z1d.2xlarge). Refer to `./documents/FPGA-designs.pdf` for a guide on how to do it.
- **Step 2.** Transfer the `./l_estimation_results/resources/xrt_*.run_summary` files from your terminal to the remote development instance (z1d.2xlarge). If you are using Visual Studio Code, you can drag and drop these files directly into the appropriate folder on the remote instance you are connected to.
- **Step 3. Launch a NICE DCV Remote Desktop session (next slide)**

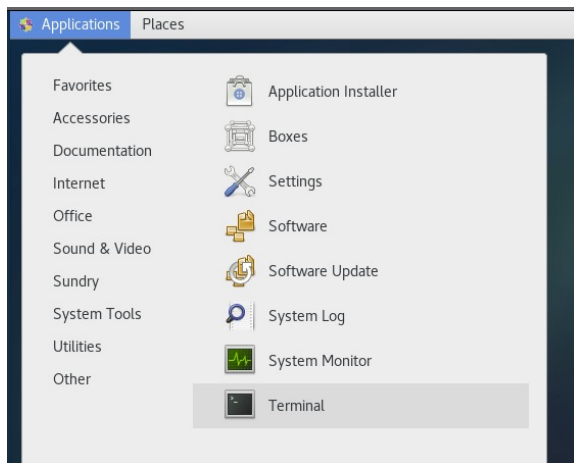
# Start NICE DCV Remote Desktop Session

1. Install the remote desktop manager NICE DCV in your computer and in your development instance, z1d.2xlarge. See instruction [here](#) and [here](#).
2. Launch a DCV session from the terminal of your development instance, `z1d.2xlarge` `dcv create-session centos`
3. Launch the NICE DCV app on your computer
  - To log-in: put the Public ip address of your AWS instance (left)
  - As username use Centos. As password use the password you set up at step 1 (right).



# Launch Vitis Analyzer

1. In the NICE DCV Remote Desktop, Open the terminal: **Applications > System Tools > Terminal**



2. Type `vitis_analyzer &` to launch the Vitis Analyzer app

```
centos@ip-10-0-4-134:~  
File Edit View Search Terminal Help  
Traceback (most recent call last):  
  File "/home/centos/anaconda3/bin/conda", line 7, in <module>  
    from conda.cli import main  
ModuleNotFoundError: No module named 'conda'  
centos@ip-10-0-4-134 ~]$ vitis_analyzer &  
1] 4724  
centos@ip-10-0-4-134 ~]$ XILINX_XRT : /opt/xilinx/xrt  
PATH : /opt/xilinx/xrt/bin:/opt/Xilinx/Vitis_HLS/2021.2/bin:/opt/Xi  
linx/Vitis/2021.2/bin:/opt/Xilinx/Vivado/2021.2/bin:/usr/local/bin:/bin:/usr/bin  
/usr/local/sbin:/usr/sbin:/srv/git/centos-git-common:/home/centos/.local/bin:/h  
me/centos/bin:/srv/git/centos-git-common  
D LIBRARY_PATH : /opt/xilinx/xrt/lib:  
YTHONPATH : /opt/xilinx/xrt/python:  
  
**** Vitis Analyzer v2021.2 (64-bit)  
**** SW Build 3367213 on Tue Oct 19 02:47:39 MDT 2021  
** Copyright 1986-2021 Xilinx, Inc. All Rights Reserved.  
  
tart_gui
```

# Vitis Analyzer

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## VITIS ANALYZER

### OPEN

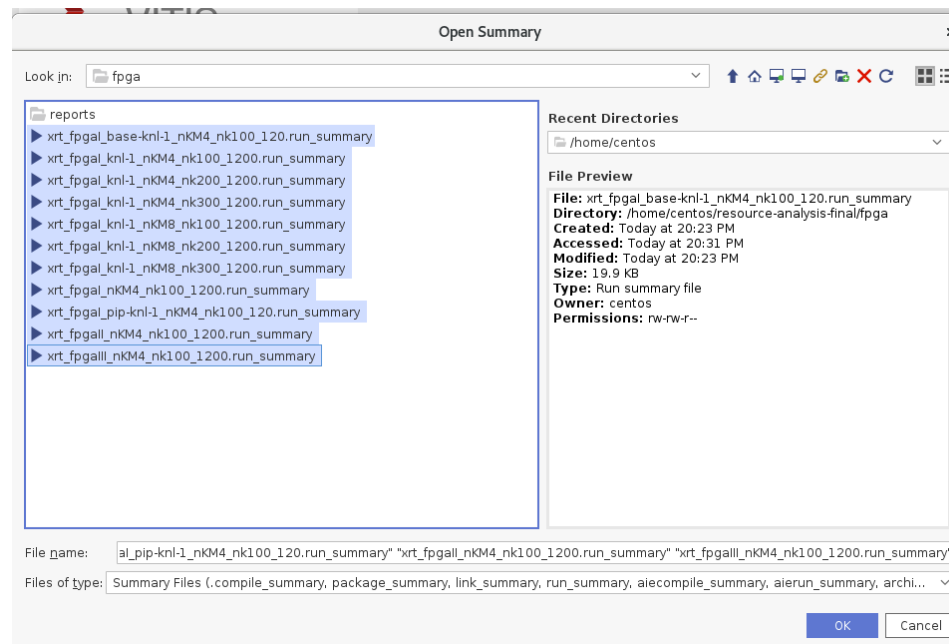
[Open Summary](#)  
[Open Binary Container](#)  
[Open Directory](#)

### RESOURCES

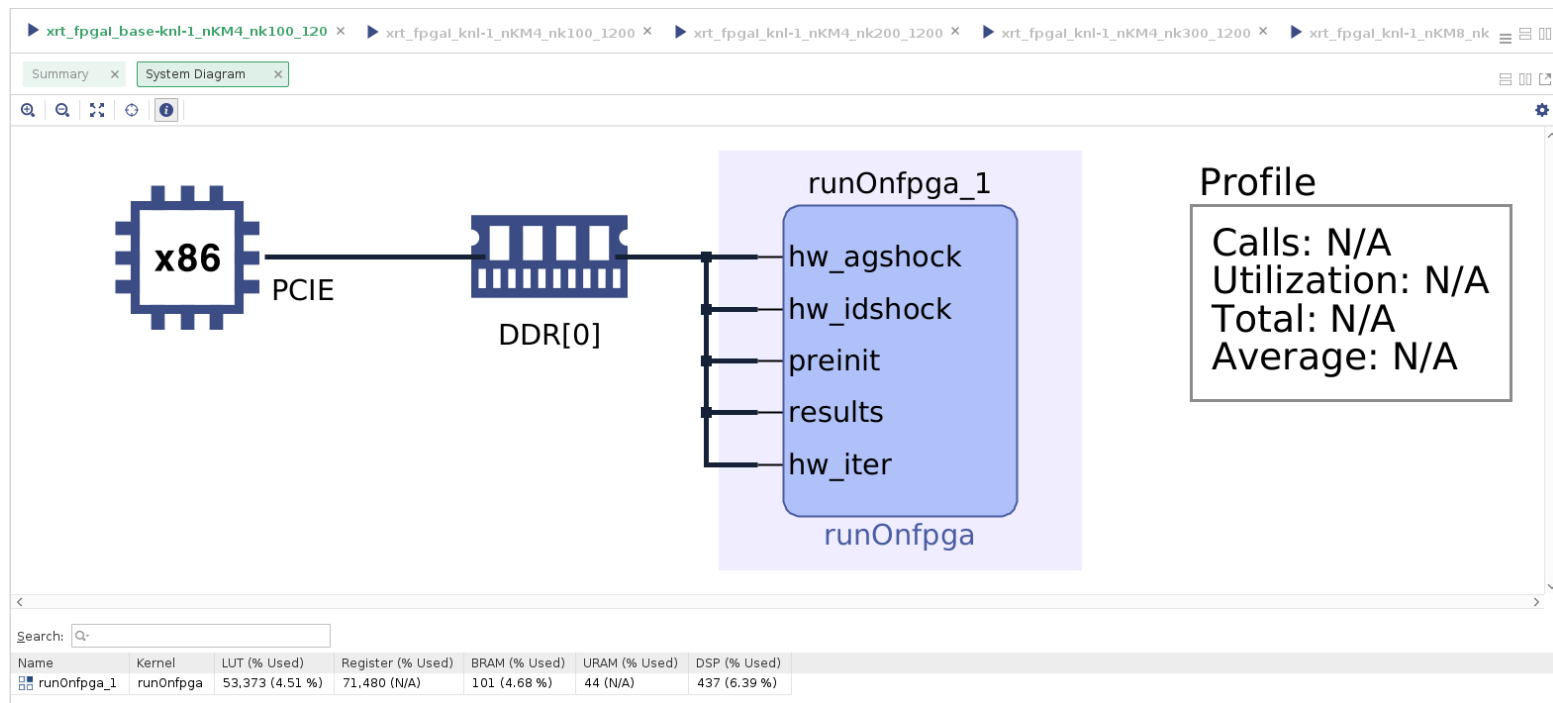
[Documentation](#)  
[Xilinx Developer](#)

# Analyse the Reports

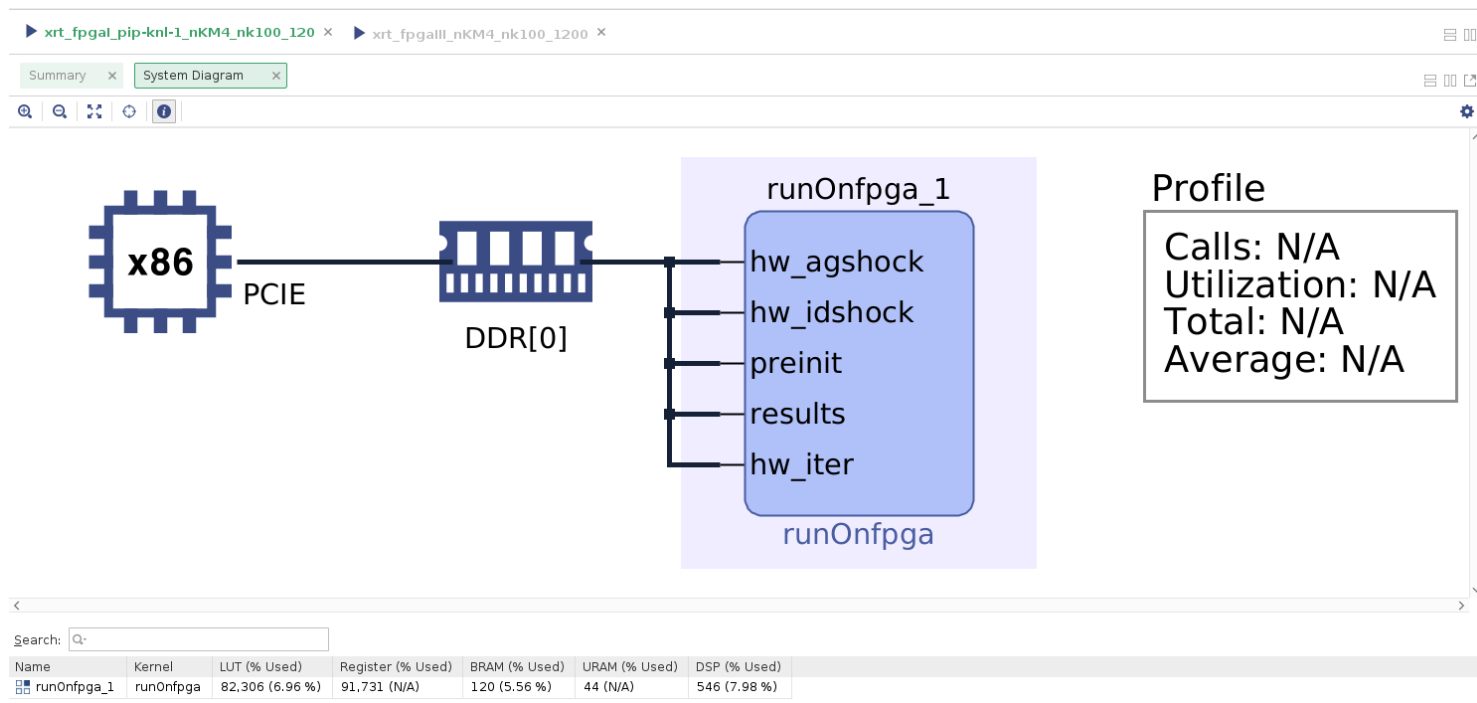
1. In the Vitis analyzer, File > Open Summary
2. Collect the reports



# baseline

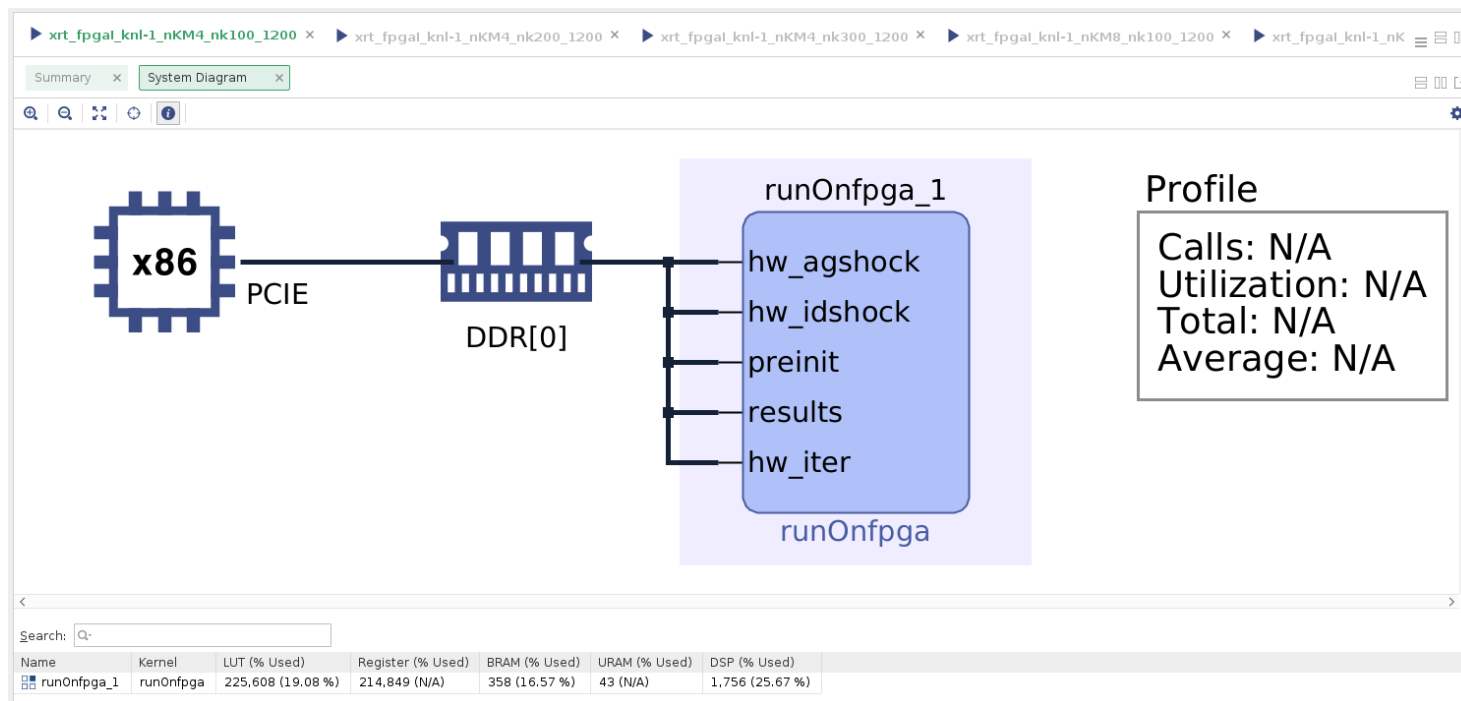


# Kn1-pipeline-100-4

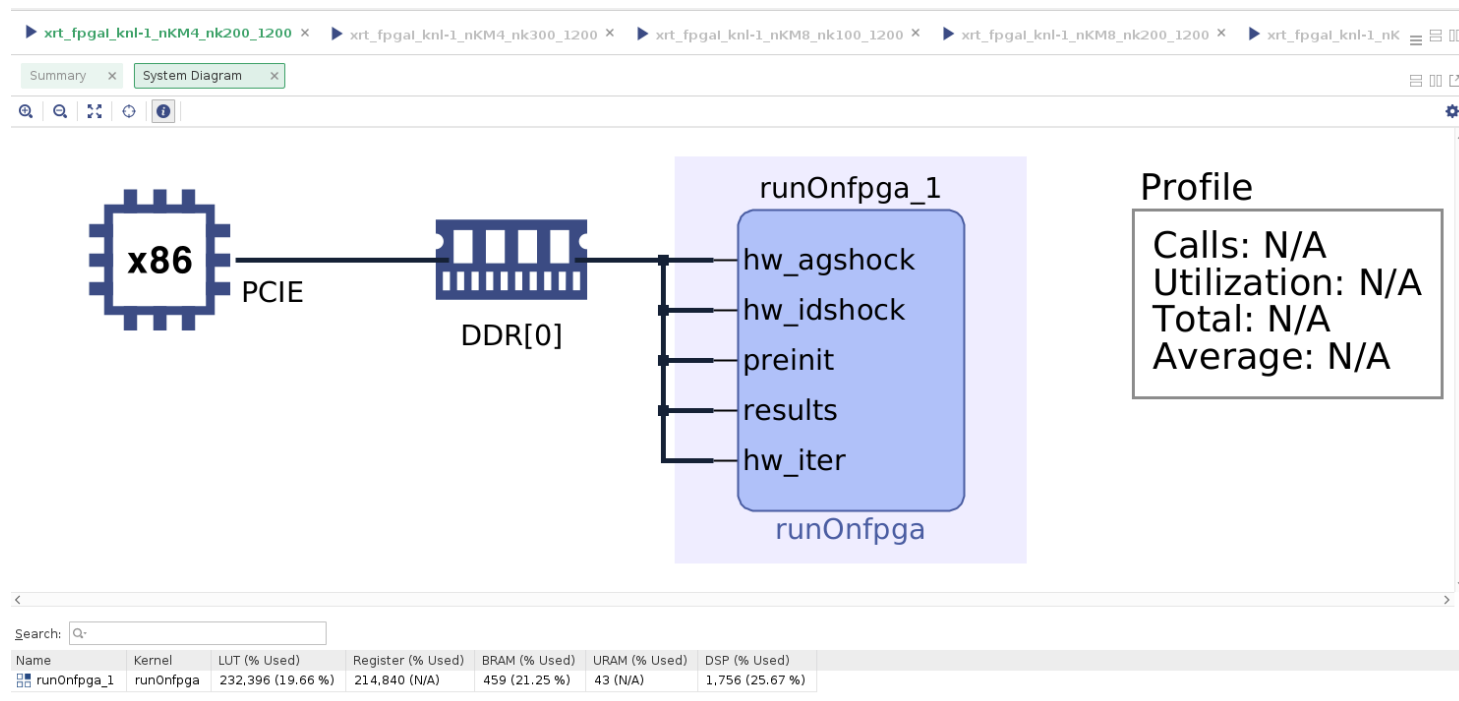




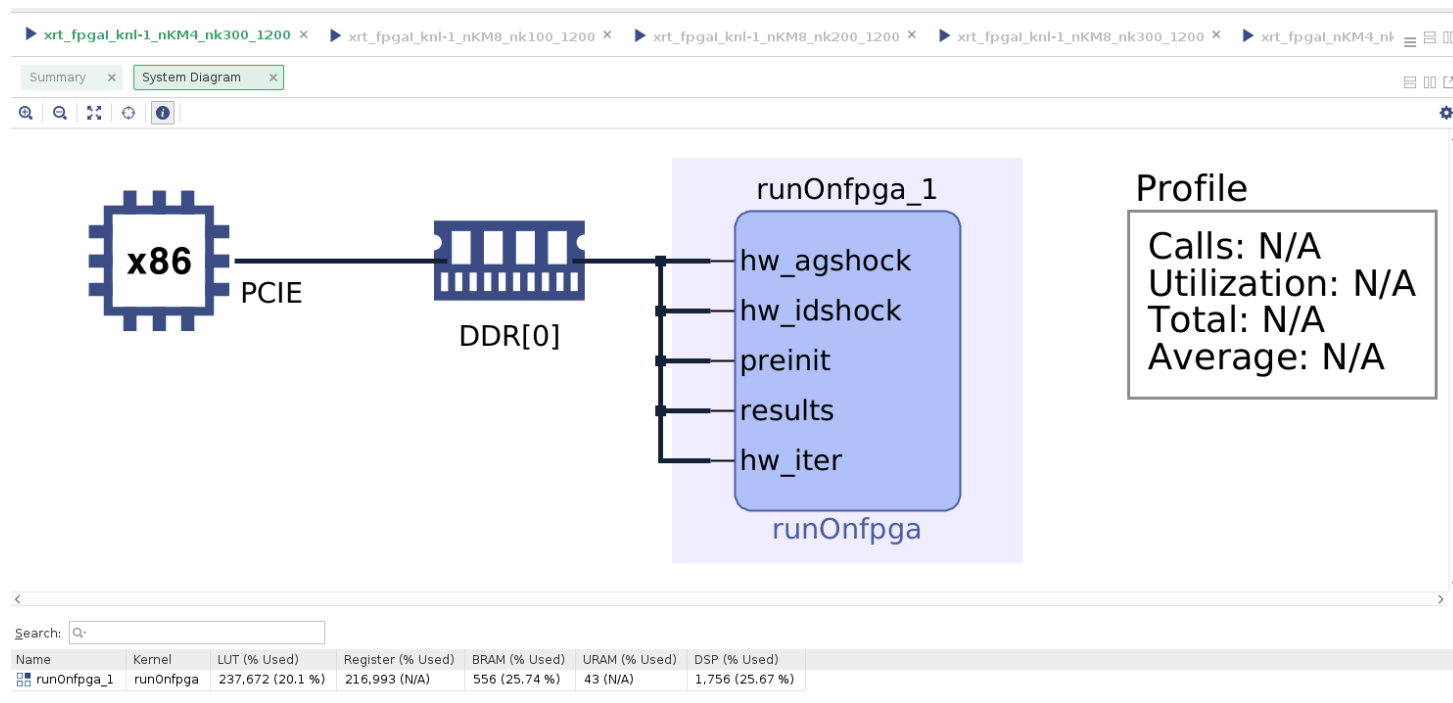
# Kni-100-4



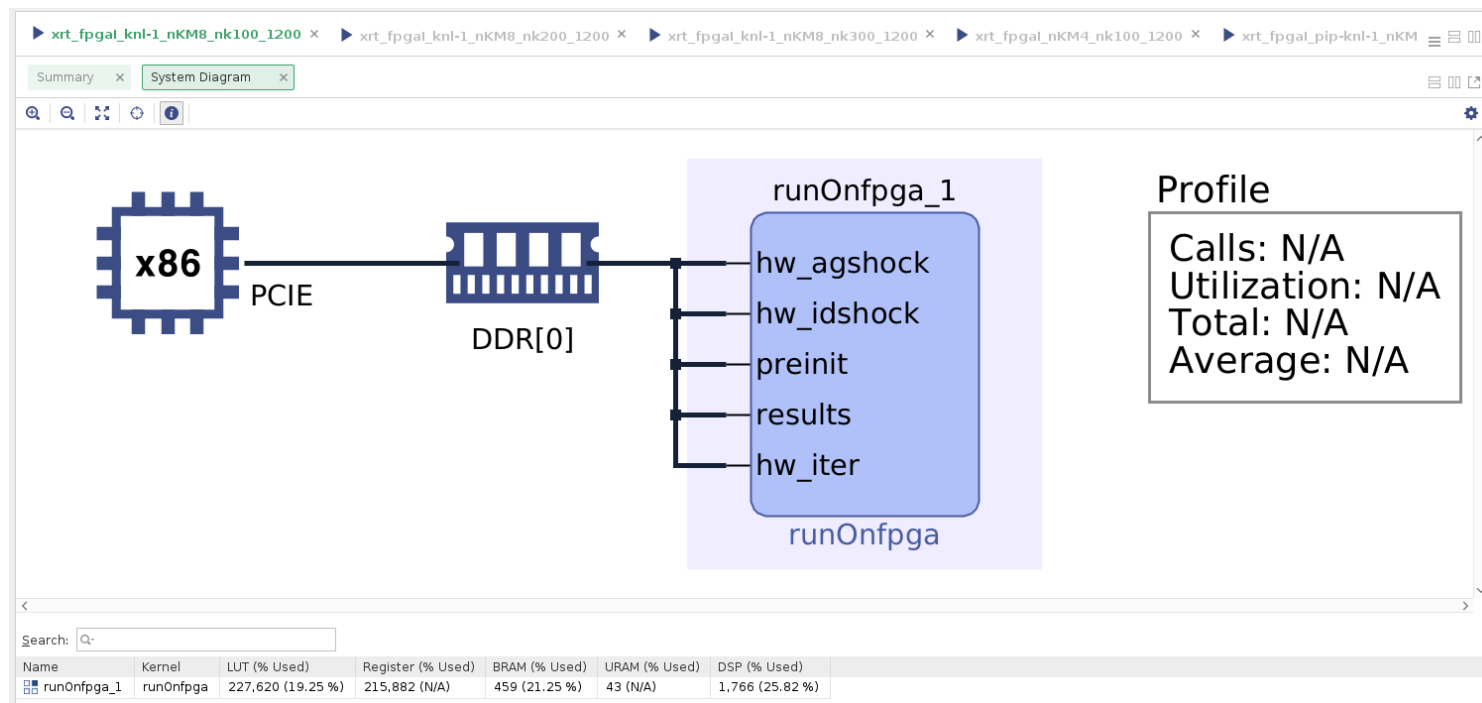
# kn1-200-4



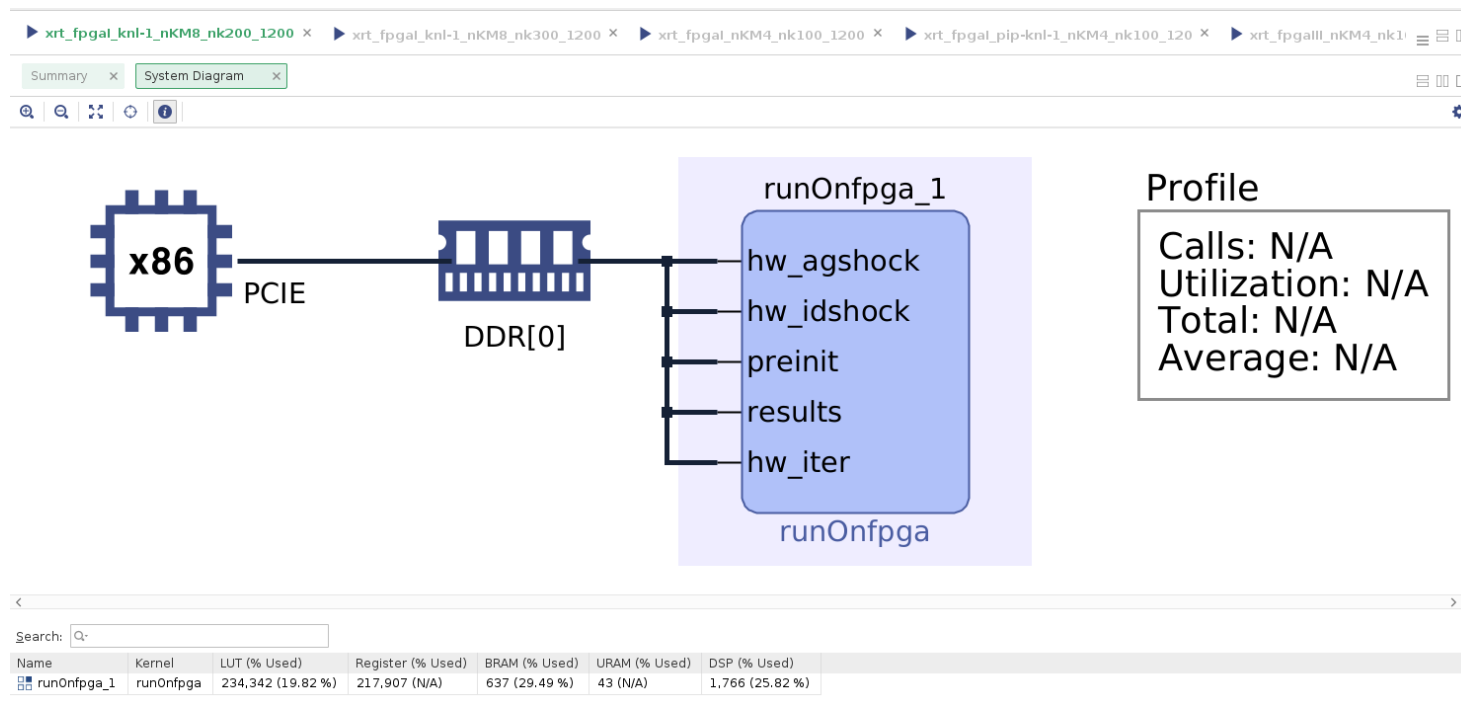
# kn1-300-4



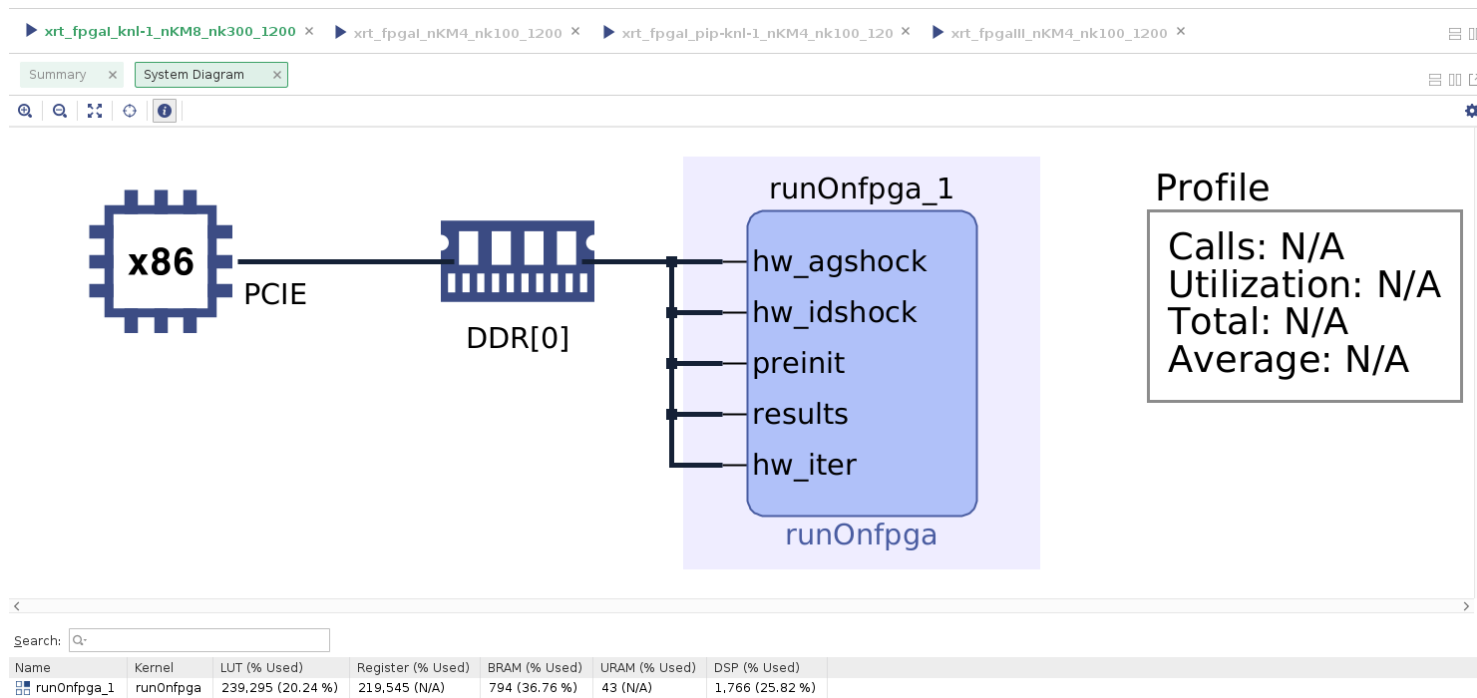
# Kn1-100-8



# Kn1-200-8



# Kn1-300-8



# Kn3-100-4

