

The timing diagram illustrates the behavior of a 4-bit counter and its associated signals over a 30-second period. The clock signal (clk=1) is a periodic square wave. The counter output (numero[7:0]) starts at 00 and increments by 1 on each clock edge, reaching 08 at the end of the 30-second interval. The result signal (result[7:0]) is initially in a high-impedance state (xx) and becomes valid (00) when the counter reaches 08. The res[7:0] signal is also in a high-impedance state (xx) and becomes valid (00) when the counter reaches 08. The res[7:0] signal is then updated to 0A at the next clock edge and remains at 0A until the counter reaches 0E, where it is updated to 10. The res[7:0] signal is then updated to 1C at the next clock edge and remains at 1C until the counter reaches 1E, where it is updated to 20. The res[7:0] signal is then updated to 20 at the next clock edge and remains at 20 until the counter reaches 2E, where it is updated to 20. The res[7:0] signal is then updated to 20 at the next clock edge and remains at 20 until the counter reaches 2E, where it is updated to 20.

Time	clk=1	numero[7:0]	result[7:0]	res[7:0]
00	0	00	xx	xx
01	1	01	xx	xx
02	0	02	xx	xx
03	1	03	xx	xx
04	0	04	xx	xx
05	1	05	xx	xx
06	0	06	xx	xx
07	1	07	xx	xx
08	0	08	00	xx
09	1	09	00	xx
10	0	0A	00	xx
11	1	0B	00	xx
12	0	0C	00	xx
13	1	0D	00	xx
14	0	0E	00	xx
15	1	0F	00	xx
16	0	10	0A	xx
17	1	11	0A	xx
18	0	12	0A	xx
19	1	13	0A	xx
20	0	14	0A	xx
21	1	15	0A	xx
22	0	16	0A	xx
23	1	17	0A	xx
24	0	18	0A	xx
25	1	19	0A	xx
26	0	1A	0A	xx
27	1	1B	0A	xx
28	0	1C	0A	xx
29	1	1D	0A	xx
30	0	1E	0A	xx

[illegible]

The timing diagram illustrates the behavior of a 4-bit counter and its associated signals over a 30-second period. The clock signal (clk=1) is a periodic square wave. The counter output (numero[7:0]) starts at 00 and increments by 1 on each clock edge, reaching 08 at the end of the 30-second interval. The result signal (result[7:0]) is initially in a high-impedance state (xx) and becomes valid (00) when the counter reaches 08. The res[7:0] signal is also in a high-impedance state (xx) and becomes valid (00) when the counter reaches 08. The res[7:0] signal is then updated to 0A at the next clock edge and remains at 0A until the counter reaches 0E, where it is updated to 10. The res[7:0] signal is then updated to 1C at the next clock edge and remains at 1C until the counter reaches 1E, where it is updated to 20. The res[7:0] signal is then updated to 20 at the next clock edge and remains at 20 until the counter reaches 2E, where it is updated to 20. The res[7:0] signal is then updated to 20 at the next clock edge and remains at 20 until the counter reaches 2E, where it is updated to 20.

Time	clk=1	numero[7:0]	result[7:0]	res[7:0]
00	0	00	xx	xx
01	1	01	xx	xx
02	0	02	xx	xx
03	1	03	xx	xx
04	0	04	xx	xx
05	1	05	xx	xx
06	0	06	xx	xx
07	1	07	xx	xx
08	0	08	00	xx
09	1	09	00	xx
10	0	0A	00	xx
11	1	0B	00	xx
12	0	0C	00	xx
13	1	0D	00	xx
14	0	0E	00	xx
15	1	0F	00	xx
16	0	10	0A	xx
17	1	11	0A	xx
18	0	12	0A	xx
19	1	13	0A	xx
20	0	14	0A	xx
21	1	15	0A	xx
22	0	16	0A	xx
23	1	17	0A	xx
24	0	18	0A	xx
25	1	19	0A	xx
26	0	1A	0A	xx
27	1	1B	0A	xx
28	0	1C	0A	xx
29	1	1D	0A	xx
30	0	1E	0A	xx