AS72651

6-Channel NIR *Spectral_ID* device with Electronic Shutter & Smart Interface

General Description

The AS72651 is a digital 6-channel spectrometer for spectral identification in the near IR light wavelengths. It has 6 independent optical filters whose spectral response is defined in the NIR wavelengths from 600nm to 1,000nm with FWHM of 20nm. The device also has LED drivers with programmable currents that are provided for electronic shutter applications.

The AS72651, AS72652 (spectral response from 560nm to 940nm with FWHM of 20nm), and AS72653 (spectral response from 410nm to 535nm with FWHM of 20nm) form a 18-channel spectrometer.

The AS72651 integrates band-pass/Gaussian filters into standard CMOS silicon via Nano-optic deposited interference filter technology and is packaged an LGA package that provides a built in aperture to control the light entering the sensor array.

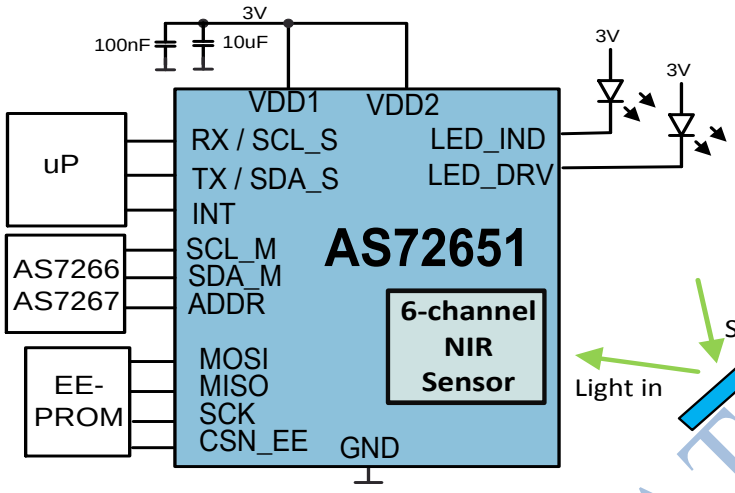
Key Benefits and Features

Figure 1: AS72651 Benefits and Features

Benefits	Features
Very accurate light measurements	Across selected bandwidths
6-channel spectrometer	FWHM of 20nm
No lifetime drift with high temperature stability	Filters realized by silicon interference filters
UART or I^2C digital Interface	Direct register/sensor read and write (I^2C), or, Smart AT commands, no driver needed (UART)
Signal conditioning not necessary	Digital sensor 16-bit ADC with digital access
LED Driver output	Programmable LED driver current outputs
Temperature monitoring	On-chip temperature sensor
Commercial temperature range	Temperature range: -40 to 85°C
Low voltage operation	VDD LV range: 2.7V to 3.6V with I^2C interface
Enables very small PCB design.	20 pin LGA package

Application

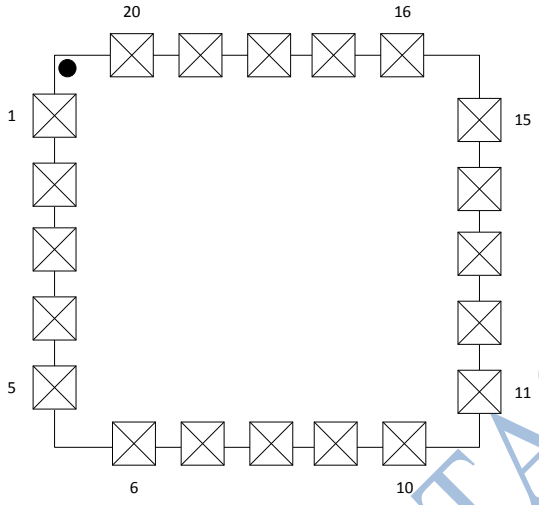
Figure 2: 18-Channel *Spectral_ID* System



18-Channel Spectral_ID System: This figure shows the uP connection to AS72651 6-Channel *Spectral_ID* Sensor and the connection to AS72652/AS72653 *Spectral_ID* sensors.

Pin Assignment

Figure 3: AS72651 Pin assignment



AS72651 Pin Assignment: This figure shows the pin assignment and location viewed from top for LGA package.

Pin Description

Figure 4: AS72651 Pin Description

Pin #	Pin Name	Pin Type	Description
1	SDA_M	Digital Input and Output	I^2C master data for communicating with AS72652 and AS72653
2	RESN	Digital Input	Reset pin, active low
3	SCK	Digital Output	SPI serial clock
4	MOSI	Digital Input and Output	SPI MOSI
5	MISO	Digital Input and Output	SPI MISO
6	CSN_EE	Digital Output	Chip select for external EEPROM, active low
7	CSN_SD	Digital Output	Chip select for SD Card interface, active low
8	I2C_ENB	Digital Input	Selects UART (low) or I^2C (high) operation
9	INT	Digital Output (open drain)	INT is active Low
10	NF		Not Functional. No Connect
11	RX / SCL_S	Digital Input	RX (UART) or SCL_S (I^2C slave) depending on I2C_ENB setting

12	TX / SDA_S	Digital Input and Output	TX (UART) or SDA_S (I^2C slave) depending on I2C_ENB setting
13	ADDR	Digital Output (open drain)	Sets address for AS72653
14	VDD2	Voltage Supply	Voltage Supply
15	LED_DRV	Analog Output	LED Driver output for driver LED, current sink
16	GND	Supply	Ground
17	VDD1	Voltage Supply	Voltage Supply
18	LED_IND	Analog Output	LED Driver output for Indicator LED, current sink
19	NF		Not Functional. No Connect
20	SCL_M	Digital Output	I^2C master clock for communicating with AS72652 and AS72653

Ordering Information

Figure 5: AS72651 Ordering Information

Ordering Code	Description	Delivery Form	Package
AS72651-xxxx	6 Channel NIR Spectrometer	Tape & Reel	20-pin LGA

Note:

- All products are RoHS compliant and ams green.
- Buy our products or get free samples online at www.ams.com/ICdirect
- Technical Support is available at www.ams.com/Technical-Support
- For further information and requests, email us at sales@ams.com
- (or) find your local distributor at www.ams.com/distributor

Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under “Operating Conditions” is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 6: AS72651 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Comments
Electrical Parameters					
V_{DD1_MAX}	Supply voltage VDD1	-0.3	5	V	pin VDD1 to GND,
V_{DD2_MAX}	Supply voltage VDD2	-0.3	5	V	pin VDD2 to GND,
V_{DD1_IO}	VDD1-VDD2 spec	-0.3	VDD1 + 0.3	V	Voltage pins to GND
V_{DD2_IO}	VDD2-VDD1 spec	-0.3	VDD2 + 0.3	V	Voltage pins to GND
Electrostatic Discharge					
V_{ESD}	Electrostatic discharge	±2		kV	Norm: JS-001-2014
Temperature Ranges and Storage Conditions					
T_{STRG}	Storage temperature	-40	85	°C	
T_{BODY}	Package Body Temperature		260	°C	Norm: IPC/JEDEC J-STD-020. The reflow peak soldering temperature (body temperature) is specified according IPC/JEDEC J-STD-020 “Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices”
	Humidity non-condensing	5	85	%	
	Moisture Sensitive Level	3			Represents a 168 hours max. floor life time

Optical Characteristics

Data Conversion Description

AS72651 spectral conversion is implemented via two Photodiode banks per device. The First Bank, Bank 0 consists of data from the S, T, U, V Photodiodes. Bank 1 consists of data from the R, T, U, W Photodiodes. The first conversion of Bank 0 requires the integration time set (IT mSecs) to complete (minimum integration time is 2.8msecs); the 2nd conversion requires an additional IT mSecs. If data is required from all 6 photodiodes then the device must perform 2 full conversions (2 x Integration Time). When the data is ready the Data_RDY bit will be set high.

BANK Mode 0: Data will be available in registers S, T, U & V (R and W registers will be zero)

BANK Mode 1: Data will be available in registers R, T, U & W (V and W registers will be zero)

BANK Mode 2: Data will be available in registers R, S, T, U, V & W

When the bank setting is Mode 0, Mode 1, or Mode 2, the spectral data conversion process operates continuously, with new data available after each IT mSecs period. In the continuous modes, if an external microprocessor is not vigilant about responding to interrupts promptly, it may be possible for, say, the S, T, and V register values to have come from one spectral conversion cycle, and the U register value to come from the following spectral conversion cycle.

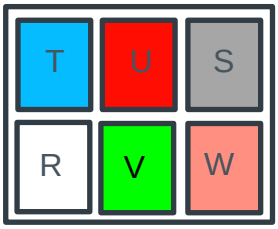
The AS72651 functions as a controller for the AS72652 and AS72653 to allow for an eighteen channel spectral data conversion solution. Whenever the AS72651 detects the presence of accompanying AS72652 and AS72653 devices it will confirm them for the same conversion modes as itself. For the eighteen channel:

Bank Mode 0: Data will be available in registers S, T, U, V; I, G, H, K; C, A, B, E;

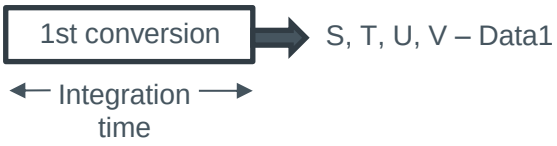
Bank Mode 1: Data will be available in registers R, T, U, W; J, G, H, L; D, A, B, F;

Bank Mode 2: Data will be available in registers R, S, T, U, V, W; J, I, G, H, K, D; D, C, A, B, E, F;

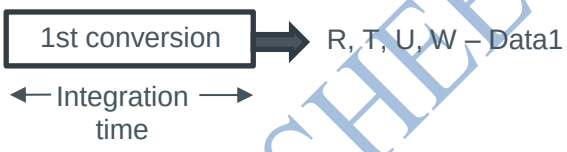
Photo Diode Array



BANK Mode 0



BANK Mode 1



BANK Mode 2

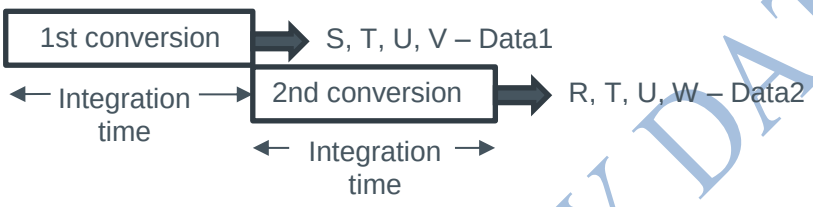
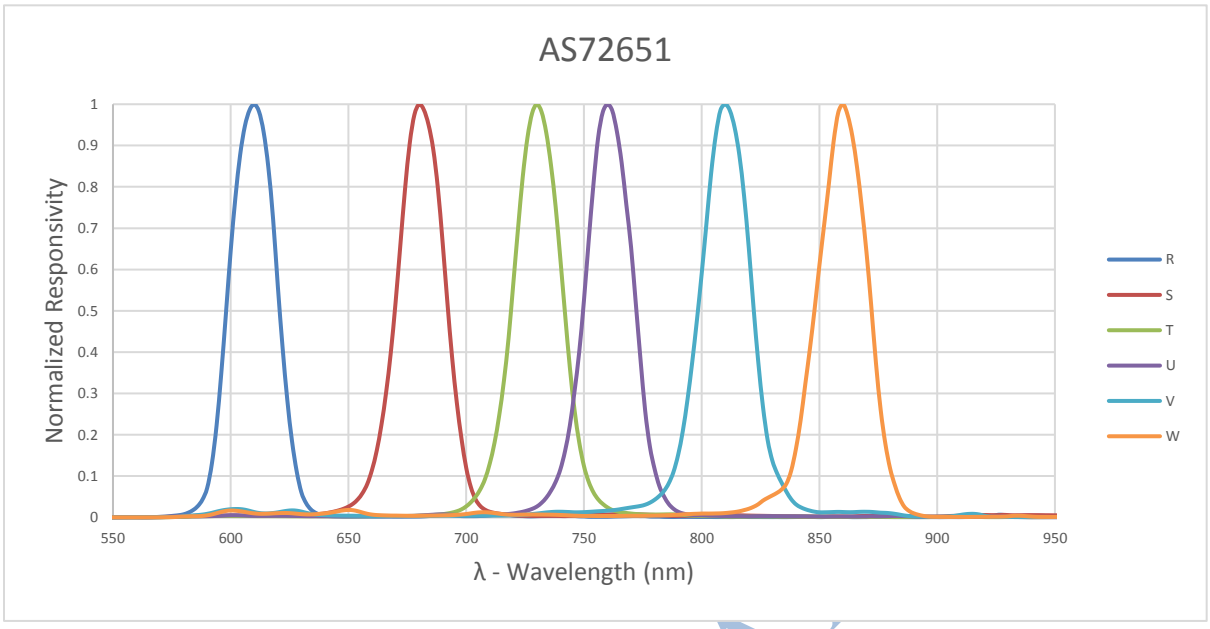
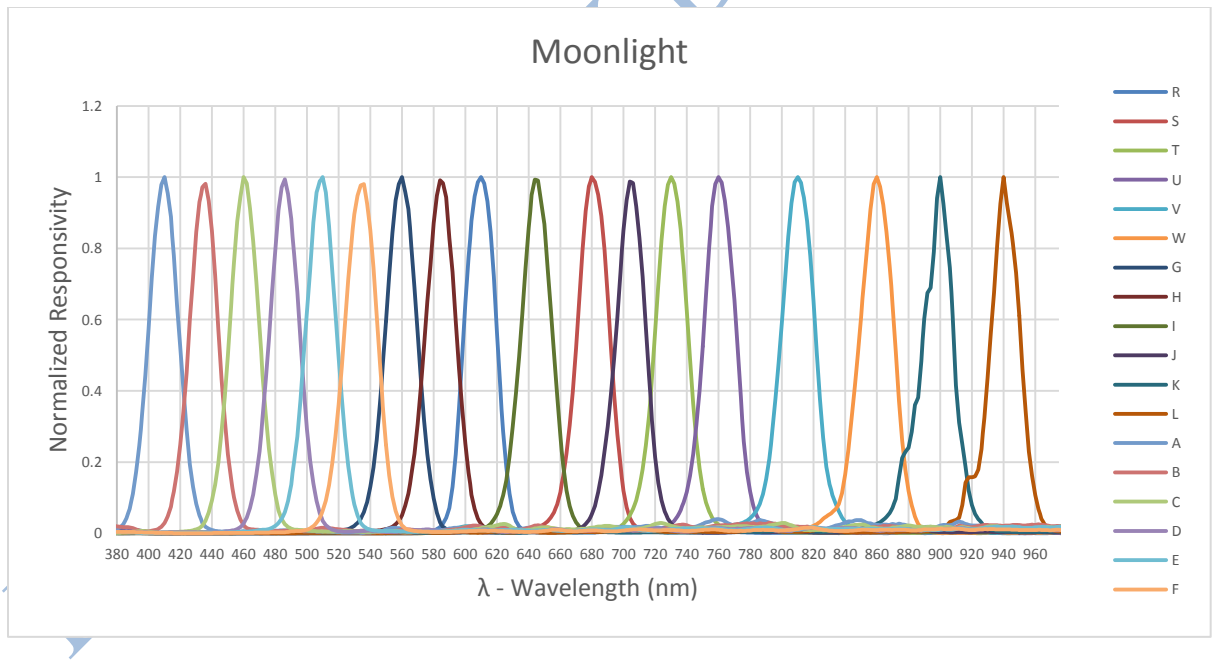


Figure 7: Typical Spectral Responsivity



6-Channel *Spectral_ID* Gaussian Filters Typical Optical Characteristics: This figure shows the spectral response of the AS72651 6-Channel *Spectral_ID* Sensor.



18-Channel *Spectral_ID* Gaussian Filters Typical Optical Characteristics: This figure shows the spectral response of the 18-Channel *Spectral_ID* Sensor.

Figure 8: AS7265 Optical Characteristics (Pass band)

Symbol	Parameter	Test Conditions	Channel (nm)	Min	Typ	Max	Unit
R	Channel R	Incandescent(1, 3)	610		35		counts/ (µW/cm^2)
S	Channel S	Incandescent(1, 3)	680		35		counts/ (µW/cm^2)
T	Channel T	Incandescent(1, 3)	730		35		counts/ (µW/cm^2)
U	Channel U	Incandescent(1, 3)	760		35		counts/ (µW/cm^2)
V	Channel V	Incandescent(1, 3)	810		35		counts/ (µW/cm^2)
W	Channel W	Incandescent(1, 3)	860		35		counts/ (µW/cm^2)
FWHM	Full Width Half Max		20		20		nm
Wacc	Wavelength accuracy				+/-5		nm
dark	Dark channel counts	GAIN=64, T_{AMB}=25°C				5	counts
f	Angle of incidence			-10	0	10	deg

Note 1: Each channel is tested with GAIN = 16X, Integration Time (INT_T) = 166ms and VDD = VDD1 = VDD2 = 3.3V, T_{AMB}=25°C
Note 2: The accuracy of the channel counts should be +/- 10%
Note 3: The source light is an incandescent light with an irradiance of ~1500uW/cm2 (300-1000nm). The energy at each channel (R, S, T, U, V, W) is calculated with a +/- 33nm bandwidth around the center wavelengths (610, 680, 730, 760, 810, 860nm).

Optical Characteristics: This figure shows the pass band optical characteristics of the AS72651

Electrical Characteristics

All limits are guaranteed with VDD = VDD1 = VDD2 = 3.3V,T_{AMB} = +25ºC. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Figure 9: AS72651 Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
General Operating Conditions						
VDD1 /VDD2	Voltage Operating Supply	UART Interface	2.97	3.3	3.6	V
VDD1 /VDD2	Voltage Operating Supply	I²C Interface	2.7	3.3	3.6	V
T_{AMB}	Operating Temperature		-40	25	85	°C
I_{VDD}	Operating Current				5	mA
$I_{STANDBY}$(1)	Standby Current			12		µA
Internal RC Oscillator						
F_{OSC}	Internal RC oscillator frequency		15.7	16	16.3	MHz
t_{JITTER}(2)	Internal clock Jitter	@25°C			1.2	ns
Temperature Sensor						
D_{TEMP}	Absolute accuracy of the temperature measurement		-5		5	°C
Indicator LED						
I_{IND}	LED Current		1	4	8	mA
I_{ACC}	Accuracy of Current		-10		10	%
V_{LED}	Voltage range of connected LED	Vds of current sink	0.2			V
LED_DRV						
I_{LED1}	LED Current	12.5, 25, 50 or 100	12.5		100	mA
I_{ACC}	Accuracy of Current		-10		10	%
V_{LED}	Voltage range of connected LED	Vds of current sink	0.2			V
Digital Inputs and Outputs						
I_{IH}, I_{IL}	Logic Input Current	Vin=0V or VDD	-1		1	uA

V_{IH}	CMOS Logic High Input		0.7* VDD		VDD	V
V_{IL}	CMOS Logic Low Input		0		0.3* VDD	V
V_{OH}	CMOS Logic High Output	I=1mA			VDD-0.4	V
V_{OL}	CMOS Logic Low Output	I=1mA			0.4	V
t_{RISE}(2)	Current rise time	C(Pad)=30pF			5	ns
t_{FALL}(2)	Current fall time	C(Pad)=30pF			5	ns

Note(s) and/or Footnote(s):

1. 15uA with over temperature
2. Guaranteed, not tested in production

Figure 10: AS72651 I²C Slave Timing Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I²C Interface						
f_{SCLK}	SCL Clock Frequency		0		400	kHz
t_{BUF}	Bus Free Time Between a STOP and START		1.3			µs
$t_{HD:STA}$	Hold Time (Repeated) START		0.6			µs
t_{LOW}	LOW Period of SCL Clock		1.3			µs
t_{HIGH}	HIGH Period of SCL Clock		0.6			µs
$t_{SU:STA}$	Setup Time for a Repeated START		0.6			µs
$t_{HD:DAT}$	Data Hold Time		0		0.9	µs
$t_{SU:DAT}$	Data Setup Time		100			ns
t_R	Rise Time of Both SDA and SCL		20		300	ns
t_F	Fall Time of Both SDA and SCL		20		300	ns
$t_{SU:STO}$	Setup Time for STOP Condition		0.6			µs

C_B	Capacitive Load for Each Bus Line	CB — total capacitance of one bus line in pF			400	pF
$C_{I/O}$	I/O Capacitance (SDA, SCL)				10	pF

Figure 11: I²C Slave Timing Diagram

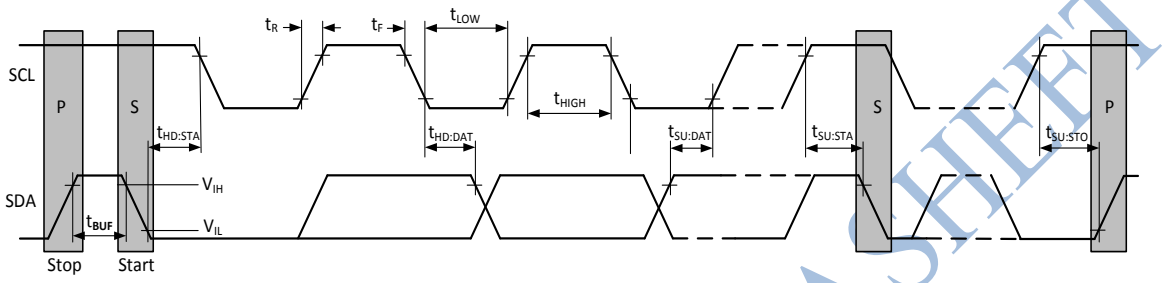


Figure 12: AS72651 SPI Timing Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SPI Interface						
f_{SCK}	Clock frequency		0		16	MHz
t_{SCK_H}	Clock high time		40			ns
t_{SCK_L}	Clock low time		40			ns
t_{SCK_RISE}	SCK rise time		5			ns
t_{SCK_FALL}	SCK fall time		5			ns
t_{CSN_S}	CSN setup time	Time between CSN high-low transition to first SCK high transition	50			ns
t_{CSN_H}	CSN hold time	Time between last SCK falling edge and CSN low-high transition	100			ns
t_{CSN_DIS}	CSN disable time		100			ns
t_{DO_S}	Data-out setup time		5			ns
t_{DO_H}	Data-out hold time		5			ns
t_{DI_V}	Data-in valid		10			ns

Note(s) and/or Footnote(s):

1. Guaranteed, not tested in production

Figure 13: SPI Master Write Timing Diagram

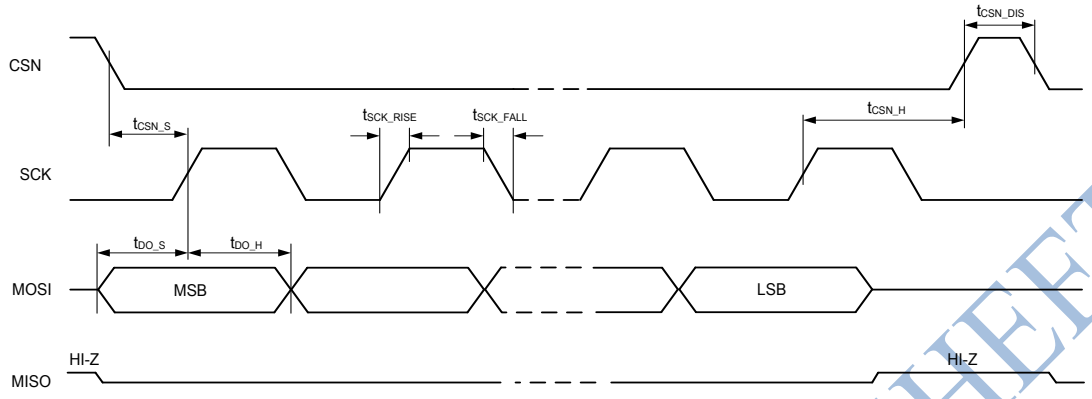
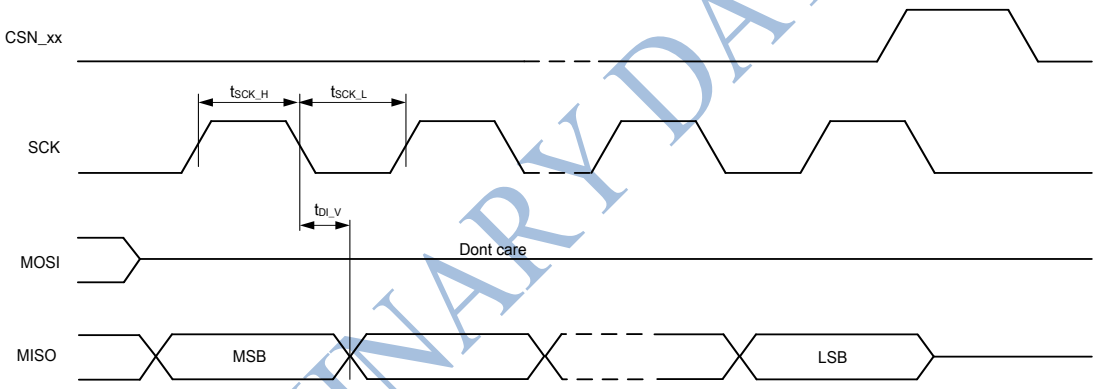
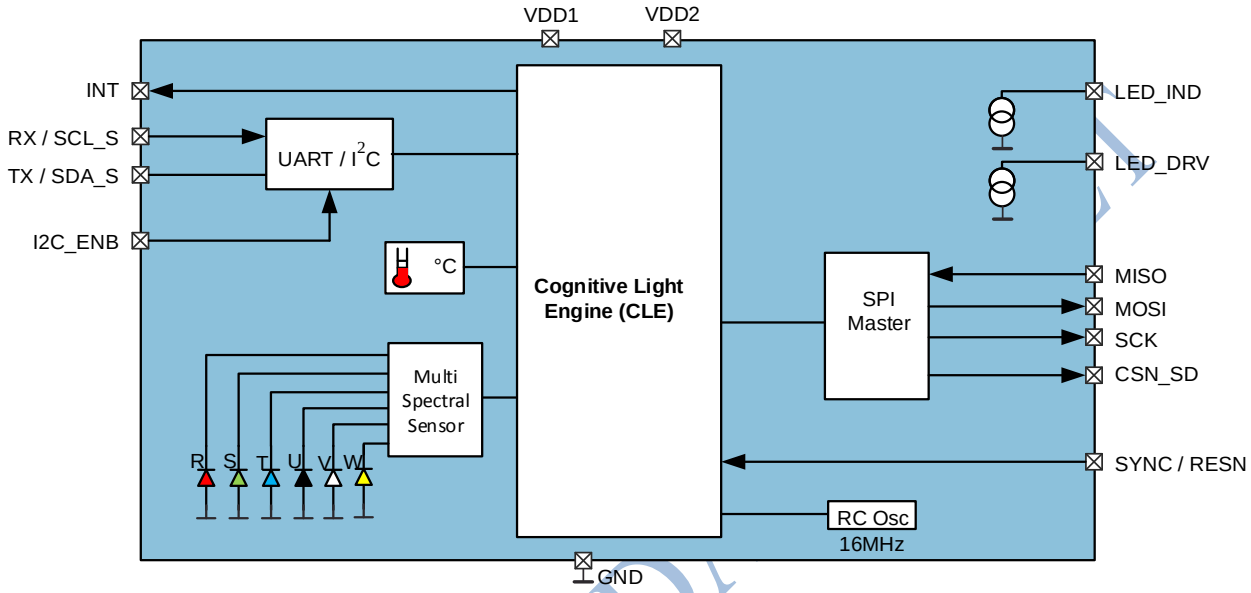


Figure 14: SPI Master Read Timing Diagram



Detailed Descriptions

Figure 15: Internal Block Diagram



6-channel NIR *Spectral_ID* detector

The 6-channel *Spectral_ID* is a next-generation digital spectral sensor device. Each channel has a Gaussian/Band-pass filter characteristic with a FWHM (Full Width Half maximum) bandwidth of 20nm. The channels are spaced roughly at 50nm intervals in the NIR spectrum: R, S, T, U, V, W. The sensor contains an integrating analog-to-digital converter (16-bit resolution ADC), which integrates the current from a photodiode. Upon completion of the conversion cycle, the conversion result is transferred to the corresponding data registers. The transfers are double-buffered to ensure that the integrity of the data is maintained.

Interference filters realize the response, which enables no lifetime drift and very high temperature stability. Interference filters are sensitive to the angle of incidence. Maintaining 0° angle (+/-20.5° max) of incidence will give the specified results. Ensure, by using optics or apertures, to stay within +/- 20.5° angle of incidence. Angles of light beyond this may shift the spectral response of the filters. The LGA package aperture controls the light input to maintain the 0° angle constraint at the sensors.

RC Oscillator

The timing generation circuit consists of an on-chip 16MHz, temperature compensated, oscillator, which provides the master clock for the AS72651.

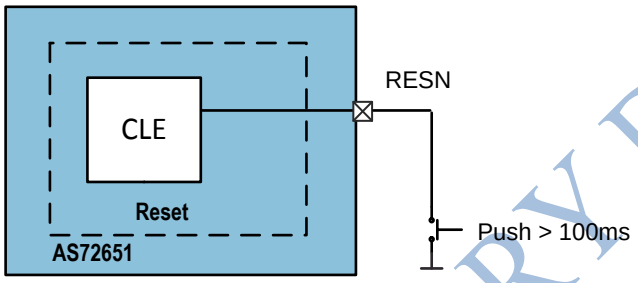
Temperature Sensor

The Temperature Sensor is constantly measuring the on-chip temperature and enables temperature compensation procedures.

Reset

Pulling down the RESN pin for longer than 100ms resets the AS72651.

Figure 16: Reset Circuit



Indicator LED

The LED, connected to pin LED_IND, can be used to indicate programming progress of the device.

While programming the AS72651 via the external SD card the indicator LED starts flashing (500ms pulses). When programming is completed the indicator LED is switched off. The LED (LED0) can be turned ON/OFF via AT commands or via I^2C register control. The LED sink current is programmable from 1mA, 2mA, 4mA and 8mA.

Electronic Shutter with LED_DRV Driver Control

There are two LED driver outputs that can be used to control up to 2 LEDs. This will allow different wavelength light sources to be used in the same system. The LED output sink currents are programmable and can drive external LED sources: LED_IND from 1mA, 2mA, 4mA and 8mA and LED_DRV from 12.5mA, 25mA, 50mA and 100mA. The sources can be turned off and on via I^2C registers control or AT commands and provides the device with an electronic shutter.

I²C Slave Interface

If selected by the I2C_ENB pin setting, interface and control can be accomplished through an I²C compatible slave interface to a set of registers that provide access to device control functions and output data. These registers on the AS72651 are, in reality, implemented as *virtual* registers in software. The actual I2C slave hardware registers number only three and are described in the table below. The steps necessary to access the virtual registers defined in the following are explained in pseudocode for external I2C master writes and reads below.

I²C Feature List

- Fast mode (400kHz) and standard mode (100kHz) support.
- 7+1-bit addressing mode.
- Write format: Byte.
- Read format: Byte.
- SDA input delay and SCL spike filtering by integrated RC-components.

Figure 17. I²C Slave Device Address and Physical Registers

Entity	Description	Note
Device Slave Address	8-bit Slave Address	byte = 1001 001*x* x= 1 for Master Read (byte = 93 hex) x= 0 for Master Write (byte = 92 hex)
STATUS Register	I2C slave interface STATUS register. Read-only.	Register Address = 0x00 Bit 1: TX_VALID 0 -> New data may be written to WRITE register 1 -> WRITE register occupied. Do NOT write. Bit 0: RX_VALID 0 -> No data is ready to be read in READ register. 1 -> Data byte available in READ register.
WRITE Register	I2C slave interface WRITE register. Write-only.	Register Address = 0x01 8-Bits of data written by the I2C Master intended for receipt by the I2C slave. Used for both *virtual* register addresses and write data.
READ Register	I2C slave interface READ register. Read-only.	Register Address = 0x02 8-Bits of data to be read by the I2C Master.

I²C Virtual Register Write Access

Figure 19 shows the pseudocode necessary to write virtual registers on the AS72651. Note that, because the actual registers of interest are realized as virtual registers, we need a means of indicating whether a read or write operation of a given virtual register is pending. To convey this information, we use the most significant bit of the virtual register address as a marker. If it is 1, then a write is pending, otherwise the slave is expecting a virtual read operation. The pseudocode illustrates the proper technique for polling of the I²C slave status register to ensure the slave is ready for each transaction.

Figure 18: I²C Virtual Register Byte Write

Pseudocode

```
Poll I²C slave STATUS register;
If TX_VALID bit is 0, a write can be performed on the interface;
Send a virtual register address and set the MSB of the register address to 1 to
indicate the pending write;
Poll I²C slave STATUS register;
If TX_VALID bit is 0, the virtual register address for the write has been received and
the data may now be written;
Write the data.
```

Sample Code:

```
#define I2C_AS72XX_SLAVE_STATUS_REG     0x00
#define I2C_AS72XX_SLAVE_WRITE_REG      0x01
#define I2C_AS72XX_SLAVE_READ_REG       0x02
#define I2C_AS72XX_SLAVE_TX_VALID       0x02
#define I2C_AS72XX_SLAVE_RX_VALID       0x01

void i2cm_AS72xx_write(uint8_t virtualReg, uint8_t d)
{
       volatile uint8_t    status;

       while (1)
       {
              // Read slave I2C status to see if we can write the reg address.
              status = i2cm_read(I2C_AS72XX_SLAVE_STATUS_REG);

              if ((status & I2C_AS72XX_SLAVE_TX_VALID) == 0)
                     // No inbound TX pending at slave.  Okay to write now.
                     break ;
       }
       // Send the virtual register address
       // (setting bit 7 to indicate a pending write).
       i2cm_write(I2C_AS72XX_SLAVE_WRITE_REG, (virtualReg | 0x80)) ;

       while (1)
       {
              // Read the slave I2C status to see if we can write the data byte.
              status = i2cm_read(I2C_AS72XX_SLAVE_STATUS_REG) ;

              if ((status & I2C_AS72XX_SLAVE_TX_VALID) == 0)
                     // No inbound TX pending at slave.  Okay to write data now.
                     break ;
       }
       // Send the data to complete the operation.
```

```
        i2cm_write(I2C_AS72XX_SLAVE_WRITE_REG, d) ;
}
```

I²C Virtual Register Read access

Figure 20 shows the pseudocode necessary to read virtual registers on the AS72651. Note that in this case, since we are performing a read of a virtual register, we do not modify the register address.

Figure 19: I²C Virtual Register Byte Read

Pseudocode

```
Poll I2C slave STATUS register;
If TX_VALID bit is 0, the virtual register address for the read may be written;
Send a virtual register address;
Poll I2C slave STATUS register;
If RX_VALID bit is 1, the read data is ready;
Read the data.
```

Sample Code:

```
uint8_t i2cm_AS72xx_read(uint8_t virtualReg)
{
        volatile uint8_t status, d ;

        while (1)
        {
                // Read slave I2C status to see if we can write the reg address.
                status = i2cm_read(I2C_AS72XX_SLAVE_STATUS_REG) ;

                if ((status & I2C_AS72XX_SLAVE_TX_VALID) == 0)
                        // No inbound TX pending at slave.  Okay to write now.
                        break ;
        }
        // Send the virtual register address
        // (setting bit 7 to indicate a pending write).
        i2cm_write(I2C_AS72XX_SLAVE_WRITE_REG, virtualReg) ;

        while (1)
        {
                // Read the slave I2C status to see if our read data is available.
                status = i2cm_read(I2C_AS72XX_SLAVE_STATUS_REG) ;

                if ((status & I2C_AS72XX_SLAVE_RX_VALID) != 0)
                        // Read data is ready for us.
                        break ;
        }
        // Read the data to complete the operation.
        d = i2cm_read(I2C_AS72XX_SLAVE_READ_REG) ;
        return d ;s
}
```

The details of the `i2cm_read()` and `i2cm_write()` functions in Figures 19 and 20 are dependent upon the nature and implementation of the external I2C master device.

I²C Virtual Register Set

The Figure below provides a summary of the AS72651 I²C register set. Figures after that provide additional details. All register data is hex, and all multi-byte entities are Big Endian (most significant byte is situated at the lowest register address).

Figure 20: I²C Register Set Summary

Register Name	Address	R/W	Register Function	Reset Value
HW_Version	0x00:01	R	HW Version (2 bytes)	HW Version
FW_Version	0x02:03	R	FW Version (2 bytes)	FW Version
Control_Setup	0x04 = R 0x84 = W	R/W	Enables interrupt output, Sets Gain, Photo Diode Bank Select, Data Ready, and soft reset	0x08
INT_T	0x05 = R 0x85 = W	R/W	Sets Integration time	0xFF
Device_Temp	0x06	R	Device temp (deg C)	
LED_Control	0x07 = R 0x87 = W	R/W	Sets LED_DRV / LED_IND pins	0x00
R_High	0x08	7:0	R High Data Byte	0x00
R_Low	0x09	7:0	R Low Data Byte	0x00
S_High	0x0A	7:0	S High Data Byte	0x00
S_Low	0x0B	7:0	S Low Data Byte	0x00
T_High	0x0C	7:0	T High Data Byte	0x00
T_Low	0x0D	7:0	T Low Data Byte	0x00
U_High	0x0E	7:0	U High data Byte	0x00

U_Low	0x0F	7:0	U Low data Byte	0x00
V_High	0x10	7:0	V High data Byte	0x00
V_Low	0x11	7:0	V Low data Byte	0x00
W_High	0x12	7:0	W High data Byte	0x00
W_Low	0x13	7:0	W Low data Byte	0x00
J_High	0x14	7:0	AS72652 J High Data Byte	0x00
J_Low	0x15	7:0	AS72652 J Low Data Byte	0x00
I_High	0x16	7:0	AS72652 I High Data Byte	0x00
I_Low	0x17	7:0	AS72652 I Low Data Byte	0x00
G_High	0x18	7:0	AS72652 G High Data Byte	0x00
G_Low	0x19	7:0	AS72652 G Low Data Byte	0x00
H_High	0x1A	7:0	AS72652 H High data Byte	0x00
H_Low	0x1B	7:0	AS72652 H Low data Byte	0x00
K_High	0x1C	7:0	AS72652 K High data Byte	0x00
K_Low	0x1D	7:0	AS72652 K Low data Byte	0x00
L_High	0x1E	7:0	AS72652 L High data Byte	0x00
L_Low	0x1F	7:0	AS72652 L Low data Byte	0x00
D_High	0x20	7:0	AS72653 D High Data Byte	0x00
D_Low	0x21	7:0	AS72653 D Low Data Byte	0x00
C_High	0x22	7:0	AS72653 C High Data Byte	0x00
C_Low	0x23	7:0	AS72653 C Low Data Byte	0x00

A_High	0x24	7:0	AS72653 A High Data Byte	0x00
A_Low	0x25	7:0	AS72653 A Low Data Byte	0x00
B_High	0x26	7:0	AS72653 B High data Byte	0x00
B_Low	0x27	7:0	AS72653 B Low data Byte	0x00
E_High	0x28	7:0	AS72653 E High data Byte	0x00
E_Low	0x29	7:0	AS72653 E Low data Byte	0x00
F_High	0x2A	7:0	AS72653 F High data Byte	0x00
F_Low	0x2B	7:0	AS72653 F Low data Byte	0x00
Device_Temp_6	0x2C	R	AS72652 Device temp (deg C)	0x00
Device_Temp_7	0x2D	R	AS72653 Device temp (deg C)	0x00
LED_Control_6	0x2E = R 0xAE = W	R/W	Sets AS72652 LED_DRV / LED_IND pins	0x00
LED_Control_7	0x2F = R 0xAF = W	R/W	Sets AS72653 LED_DRV / LED_IND pins	0x00

Figure 21: HW/FW Version Registers: Read Only

Register	Address	Bits	Description
HW_Version	0x00:01	R	HW Version (2 bytes), includes 9 bits of ams ID and 4 bits of device identification
FW_Version	0x02:03	R	AS72651 FW Version (2 bytes)

Figure 22: Control Register (0x04/0x84): Read/Write

7	6	5	4	3	2	1	0
RST	INT	GAIN		BANK		Data_ RDY	RSVD0

Fields	Bits	Description
RST	7	Soft Reset (=1) Set to 1 for soft reset, goes to 0 automatically after reset.
INT	6	Enable interrupt pin output (INT), Enable=1. Disable=0
GAIN	5:4	Sensor Channel Gain Setting (all sensors) ‘b00=1x; ‘b01=3.7x; ‘b10=16x; ‘b11=64x
BANK	3:2	Data Conversion Type (continuous): ‘b00 = Mode 0; ‘b01 = Mode 1; ‘b10 = Mode 2; ‘b11 = Reserved;
DATA_ RDY	1	1= Data Ready to Read, sets INT active if interrupt is enabled. Can be polled if not using INT used.
RSVD0	0	Reserved; Unused

Interrupt Operation

If BANK is set to Mode 0 or Mode 1 then the data is ready after the 1st integration time. If BANK is set to Mode 2 then the data is ready after two integration times. If the interrupt is enabled (INT = 1) then when the data is ready, the INT line is pulled low and DATA_RDY is set to 1. The INT line is released (returns high) when the control register is read. DATA_RDY is cleared to 0 when any of the sensor data registers are read. Since each sensor value is 2 bytes, after the 1st byte is read the 2nd byte is shadow-protected in case an integration cycle completes just after the 1st byte is read.

In continuous spectral conversion mode (BANK setting of Mode 0, Mode 1, or Mode 2), the sensors continue to gather information at the rate of the integration time, hence if the sensor registers are not read when the interrupt line goes low, it will stay low and the next cycle's sensor data will be available in the registers at the end of the next integration cycle.

Figure 23: Integration Time Register (0x05): Read/Write

Register	Address	Bits	Description
INT_T	0x05 = R 0x85 = W	7:0	Integration time = <value>*2.8ms

Figure 24: Device Temperature (0x06): Read Only

Register	Address	Bits	Description
Device_Temp	0x06	7:0	AS72651 Device temp, data byte (deg C)

Figure 25: LED Control Register (0x07/0x87): Read/Write

7	6	5	4	3	2	1	0
Reserved		ICL_DRV 1:0		LED DRV	ICL_IND 1:0		LED_IND

Fields	Bits	Description
Reserved	7:6	Reserved
ICL_DRV	5:4	LED_DRV Current Limit 'b00=12.5mA; 'b01=25mA; 'b10=50mA; 'b11=100mA
LED_DRV	3	Enable LED_DRV 1 = Enabled, 0 = Disabled

ICL_IND	2:1	LED_IND Current Limit ‘b00=1mA; ‘b01=2mA; ‘b10=4mA; ‘b11=8mA
LED_IND	0	Enable LED_IND Enabled=1. Disabled=0

Figure 26: Data Registers: Read Only

Register	Address	Bits	Description
R_High	0x08	7:0	R High Data Byte
R_Low	0x09	7:0	R Low Data Byte
S_High	0x0A	7:0	S High Data Byte
S_Low	0x0B	7:0	S Low Data Byte
T_High	0x0C	7:0	T High Data Byte
T_Low	0x0D	7:0	T Low Data Byte
U_High	0x0E	7:0	U High data Byte
U_Low	0x0F	7:0	U Low data Byte
V_High	0x10	7:0	V High data Byte
V_Low	0x11	7:0	V Low data Byte
W_High	0x12	7:0	W High data Byte
W_Low	0x13	7:0	W Low data Byte

Figure 27: AS72652 Data Registers: Read Only

Register	Address	Bits	Description
J_High	0x14	7:0	AS72652 J High Data Byte
J_Low	0x15	7:0	AS72652 J Low Data Byte
I_High	0x16	7:0	AS72652 I High Data Byte
I_Low	0x17	7:0	AS72652 I Low Data Byte
G_High	0x18	7:0	AS72652 G High Data Byte
G_Low	0x19	7:0	AS72652 G Low Data Byte
H_High	0x1A	7:0	AS72652 H High data Byte
H_Low	0x1B	7:0	AS72652 H Low data Byte
K_High	0x1C	7:0	AS72652 K High data Byte
K_Low	0x1D	7:0	AS72652 K Low data Byte
L_High	0x1E	7:0	AS72652 L High data Byte
L_Low	0x1F	7:0	AS72652 L Low data Byte

Values return 0x00 if the AS72652 is not present.

Figure 28: AS72653 Data Registers: Read Only

Register	Address	Bits	Description
D_High	0x20	7:0	AS72653 D High Data Byte
D_Low	0x21	7:0	AS72653 D Low Data Byte
C_High	0x22	7:0	AS72653 C High Data Byte

C_Low	0x23	7:0	AS72653 C Low Data Byte
A_High	0x24	7:0	AS72653 A High Data Byte
A_Low	0x25	7:0	AS72653 A Low Data Byte
B_High	0x26	7:0	AS72653 B High data Byte
B_Low	0x27	7:0	AS72653 B Low data Byte
E_High	0x28	7:0	AS72653 E High data Byte
E_Low	0x29	7:0	AS72653 E Low data Byte
F_High	0x2A	7:0	AS72653 F High data Byte
F_Low	0x2B	7:0	AS72653 F Low data Byte

Values return 0x00 if the AS72653 is not present.

Figure 29: Device Temperature (0x2C): Read Only

Register	Address	Bits	Description
Device_Temp_6	0x2C	7:0	AS72652 Device temp, data byte (deg C)

Figure 30: Device Temperature (0x2D): Read Only

Register	Address	Bits	Description
Device_Temp_7	0x2D	7:0	AS72653 Device temp, data byte (deg C)

Figure 31: LED1 Control Register (0x2E/0xAE): Read/Write

7	6	5	4	3	2	1	0

Reserved	ICL_DRV 1:0	LED DRV	ICL_IND 1:0	LED_IND

Fields	Bits	Description
Reserved	7:6	Reserved
ICL_DRV	5:4	AS72652 LED_DRV Current Limit ‘b00=12.5mA; ‘b01=25mA; ‘b10=50mA; ‘b11=100mA
LED_DRV	3	AS72652 Enable LED_DRV 1 = Enabled, 0 = Disabled
ICL_IND	2:1	AS72652 LED_IND Current Limit ‘b00=1mA; ‘b01=2mA; ‘b10=4mA; ‘b11=8mA
LED_IND	0	AS72652 Enable LED_IND Enabled=1. Disabled=0

Figure 32: LED2 Control Register (0x2F/0xAF): Read/Write

7	6	5	4	3	2	1	0
Reserved		ICL_DRV 1:0		LED DRV	ICL_IND 1:0		LED_IND

Fields	Bits	Description
Reserved	7:6	Reserved
ICL_DRV	5:4	AS72653 LED_DRV Current Limit ‘b00=12.5mA; ‘b01=25mA; ‘b10=50mA; ‘b11=100mA

LED_DRV	3	AS72653 Enable LED_DRV 1 = Enabled, 0 = Disabled
ICL_IND	2:1	AS72653 LED_IND Current Limit ‘b00=1mA; ‘b01=2mA; ‘b10=4mA; ‘b11=8mA
LED_IND	0	AS72653 Enable LED_IND Enabled=1. Disabled=0

UART Interface

If selected by the I2C_ENB pin setting, the UART module implements the TX and RX signals as defined in the RS-232 / V.24 standard communication protocol.

It has on both, receive and transmit path, a 16 entry deep FIFO. It can generate interrupts as required.

UART Feature List

- Full Duplex Operation (Independent Serial Receive and Transmit Registers) with FIFO buffer of 8 byte for each.
- At a clock rate of 16MHz it supports communication at 115200Baud.
- Supports Serial Frames with 8 Data Bits, 1 Parity Bit and 1 Stop Bit.
- High Resolution Baud Rate Generator.

Theory of Operation

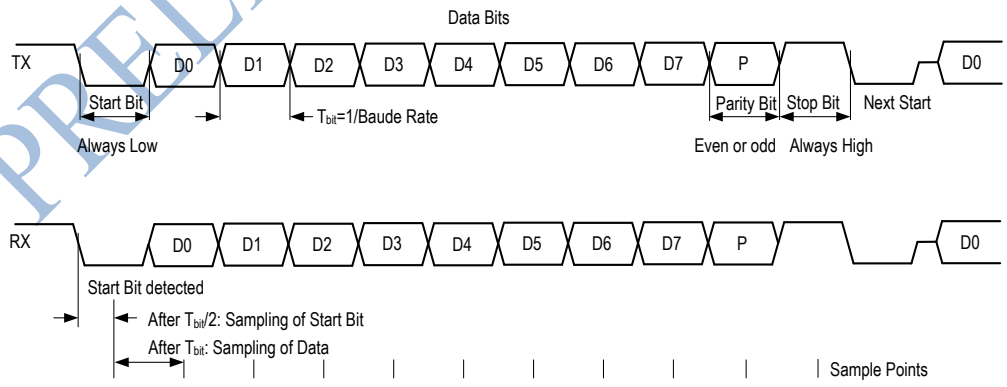
TRANSMISSION

If data is available in the transmit FIFO, it will be moved into the output shift register and the data will be transmitted at the configured Baud Rate, starting with a Start Bit (logic zero) and followed by a Stop Bit (logic one).

RECEPTION

At any time, with the receiver being idle, if a falling edge of a start bit is detected on the input, a byte will be received and stored in the receive FIFO. The following Stop Bit will be checked to be logic one.

Figure 33: UART Protocol



AT Command Interface

The microprocessor interface to control the NIR *Spectral_ID* Sensor is via the UART, using the AT Commands across the UART interface.

The 6-channel Spectral _ID sensor provides a text-based serial command interface borrowed from the "AT Command" model used in early Hayes modems. For example:

- Read DATA value: ATDATA → <data>OK
- Set the gain of the sensor to 1x: ATGAIN =0 → OK

The "AT Command Interface Block Diagram", shown below between the network interface and the core of the system, provides access to the Smart Lighting Manager's lighting control and configuration functions.

Figure 34: AT Command Interface Block Diagram

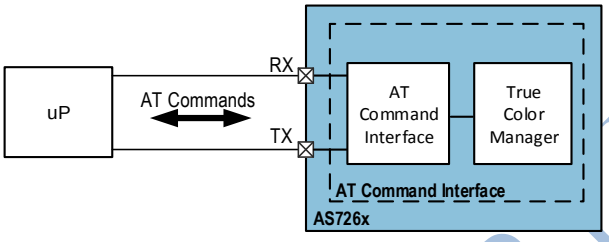


Figure 35: AT Commands

Command	Response	Description/Parameters
Spectral Data per Channel		
ATDATA	<R_*value*>, <S_*value*>, <T_*value*>, <U_*value*>, <V_*value*>, <W_*value*>, <J_*value*>, <I_*value*>, <G_*value*>, <H_*value*>, <K_*value*>, <L_*value*>, <D_*value*>, <C_*value*>,	Read R, S, T, U, V & W data for the AS72651. Returns comma-separated 16-bit integers. Read J, I, G, H, K & L data for the AS72652. Returns comma-separated 16-bit integers. Returns all zero data if not present. Read D, C, A, B, E & F data for the AS72653. Returns comma-separated 16-bit integers. Returns all zero data if not present.

	<A_*value*>, <B_*value*>, <E_*value*>, <F_*value*> OK	
ATXYZR	<A_*value*>, <B_*value*>, <C_*value*>, <D_*value*>, <E_*value*>, <F_*value*>, <G_*value*>, <H_*value*>, <R_*value*>, <I_*value*>, <S_*value*>, <J_*value*>, <T_*value*>, <U_*value*>, <V_*value*>, <W_*value*>, <K_*value*>, <L_*value*> OK	Read all 18 Channels data in order of wavelengths. Read R, S, T, U, V & W data for the AS72651. Returns comma-separated 16-bit integers. Read J, I, G, H, K & L data for the AS72652. Returns comma-separated 16-bit integers. Returns all zero data if not present. Read D, C, A, B, E & F data for the AS72653. Returns comma-separated 16-bit integers. Returns all zero data if not present.
Sensor Configuration		
ATINTTIME=<*value*>	OK OK OK	Set integration time to AS72651/AS72652/AS72653. Values should be in the range [1..255], with integration time = <*value*> * 2.8msecs.
ATINTTIME	<*value*> OK <*value*> OK <*value*> OK	Read all sensors integration time, with integration time = <*value*> * 2.8msecs.
ATGAIN=<*value*>	OK OK OK	Set gain to AS72651/AS72652/AS72653: 0=1X, 1=3.7X, 2=16X, 3=64X
ATGAIN	<*value*> OK <*value*> OK <*value*> OK	Read all sensors gain setting, returning 0, 1, 2, or 3 as defined immediately above.
ATTEMP	<*value1*> <*value2*> <*value3*> OK	Read temperature of AS72651, AS72652, AS72653 in Celsius
ATTCSMD=<*value*>	OK	Set Bank Mode

		0 = BANK Mode 0; 1 = BANK Mode 1; 2 = BANK Mode 2;
ATTCSMD	<*value*> OK	Read Bank Mode, see above
LED Driver Controls		
ATLED0=<*value*>	OK	Sets AS72651 LED_IND: 100=ON, 0=OFF
ATLED0	<100|0>OK	Reads AS72651 LED_IND setting: 100=ON, 0=OFF
ATLED1=<*value*>	OK	Sets AS72651 LED_DRV: 100=ON, 0=OFF
ATLED1	<100|0>OK	Reads AS72651 LED_DRV setting: 100=ON, 0=OFF
ATLED2=<*value*>	OK	Sets AS72652 LED_DRV: 100=ON, 0=OFF
ATLED2	<100|0>OK	Reads AS72652 LED_DRV setting: 100=ON, 0=OFF
ATLED3=<*value*>	OK	Sets AS72653 LED_DRV: 100=ON, 0=OFF
ATLED3	<100|0>OK	Reads AS72653 LED_DRV setting: 100=ON, 0=OFF
ATLEDC=<*value*>	OK	Sets LED_IND and LED_DRV current for the AS72651 LED_IND: bits 3:0; LED_DRV: 7:4 bits LED_IND: ‘b00=1mA; ‘b01=2mA; ‘b10=4mA; ‘b11=8ma LED_DRV: ‘b00=12.5mA; ‘b01=25mA; ‘b10=50mA; ‘b11=100ma
ATLEDC	<value>OK	Reads the AS72651 LED_IND and LED_DRV current settings as shown above
ATLEDD=<*value*>	OK	Sets LED_IND and LED_DRV current for the AS72652 if present LED_IND: bits 3:0; LED_DRV: 7:4 bits LED_IND: ‘b00=1mA; ‘b01=2mA; ‘b10=4mA; ‘b11=8ma LED_DRV: ‘b00=12.5mA; ‘b01=25mA; ‘b10=50mA; ‘b11=100ma
ATLEDD	<value>OK	Reads the AS72652 LED_IND and LED_DRV current settings as shown above

ATLEDE=<*value*>	OK	Sets LED_IND and LED_DRV current for the AS72653 if present LED_IND: bits 3:0; LED_DRV: 7:4 bits LED_IND: ‘b00=1mA; ‘b01=2mA; ‘b10=4mA; ‘b11=8ma LED_DRV: ‘b00=12.5mA; ‘b01=25mA; ‘b10=50mA; ‘b11=100ma
ATLEDE	<value>OK	Reads the AS72653 LED_IND and LED_DRV current settings as shown above
NOP, Version Access, System Reset		
AT	OK → Success ERROR → Failure	NOP
ATSRST	None	Software Reset – no response
ATVERSW	<*SWversion#*>OK ERROR → Failure	Returns the system software version number
ATVERHW	<*HWversion#*>OK ERROR → Failure	Returns the system hardware revision and product ID, with bits 7:4 containing the part ID, and bits 3:0 yielding the chip revision value.
ATPRES	<value>OK	0 Only AS72651 present 1 AS72651,AS72652 present 2 AS72651,AS72653 present 3 AS72651,AS72652 and AS72653 present
Firmware Update		
ATFWU=<*value*>	OK	<*value*>= 16-bit checksum. Initial the firmware update process. Bytes that follow is always 56 KBytes
ATFW=<*value*>	OK	Download new firmware Up to 7 bytes represented as hex chars with no leading or trailing 0x. Repeat command till all 56Kbytes of firmware are downloaded
ATFWS	OK	Causes the active image to switch between the two possible current images and then resets the IC

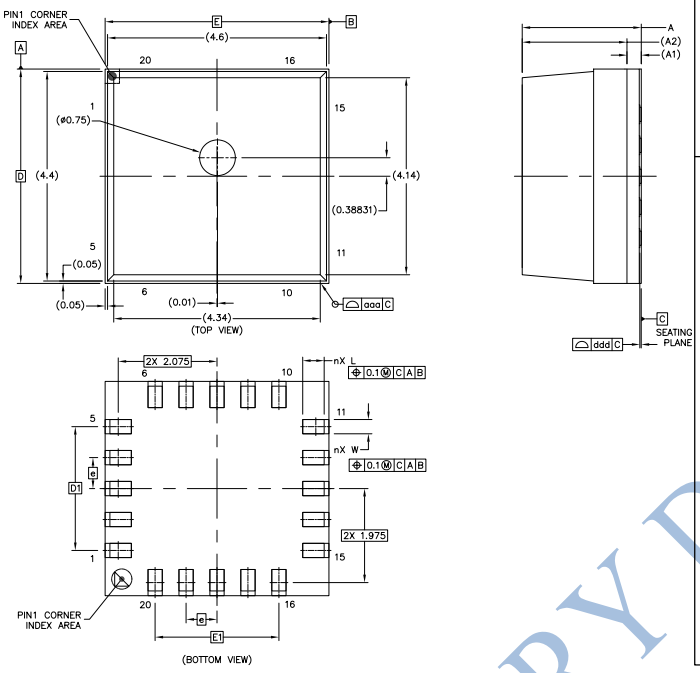
In the tables, numeric values may be specified with no leading prefix, in which case they will be interpreted as decimals, or with a leading “0x” to indicate that they are hexadecimal numbers, or with a leading “‘b” to indicate that they are binary numbers. The commands are loosely grouped into functional

areas. Texts appearing between angle brackets (‘<‘ and ‘>‘) are commands or response arguments. A carriage return character, a linefeed character, or both may terminate commands and responses. Note that any command that encounters an error will generate the “ERROR” response shown, for example, in the NOP command at the top of the first table, but has been omitted elsewhere in the interest of readability and clarity.

Package Drawings

Figure 36: AS72651 Package Drawings

AS72651 LGA Package Drawing



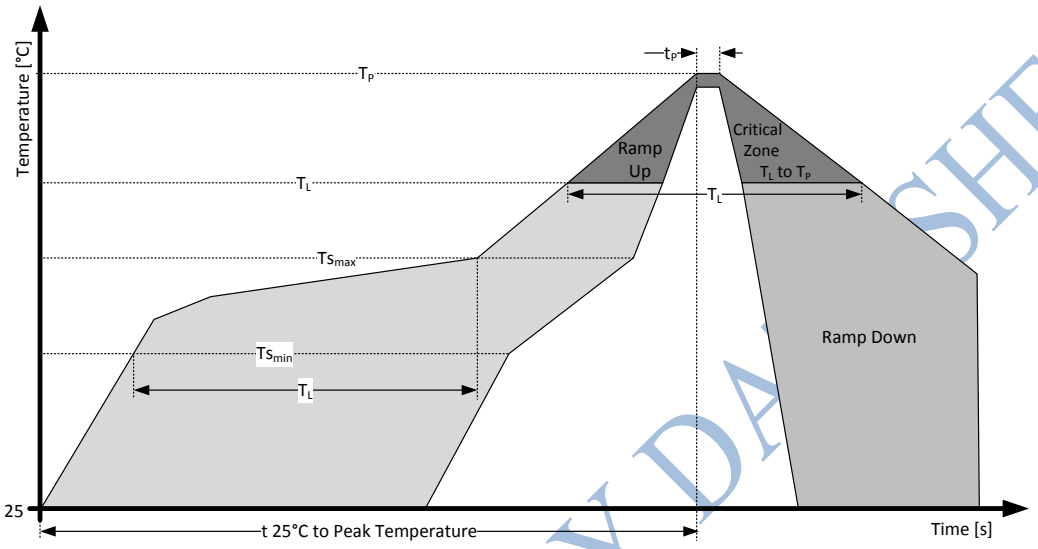
	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	2.4	2.5	2.6
SUBSTRATE THICKNESS	A1		0.3	REF
LID THICKNESS	A2		2.2	REF
FILM THICKNESS	A3		---	REF
BODY SIZE	D		4.5	BSC
	E		4.7	BSC
LEAD WIDTH	W	0.25	0.3	0.35
LEAD LENGTH	L	0.4	0.45	0.5
LEAD PITCH	e		0.65	BSC
LEAD COUNT	n		20	
EDGE BALL CENTER TO CENTER	D1		2.6	BSC
	E1		2.6	BSC
BODY CENTER TO CONTACT BALL	SD		---	BSC
	SE		---	BSC
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	bbb		---	
COPLANARITY	ddd		0.08	
BALL OFFSET (PACKAGE)	eee		---	
BALL OFFSET (BALL)	fff		---	

Note: Exposure to UV radiation could cause slight optical response degradation.

Solder Reflow Profile

The PCB assembly should be instrumented and the reflow oven's process parameters established to ensure the solder paste manufacturer's reflow profile specification is met during the assembly process. The maximum PCB temperature recommended by the supplier must not be exceeded.

Figure 37: Recommended Reflow Soldering Profile



Profile Feature	Lead-free Assembly
Average ramp-up rate (T_{Smax} to T_P)	3 °C/second max.
Preheat -Temperature Min (T_{Smin}) -Temparature Max (T_{Smax}) -Time (t_L)	 150 °C 200 °C 60 – 120 seconds
Time maintained above: -Temperature (T_L) -Time (t_L)	 217 °C 60 – 150 seconds
Peak/classification temperature (T_P)	260 °C
Time within 5 °C of actual peak temperature (T_P)	30 seconds
Ramp-down rate	6 °C/second max.
Time 25 °C to peak temperature	8 minutes max.

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