PicoP® Scanning Engine (PSE-0403-1xx) Datasheet

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ABSTRACT

This document summarizes in detail the mechanical, optical and electrical characteristics of MicroVision's PicoP® Scanning Engine (PSE-0403-1xx).

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LASER SAFETY NOTICE

PicoP® Scanning Engine (PSE) is configured during manufacturing to meet class 2 or class 3R laser safety requirements as defined in IEC 60825-1, ed.3. PSE is intended to be embedded inside a host system, therefore the system integrator must ensure that the end product meets all applicable laser safety requirements and must obtain any needed product certifications.

Contents

1. Introduction

This datasheet describes the mechanical, optical and electrical characteristics and interfaces of MicroVision's PicoP® Scanning Engine (PSE). The PSE implements a MEMS Laser Beam Scanning (LBS) display engine based on MicroVision's patented PicoP Scanning Technology. The PSE is intended to be used by customers wishing to embed a small and thin full-color, laser projector inside their product.

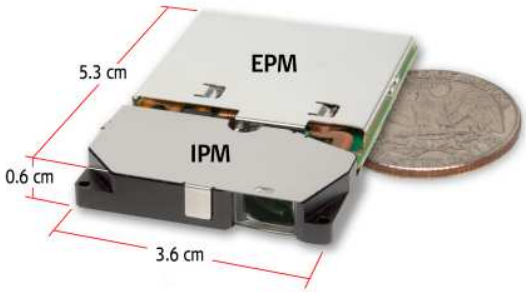


Figure 1. PSE-0403 PicoP Scanning Engine (PSE).

The PSE consists of an Integrated Photonics Module (IPM) and Electronics Platform Module (EPM). *The EPM and IPM are a matched pair and may not be swapped between different PSEs.*

The PSE block diagram is illustrated in Figure 2 below.

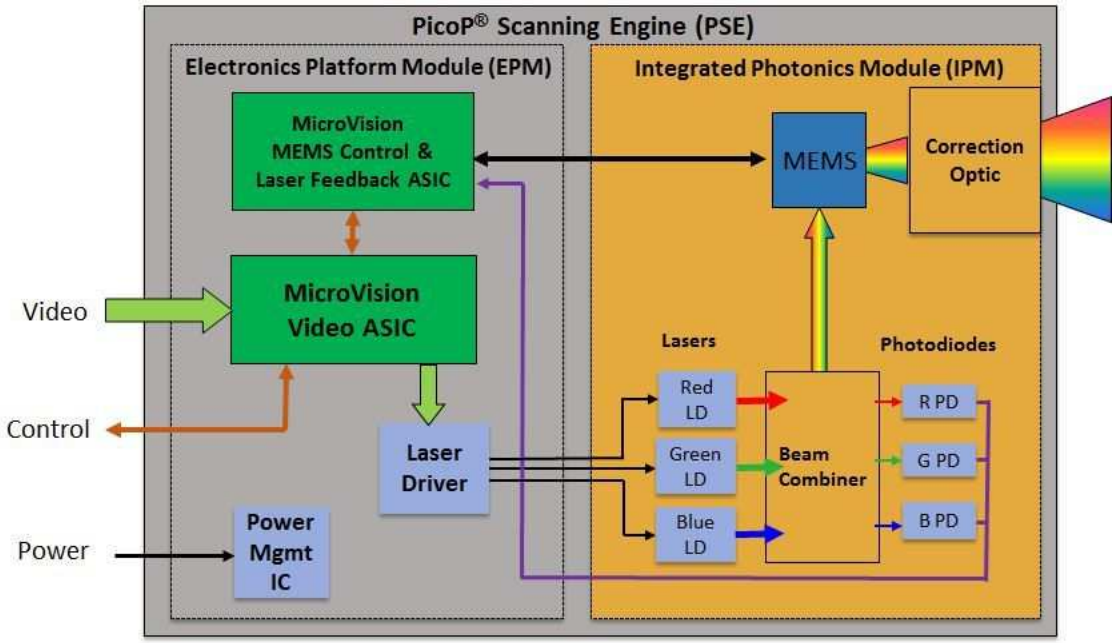


Figure 2. PSE block diagram.

2. Specifications

Characteristic	Specification[1]	
Display Performance	Display Technology	Laser Beam Scanning Technology
	Input Resolution	1280x720[2]
	Output Resolution	1280x720
	Brightness	35 ANSI lumens 45 Video lumens[3]
	Color Depth	64K colors
	Aspect Ratio	16:9
	Throw Ratio	1.2:1
	Focus Range	Standard model -101: Infinite focus Short focus model -102: 75mm +- 5mm
	Display Refresh Rate	60Hz
	Input Frame Rate	60fps
	Sequential Contrast	80,000:1
	Brightness Uniformity	>70%
	Color Gamut (rel. HDMI)	>200%
	Start-up Time	<6.5 sec
Physical	Scanning Engine Size	36.2x53.4x6.0mm
	Optical Module Size	36.2x21.4x6.0mm
	Weight	<20g
	Video Interface	Digital RGB (16bit 5:6:5, 1.8-3.4V)
	Control Interface	Full Speed USB, UART
Power	Single Supply Input Voltage	3.0-4.5V
	Power @ 27% Video Image	<2.20W (at 25°C)
	Power @ Full White Image	<4.70W (at 25°C)
Environmental	Operating Temperature	0°C ...+60°C
	Storage Temperature	-30°C ...+70°C
	Life time	TBD hours
Light Source	3 Lasers	Red: ~638nm Green: ~520nm Blue: ~450nm
	Laser Safety Classification	Class 3R Laser Product IEC60825 Ed. 2
Models	Model Numbers	PSE-0403-101 : Infinite focus PSE-0403-102 : Short focus

[1]Note: Specifications subject to change without notice
[2] For other resolutions, please contact your MicroVision representative
[3] For definition, please see Chapter 2.1 "Display Performance Specifications"

2.1 Display Performance Specifications

Brightness

The ANSI Brightness is measured at 25°C ambient temperature using a full white screen. The light emission in lux is first measured on 9 points. The positions of these 9 measurement points are represented in Figure 2 by the circles 1 – 9. The 9 measurements are then averaged and normalized to the screen size to provide the ANSI brightness measurements in Lumens.

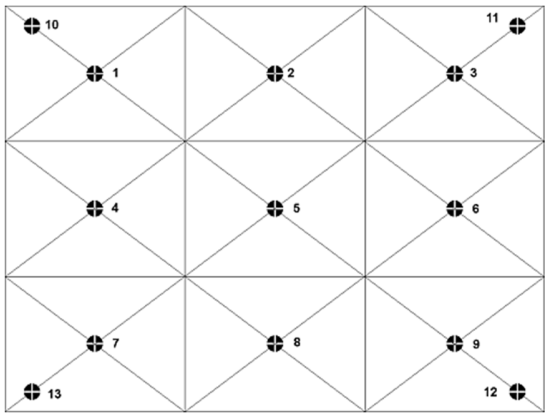


Figure 3. ANSI 9-point brightness measurement locations.

The Video Lumens are achieved by boosting the brightness of video codes around code level 0.3, which are the most common video code values in typical pictures and movie frames. The brightness of these video codes is boosted up to 30% to correspond to a brightness of a 40 lumen projector displaying typical pictures of movies. The 100% white brightness is kept the same as measured with the ANSI 9-point brightness measurement.

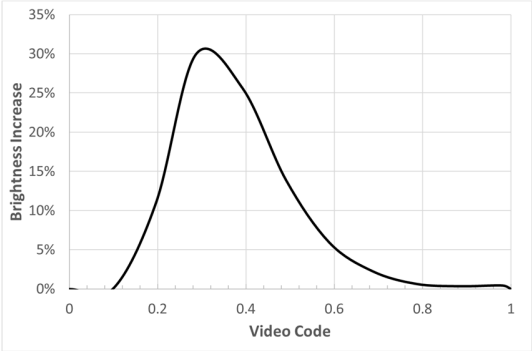


Figure 4. Brightness boost of lower video codes.

The brightness boost can be enabled or disabled thru the PSE control interface.

The PSE brightness depends on the PSE case temperature and the brightness may decrease when the PSE case temperature increases.

Color Depth

The PSE Color Depth is 16-bith High Color, with 5 bits for red, 6 bits for green, and 5 bits for blue.

Throw Ratio

The throw ratio of is defined as the distance between the projector and the screen divided by the horizontal width of the projected image.

Sequential Contrast

Sequential contrast is measured as the ratio of the luminance values at the center of the image between a constant 100% white image and a constant 0% black image.

Brightness Uniformity

The brightness uniformity is the uniformity of the measured display brightness at the 9 measurement locations shown in Figure 3 above.

2.2 Power Specifications

The PSE accepts a single supply input voltage within a range of 3.0 – 4.5V. The PSE power management has been designed to be compatible with a typical Lithium-Ion supply voltage of 3.6-3.7V.

The Power consumption is measured at 25°C. At a higher operating temperatures, the power consumption will increase, as shown in Table 1 below:

Table 1. Power consumption over temperature.

PSE Case Temp	Power @ 27% Video Image	Power @ Full White Image
25°C	2.2W	4.7W
50°C	2.4W	5.0W

2.3 Environmental Specifications

The Operating Temperature range means operating range for PSE Case temperature. The end product needs to be designed thermally to keep PSE within this range regardless of the end product's ambient operating temperature.

3. Mechanical Interface

3.1 PSE Mechanical Dimensions

The PSE mechanical dimensions are shown below (Figure 5). The envelope shown in Figure 5 provides the nominal dimensions of the PSE. Please see document DC0135108 for more details on mechanical tolerances.

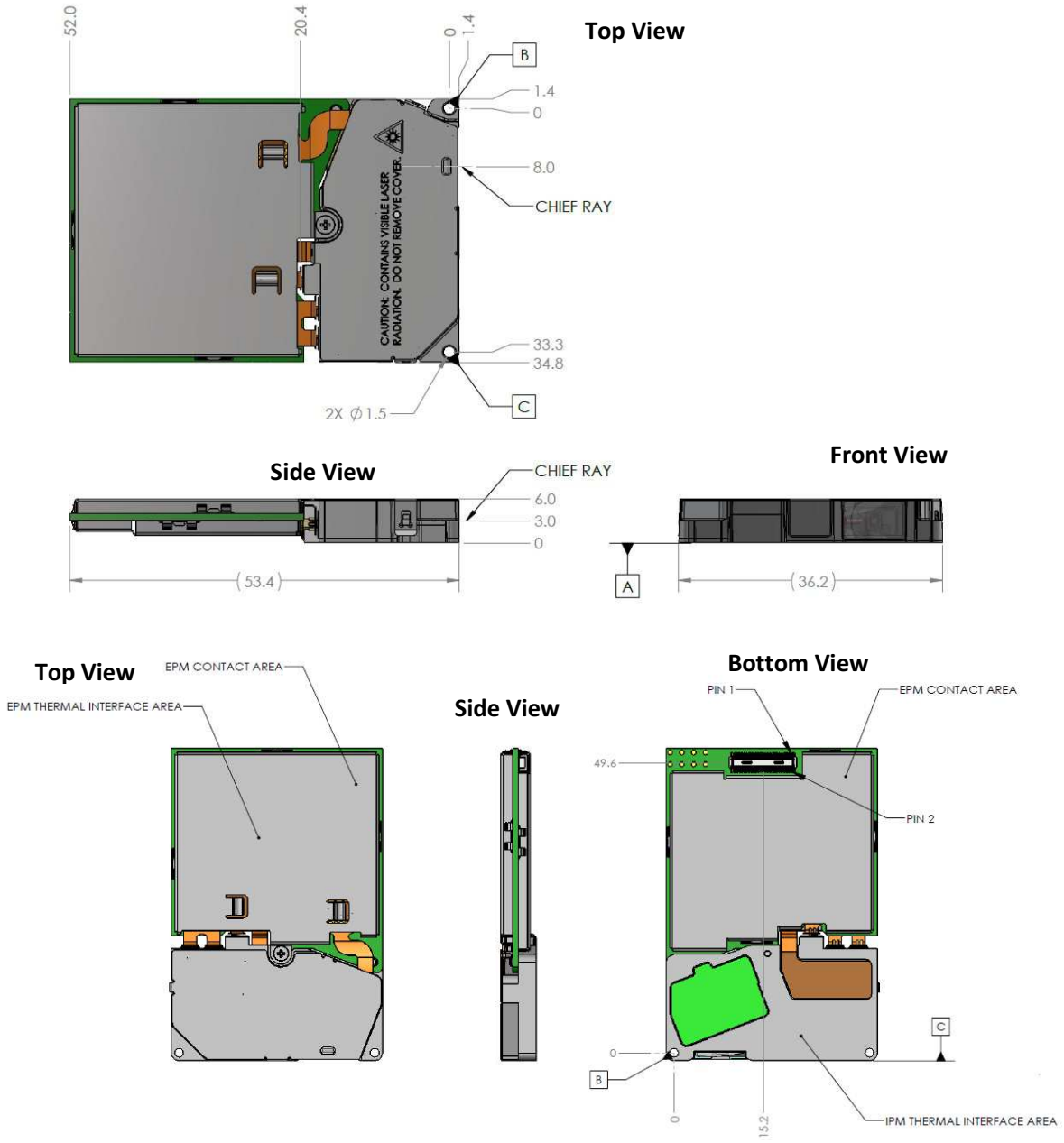


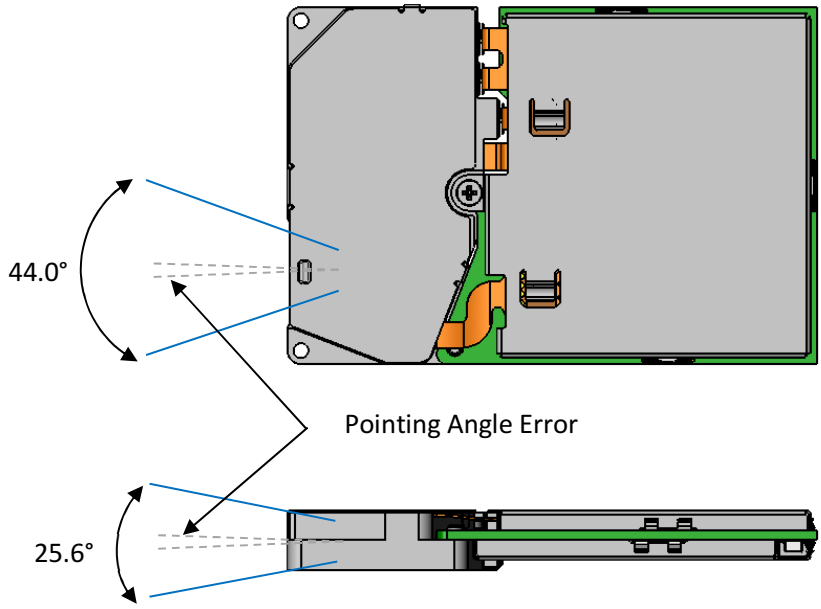
Figure 5. PSE sketch showing dimensions and mount points.

In addition to the overall dimensions of the assembly, Figure 5 also shows the exit position of the chief ray, the position of the scanning MEMS mirror, and the primary mounting points on the PSE.

Two mount points are provided to mechanically mount the PSE to a host system. Figure 5 shows the position of these mount points. The IPM is rigidly mounted to the electronics board and shields and the system connector on the PSE may provide additional stability. Further mechanical support should be provided at the indicated thermal interface areas.

3.2 Field of View (Scan Cone)

The field of view dimensions are detailed in Figure 6.



Pointing Angle Error	± 2.0°
Horizontal Field of View	44.0°
Vertical Field of View	25.6°

Figure 6. PSE field of view dimensions.

3.3 Shock

The mechanical mounting of the PSE inside the host device should be designed such that acceleration and any secondary impacts on the IPM during drop are minimized.

4. Electrical Interface

The PSE provides electrical connectivity through a single board to board connector, as shown in Figure 5 (bottom view). The PSE electrical interface consists of power, power enable, a digital video interface (5-6-5 R-G-B), PSE control and communication signals, and optional MEMS position feedback, as illustrated in Figure 7 below.

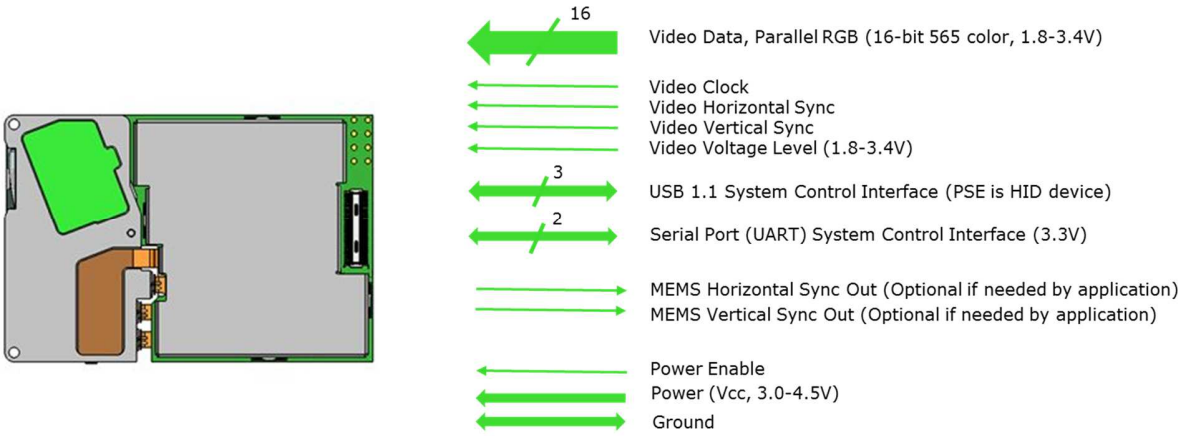


Figure 7. PSE electrical interface overview.

4.1 PSE Electrical Signals

The PSE provides a Hirose DF40 Series 50-position, 0.4 mm contact pitch, dual row board to board connector with a male end (Hirose DF40C-50DP-0.4V). The signals carried by the PSE connector and the digital flex cable are described in table 2 below. The pin assignment for the 50 pin interface connector is provided on page 13.

Table 2. PSE signals and signal characteristics.

Signal	Type	Signal level	
			Video Signals
G7, G6, G5, G4, G3, G2	I	V_{VID-IO}	GREEN data (G7 is MSB, G2 is LSB).
R7, R6, R5, R4, R3	I	V_{VID-IO}	RED data (R7 is MSB, R3 is LSB).
B7, B6, B5, B4, B3	I	V_{VID-IO}	Blue data (B7 is MSB, B3 is LSB).
CLK	I	V_{VID-IO}	Video clock used to sample data, HSYNC, and VSYNC.
HSYNC	I	V_{VID-IO}	Horizontal sync signal.
VSYNC	I	V_{VID-IO}	Vertical sync signal.
LSV	I	1.8 – 3.4V	Sets V_{VID-IO}, the voltage level for the video input signals. Must be between 1.8V to 3.4V. Supply must be able to source 20mA.
			Power Enable Interface
PE	I	3.3V	Power enable [Note 1]. On low side, driver must maintain < 0.2V while sinking 1mA. Absolute maximum: -0.3V to Vcc+0.3V.
			Communication Interface
USB_VBUS	I	5V	USB VBUS [Note 2]
USB_DP	I/O	V_{USB}	USB D+. Follow the USB 1.1 specification.
USB_DM	I/O	V_{USB}	USB D-. Follow the USB 1.1 specification.
UART_Tx	O	3.3V	UART Transmit data. 8 bit data, negative parity, 1 stop bit with no RTS/CTS flow control. Baud rate to 57600. Driver capable of sourcing/sinking 2 mA current.
UART_Rx	I	3.3V	UART Receive data. Typical input capacitive load 22 pF. V_{ILO} < 0.8V, V_{IHI} > 2.0V. 8 bit data, negative parity, 1 stop bit with no RTS/CTS flow control. Baud rate 57600.
			Miscellaneous Signals
Reserved	--	--	Reserved for future use – Do not connect to these pins
VSYNC_O	O	3.3V	Vertical Sync synchronized to MEMS. Used for synchronizing camera with display frame. Driver capable of sourcing/sinking 16 mA current
HSYNC_O	O	3.3V	Horizontal Sync synchronized to MEMS. Driver capable of sourcing/sinking 16 mA current
			Power Supply
VCC	--	3.0–4.5V	Power supply. 2.0 W typical power draw (27% video), 3.9 W max (@50°C).
GND	--	--	--

Notes:

[1] The PSE will draw < 1µA (maximum 10 µA) of current unless PE is asserted. All other input signals must remain at 0 V when PE is de-asserted.

[2] Used for USB interface detection only. The PSE does not attempt to draw power from USB_VBUS. Follow the USB specification for range.

The V_{VID-IO} video signal voltage levels defined above are described in the table 3 below. Typical input capacitance of 12 pF.

Table 3. PSE Video input voltage levels.

	V_{VID-IO}	Min	Max
High level input voltage V_{VID-IO} (1.8 to 3.4 V)	1.8	1.2	--
	2.5	1.6	--
	3.3	2.0	--
Low level input voltage V_{VID-IO}	1.8	--	0.6
	2.5	--	0.7
	3.3	--	0.8

Figure 8 shows the pin number convention for the 50 pin Hirose DF40C-50DP-0.4V connector.

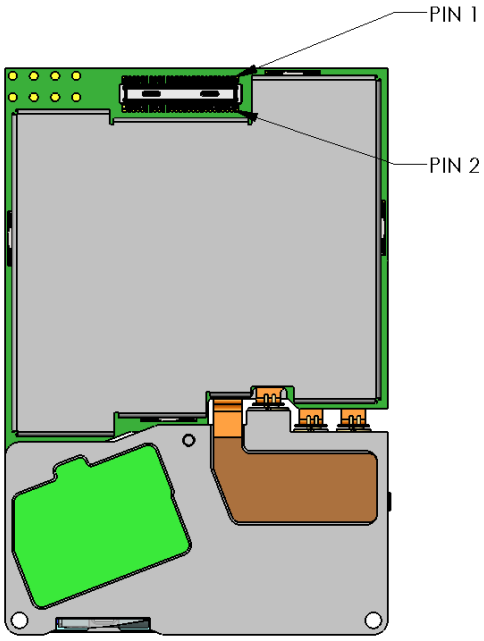


Figure 8. PSE connector pin numbering orientation.

The table 4 on the following page shows the pin assignments for the 50 pin Hirose connector.

Table 4. PSE connector pin assignments.

PSE connector pin #	Signal
1	GND
2	GND
3	B4
4	GND
5	VSYNC
6	GND
7	R5
8	GND
9	R4
10	GND
11	R3 (LSB)
12	VCC
13	G4
14	VCC
15	GND
16	VCC
17	R7 (MSB)
18	VCC
19	G6
20	VCC
21	R6
22	VCC
23	G5
24	VCC
25	G2 (LSB)
26	Reserved
27	GND
28	Reserved
29	B7 (MSB)
30	Reserved
31	B3 (LSB)
32	PE
33	B5
34	GND
35	GND
36	Reserved
37	B6
38	LSV
39	G7 (MSB)
40	UART_Tx
41	CLK
42	UART_Rx
43	G3
44	USB_VBUS
45	HSYNC
46	USB_DP
47	VSYNC_O
48	USB_DM
49	HSYNC_O
50	GND

4.2 Digital Video Interface

The PSE expects to receive a progressive stream of video frames, lines, and pixels, according to Figures 9 - 11 below. The exact video parameters are configured using the control interface (see section 4.6 below).

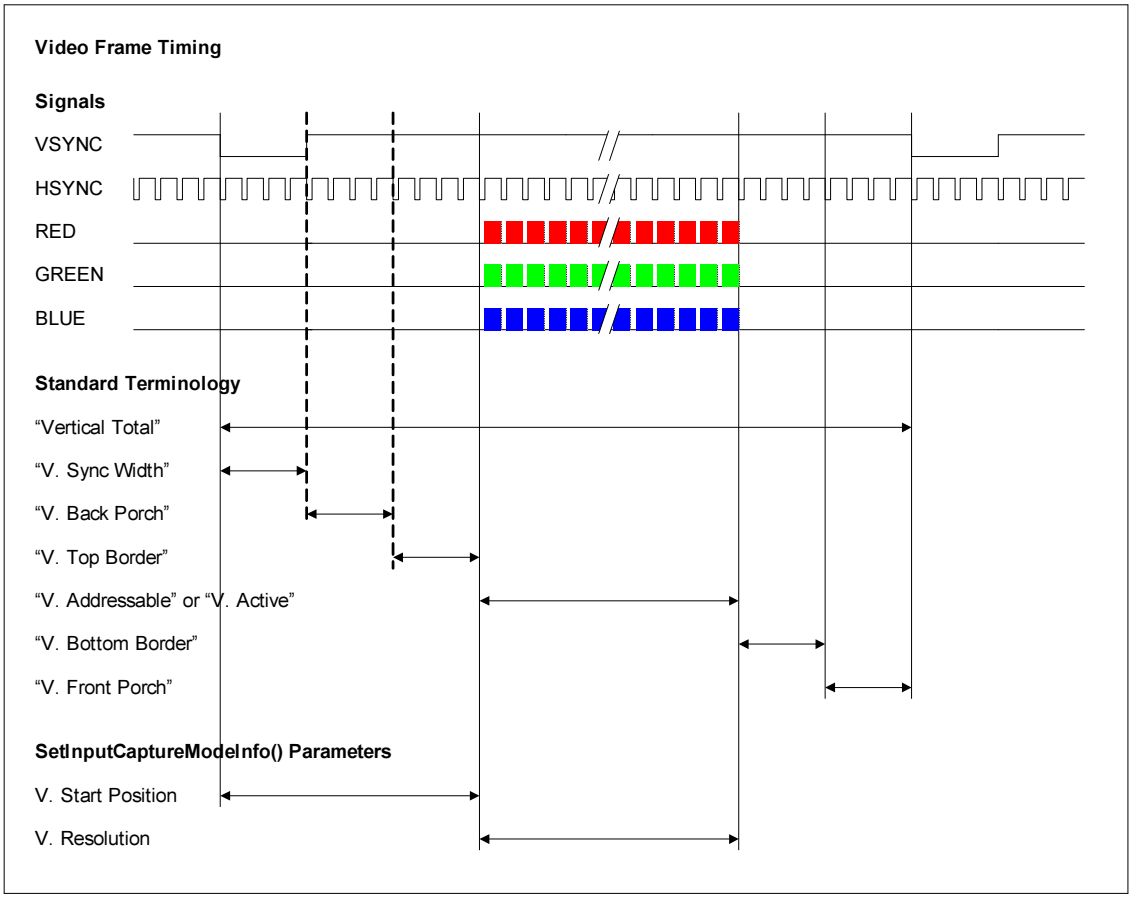


Figure 9. PSE video frame timing.

Figure 9 shows a typical video frame. The PSE counts a certain number of HSYNC pulses after the leading edge of VSYNC before capturing the active video lines. The VSYNC polarity, HSYNC polarity, V. Start Position, and V. Resolution are configurable (Figure 9 shows inverted polarity for both VSYNC and HSYNC).

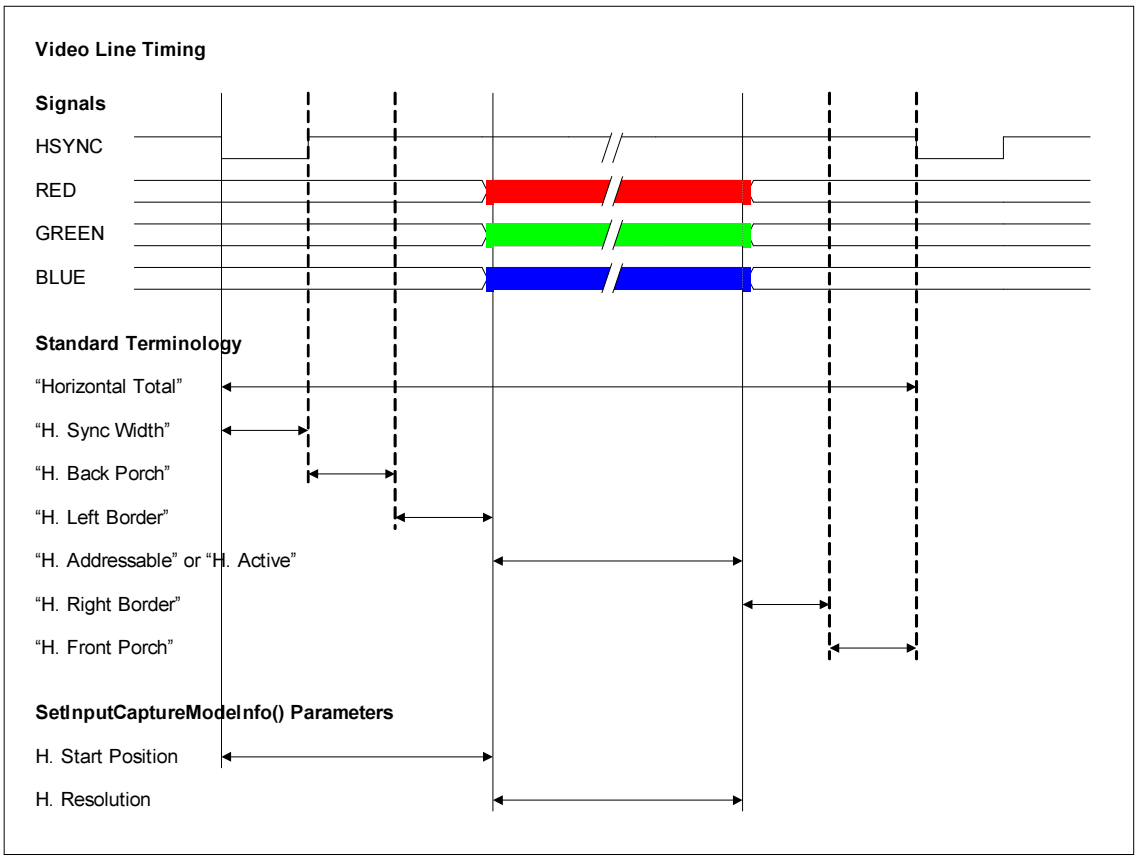


Figure 10. PSE video line timing.

Figure 10 shows a typical video line. The PSE counts a certain number of CLK pulses after the leading edge of HSYNC before capturing the active video pixels. The HSYNC polarity, H. Start Position, and H. Resolution are configurable (Figure 10 shows inverted polarity for HSYNC).

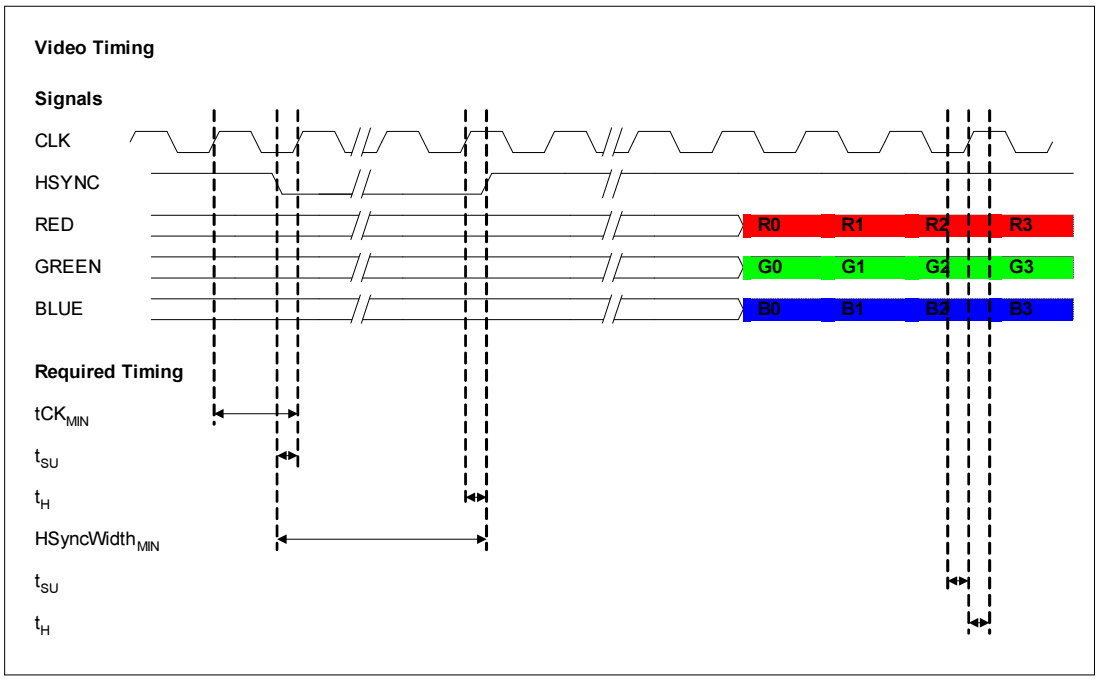


Figure 11. PSE video sample timing.

Figure 11 shows pixel-level video timing. The digital interface is synchronous to the CLK input, however the PSE may be configured to sample the digital video interface on either the rising edge or the falling edge of the CLK input. Figure 10 shows the case where the rising edge of CLK is used, and therefore setup and hold time requirements refer to the rising edge.

Table 5. PSE video interface timing characteristics.

Parameter	Time
tCK_{MIN} Minimum CLK period	12.5 ns
t_{SU} Minimum setup time before selected CLK edge	4.5 ns
t_H Minimum hold time after selected CLK edge	2.5 ns
$HSyncWidth_{MIN}$ Minimum duration of HSYNC pulse	3 x tCK_{MIN}
$VSyncWidth_{MIN}$ Minimum duration of VSYNC pulse	3 x HSYNC Period

The PSE powers up configured for standard 1280 x 720 pixel input resolution. The PSE can be configured to accept arbitrary input resolutions below 1280 x 720 using the control interface. Table 6 below shows the default values and also typical values for other common formats.

Table 6. PSE video formats.

Resolution	VSYNC Polarity	HSYNC Polarity	Leading edge of VSYNC to first active line (V. Start Position)	Leading edge of HSYNC to first active pixel (H. Start Position)
1280 x 720 (Default)	Positive	Positive	25 HSYNC pulses	260 Pixel clocks
848 x 480	Negative	Negative	25 HSYNC pulses	191 Pixel clocks

4.3 MEMS Sync Interface

The PSE provides output signals that are synchronized to the motion of the scanning MEMS mirror. These signals (HSYNC_O and VSYNC_O) are buffered 3.3V outputs and are capable of sourcing or sinking 16mA. HSYNC_O transitions at the middle of every scanline. The VSYNC_O pulse occurs at the middle of the vertical retrace when the MEMS sweeps back to the beginning of the raster. Note that the relation of the vertical retrace to the MEMS horizontal frequency varies between different MEMS, thus the relation of HSYNC_O and VSYNC_O timing will be different for different PSEs. Figure 12 shows details of the MEMS sync timing.

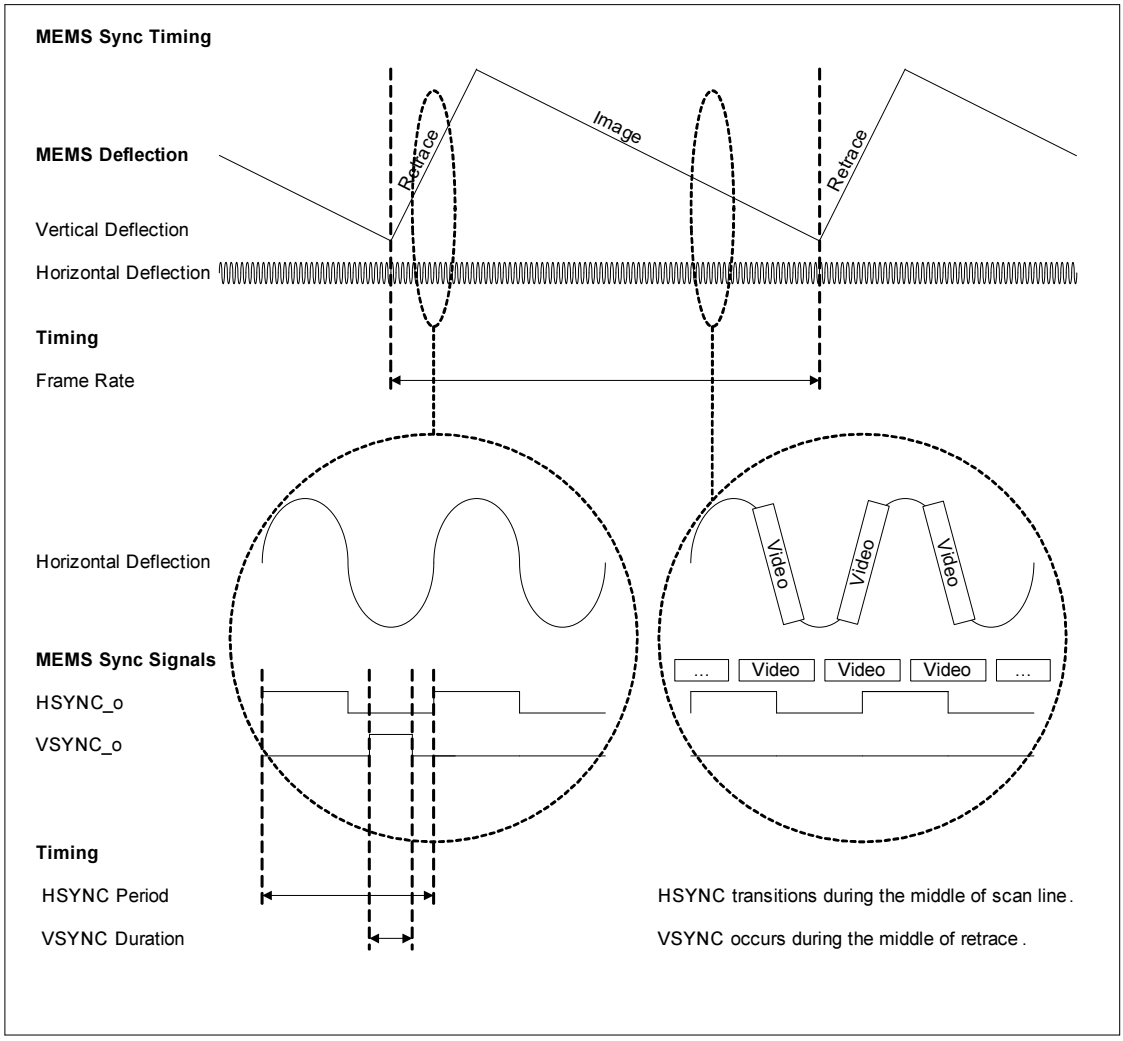


Figure 12. MEMS Synchronization Timing.

4.4 Power Interface

The PSE will typically draw less than 1 µA (maximum 10 µA) of current unless PE (power enable) is asserted. The host must ensure that the power rail voltage supplied to the PSE exceeds 3.0 V before PE is asserted. The host may then poll the PSE module to determine its status using the GetSystemStatus() function (please refer to DA0135396 and DC0124088).

An LED provides an indication that power is supplied to the PSE board.

The host is expected to monitor the battery voltage and turn PSE off when the power rail voltage falls below 3.0 V.

4.5 Electromagnetic Compatibility

The PSE is designed to be compliant with FCC electromagnetic capabilities defined by Part 15, Subpart J, Class B as well as EN55022:1998 Class B and EN55024:1998 when appropriately housed inside a host device.

During integration of PSE in customer product, take appropriate ESD precautions to prevent ESD damage.

The maximum magnetic field external to the PSE is 2000 gauss. The field drops to less than 50 gauss 10 mm away. PSE functionality can be affected by external magnetic fields. These affects can range from image quality issues up to damage to the MEMS mirror. Functionality of the PSE in proximity to permanent magnets should be verified early in the development process.

4.6 Control & Service Interface

The PSE module Control & Service interface provides a path for the host device to:

1. Issue commands to the PSE for user control, such as
    - Brightness adjustment
    - Keystone correction
    - Color alignment and scanline phase delay adjustment
2. Upgrade software,
3. Access service/manufacturing functions such as system status.

The PSE module also informs the host of exceptions that may require host intervention through this interface.

Please refer to the PSE Programmer's Guide (DA0135396) for a description of the communication interface and control functions.

This interface is implemented to support the UART and USB standards. If USB_VBUS is asserted, the PSE will communicate through USB.

In order to provide maximum flexibility for end customers, MicroVision recommends that color alignment and phase adjustments be exposed to the end customer under system setup functionality.

The PSE module will initiate shutdown under fault conditions that include:

- Laser over power fault
- MEMS under/over angle fault
- Over temperature fault

5. Thermal Interface

Video Level	27% video (Typical video and pictures) at 50°C	Max 100% video (full white) at 50°C
Power Dissipation	2.4W	5.0W

The host system must provide appropriate thermal management to maintain the IPM base surface below 55°C and the PCB top EMI shield surface below 70°C. Figure 13 below indicates the primary heat generating surfaces that require heat sinking. The IPM bottom surface should be connected to a surface capable of dissipating up to 2.2 W. The electronics top shield should be connected to a surface capable of dissipating up to 1.8 W independently. These values are for maximum possible heat generation (i.e., displaying full white image). The heat dissipating surfaces should also be used to provide mechanical stability for the PSE. The PSE will automatically shut down if the internal IPM temperature exceeds 60°C.

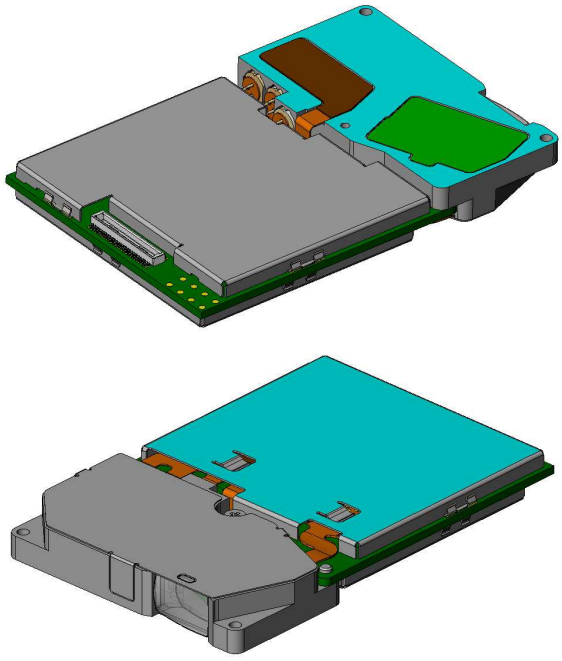


Figure 13. Heat dissipating surfaces of PSE. Shown in blue are IPM housing bottom and EPM top shield.

6. References

The following documents may be useful for reference in connection with this datasheet.

- DA0135286 PSE-0403 Product Brief
- DC0135108 PSE Assembly Drawing
- DA0135396 PSE Programmer's Guide
- DC0124088 PicoP Application Layer Command Reference
- DC0120809 PicoP Command Protocol (PPCP) Specification
- IEC 60825-1:2007 Safety of Laser Products – Part 1: Equipment Classification, Requirements and User's Guide
- CDRH Laser Notice No. 50 Laser Products-Conformance with IEC 60825-1