COMSATS University Islamabad

Spring 2021

EEE440 Computer Architecture

Sessional-II

Program: BCS-7A, B, C
Semester: Spring 2021
Instructor: M. Dilshad Sabir

Total Marks: 15
Date: 06 May, 2021
Time: 60 min

Question No. 01 Consider the following code, which multiplies two vectors that contain single-precision complex values:

```
for (i=0;i<300;i++) {
c_re[i] = a_re[i] * b_re[i] – a_im[i] * b_im[i];
c_im[i] = a_re[i] * b_im[i] + a_im[i] * b_re[i];
}
```

Assume that the processor runs at 700 MHz and has a maximum vector length of 64. The load/store unit has a start-up overhead of 15 cycles; the multiply unit, 8 cycles; and the add/subtract unit, 5 cycles.

a. What is the arithmetic intensity of this kernel? [2.5]
b. Convert this loop into VMIPS assembly code using strip mining. [2.5]
c. Assuming chaining and a single memory pipeline, how many chimes are required? How many clock cycles are required per complex result value, including start-up overhead? [2.5]
d. If the vector sequence is chained, how many clock cycles are required per complex result value, including overhead? [2.5]

Question No. 02 Consider a 32-bit microprocessor that has an on-chip 16 K-byte four-way set-associative cache. Assume that the cache has a line size of four 32-bit works. Draw a block diagram of this cache showing its organization and how different address fields are used to determine a cache hit/miss. [5]