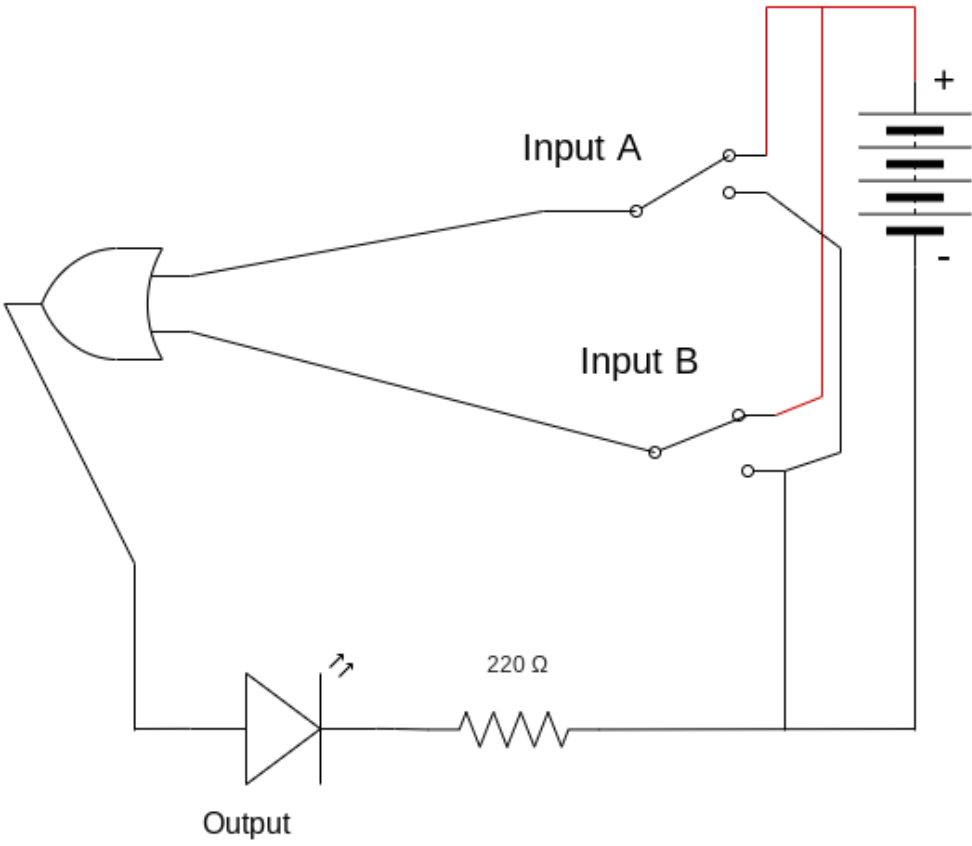
Alejandro Castaneda
TEJ3M1
Unit #4-11

AND Gate with Transistor

And Gate with Transistor		
Input A	Input B	Output
0	0	0
0	1	0
1	0	0
1	1	1



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