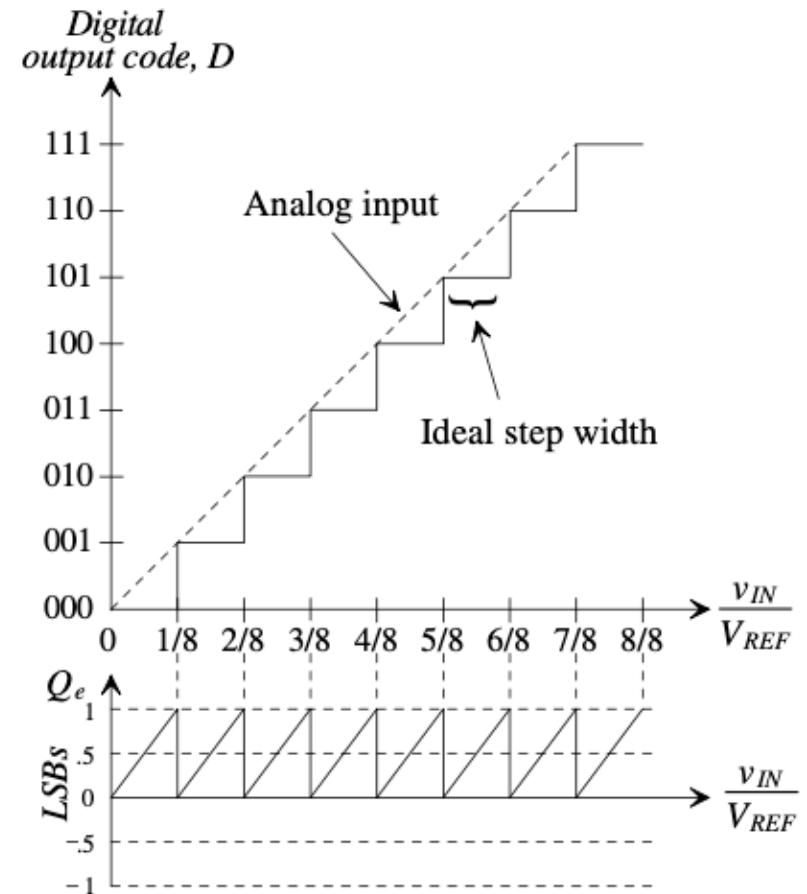
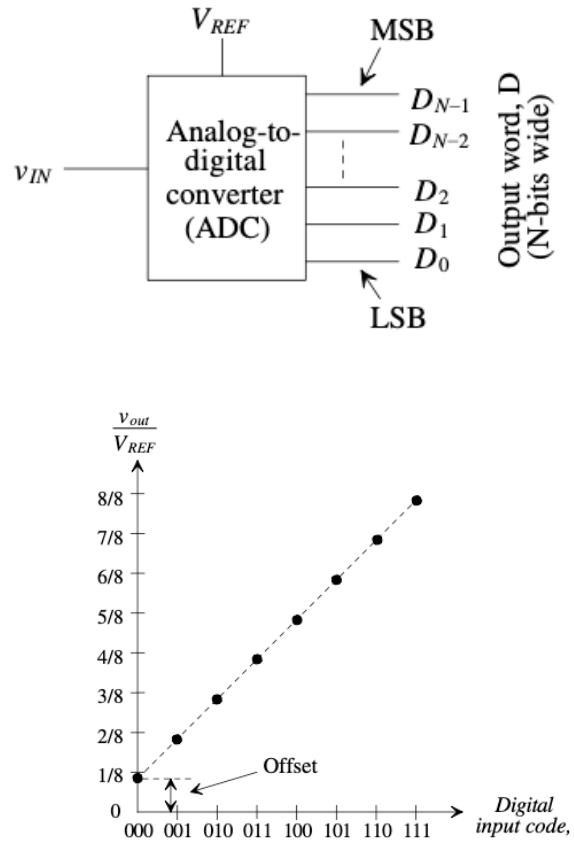


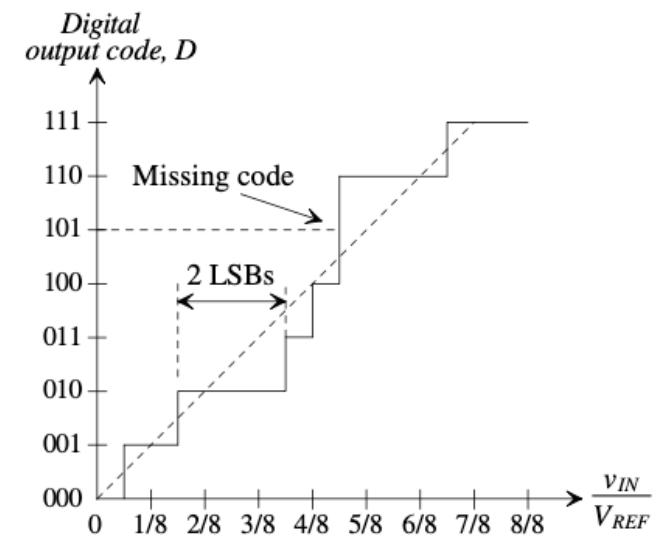
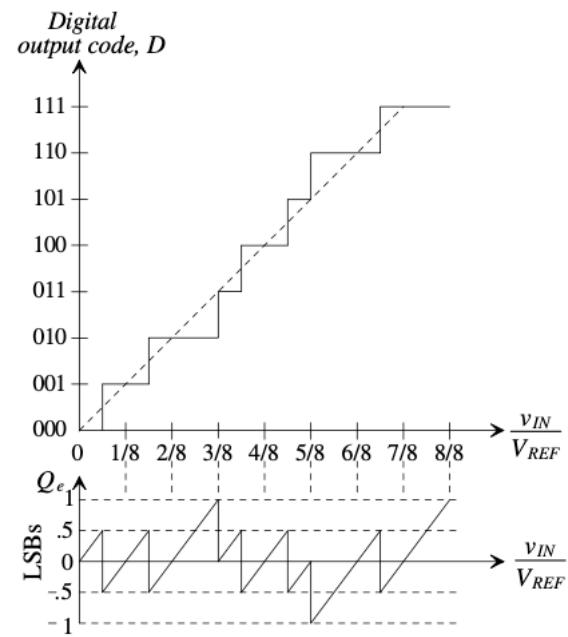
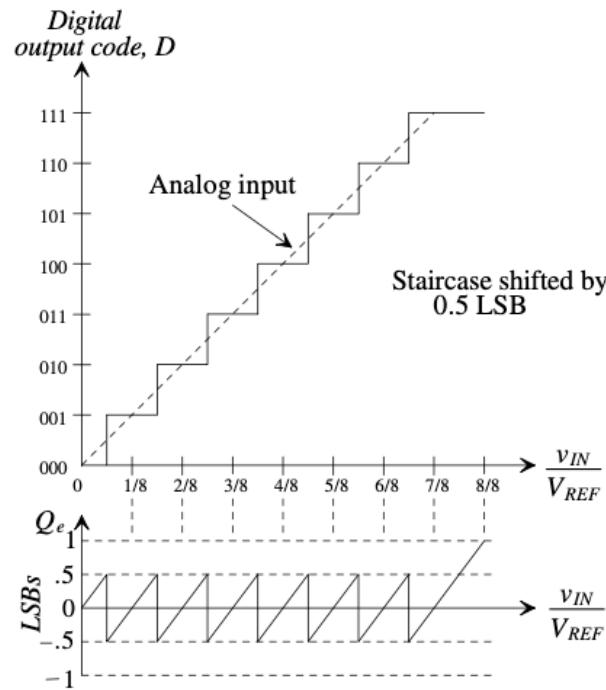
# Analysis of the SAR-ADC mismatch

- Explaining what is Integral and Differential non-linearity in DACs and ADCs
- Simulation & Performed analysis
- Results
- Next Steps regarding LVS

# Integral and Differential non-linearities



# Integral and Differential non-linearities



# Simulation and performed analysis

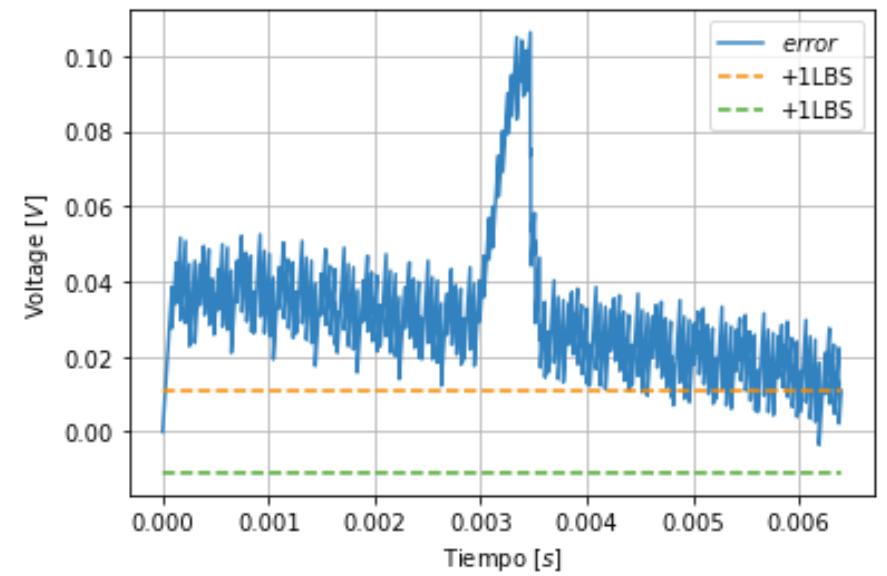
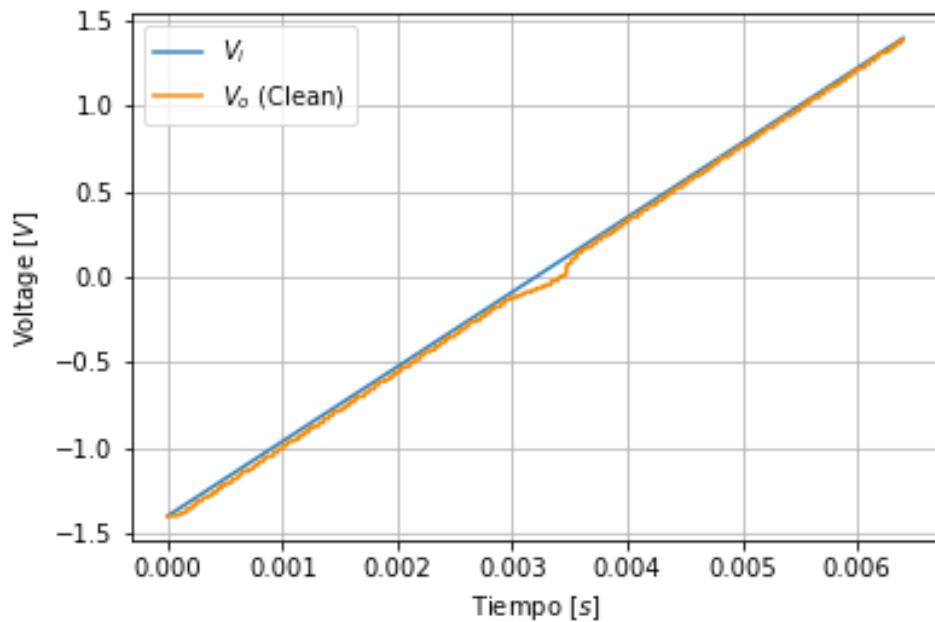
```
def rawread(fname: str):

    fp = open(fname, 'rb')
    plot = {}
    count = 0
    arrs = []
    plots = []
    while (True):
        try:
            mdata = fp.readline(BSIZE_SP).split(b':', maxsplit=1)
        except:
            raise
        if len(mdata) == 2:
            if mdata[0].lower() in MDATA_LIST:
                plot[mdata[0].lower()] = mdata[1].strip()
            if mdata[0].lower() == b'variables':
                nvars = int(plot[b'no. variables'])
                npoints = int(plot[b'no. points'])
                plot['varnames'] = []
                plot['varunits'] = []
                for varn in range(nvars):
                    varspec = (fp.readline(BSIZE_SP).strip()
                               .decode('ascii').split())
                    assert(varn == int(varspec[0]))
                    plot['varnames'].append(varspec[1])
                    plot['varunits'].append(varspec[2])
            if mdata[0].lower() == b'binary':
                rowdtype = np.dtype({'names': plot['varnames'],
                                    'formats': [np.complex_ if b'complex'
                                                in plot[b'flags']
                                                else np.float_] * nvars})
```

```
#procesando la matriz de bits y ploteando
R = 8
L = 2**R
vp = 1.4
vn = -1.4
vref = (vp - (vn))
v_lvl = vref/L
level_out = []
for x in binary_out:
    x_dec = int(''.join(map(lambda x: str(int(x)), x)), 2)
    level_out.append(x_dec)
level_out = np.array(level_out)
v_out = vn + (level_out * v_lvl)
vinp = arrs[0][b"v(vinp)"]
vinn = arrs[0][b"v(vinn)"]
vcm = 0.7
vin = 2 * (vinp - vcm)
time = arrs[0]["time"]
```

$$1LSB = \frac{V_{ref}}{2^N} = \frac{2.8}{2^8} \approx 11mV$$

# Simulation and performed analysis



$$1LSB = \frac{V_{ref}}{2^N} = \frac{2.8}{2^8} \approx 11mV$$

# Next steps regarding LVS

- I've performed LVS with simpler designs using NetGen and sky130
- Why the xschem spice is different for LVS?
- Which .mag file should I use?
- Can the LVS be executed with a GDS file?

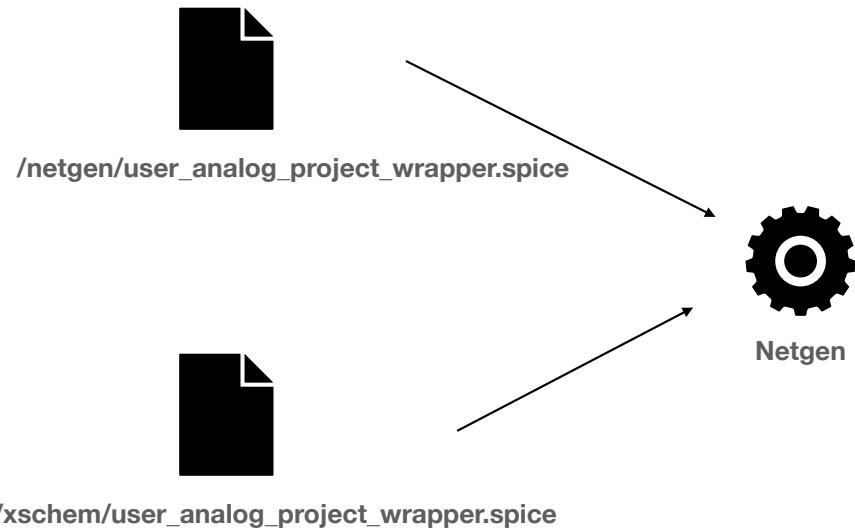
# **SAR-ADC**

## **Activity Report**

**Alejandro Juárez Lora, July 31st, 2023**

# LVS

## Running Netgen with original files



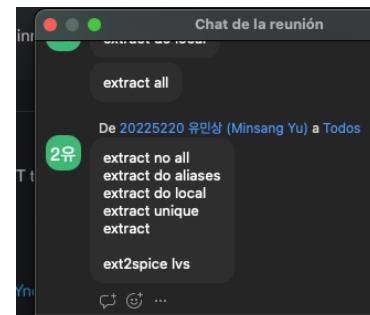
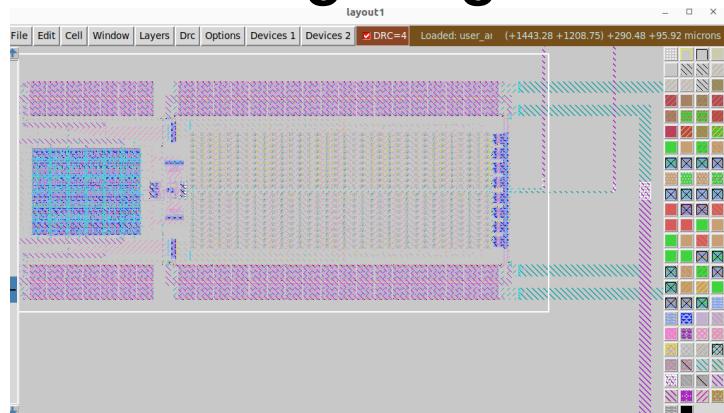
```
St
Contents of circuit 1: Circuit: 'user_analog_project_wrapper'
H|Circuit user_analog_project_wrapper contains 2485 device instances.
  Class: sky130_fd_pr_nfet_01v8 instances: 1222
D|  Class: sky130_fd_pr_cap_mim_m3_1 instances: 20
  Class: sky130_fd_pr_nfet_01v8_lvt instances: 16
D|  Class: sky130_fd_pr_pfet_01v8_hvt instances: 1211
  Class: sky130_fd_pr_pfet_01v8 instances: 12
M|  Class: sky130_fd_pr_pfet_01v8_lvt instances: 4
Circuit contains 1432 nets, and 658 disconnected pins.
Contents of circuit 2: Circuit: 'user_analog_project_wrapper'
P|Circuit user_analog_project_wrapper contains 39 device instances.
  Class: sky130_fd_pr_cap_mim_m3_1 instances: 2
V|  Class: sky130_fd_pr_cap_mim_m3_2 instances: 2
  Class: sky130_fd_pr_res_xhigh_po_0p69 instances: 5
T|  Class: sky130_fd_sc_hvl_buf_8 instances: 4
  Class: sky130_fd_sc_hvl_schmittbuf_1 instances: 2
i|  Class: sky130_fd_pr_nfet_g5v0d10v5 instances: 6
  Class: sky130_fd_sc_hvl_inv_8 instances: 2
O|  Class: sky130_fd_pr_pfet_g5v0d10v5 instances: 16
Circuit contains 30 nets, and 29 disconnected pins.

Circuit 1 contains 2485 devices, Circuit 2 contains 39 devices. *** MISMATCH ***
Circuit 1 contains 1256 nets, Circuit 2 contains 30 nets. *** MISMATCH ***

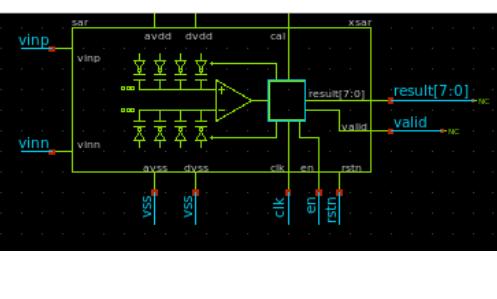
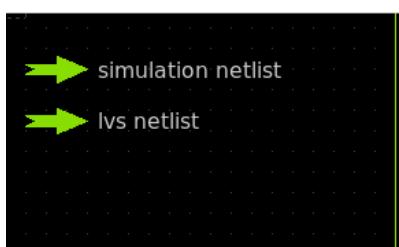
Final result:
Netlists do not match.
Logging to file "comp.out" disabled
LVS Done.
alex@alex-Parallels-Virtual-Platform:~/Desktop/SAR_IPN/netgen$
```

# LVS

## Running Netgen with re-compiled files



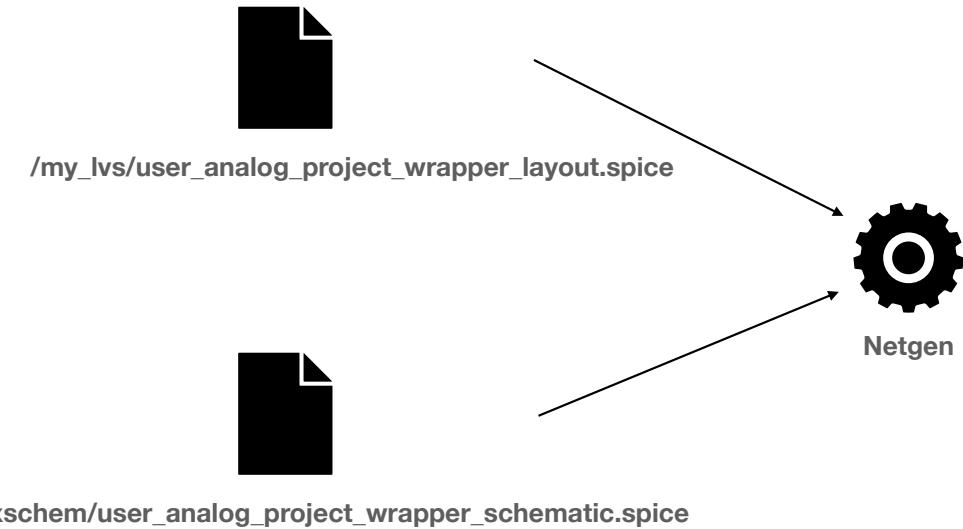
/my\_lvs/user\_analog\_project\_wrapper\_layout.spice



/my\_lvs/user\_analog\_project\_wrapper\_schematic.spice

# LVS

## Running Netgen with re-compiled files



```
St
HFlattening instances of SAR in file user_analog_project_wrapper_layout.spice
HFlattening instances of sar in file user_analog_project_wrapper_schematic.spice

DContents of circuit 1: Circuit: 'user_analog_project_wrapper'
Circuit user_analog_project_wrapper contains 2437 device instances.
D Class: sky130_fd_pr_nfet_01v8 instances: 1175
M Class: inv_4 instances: 16
M Class: sky130_fd_pr_cap_mim_m3_1 instances: 20
M Class: sky130_fd_pr_nfet_01v8_lvt instances: 10
P Class: sky130_fd_sc_hd_inv_2 instances: 37
P Class: latch instances: 1
V Class: sky130_fd_sc_hd_decap_3 instances: 1
V Class: sky130_fd_sc_hd_decap_8 instances: 1
T Class: sky130_fd_pr_pfet_01v8_hvt instances: 1162
T Class: sky130_fd_pr_pfet_01v8 instances: 14
Circuit contains 1421 nets, and 671 disconnected pins.
ICContents of circuit 2: Circuit: 'user_analog_project_wrapper'
Circuit user_analog_project_wrapper contains 1 device instances.
O Class: latch instances: 1
Circuit contains 21 nets, and 30 disconnected pins.

Circuit 1 contains 2437 devices, Circuit 2 contains 1 devices. *** MISMATCH ***
Circuit 1 contains 1255 nets, Circuit 2 contains 6 nets. *** MISMATCH ***

Final result:
Netlists do not match.
Logging to file "comp.out" disabled
LVS Done.
alex@alex-Parallels-Virtual-Platform:~/Desktop/SAR_IPN/my_lvs$
```

# **Future work**

## **Next steps**

- Post-layout simulation
  - Ext2sim command
- Create own layout
  - Mixed signal synthesis with OpenROAD, analog blocks as a blackbox

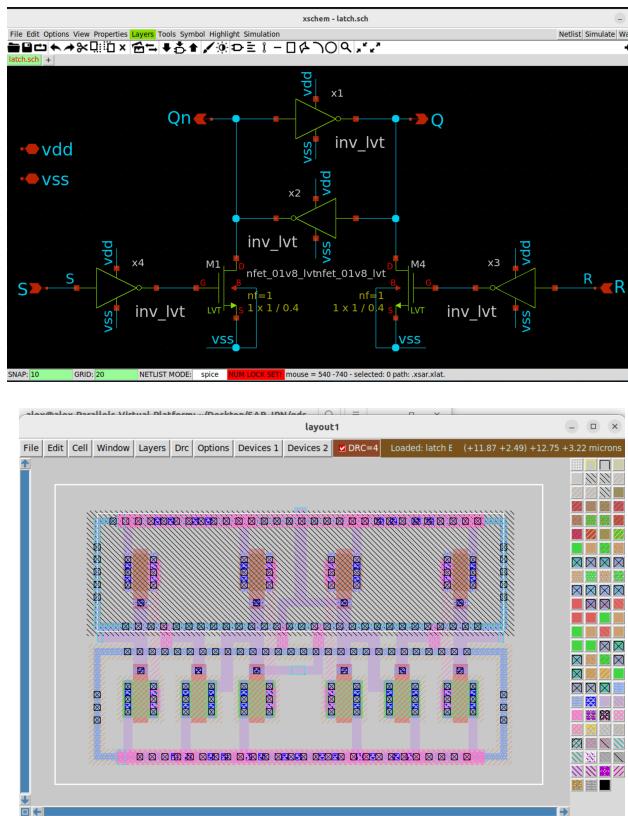
# **SAR-ADC**

## **Activity Report**

**Alejandro Juárez Lora, Sept 4, 2023**

# LVS Advancements

## Latch, separately extracted



```

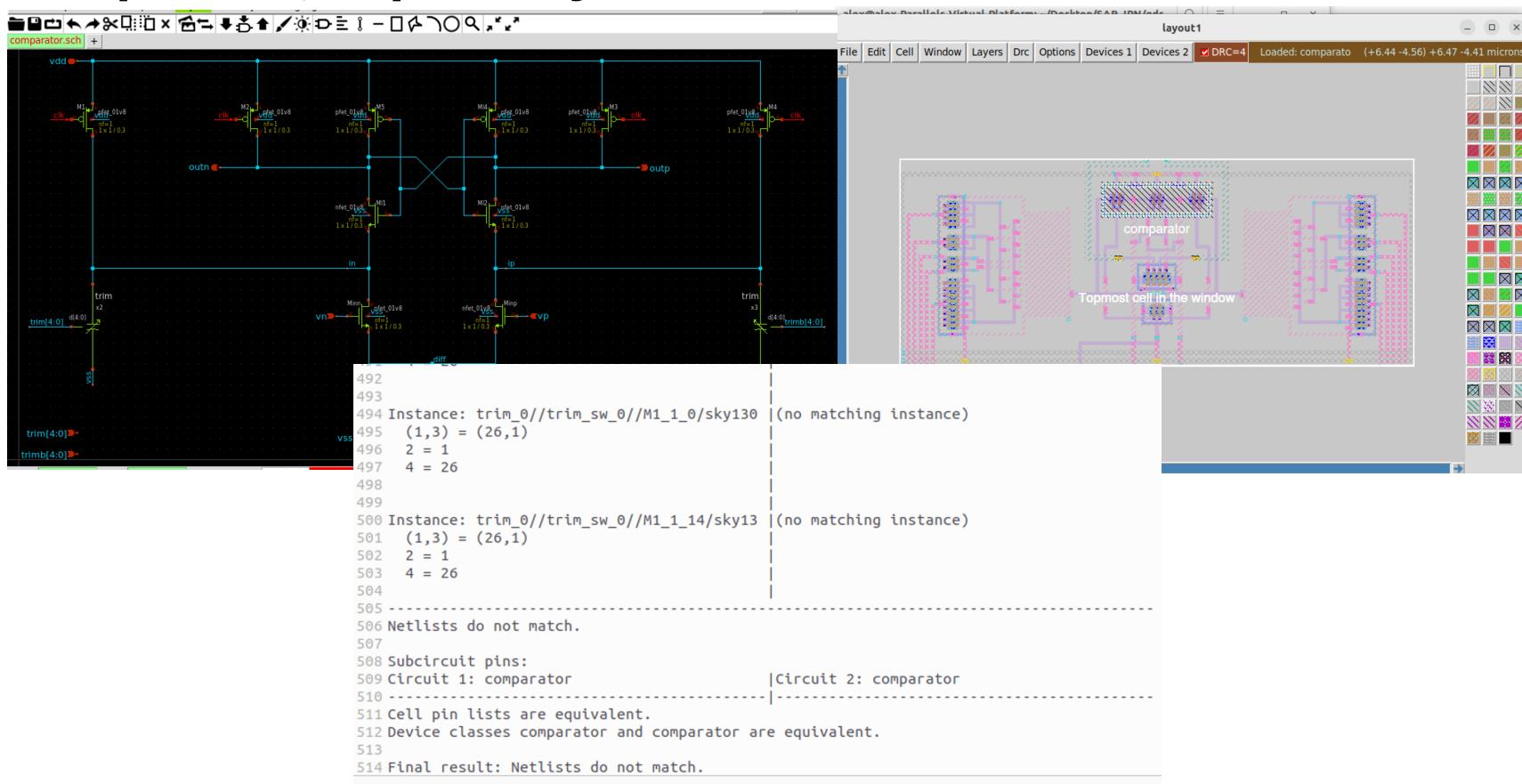
latch.out
~/Desktop/SAR_IPN/my_lvs/latch

56
57 Net: VSUBS
58 sky130_fd_pr_nfet_01v8_lvt/4 = 1 |(no matching net)
59 -
60 Netlists do not match.
61 Flattening non-matched subcircuits inv_lvt inv_lvt
62 Flattening unmatched subcell M2_1 in circuit latch (0)(1 instance)
63 Flattening unmatched subcell M1_2 in circuit latch (0)(1 instance)
64
65 Subcircuit summary:
66 Circuit 1: latch |Circuit 2: latch
67 -
68 sky130_fd_pr_nfet_01v8_lvt (6) |sky130_fd_pr_nfet_01v8_lvt (6)
69 sky130_fd_pr_pfet_01v8_lvt (4) |sky130_fd_pr_pfet_01v8_lvt (4)
70 Number of devices: 10 |Number of devices: 10
71 Number of nets: 8 |Number of nets: 8
72 -
73 Resolving symmetries by property value.
74 Resolving symmetries by pin name.
75 Netlists match uniquely.
76
77 Subcircuit pins:
78 Circuit 1: latch |Circuit 2: latch
79 -
80 S |S
81 R |R
82 vdd |vdd
83 Qn |Qn
84 Q |Q
85 vss |vss
86 -
87 Cell pin lists are equivalent.
88 Device classes latch and latch are equivalent.
89
90 Final result: Circuits match uniquely.
91 .

```

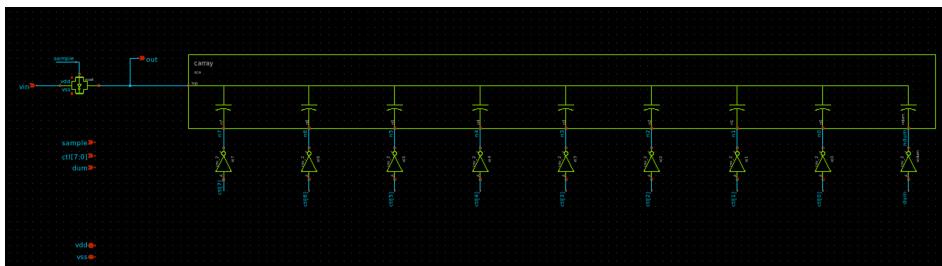
# LVS Advancements

## Comparator, separately extracted

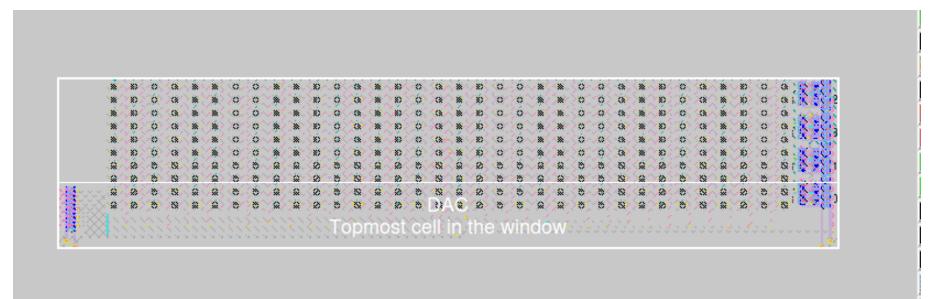


# LVS Advancements

## DAC, separately extracted



```
738 Net: /sw_top_2/dummy_41          |(no matching net)
739  inv_4/proxyproxya_75_55# = 1
740
741 Net: /sw_top_1/dummy_36          |(no matching net)
742  inv_4/proxyproxya_75_305# = 1
743
744 Net: /sw_top_1/dummy_42          |(no matching net)
745  inv_4/proxyproxya_75_305# = 1
746
747 Net: /sw_top_2/dummy_36          |(no matching net)
748  inv_4/proxyproxya_75_305# = 1
749
750 Net: /sw_top_2/dummy_42          |(no matching net)
751  inv_4/proxyproxya_75_305# = 1
752
753 Net: /sw_top_1/dummy_37          |(no matching net)
754  inv_4/proxyproxya_157_55# = 1
755
756 Net: /sw_top_1/dummy_43          |(no matching net)
757  inv_4/proxyproxya_157_55# = 1
758
759 Net: /sw_top_2/dummy_37          |(no matching net)
760  inv_4/proxyproxya_157_55# = 1
```



```
1230 Netlists do not match.
1231
1232 Subcircuit pins:
1233 Circuit 1: DAC
1234 -----
1235 ctl7
1236 ctl6
1237 dum
1238 ctl0
1239 ctl1
1240 ctl5
1241 ctl4
1242 ctl2
1243 ctl3
1244 en_buf
1245 out
1246 sample
1247 vin
1248 enb
1249 Cell pin lists are equivalent.
1250 Device classes DAC and dac are equivalent.
1251
1252 Final result: Netlists do not match.
```

# LVS Advancements

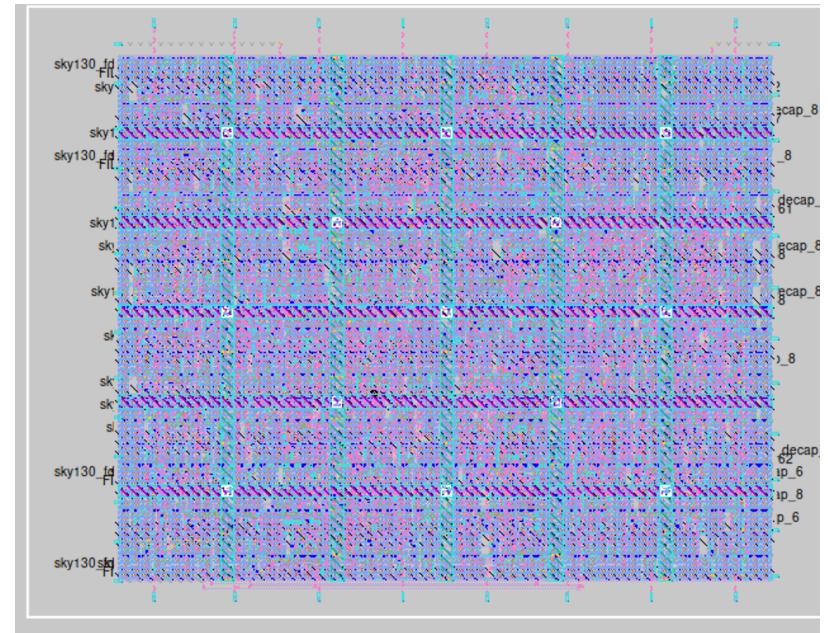
## sarlogic, separately extracted

Open +/-

**sar\_logic\_sky.sp**  
-/Desktop/SAR\_IPN/xschem/sar/control

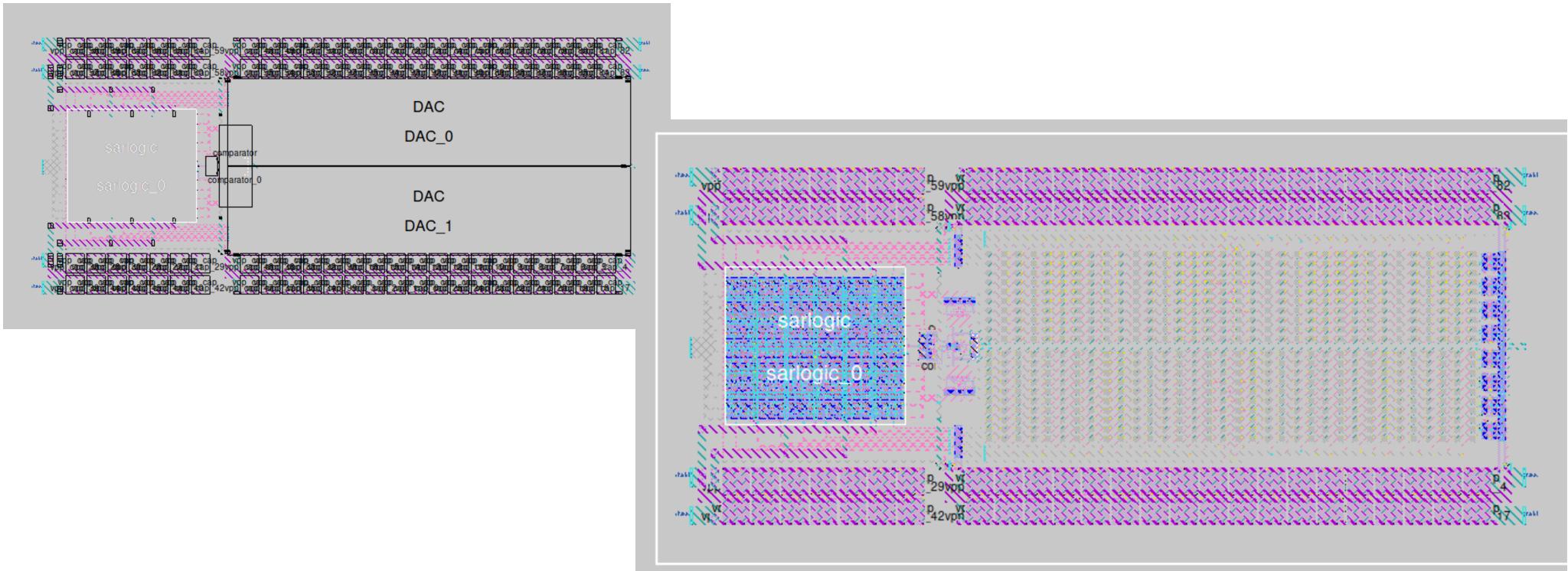
```
1 * SPICE netlist generated by Yosys 0.9 (git sha1 1979e0b)
2
3 .SUBCKT sar_logic clk rstn en comp cal valid result_0_ result_1_ result_2_ result_3_ result_4_
ctlp_0_ ctlp_1_ ctlp_2_ ctlp_3_ ctlp_4_ ctlp_5_ ctlp_6_ ctlp_7_ ctnl_0_ ctnl_1_ ctnl_2_ ctnl_3_
trim_1_ trim_2_ trim_3_ trim_4_ trimb_0_ trimb_1_ trimb_2_ trimb_3_ trimb_4_ clkc
4 X0 1 state_2_ VPWR VGND VPB VNB sky130_fd_sc_hd_clkinv_1
5 X1 2 cal_count_1_ VPWR VGND VPB VNB sky130_fd_sc_hd_clkinv_1
6 X2 3 cal_count_2_ VPWR VGND VPB VNB sky130_fd_sc_hd_clkinv_1
7 X3 ctlp_4_ mask_4_ result_4_ VPWR VGND VPB VNB sky130_fd_sc_hd_lpflow_inputiso1p_1
8 X4 ctnl_4_ ctlp_4_ VPWR VGND VPB VNB sky130_fd_sc_hd_clkinv_1
9 X5 ctlp_5_ result_5_ mask_5_ VPWR VGND VPB VNB sky130_fd_sc_hd_lpflow_inputiso1p_1
10 X6 ctnl_5_ ctlp_5_ VPWR VGND VPB VNB sky130_fd_sc_hd_clkinv_1
11 X7 ctlp_6_ result_6_ mask_6_ VPWR VGND VPB VNB sky130_fd_sc_hd_lpflow_inputiso1p_1
12 X8 ctnl_6_ ctlp_6_ VPWR VGND VPB VNB sky130_fd_sc_hd_clkinv_1
13 X9 ctlp_7_ result_7_ mask_7_ VPWR VGND VPB VNB sky130_fd_sc_hd_lpflow_inputiso1p_1
14 X10 ctnl_7_ ctlp_7_ VPWR VGND VPB VNB sky130_fd_sc_hd_clkinv_1
15 X11 4 cal_it_3_ cal_it_2_ cal_it_0_ cal_it_1_ VPWR VGND VPB VNB sky130_fd_sc_hd_and4b_1
16 X12 5 cal_it_3_ cal_it_2_ cal_it_0_ cal_it_1_ VPWR VGND VPB VNB sky130_fd_sc_hd_nand4b_1
17 X13 6 cal_it_0_ 5 VPWR VGND VPB VNB sky130_fd_sc_hd_nand2_1
18 X14 7 state_1_ state_0_ VPWR VGND VPB VNB sky130_fd_sc_hd_nand2b_1
19 X15 8 state_1_ state_0_ state_2_ VPWR VGND VPB VNB sky130_fd_sc_hd_nand3b_1
20 X16 9 4 8 VPWR VGND VPB VNB sky130_fd_sc_hd_nor2_1
21 X17 10 trim_mask_0_ cal_it_0_ VPWR VGND VPB VNB sky130_fd_sc_hd_nand2_1
22 X18 11 4 10 8 VPWR VGND VPB VNB sky130_fd_sc_hd_a21oi_1
23 X19 12 state_2_ en 7 VPWR VGND VPB VNB sky130_fd_sc_hd_o21bai_1
```

12219 VPWR |(no matching pin)  
12220 VGND |(no matching pin)  
12221 -----  
12222 Cell pin lists for sarlogic and sar\_logic altered to match.  
12223 Device classes sarlogic and sar\_logic are equivalent.  
12224  
12225 Final result: Top level cell failed pin matching.



# LVS Advancements

Possible mismatch reason: capacitors out of hierarchy



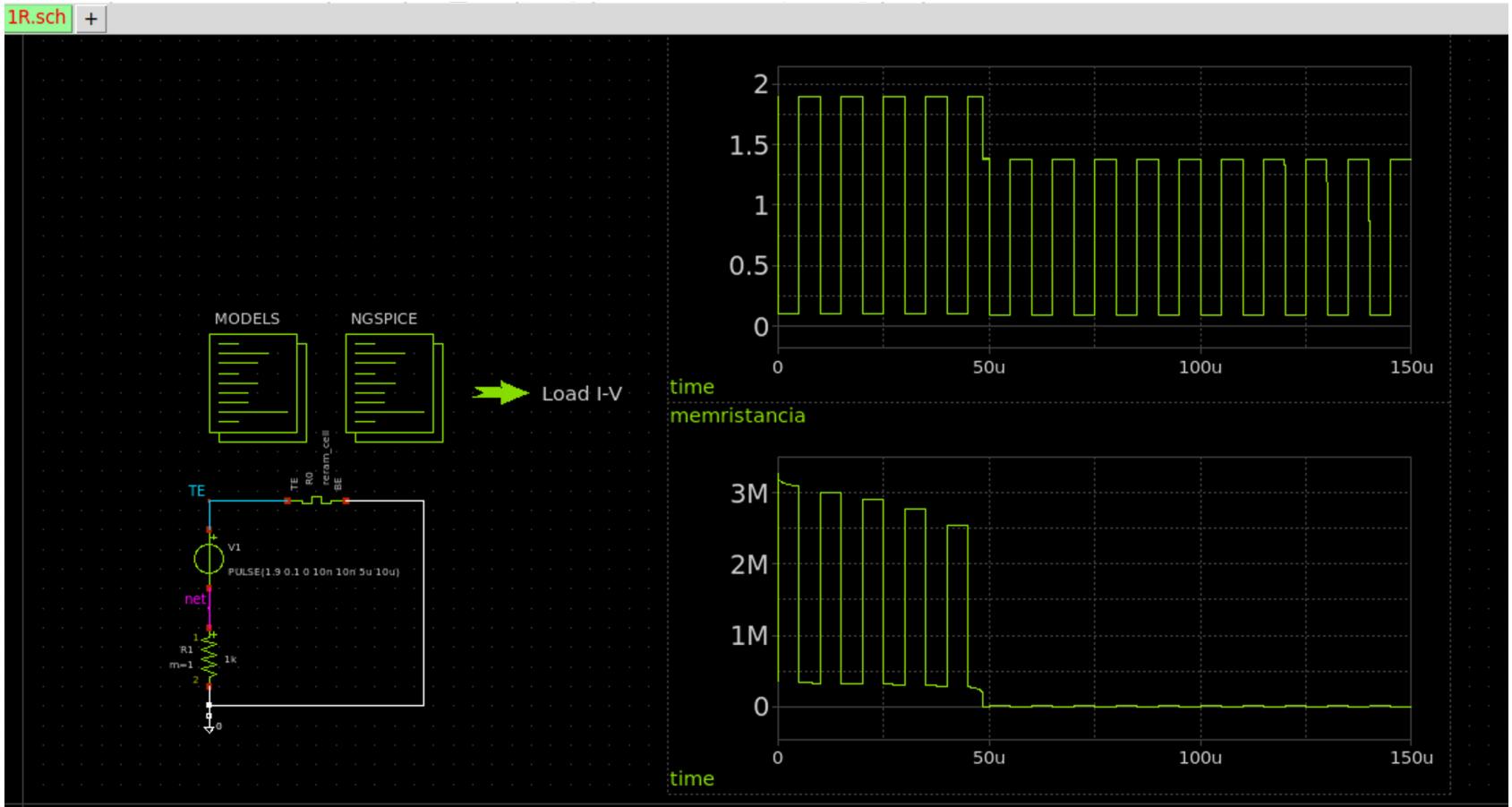
# **SAR-ADC**

## **Activity Report**

**Alejandro Juárez Lora, Sept 4, 2023**

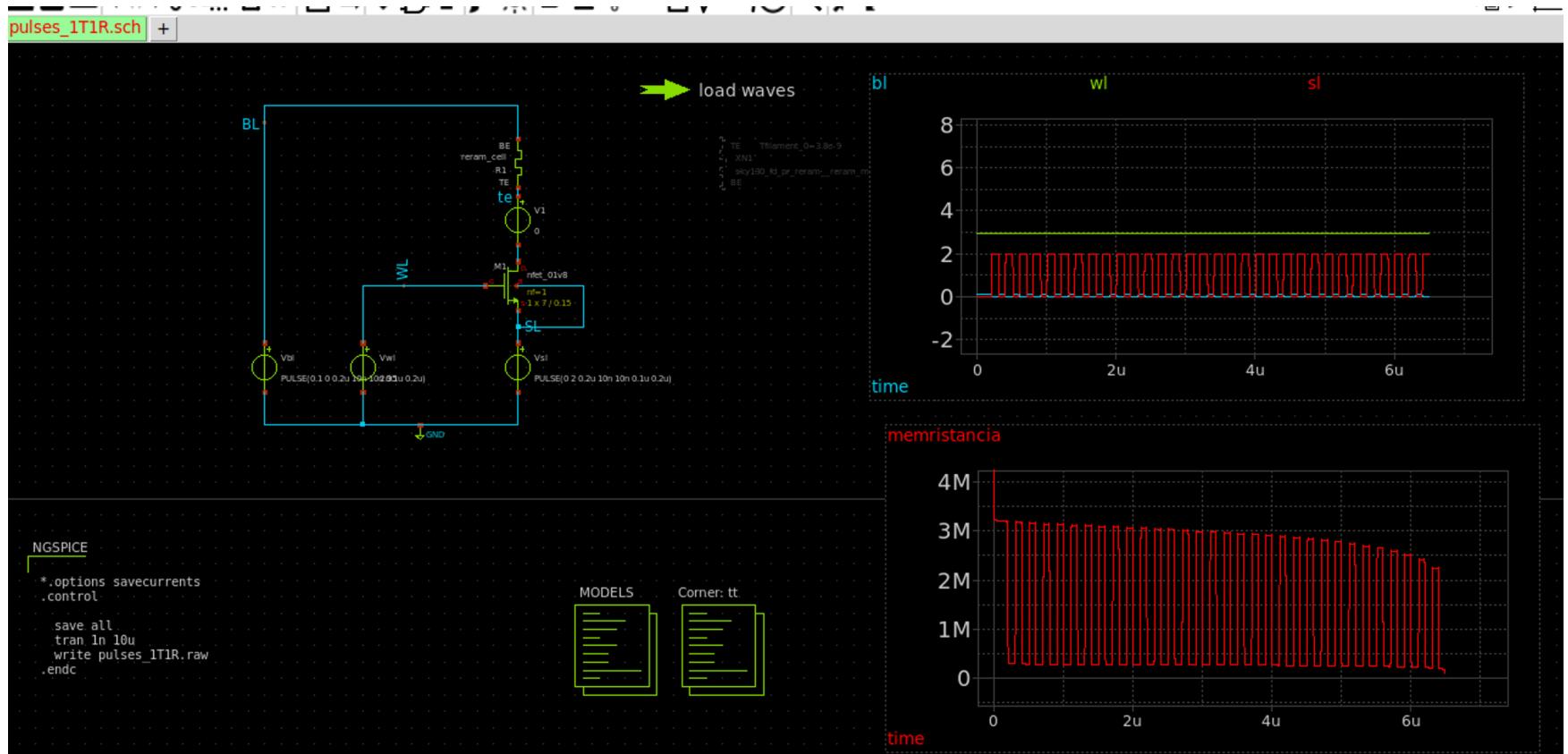
# RRAM simulation

1R.sch



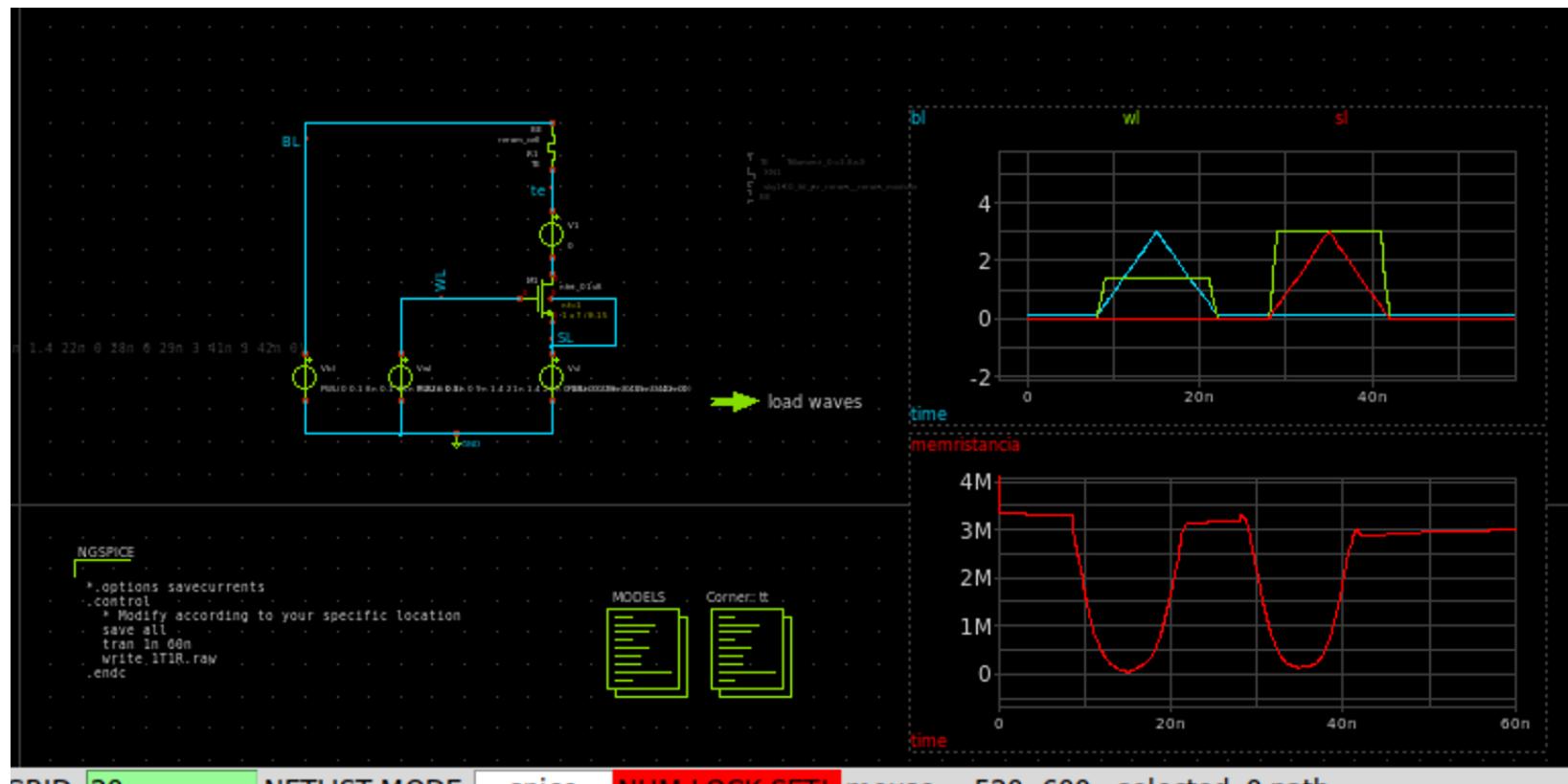
# RRAM simulation

## 1T1R.sch (pulses)



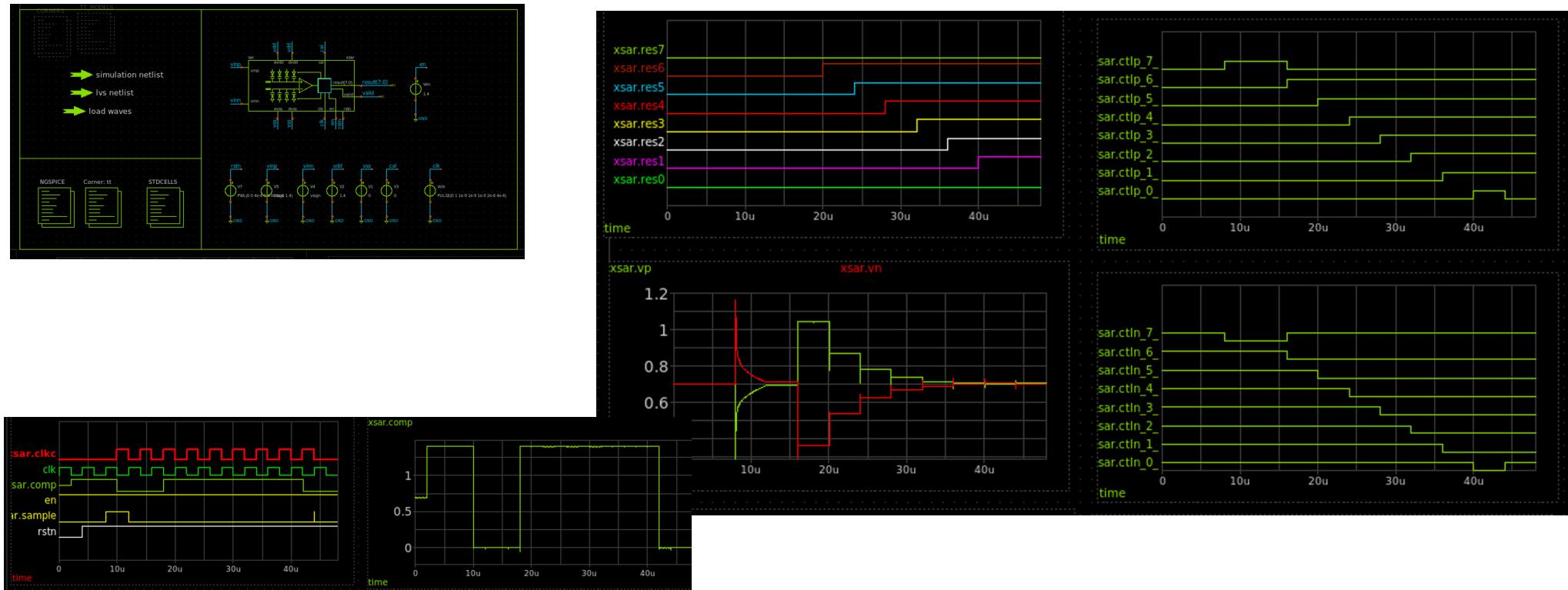
# RRAM simulation

## 1T1R.sch (read & write)



# Simulation

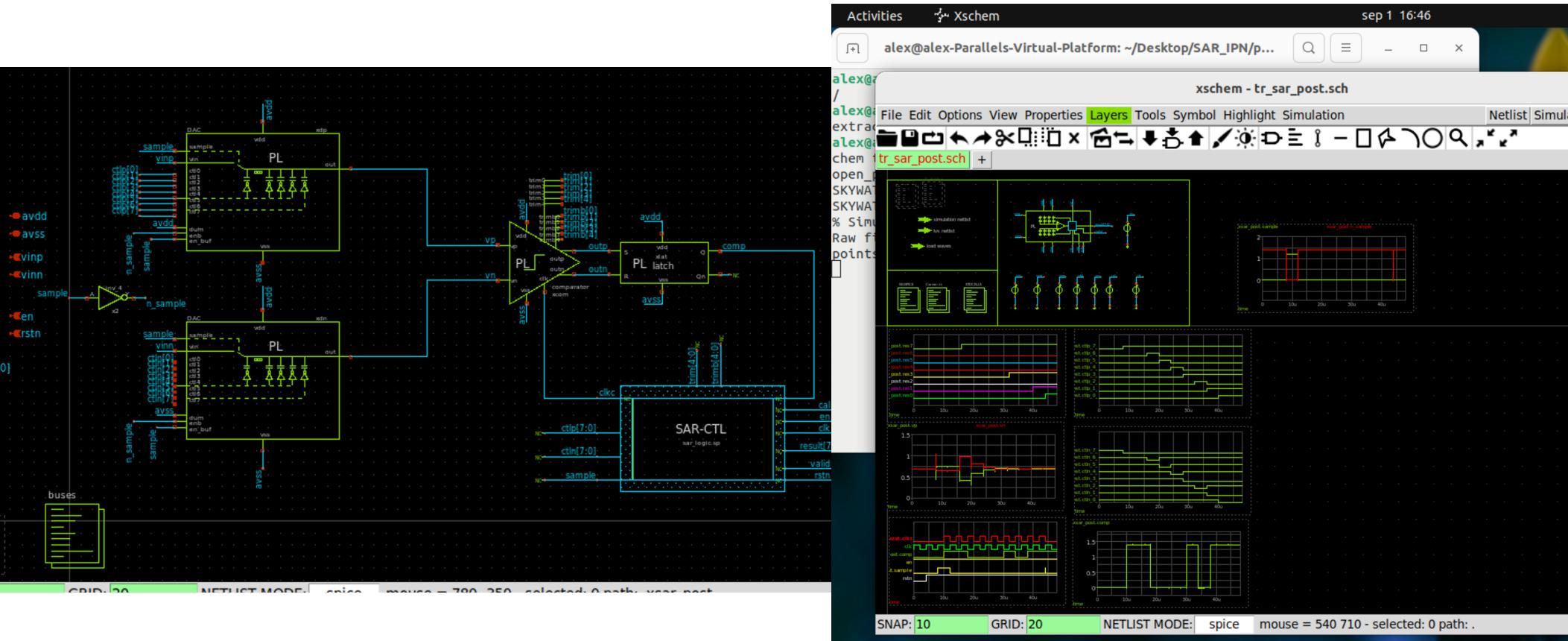
## **Pre-layout simulation: What are we expecting to obtain**



# Post layout Simulation

Mixed signal simulation, with light parasitic extraction

extract  
ext2spice -F



# Post layout Simulation

## Transistors with zero width and length appeared

```

extract do local
extract all
ext2sim labels on
ext2sim
extresist tolerance 10
extresist
ext2spice hierarchy on
ext2spice cthresh 0 rthresh 0
ext2spice extresist on
ext2spice -F -B

```

```

extract
ext2spice -F

```

```

Users > alejandrojuarezlora > EDA > SAR_IPN > post_layout_separated > extracted.spice
779 1 vdd vss 2.09f
780 2 w_302_2337# vss 4.58f
781
782
783 subckt comparator trim_3 trim_2 trim_0 trim_1 trim_4 trimb_4 trimb_1 trimb_0 trimb_
784 trimb_3 outn outp clk vdd vp vn vss
785 trim_0 trim_0/n3 trim_0/n4 trim_0/n2 trim_0/n1 trim_0/n0 trim_4 trim_3 trim_2 trim_
786 trim_0 vss trim_0/drain trim
787 trim_1 trim_1/n3 trim_1/n4 trim_1/n2 trim_1/n1 trim_1/n0 trimb_4 trimb_3 trimb_2
788 trimb_1 trim_0 vss trim_1/drain trim
789 comparator_core_0 vdd outp outn clk trim_1/drain trim_0/drain comparator_core_0/dif
790 vp vn vss comparator_core
791 0 trim_0/n4 trim_0/drain 6.86f
792 1 trim_0/n3 trim_0/drain 3.41f
793 2 trim_1/n4 trim_1/drain 6.86f
794 3 vss vdd 5.14f
795 4 trim_1/drain trim_1/n3 3.41f
796 5 clk 0 3.16f
797 6 vdd 0 6.8f
798 7 trim_1/drain 0 -3.83f
799 8 trim_0/drain 0 -3.86f
800 9 vss 0 5.55f
801
802
803 subckt sky130_fd_sc_hd_decap_4 VGND VPWR VPB VNB
804 0 VGND VPWR VGND VNB sky130_fd_pr_nfet_01v8 ad=0.286 pd=3.24 as=0.143 ps=1.62 w=0.
805 1 VPWR VGND VPWR VPB sky130_fd_pr_pfet_01v8_hvt ad=0.452 pd=4.52 as=0.226 ps=2.26
806
807
808 subckt sky130_fd_sc_hd_decap_8 VPWR VGND VPB VNB
809 0 VGND VPWR VGND VNB sky130_fd_pr_nfet_01v8 ad=0.286 pd=3.24 as=0.143 ps=1.62 w=0.
810 1 VPWR VGND VPWR VPB sky130_fd_pr_pfet_01v8_hvt ad=0.452 pd=4.52 as=0.226 ps=2.26
811
812
813 subckt sky130_fd_sc_hd_inv_2 VPWR VGND VPB VNB Y A

```

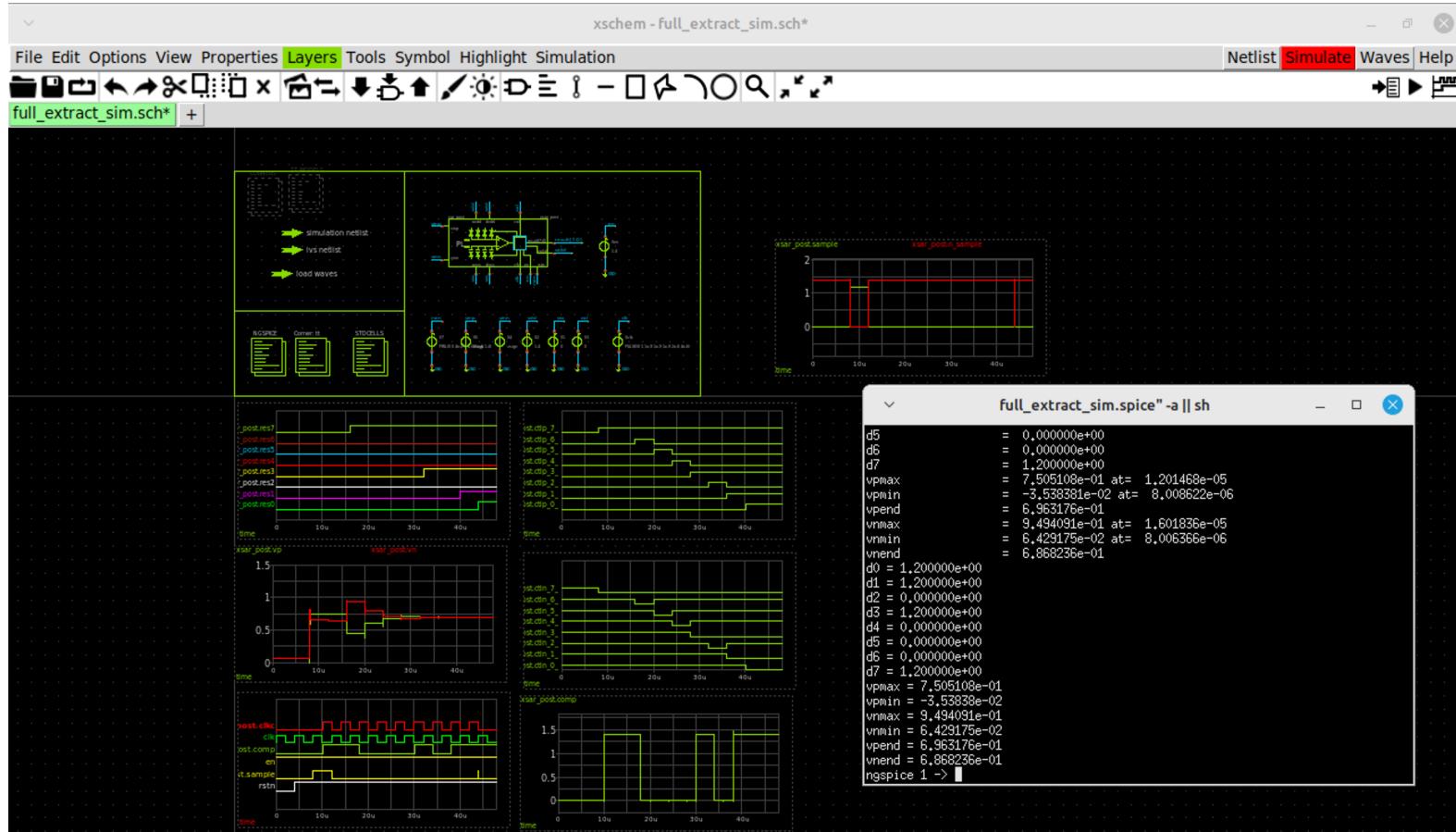
```

Users > alejandrojuarezlora > EDA > SAR_IPN > post_layout_sep_full > comparator.spice
327 C49 diff vss 0.226f
328 .ends
329
330
331 subckt comparator trim_3 trim_2 trim_0 trim_1 trim_4 trimb_4 trimb_1 trimb_0 trimb_
332 + trimb_3 outn outp clk vdd vss vn vp
Xtrim_0 trim_0/n1 trim_0/n0 trim_4 trim_3 trim_2 trim_1 trim_0 trim_0/n4 trim_0/n2
+ vss trim_0/drain trim_0/n3 trim
Xtrim_1 trim_1/n1 trim_1/n0 trimb_4 trimb_3 trimb_2 trimb_1 trimb_0 trim_1/n4 trim_
+ vss trim_1/drain trim_1/n3 trim
Xcomparator_core_0 outn clk trim_1/drain trim_0/drain comparator_core_0/diff outp
+ comparator_core_0/w_302_2337# vdd vn vp vss comparator_core
338 * X0 trim_0/n4 trim_4/t7 vss vss sky130_fd_pr_nfet_01v8_lvt ad=0.29 pd=2.58 as=0.2
339 * X1 trim_0/n3 trim_3/t2 vss vss sky130_fd_pr_nfet_01v8_lvt ad=0.29 pd=2.58 as=0.2
340 * X2 vss trim_3/t3 trim_1/n3 vss sky130_fd_pr_nfet_01v8_lvt ad=0.29 pd=2.58 as=0.
341 * X3 trim_1/n3 trimb_3/t2 vss vss sky130_fd_pr_nfet_01v8_lvt ad=0.29 pd=2.58 as=0.
342 * X4 trim_0/n4 trim_4/t4 vss vss sky130_fd_pr_nfet_01v8_lvt ad=0.29 pd=2.58 as=0.2
343 * X5 trim_1/n4 trim_4/t4 vss vss sky130_fd_pr_nfet_01v8_lvt ad=0.29 pd=2.58 as=0.
344 * X6 trim_0/n4 trim_4/t1 vss vss sky130_fd_pr_nfet_01v8_lvt ad=0.29 pd=2.58 as=0.2
345 * X7 vss trim_3/t1 trim_0/n3 vss sky130_fd_pr_nfet_01v8_lvt ad=0.29 pd=2.58 as=0.2
346 * X8 trim_1/n4 trimb_4/t1 vss vss sky130_fd_pr_nfet_01v8_lvt ad=0.29 pd=2.58 as=0.
347 * X9 vss trimb_3/t1 trim_1/n3 vss sky130_fd_pr_nfet_01v8_lvt ad=0.29 pd=2.58 as=0.
348 * X10 trim_0/n2 trim_2/t1 vss vss sky130_fd_pr_nfet_01v8_lvt ad=0.29 pd=2.58 as=0.
349 * X11 trim_1/drain vp/t0 comparator_core_0/diff vss sky130_fd_pr_nfet_01v8 ad=0.29
350 * X12 comparator_core_0/diff vn/t0 trim_0/drain vss sky130_fd_pr_nfet_01v8 ad=0.29
351 * X13 vss trim_4/t6 trim_0/n4 vss sky130_fd_pr_nfet_01v8_lvt ad=0.29 pd=2.58 as=0.
352 * X14 trim_1/n2 trimb_2/t1 vss vss sky130_fd_pr_nfet_01v8_lvt ad=0.29 pd=2.58 as=0
353 * X15 vss trimb_4/t6 trim_1/n4 vss sky130_fd_pr_nfet_01v8_lvt ad=0.29 pd=2.58 as=0
354 * X16 vss trimb_4/t5 trim_1/n4 vss sky130_fd_pr_nfet_01v8_lvt ad=0.29 pd=2.58 as=0
355 * X17 comparator_core_0/diff clk/t1 vss vss sky130_fd_pr_nfet_01v8 ad=0.29 pd=2.58
356 * X18 trim_1/drain clk/t4 vdd comparator_core_0/w_302_2337# sky130_fd_pr_pfet_01v8
357 * X19 vss trim_4/t5 trim_0/n4 vss sky130_fd_pr_nfet_01v8_lvt ad=0.29 pd=2.58 as=0.
358 * X20 outp outn/t0 vdd comparator_core_0/w_302_2337# sky130_fd_pr_pfet_01v8 ad=0.2
359 * X21 vdd outp/t1 outn comparator_core_0/w_302_2337# sky130_fd_pr_pfet_01v8 ad=0.2
360 * X22 outn clk/t5 vdd comparator_core_0/w_302_2337# sky130_fd_pr_pfet_01v8 ad=0.2
361 * X23 trim_0/n3 trim_3/t0 vss vss sky130_fd_pr_nfet_01v8_lvt ad=0.29 pd=2.58 as=0

```

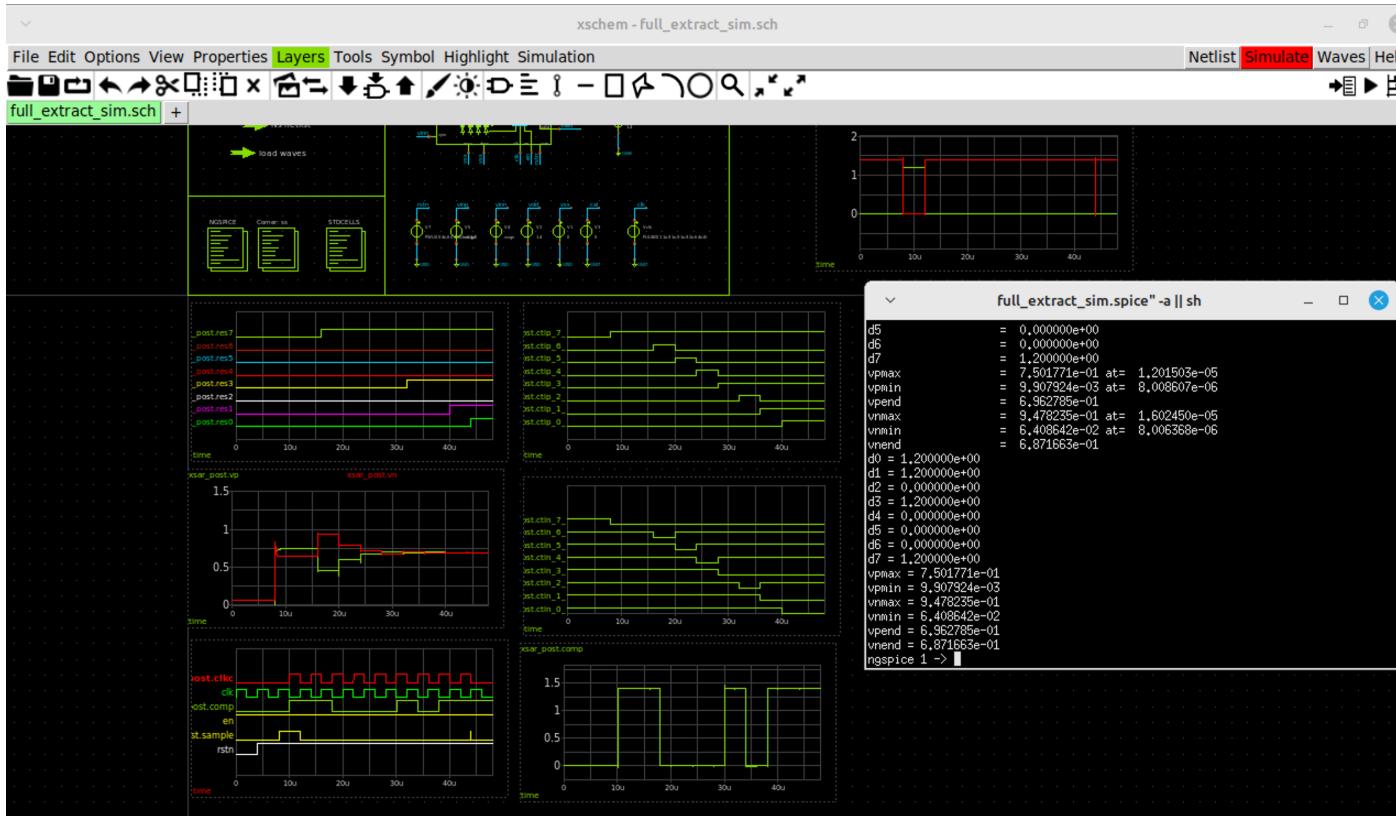
# Post layout Simulation

Mixed signal simulation, with full parasitic extraction (tt corner)



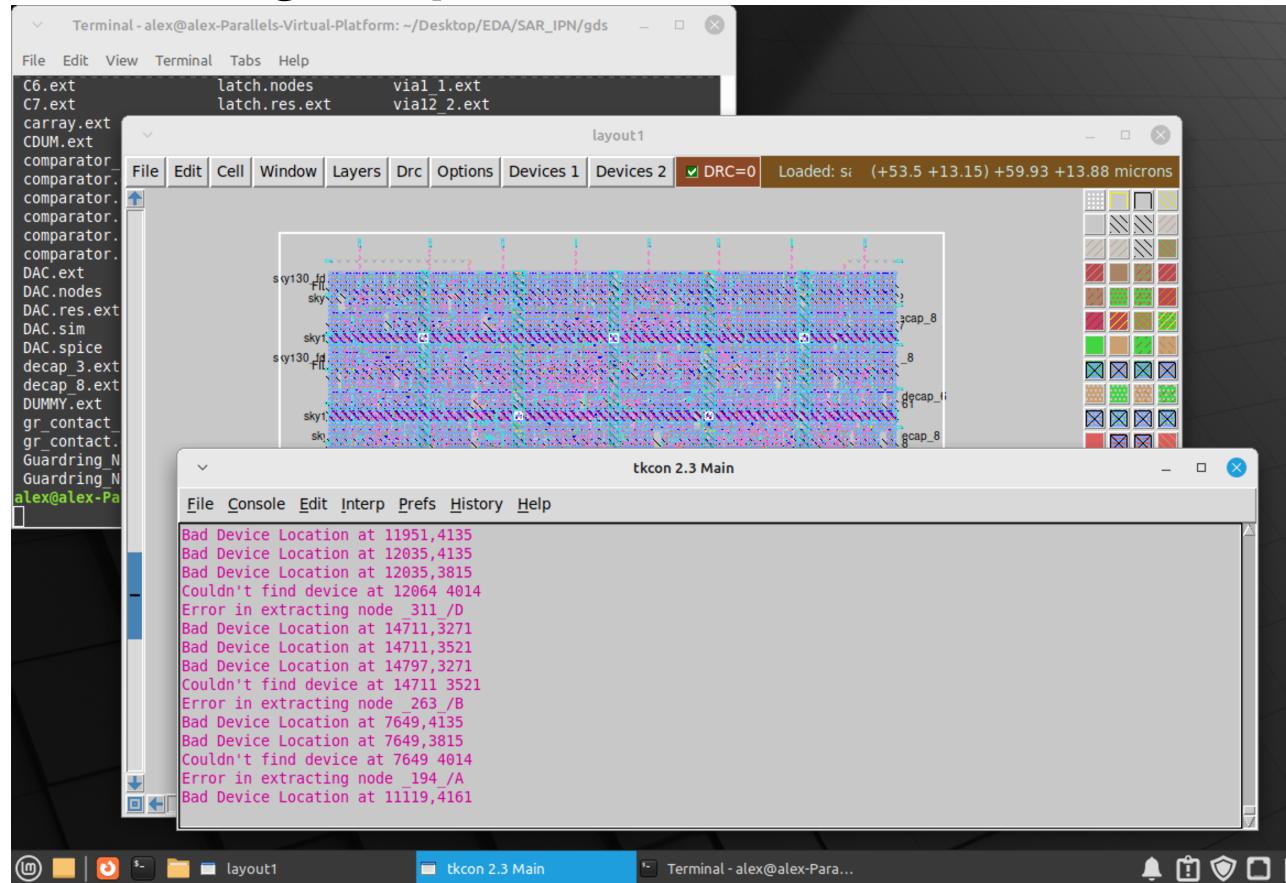
# Post layout Simulation

Mixed signal simulation, with full parasitic extraction (ss corner)



# Parasitic extraction for digital part

## Errors appear during the process



# Post layout Simulation

## All parts of the SAR-ADC parasitic extracted...



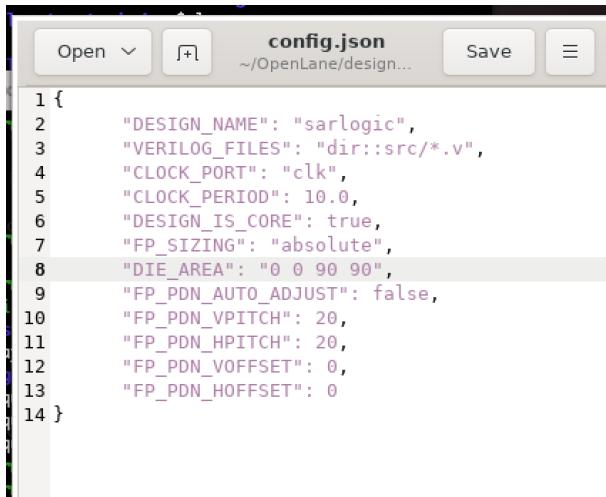
# **SAR-ADC**

## **Activity Report**

**Alejandro Juárez Lora, Sept 18, 2023**

# Obtaining the sar logic layout

## Configuration of OpenLane Scripts



A screenshot of a code editor window titled "config.json". The file path is shown as "~/OpenLane/design...". The editor has standard buttons for "Open", "Save", and a menu icon. The code content is as follows:

```
1 {
2     "DESIGN_NAME": "sarlogic",
3     "VERILOG_FILES": "dir::src/*.v",
4     "CLOCK_PORT": "clk",
5     "CLOCK_PERIOD": 10.0,
6     "DESIGN_IS_CORE": true,
7     "FP_SIZING": "absolute",
8     "DIE_AREA": "0 0 90 90",
9     "FP_PDN_AUTO_ADJUST": false,
10    "FP_PDN_VPITCH": 20,
11    "FP_PDN_HPITCH": 20,
12    "FP_PDN_VOFFSET": 0,
13    "FP_PDN_HOFFSET": 0
14 }
```

```
cd $OPENLANE_DIR
make mount
./flow.tcl -design sarlogic -init_design_config -add_to_designs
./flow.tcl -design sarlogic -tag prueba
```



A screenshot of a terminal window. The title bar shows the user's name and session information: "alejandrojuarezlora — alex@alex-Parallels-Virtual-Platform: ~/OpenLane/designs/sarlogic/src\$". The terminal displays the following commands and their output:

```
[alejandrojuarezlora — alex@alex-Parallels-Virtual-Platform: ~/OpenLane/designs/sarlogic/src]$ pwd
/home/alex/OpenLane/designs/sarlogic/src
[alejandrojuarezlora — alex@alex-Parallels-Virtual-Platform: ~/OpenLane/designs/sarlogic/src]$ ls
sarlogic.vf
[alejandrojuarezlora — alex@alex-Parallels-Virtual-Platform: ~/OpenLane/designs/sarlogic/src]$
```

# Obtaining the sar logic layout

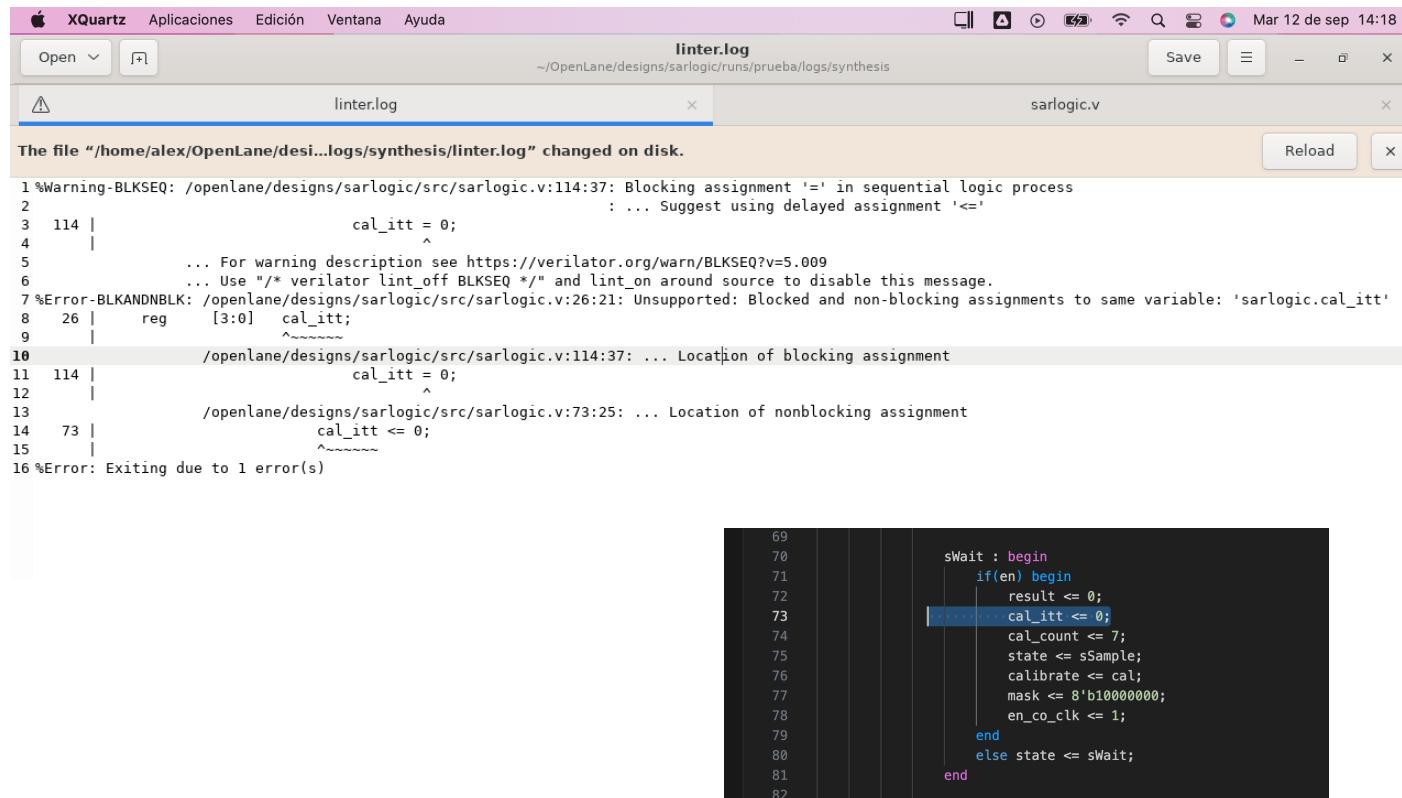
## Modifications to the Verilog file

XQuartz Aplicaciones Edición Ventana Ayuda

linter.log ~/OpenLane/designs/sarlogic/runs/prueba/logs/synthesis Mar 12 de sep 14:18

The file "/home/alex/OpenLane/desi...logs/synthesis/linter.log" changed on disk.

```
1 %Warning-BLKSEQ: /openlane/designs/sarlogic/src/sarlogic.v:114:37: Blocking assignment '=' in sequential logic process
2                                     : ... Suggest using delayed assignment '<='
3   114 |           cal_itt = 0;
4   |           ^
5   |           ... For warning description see https://verilator.org/warn/BLKSEQ?=5.009
6   |           ... Use /* verilator lint_off BLKSEQ */ and lint_on around source to disable this message.
7 %Error-BLKANDNBLK: /openlane/designs/sarlogic/src/sarlogic.v:26:21: Unsupported: Blocked and non-blocking assignments to same variable: 'sarlogic.cal_itt'
8   26 |   reg [3:0] cal_itt;
9   |
10  |           /openlane/designs/sarlogic/src/sarlogic.v:114:37: ... Location of blocking assignment
11 114 |           cal_itt = 0;
12  |
13  |           /openlane/designs/sarlogic/src/sarlogic.v:73:25: ... Location of nonblocking assignment
14  73 |           cal_itt <= 0;
15  |
16 %Error: Exiting due to 1 error(s)
```



```
69
70          sWait : begin
71              if(en) begin
72                  result <= 0;
73                  cal_itt <= 0;
74                  cal_count <= 7;
75                  state <= sSample;
76                  calibrate <= cal;
77                  mask <= 8'b10000000;
78                  en_co_clk <= 1;
79              end
80              else state <= sWait;
81          end
82      
```

module sarlogic( Untitled-1 •

```
1   module sarlogic(
2       input    clk,
3       input    rstn,
4       input    en,
5       input    comp,
6       input    cal,
7       output   valid,
8       output   reg [7:0] result,
9       output   sample,
10      output  [7:0] ctpl,
11      output  [7:0] ctln,
12      output  [4:0] trim,
13      output  [4:0] trimb,
14      output   clkc);
15
16      reg    calibrate;
17      reg    [2:0] state;
18      reg    [7:0] mask;
19      reg    [4:0] trim_mask;
20      /*reg   [7:0] result;*/
21      reg    [4:0] trim_val;
22      /*reg   sample;*/
23      //reg   co_clk;
24      reg    en_co_clk;
25      reg    [3:0] cal_count;
26      reg    [3:0] cal_itt;
27
28      parameter sInit=0, sWait=1, sSample=2, sConv=3, sDone=4, sCal=5;
29
30      /*initial begin
31         state <= sInit;
32         mask <= 0;
33         trim_mask <= 0;
34         result <= 0;
35         co_clk <= 0;
36         en_co_clk <= 0;
37         cal_itt <= 0;
38         cal_count <= 7;
39         trim_val <= 0;
40         calibrate <= 0;
41     end*/
42
43     /*always @(clk) begin
44         clkc <= (~clk & en_co_clk);
45     end*/
46     assign clkc = (~clk & en_co_clk);
```

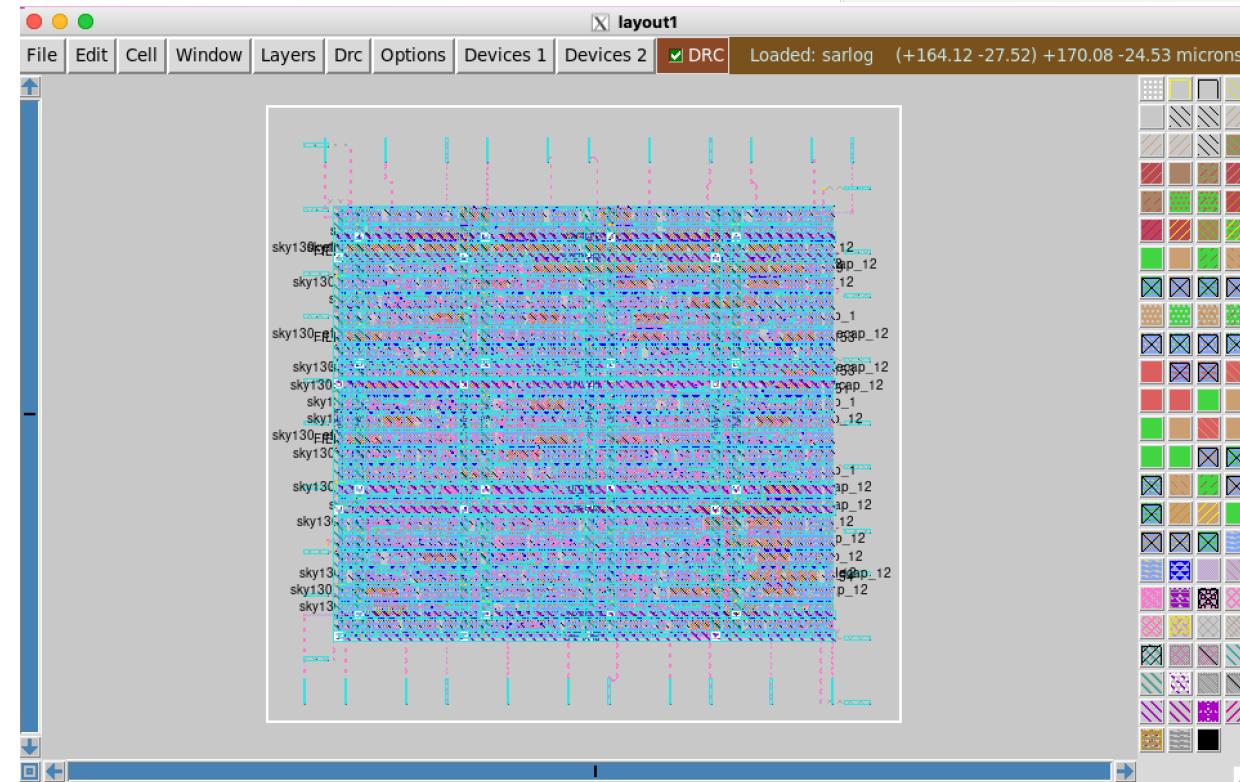
# Obtaining the sar logic layout

## Resulting Layout

```

2 61. Printing statistics.
3
4 === sarlogic ===
5
6 Number of wires: 188
7 Number of wire bits: 217
8 Number of public wires: 46
9 Number of public wire bits: 75
10 Number of memories: 0
11 Number of memory bits: 0
12 Number of processes: 0
13 Number of cells: 212
14   sky130_fd_sc_hd_a21bo_2 3
15   sky130_fd_sc_hd_a21o_2 16
16   sky130_fd_sc_hd_a21oi_2 2
17   sky130_fd_sc_hd_a31o_2 12
18   sky130_fd_sc_hd_a31oi_2 1
19   sky130_fd_sc_hd_a32o_2 2
20   sky130_fd_sc_hd_and2_2 18
21   sky130_fd_sc_hd_and2b_2 3
22   sky130_fd_sc_hd_and3_2 9
23   sky130_fd_sc_hd_and4b_2 2
24   sky130_fd_sc_hd_buf_1_2 36
25   sky130_fd_sc_hd_comb_1 1
26   sky130_fd_sc_hd_dfrtp_2 38
27   sky130_fd_sc_hd_dfrtp_2 4
28   sky130_fd_sc_hd_inv_2 16
29   sky130_fd_sc_hd_mux2_2 4
30   sky130_fd_sc_hd_nand2_2 5
31   sky130_fd_sc_hd_nand2b_2 1
32   sky130_fd_sc_hd_nor2_2 1
33   sky130_fd_sc_hd_o21a_2 3
34   sky130_fd_sc_hd_o21ai_2 3
35   sky130_fd_sc_hd_o221a_2 1
36   sky130_fd_sc_hd_o22a_2 3
37   sky130_fd_sc_hd_o22ai_2 1
38   sky130_fd_sc_hd_o311a_2 1
39   sky130_fd_sc_hd_or2_2 17
40   sky130_fd_sc_hd_or2b_2 3
41   sky130_fd_sc_hd_or3_2 1
42   sky130_fd_sc_hd_or3b_2 1
43   sky130_fd_sc_hd_xnor2_2 2
44   sky130_fd_sc_hd_xor2_2 2
45
46 Chip area for module `sarlogic': 2304.710400
47

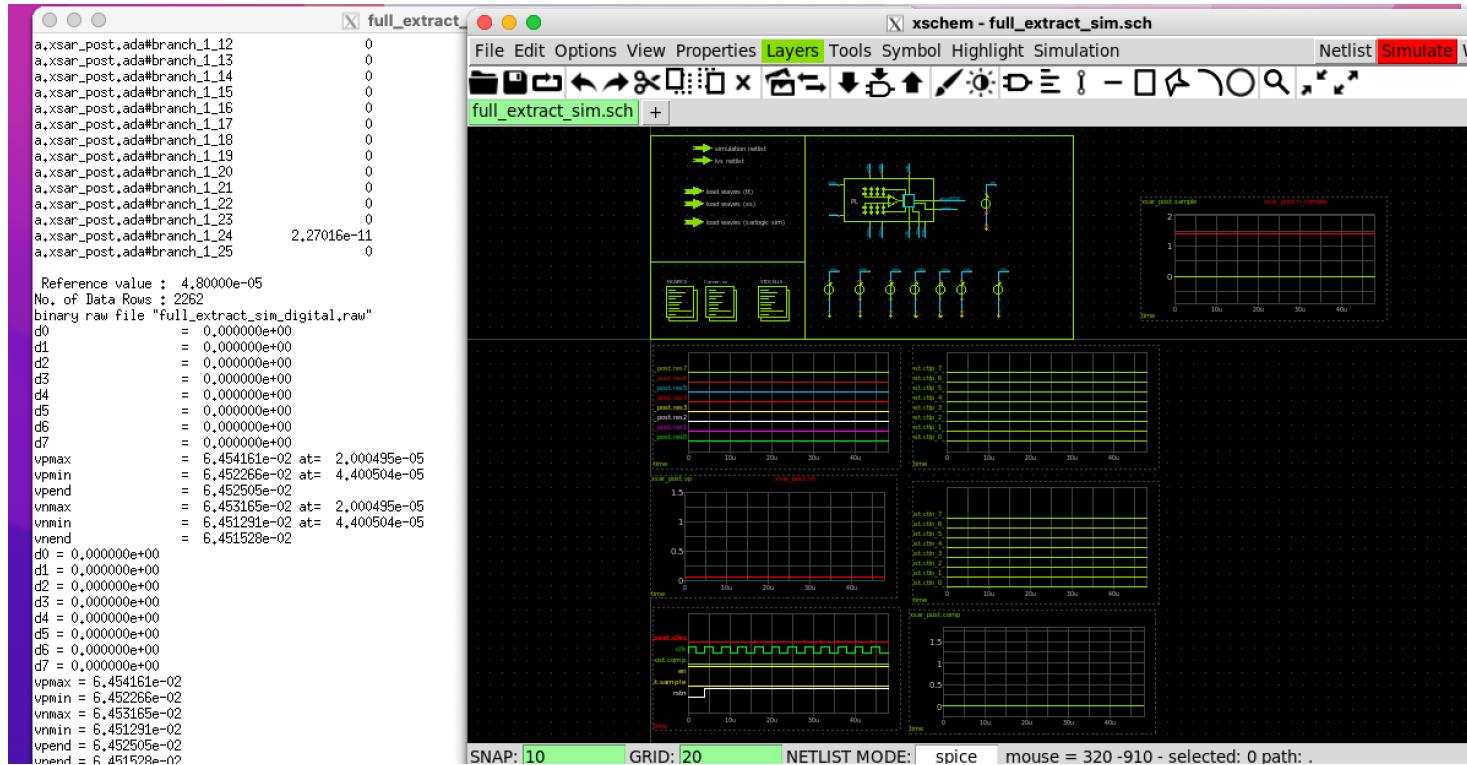
```



Typical Corner				
Group	Internal Power	Switching Power	Leakage Power	Total Power (Watts)
Sequential	2.47e-04	9.82e-05	4.47e-10	3.45e-04 35.8%
Combinational	2.61e-04	3.56e-04	5.45e-10	6.17e-04 64.2%
Macro	0.00e+00	0.00e+00	0.00e+00	0.00e+00 0.0%
Pad	0.00e+00	0.00e+00	0.00e+00	0.00e+00 0.0%
Total	5.08e-04	4.55e-04	9.92e-10	9.62e-04 100.0%
	52.8%	47.2%	0.0%	
				Ln 1, Col 1

# Post-layout simulation

## Results with simple spice extraction for the digital sarlogic



extract  
ext2spice -F

# Post-layout simulation

## Results Full parasitics for the digital sarlogic

The screenshot shows the sarlogic tool interface with the following components:

- Top Bar:** File, Edit, Cell, Window, Layers, Drc, Options, Devices 1, Devices 2, DRC (checked), Loaded: sarlogic Editing: sarlogic Tool: box Technology: sky130B.
- Left Panel:** Open dropdown, config.json (~/OpenLane/designs/sarlogic), and a code editor window displaying the configuration file content.
- Middle Panel:** A layout view titled "layout1" showing a dense grid of logic cells and interconnects. Labels like "VDD", "VSS", and "VPWB" are visible at the bottom.
- Right Panel:** A terminal window titled "1-synthesis.AREA\_0.stat.rpt" showing synthesis statistics.

**config.json Content:**

```
1 {
2   "DESIGN_NAME": "sarlogic",
3   "VERILOG_FILES": "dir::src/*.v",
4   "CLOCK_PORT": "clk",
5   "CLOCK_PERIOD": 0.1,
6   "PL_ROUTEABILITY_DRIVEN": 1,
7   "FP_SIZING": "absolute",
8   "DIE_AREA": "0 0 80 70",
9   "FP_IO_MODE": 0,
10  "FP_IO_MIN_DISTANCE": 1,
11  "FP_PIN_ORDER_CFG": "dir::pin.cfg",
12  "FP_IO_VLENGTH": 1,
13  "FP_IO_HLENGTH": 1,
14  "FP_IO_VTHICKNESS_MULT": 2,
15  "FP_IO_HTHICKNESS_MULT": 1,
16  "TOP_MARGIN_MULT": 1,
17  "BOTTOM_MARGIN_MULT": 1,
18  "LEFT_MARGIN_MULT": 1,
19  "RIGHT_MARGIN_MULT": 1,
20  "FP_IO_VLAYER": "met3"
21 }
22 }
```

**1-synthesis.AREA\_0.stat.rpt Output:**

```
1 61. Printing statistics.
2
3 === sarlogic ===
4
5   Number of wires: 181
6   Number of wire bits: 210
7   Number of public wires: 44
8   Number of public wire bits: 73
9   Number of memories: 0
10  Number of memory bits: 0
11  Number of processes: 0
12  Number of cells: 205
13    sky130_fd_sc_hd_a21bo_2 1
14    sky130_fd_sc_hd_a21o_2 7
15    sky130_fd_sc_hd_a21oi_2 10
16    sky130_fd_sc_hd_a221o_2 1
17    sky130_fd_sc_hd_a22o_2 13
18    sky130_fd_sc_hd_a22o_4 1
19    sky130_fd_sc_hd_a31o_2 1
20    sky130_fd_sc_hd_a31o_4 1
21    sky130_fd_sc_hd_a32o_2 1
22    sky130_fd_sc_hd_and2_2 7
23    sky130_fd_sc_hd_and2b_2 3
24    sky130_fd_sc_hd_and3_2 1
25    sky130_fd_sc_hd_and3b_2 2
26    sky130_fd_sc_hd_and4_4 1
27    sky130_fd_sc_hd_and4bb_2 1
28    sky130_fd_sc_hd_buf_1 16
29    sky130_fd_sc_hd_buf_2 9
30    sky130_fd_sc_hd_buf_4 2
31    sky130_fd_sc_hd_buf_6 3
32    sky130_fd_sc_hd_dfrtp_2 36
33    sky130_fd_sc_hd_dfstp_2 3
34    sky130_fd_sc_hd_inv_2 17
35    sky130_fd_sc_hd_mux2_2 5
36    sky130_fd_sc_hd_nand2_2 6
37    sky130_fd_sc_hd_nand2b_4 1
38    sky130_fd_sc_hd_nand3b_4 1
39    sky130_fd_sc_hd_nand4b_2 1
40    sky130_fd_sc_hd_nor2_2 18
41    sky130_fd_sc_hd_nor2_4 1
42    sky130_fd_sc_hd_nor3_4 1
43    sky130_fd_sc_hd_nor4b_2 1
44    sky130_fd_sc_hd_o21a_2 5
```

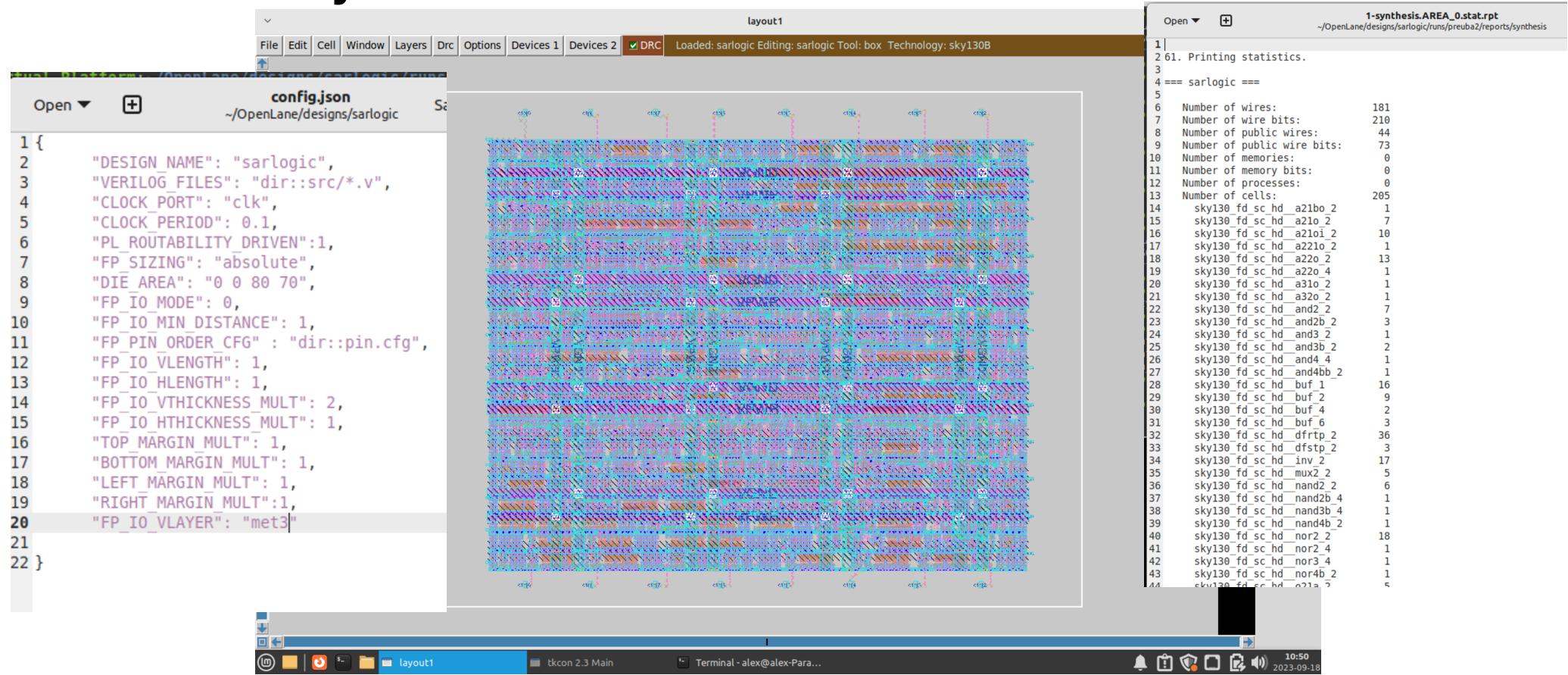
# **SAR-ADC**

## **Activity Report**

**Alejandro Juárez Lora, Sept 22, 2023**

# Post-layout simulation

## Obtained layout

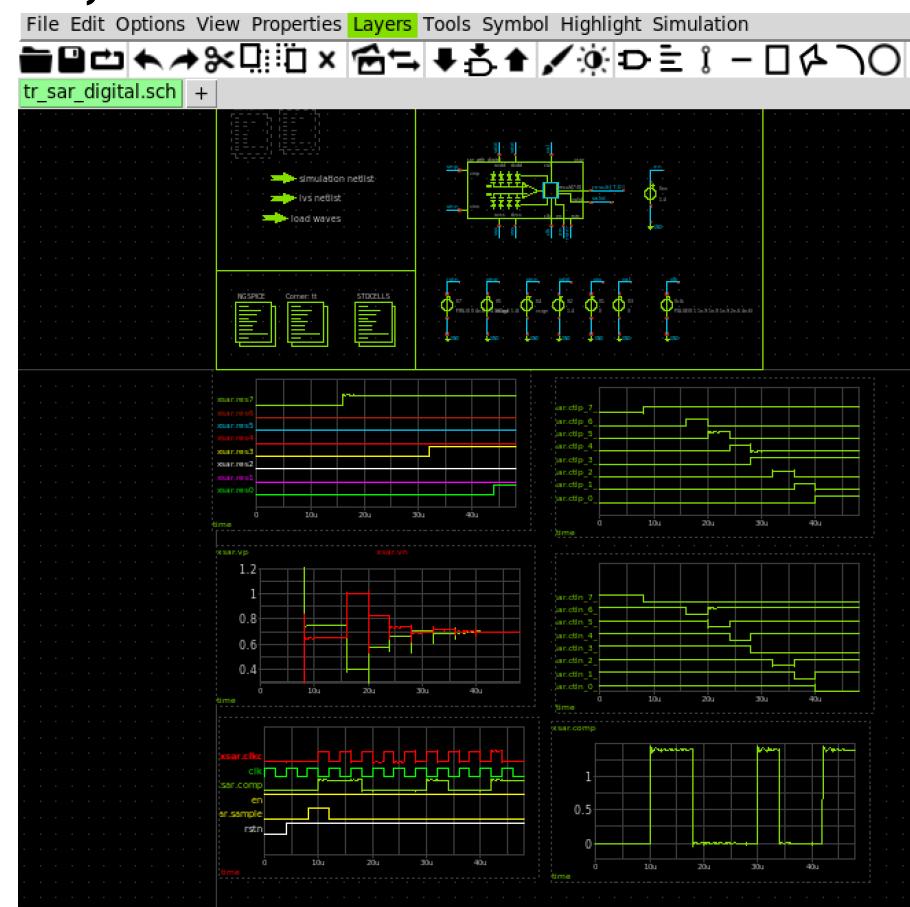


# Post-layout simulation

Only sar\_logic is layout extracted, the rest is schematic

```
sar_logic.spice
Home ~/Desktop/EDA/SAR_IPN/xschem/sar

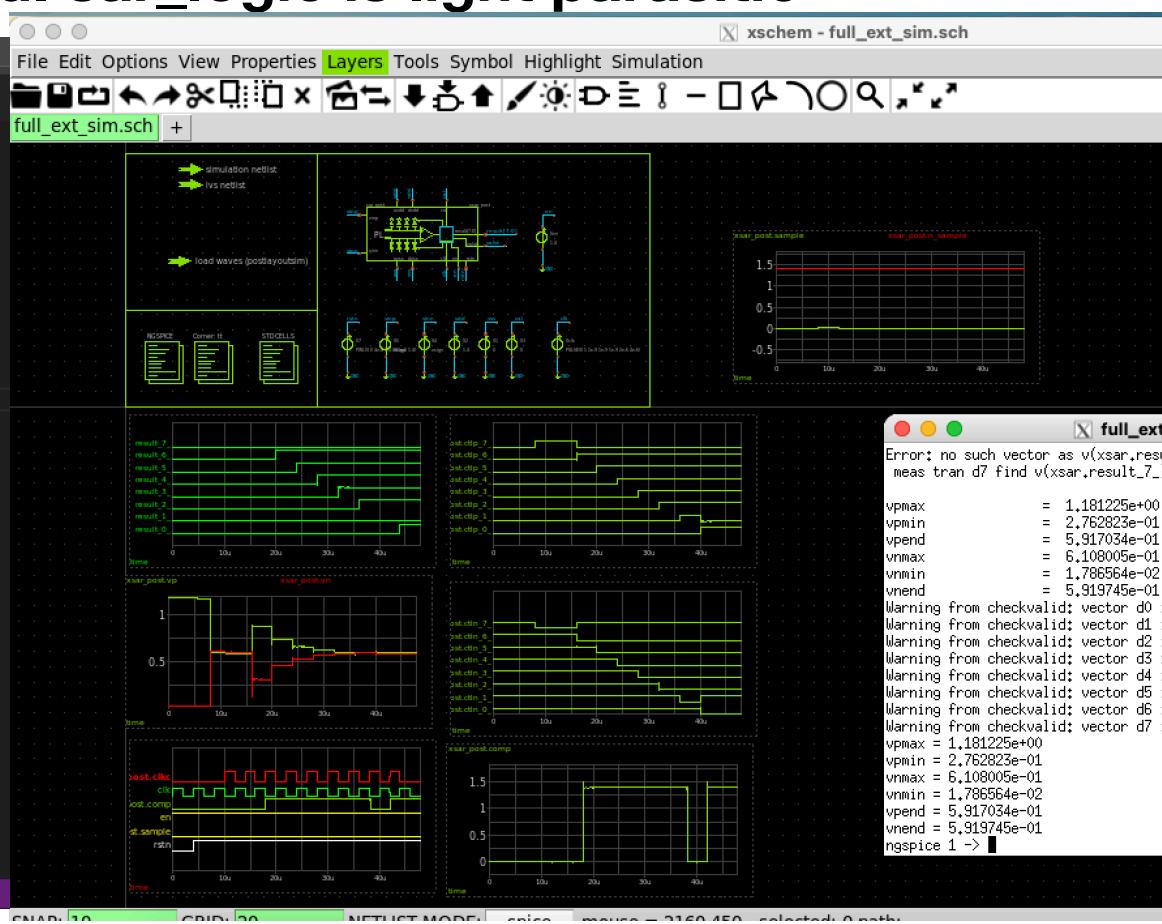
1 * SPICE3 file created from sarlogic.ext - technology: sky130B
2
3 .subckt sar_logic VGND VPWR cal clk clkc comp ctln[0] ctln[1] ctln[2] ctln[3] ctln[4]
4 + ctln[5] ctln[6] ctln[7] ctpl[0] ctpl[1] ctpl[2] ctpl[3] ctpl[4] ctpl[5] ctpl[6]
5 + ctpl[7] en result[0] result[1] result[2] result[3] result[4] result[5] result[6]
6 + result[7] rstn sample trim[0] trim[1] trim[2] trim[3] trim[4] trimb[0] trimb[1]
7 + trimb[2] trimb[3] trimb[4] valid
8 C0 _078_ net43 2.58f
9 C1 net15 VPWR 2.08f
10 C2 _092_ VPWR 3.61f
11 C3 net40 VPWR 4.73f
12 C4 net14 net43 2.29f
13 C5 _048_ VPWR 2.55f
14 C6 net45 VPWR 4.53f
15 C7 _065_ VPWR 3.3f
16 C8 net16 VPWR 2.18f
17 C9 VPWR cal_ittr[0] 2.46f
18 C10 _051_ VPWR 2.08f
19 C11 net3 VPWR 2.8f
20 C12 _053_ VPWR 2.55f
21 C13 cal_count[3] VPWR 2.99f
22 C14 _042_ VPWR 6.5f
23 C15 en_co_clk VPWR 6.66f
24 C16 _110_ VPWR 3.18f
25 C17 net4 VPWR 4.23f
26 C18 trim mask[0] VPWR 3.23f
27 C19 net47 VPWR 2.15f
28 C20 net44 VPWR 3.87f
29 C21 mask[1] VPWR 2.43f
30 C22 net2 VPWR 2.05f
31 C23 _123_ VPWR 3.25f
32 C24 net34 net37 2.05f
33 C25 net30 VPWR 4.34f
34 C26 net40 VPWR 2.22f
35 C27 _078_ VPWR 4.55f
36 C28 _062_ VPWR 3.68f
37 C29 net28 VPWR 2.08f
38 C30 _074_ VPWR 3.7f
39 C31 _063_ VPWR 2.18f
```



# Post-layout simulation

All blocks are layout extracted. sar\_logic is light parasitic

```
sarlogic.spice  ⊞ sar_logic_light.spice ×
Users > alejandrojuarezlora > EDA > SAR_IPN > full_ext_sim > sar > sarlogic > ⊞ sar_logic_light.spice
1  * SPICE3 file created from sarlogic.ext - technology: sky130B
2
3 .subckt sar_logic VGN0 VPWR cal clk clkc comp ctn[0] ctn[1] ctn[2] ctn[3] ctn[4]
4 + ctn[5] ctn[6] ctn[7] ctlp[0] ctlp[1] ctlp[2] ctlp[3] ctlp[4] ctlp[5] ctlp[6]
5 + ctlp[7] en result[0] result[1] result[2] result[3] result[4] result[5] result[6]
6 + result[7] rstn sample trim[0] trim[1] trim[2] trim[3] trim[4] trimb[0] trimb[1]
7 + trimb[2] trimb[3] trimb[4] valid
8 C0 VPWR clknet_0_clk 3.19f
9 C1 VPWR _110_ 3.18f
10 C2 VPWR net47 2.15f
11 C3 VPWR net44 3.87f
12 C4 VPWR clknet_2_2_leaf_clk 4.34f
13 C5 VPWR mask\1\ 2.43f
14 C6 VPWR cal_it\0\ 2.46f
15 C7 VPWR net26 2.42f
16 C8 VPWR net2 2.05f
17 C9 VPWR _123_ 3.25f
18 C10 VPWR clknet_2_3_leaf_clk 3.33f
19 C11 VPWR clknet_2_0_leaf_clk 7.25f
20 C12 VPWR _078_ 4.55f
21 C13 VPWR net28 2.08f
22 C14 VPWR _074_ 3.7f
23 C15 VPWR _092_ 3.61f
24 C16 VPWR net46 4.73f
25 C17 VPWR calibrate 4.54f
26 C18 net43 net14 2.29f
27 C19 VPWR net45 4.53f
28 C20 VPWR _065_ 3.3f
29 C21 VPWR _051_ 2.08f
30 C22 VPWR _053_ 2.55f
31 C23 VPWR trim mask\0\1 3.23f
```



# Post-layout simulation

**All blocks are layout extracted. sar\_logic is full parasitic**

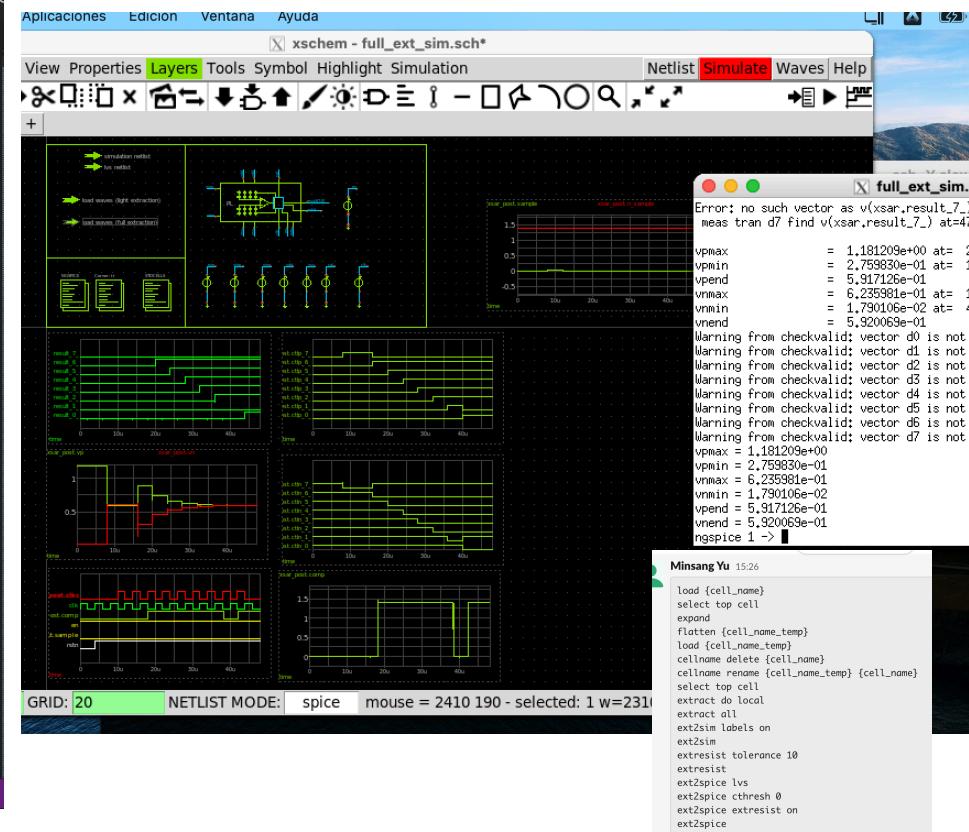
← →

Search

Generate

File: sar\_logic\_full.spice

```
s > alejandrojuarezlora > EDA > SAR_IPN > full_ext_sim > sar > sarlogic > sar_logic_full.spice
1 * SPICE3 file created from sarlogic.ext - technology: sky130B
2
3
4 .subckt sar_logic VGND VPWR cal clk clkc comp ctln[0] ctln[1] ctln[2] ctln[3] ctln[4]
5 + ctln[5] ctln[6] ctln[7] ctlp[0] ctlp[1] ctlp[2] ctlp[3] ctlp[4] ctlp[5] ctlp[6]
6 + ctlp[7] en result[0] result[1] result[2] result[3] result[4] result[5] result[6]
7 + result[7] rstin sample trim[0] trim[1] trim[2] trim[3] trim[4] trimb[0] trimb[1]
8 + trimb[2] trimb[3] trimb[4] valid
9 X0 clknet_0_clk a_8022_7119# VPWR.t1605 VPWR.t1604 sky130_fd_pr_pfet_01v8_hvt ad=0.14 pd=1.28 as=0.138 ps=1.27 w=
10 X1 VGND.t343 clknet_0_clk a_2857_7637# VGND.t342 sky130_fd_pr_nfet_01v8 ad=0.0588 pd=0.7 as=0.0588 ps=0.7 w=0.42
11 X2 a_745_10933# a_579_10933# VPWR.t1336 VPWR.t1335 sky130_fd_pr_pfet_01v8_hvt ad=0.166 pd=1.8 as=0.0864 ps=0.91 w=
12 X3 VGND.t1586 VPWR.t3333 VGND.t1585 VGND.t1584 sky130_fd_pr_nfet_01v8 ad=0.143 pd=1.62 as=0 ps=0 w=0.55 l=4.73
13 X4 a_7710_9839# a_6633_9845# a_7548_10217# VPWR.t2809 sky130_fd_pr_pfet_01v8_hvt ad=0.0567 pd=0.69 as=0.0588 ps=0
14 X5 trimb[4].t3 a_15023_8751# VPWR.t2716 VPWR.t2715 sky130_fd_pr_pfet_01v8_hvt ad=0.14 pd=1.28 as=0.14 ps=1.28 w=1
15 X6 VPWR.t2033 a_4677_7882# net15 VPWR.t2032 sky130_fd_pr_pfet_01v8_hvt ad=0.115 pd=1.08 as=0.205 ps=2.1 w=0.79 l=
16 X7 a_14172_1513# a_13257_1141# a_13825_1109# VGND.t2773 sky130_fd_pr_nfet_01v8 ad=0.0711 pd=0.755 as=0.0999 ps=0
17 X8 VGND.t2375 _066_ a_11045_5807# VGND.t2374 sky130_fd_pr_nfet_01v8 ad=0.101 pd=0.96 as=0.114 ps=1 w=0.65 l=0.15
18 X9 a_12612_8725# a_12436_9129# a_12756_9117# VGND.t462 sky130_fd_pr_nfet_01v8 ad=0.109 pd=1.36 as=0.0441 ps=0.63
19 X10 a_11856_2589# _026_ VGND.t2438 VGND.t2437 sky130_fd_pr_nfet_01v8 ad=0.066 pd=0.745 as=0.221 ps=1.89 w=0.42 l=
20 X11 a_10329_1921# a_10111_1679# VGND.t2743 VGND.t2742 sky130_fd_pr_nfet_01v8 ad=0.0999 pd=0.985 as=0.135 ps=1.15
21 X12 VPWR.t1029 clknet_2_2_leaf_clk a_9595_1679# VPWR.t1028 sky130_fd_pr_pfet_01v8_hvt ad=0.0864 pd=0.91 as=0.166
22 X13 _096_ _095_ a_4725_5487# VPWR.t1742 sky130_fd_pr_pfet_01v8_hvt ad=0.26 pd=2.52 as=0.105 ps=1.21 w=1 l=0.15
23 X14 _011_ _086_ a_1137_11721# VPWR.t1030 sky130_fd_pr_pfet_01v8_hvt ad=0.26 pd=2.52 as=0.105 ps=1.21 w=1 l=0.15
24 X15 VGND.t601 _104_ a_11321_3855# VGND.t600 sky130_fd_pr_nfet_01v8 ad=0.101 pd=0.96 as=0.114 ps=1 w=0.65 l=0.15
25 X16 VPWR.t2419 net2 a_14807_8359# VPWR.t2418 sky130_fd_pr_pfet_01v8_hvt ad=0.118 pd=1.4 as=0.0567 ps=0.69 w=0.42
26 X17 a_5340_6031# a_4425_6031# a_4993_6273# VGND.t3088 sky130_fd_pr_nfet_01v8 ad=0.0711 pd=0.755 as=0.0999 ps=0.98
27 X18 VGND.t2864 a_3339_2767# net45 VGND.t2863 sky130_fd_pr_nfet_01v8 ad=0.172 pd=1.83 as=0.0878 ps=0.92 w=0.65 l=0
28 X19 a_9195_10357# net47 VPWR.t1710 VPWR.t1709 sky130_fd_pr_pfet_01v8_hvt ad=0.0567 pd=0.69 as=0.0819 ps=0.81 w=0.
29 X20 VGND.t2136 mask\{3\} a_2368_9955# VGND.t2135 sky130_fd_pr_nfet_01v8 ad=0.1 pd=0.985 as=0.0567 ps=0.69 w=0.42
30 X21 VGND.t2080 clknet_2_1_leaf_clk.t32 a_2787_9845# VGND.t2079 sky130_fd_pr_nfet_01v8 ad=0.0567 pd=0.69 as=0.109
31 X22 VGND.t3197 082 007 VGND.t3196 sky130_fd_pr_nfet_01v8 ad=0.169 nd=1.82 as=0.0878 ns=0.92 w=0.65 l=0.15
```



# LVS

## latch lvs successful

```
select top cell
expand
flatten latch_temp
load latch_temp sar
cellname rename latch_temp latch
select top cell
extract do local
extract
ext2sim labels on
ext2sim
ext2spice lvs
ext2spice
```

```
Open ▾ + latch_lay.spice Home ~/Desktop/EDA/SAR_IPN/my_lvs/latch
1 * NGSPICE file created from latch_temp.ext - technology: sky130B
2
3 .subckt latch| vdd vss Qn S R Q
4 X0 Q Qn vdd vdd sky130_fd_pr_pfet_01v8_lvt ad=0.29 pd=2.58 as=0.29 ps=2.58 w=1 l=0.4
5 X1 Qn a_329_215# vss vss sky130_fd_pr_nfet_01v8_lvt ad=0.29 pd=2.58 as=0.29 ps=2.58 w=1 l=0.4
6 X2 vss Q Qn vss vss sky130_fd_pr_nfet_01v8_lvt ad=0.29 pd=2.58 as=0.29 ps=2.58 w=1 l=0.4
7 X3 vss R a_1663_189# vss sky130_fd_pr_nfet_01v8_lvt ad=0.29 pd=2.58 as=0.29 ps=2.58 w=1 l=0.4
8 X4 a_329_215# S vss vss sky130_fd_pr_nfet_01v8_lvt ad=0.29 pd=2.58 as=0.29 ps=2.58 w=1 l=0.4
9 X5 Q Qn vss vss sky130_fd_pr_nfet_01v8_lvt ad=0.29 pd=2.58 as=0.29 ps=2.58 w=1 l=0.4
10 X6 vdd Q Qn vdd sky130_fd_pr_pfet_01v8_lvt ad=0.29 pd=2.58 as=0.29 ps=2.58 w=1 l=0.4
11 X7 vdd R a_1663_189# vdd sky130_fd_pr_pfet_01v8_lvt ad=0.29 pd=2.58 as=0.29 ps=2.58 w=1 l=0.4
12 X8 vss a_1663_189# Q vss sky130_fd_pr_nfet_01v8_lvt ad=0.29 pd=2.58 as=0.29 ps=2.58 w=1 l=0.4
13 X9 a_329_215# S vdd vdd sky130_fd_pr_pfet_01v8_lvt ad=0.29 pd=2.58 as=0.29 ps=2.58 w=1 l=0.4
14 .ends
15
```

```
Terminal - alex@alex-Parallels-Virtual-Platform: ~/Desktop/EDA/
File Edit View Terminal Tabs Help
No property topography found for device sky130_fd_pr_pfet_01v8_lvt
Model sky130_fd_pr_pfet_01v8_lvt pin 1 == 3
No property area found for device sky130_fd_pr_pfet_01v8_lvt
No property perim found for device sky130_fd_pr_pfet_01v8_lvt
No property topography found for device sky130_fd_pr_pfet_01v8_lvt
Comparison output logged to file latch.out
Logging to file "latch.out" enabled
Circuit sky130_fd_pr_nfet_01v8_lvt contains no devices.
Circuit sky130_fd_pr_pfet_01v8_lvt contains no devices.

Contents of circuit 1: Circuit: 'latch'
Circuit latch contains 10 device instances.
  Class: sky130_fd_pr_nfet_01v8_lvt instances: 6
  Class: sky130_fd_pr_pfet_01v8_lvt instances: 4
Circuit contains 8 nets.
Contents of circuit 2: Circuit: 'latch'
Circuit latch contains 10 device instances.
  Class: sky130_fd_pr_nfet_01v8_lvt instances: 6
  Class: sky130_fd_pr_pfet_01v8_lvt instances: 4
Circuit contains 8 nets.

Circuit 1 contains 10 devices, Circuit 2 contains 10 devices.
Circuit 1 contains 8 nets, Circuit 2 contains 8 nets.

Final result:
Circuits match uniquely.
.
Logging to file "latch.out" disabled
LVS Done.
alex@alex-Parallels-Virtual-Platform:~/Desktop/EDA/SAR_IPN/my_lvs/latch$
```

```
Open ▾ + latch_sch.spice Home ~/Desktop/EDA/SAR_IPN/my_lvs/latch
1 ** sch_path: /media/psf/Home/EDA/SAR_IPN/xschem/sar/latch/latch.sch
2 .subckt latch S R vss vdd Q Qn
3 .ipin S
4 .ipin R
5 .ipin vss
6 .ipin vdd
7 .opin Q
8 .opin Qn
9 X1 vdd Qn Q vss inv_lvt
10 X2 vdd Q Qn vss inv_lvt
11 X3 vdd R net2 vss inv_lvt
12 X4 vdd S net1 vss inv_lvt
13 XM4 Q net2 vss vss sky130_fd_pr_nfet_01v8_lvt L=0.4 W=1 nf=1 ad='int((nf+1)/2) * W/nf * 0.29' as='int((nf+2)/2) * W/nf * 0.29'
14 + pd='2*int((nf+1)/2) * (W/nf + 0.29)' ps='2*int((nf+2)/2) * (W/nf + 0.29)' nrd='0.29 / W' nrs='0.29 / W'
15 + sa=0 sb=0 sd=0 mult=1 m=1
16 XM1 Qn net1 vss vss sky130_fd_pr_nfet_01v8_lvt L=0.4 W=1 nf=1 ad='int((nf+1)/2) * W/nf * 0.29' as='int((nf+2)/2) * W/nf * 0.29'
17 + pd='2*int((nf+1)/2) * (W/nf + 0.29)' ps='2*int((nf+2)/2) * (W/nf + 0.29)' nrd='0.29 / W' nrs='0.29 / W'
18 + sa=0 sb=0 sd=0 mult=1 m=1
19 .ends
20
```

# LVS

## comparator lvs unsuccessful: capacitors does not appear on

Open ▾ +

comparator\_sch.spice  
Home ~/Desktop/EDA/SAR\_IPN/my\_lvs/comparator

```

1 ** sch_path: /media/psf/Home/EDA/SAR_IPN/xschem/sar/comparator/comparator.sch
2 .subckt comparator vp clk vdd vss outn outn trim_4 trim_3 trim_2 trim_1 trim_0 trimb_4_
3 + trimb_3 trimb_2 trimb_1 trimb_0
4 *.PININFO vn:I vp:I clk:I vdd:B vss:B outp:0 outn:0 trim[4:0]:I trimb[4:0]:I
5 x2 in trim_4 trim_3 trim_2 trim_1 trim_0 vss trim
6 x3 ip trimb_4 trimb_3 trimb_2 trimb_1 trimb_0 vss trim
7 XM1 in clk vdd vdd sky130_fd_pr_pfet_01v8 L=0.3 W=1 nf=1 m=1
8 XM2 outn clk vdd vdd sky130_fd_pr_pfet_01v8 L=0.3 W=1 nf=1 m=1
9 XM5 outn vdd vdd sky130_fd_pr_pfet_01v8 L=0.3 W=1 nf=1 m=1
10 XML4 outp outn vdd vdd sky130_fd_pr_pfet_01v8 L=0.3 W=1 nf=1 m=1
11 XM3 outp clk vdd vdd sky130_fd_pr_pfet_01v8 L=0.3 W=1 nf=1 m=1
12 XM4 ip clk vdd vdd sky130_fd_pr_pfet_01v8 L=0.3 W=1 nf=1 m=1
13 XML2 outp outn ip vss sky130_fd_pr_nfet_01v8 L=0.3 W=1 nf=1 m=1
14 XM11 outn outp in vss sky130_fd_pr_nfet_01v8 L=0.3 W=1 nf=1 m=1
15 XMInn in vn diff vss sky130_fd_pr_nfet_01v8 L=0.3 W=1 nf=1 m=1
16 XMInp ip vp diff vss sky130_fd_pr_nfet_01v8 L=0.3 W=1 nf=1 m=1
17 XMdiff diff clk vss vss sky130_fd_pr_nfet_01v8 L=0.3 W=1 nf=1 m=2
18 .ends
19
20 * expanding symbol: sar/comparator/trim.sym # of pins=3
21 ** sym_path: /media/psf/Home/EDA/SAR_IPN/xschem/sar/comparator/trim.sym
22 ** sch_path: /media/psf/Home/EDA/SAR_IPN/xschem/sar/comparator/trim.sch
23 .subckt trim drain d_4 d_3 d_2 d_1 d_0 vss
24 *.PININFO vss:B d[4:0]:I drain:0
25 x4_7_ drain n4 trimcap
26 x4_6_ drain n4 trimcap
27 x4_5_ drain n4 trimcap
28 x4_4_ drain n4 trimcap
29 x4_3_ drain n4 trimcap
30 x4_2_ drain n4 trimcap
31 x4_1_ drain n4 trimcap
32 x4_0_ drain n4 trimcap
33 x3_3_ drain n3 trimcap
34 x3_2_ drain n3 trimcap
35 x3_1_ drain n3 trimcap
36 x3_0_ drain n3 trimcap
37 x2_1_ drain n2 trimcap
38 x2_0_ drain n2 trimcap
39 x1 drain n1 trimcap
40 x0 drain n0 trimcap
41 XM4_7_ n4 d_4 vss vss sky130_fd_pr_nfet_01v8 lvt L=0.3 W=1 nf=1 m=1

```

Plain T

select top cell  
expand  
extract do local  
labels on

> lvs

Open ▾ +

comparator\_lay.spice  
Home ~/Desktop/EDA/SAR\_IPN/my\_lvs/comparator

```

1 /* NGSPICE file created from comparator.ext - technology: sky130B
2
3 .subckt M1 1 a_30_n109# a_n88_n109# a_n33_n197# VSUBS
4 X0 a_30_n109# a_n33_n197# a_n88_n109# VSUBS sky130_fd_pr_nfet_01v8_lvt ad=0.29 pd=2.58 as=0.29 ps=2.58
5 .ends
6
7 .subckt trim_sw d_0 d_1 d_2 d_3 d_4 m1_1462_409# m1_1771_409# m1_136_409# m1_799_409#
8 + m1_1226_409# vss
9 XM1_1_14 vss m1_799_409# d_2 vss M1_1
10 XM1_1_15 m1_799_409# vss d_2 vss M1_1
11 XM1_1_0 vss m1_1226_409# d_0 vss M1_1
12 XM1_1_1 vss m1_1771_409# d_4 vss M1_1
13 XM1_1_2 m1_1771_409# vss d_4 vss M1_1
14 XM1_1_3 vss m1_1771_409# d_4 vss M1_1
15 XM1_1_4 m1_1771_409# vss d_4 vss M1_1
16 XM1_1_5 m1_1771_409# vss d_4 vss M1_1
17 XM1_1_6 vss m1_1771_409# d_4 vss M1_1
18 XM1_1_7 vss m1_1771_409# d_4 vss M1_1
19 XM1_1_8 m1_1771_409# vss d_4 vss M1_1
20 XM1_1_9 m1_1462_409# vss d_1 vss M1_1
21 XM1_1_10 m1_136_409# vss d_3 vss M1_1
22 XM1_1_11 vss m1_136_409# d_3 vss M1_1
23 XM1_1_12 m1_136_409# vss d_3 vss M1_1
24 XM1_1_13 vss m1_136_409# d_3 vss M1_1
25 .ends
26
27 .subckt trim n3 n4 n2 n1 n0 trim_sw_0/d_4 trim_sw_0/d_3 trim_sw_0/d_2 trim_sw_0/d_1
28 + trim_sw_0/d_0 VSUBS drain
29 Xtrim_sw_0 trim_sw_0/d_0 trim_sw_0/d_1 trim_sw_0/d_2 trim_sw_0/d_3 trim_sw_0/d_4 n1
30 + n4 n3 n2 n0 VSUBS trim_sw
31 .ends
32
33 .subckt Md iff a_n33_51# a_30_n171# a_n88_n171# VSUBS
34 X0 a_30_n171# a_n33_51# a_n88_n171# VSUBS sky130_fd_pr_nfet_01v8 ad=0.29 pd=2.58 as=0.29 ps=2.58 w=1
35 .ends
36
37 .subckt M3 a_n88_n176# a_n33_55# w_n124_n238# a_30_n176#
38 X0 a_30_n176# a_n33_55# a_n88_n176# w_n124_n238# sky130_fd_pr_pfet_01v8 ad=0.29 pd=2.58 as=0.29 ps=2.58
39 .ends
40
41 .subckt Ml1 a_n33_51# a_30_n171# a_n88_n171# VSUBS

```

Circuit contains 51 nets.  
Contents of circuit 2: Circuit: 'comparator'  
Circuit comparator contains 53 device instances.  
Class: sky130\_fd\_pr\_nfet\_01v8 instances: 5  
Class: c instances: 32  
Class: sky130\_fd\_pr\_nfet\_01v8\_lvt instances: 10  
Class: sky130\_fd\_pr\_pfet\_01v8 instances: 6  
Circuit contains 30 nets.

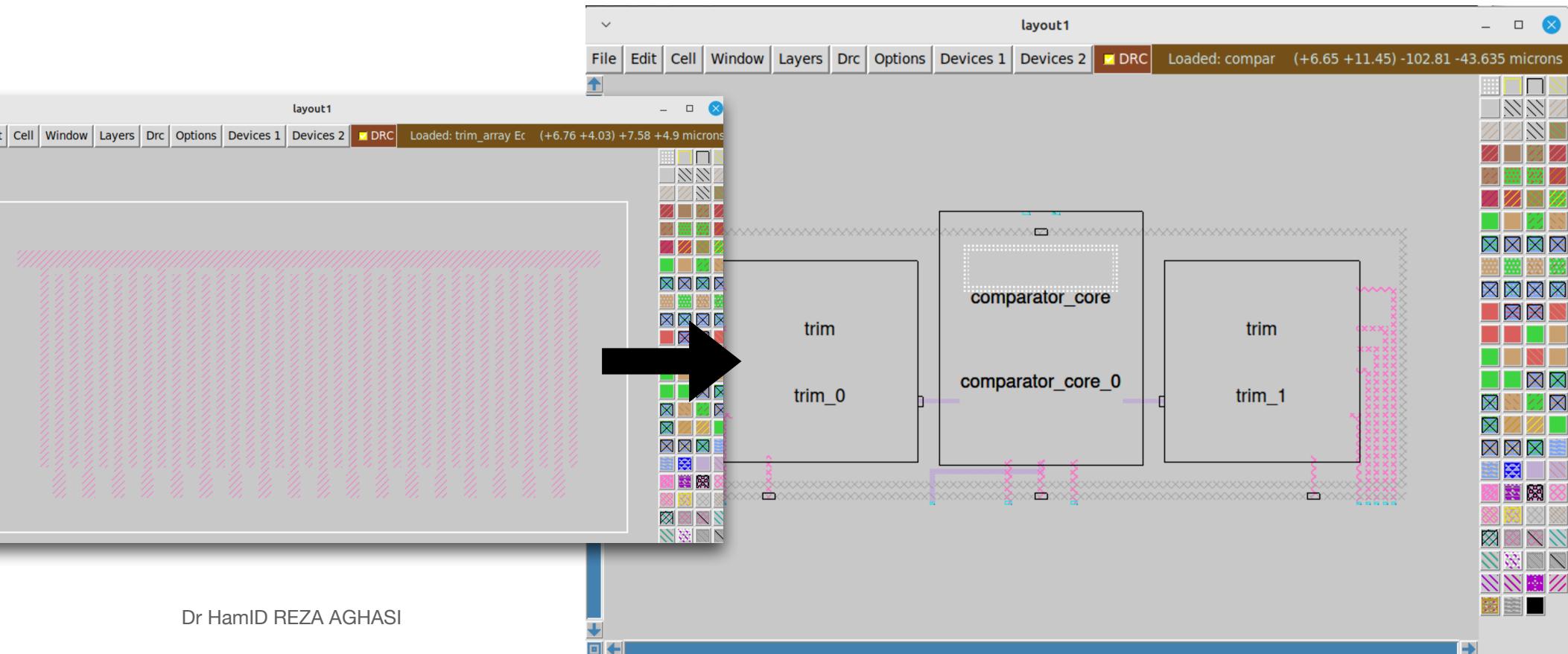
Circuit 1 contains 21 devices, Circuit 2 contains 53 devices. \*\*\* MISMATCH \*\*\*  
Circuit 1 contains 31 nets, Circuit 2 contains 30 nets. \*\*\* MISMATCH \*\*\*

Final result:  
Netlists do not match.  
Logging to file "comparator.out" disabled  
LVS Done.

alex@alex-Parallels-Virtual-Platform:~/Desktop/EDA/SAR\_IPN/my\_lvs/comparator\$

# LVS

**comparator lvs unsuccessful: capacitors are metal layers 270A course**

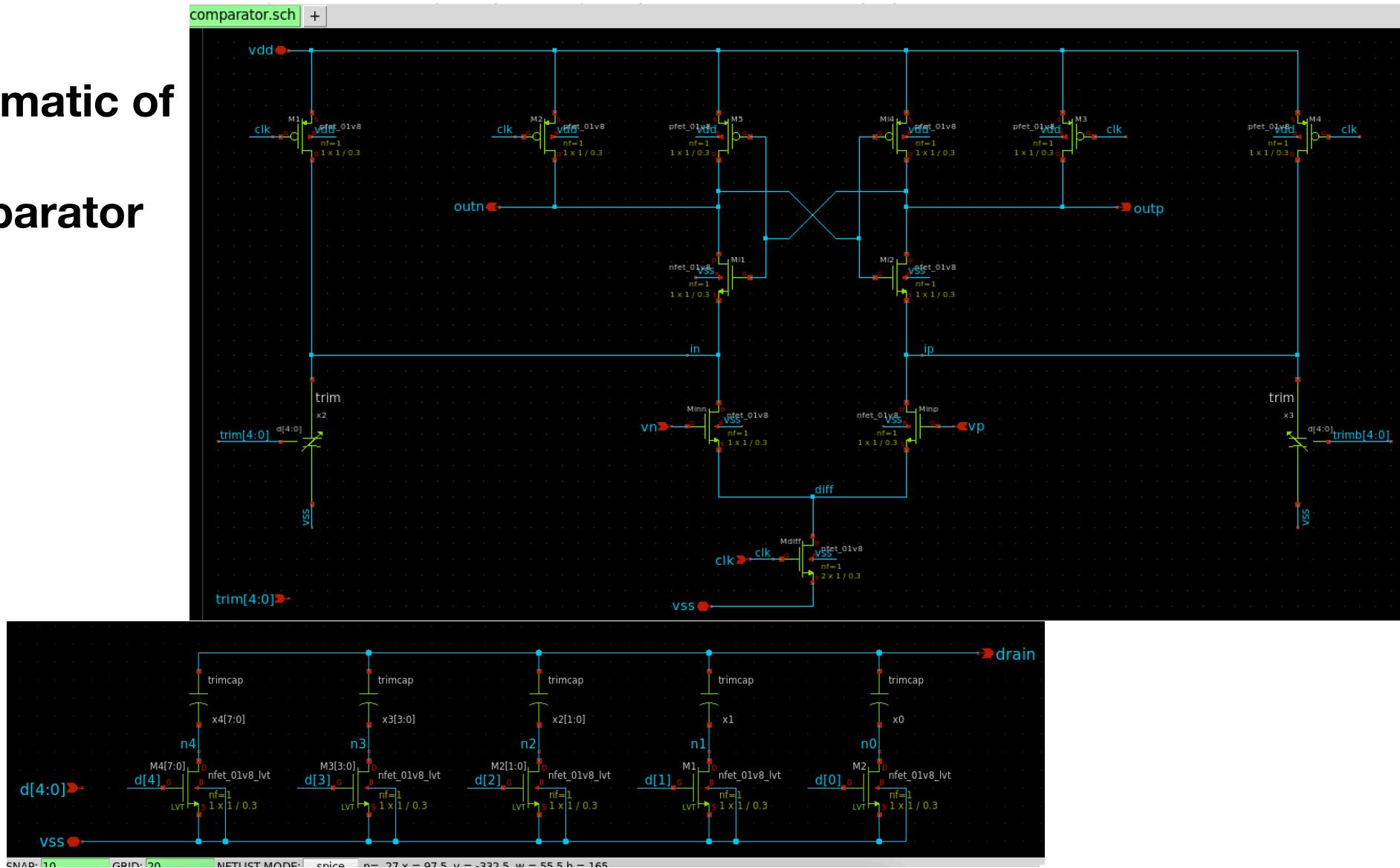


# **SAR-ADC**

## **Activity Report**

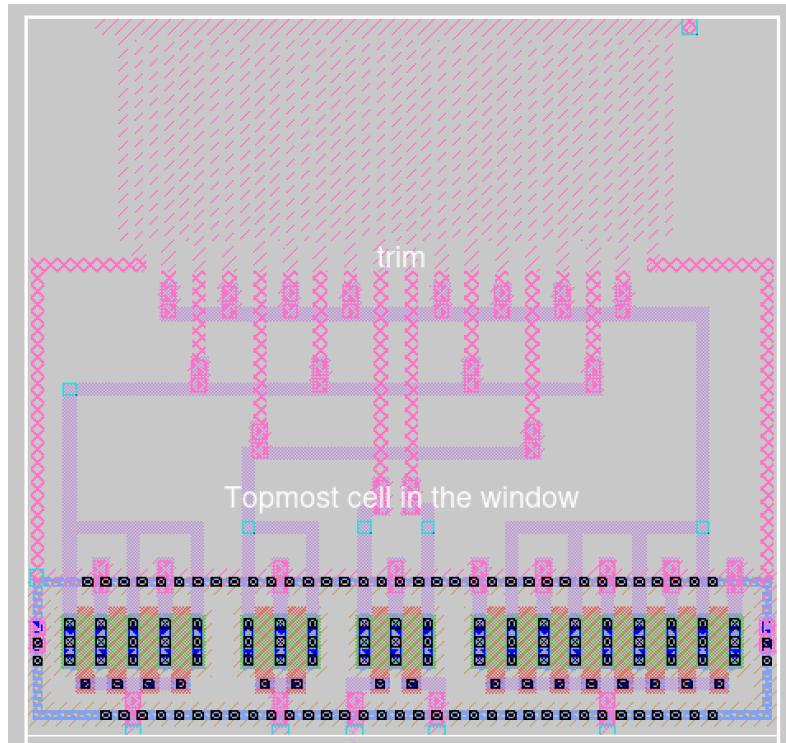
**Alejandro Juárez Lora, Oct 9, 2023**

# Schematic of the comparator



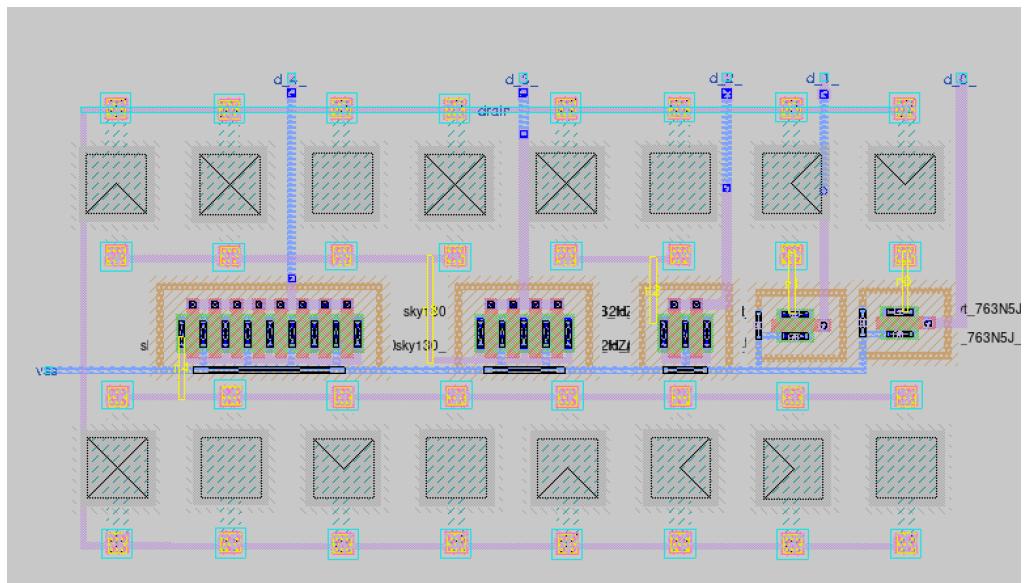
# Trim array capacitance

## Original layout



```
microns: 13.910 x 13.515 (-0.005, -0.415), ( 13.905, 13.100) 187.994
lambda: 1391.00 x 1351.50 ( -0.50, -41.50), ( 1390.50, 1310.00) 1879936.50
internal: 2782 x 2703 ( -1, -83 ), ( 2781, 2620 ) 7519746
%
```

## Redrawn layout



```
microns: 27.350 x 15.590 (-22.910, -8.460), ( 4.440, 7.130) 426.386
lambda: 2735.00 x 1559.00 (-2291.00, -846.00), ( 444.00, 713.00) 4263865.00
internal: 5470 x 3118 ( -4582, -1692 ), ( 888, 1426 ) 17055460
```

# Trim LVS Output

Open Save

trim.out

Home ~/Desktop/EDA/SAR\_IPN/my\_lvs/comparator

```

50 flattening unmatched subcell sky130_fd_pr_nfet_01v8_lvt_763N5J in circuit
51 Flattening unmatched subcell sky130_fd_pr_nfet_01v8_lvt_THUHZA in circuit
52
53 Class trim (0): Merged 11 parallel devices.
54 Class trim (1): Merged 11 parallel devices.
55 Subcircuit summary:
56 Circuit 1: trim | Circuit 2: trim
57 -----
58 sky130_fd_pr_nfet_01v8_lvt (16->5) | sky130_fd_pr_nfet_01v8_lvt
59 trimcap (16) | trimcap (16)
60 Number of devices: 21 | Number of devices: 21
61 Number of nets: 12 | Number of nets: 12
62 -----
63 Resolving symmetries by property value.
64 Resolving symmetries by pin name.
65 Netlists match with 3 symmetries.
66
67 Subcircuit pins:
68 Circuit 1: trim | Circuit 2: trim
69 -----
70 drain | drain
71 d_4_ | d_4_
72 d_3_ | d_3_
73 d_2_ | d_2_
74 d_0_ | d_0_
75 d_1_ | d_1_
76 vss | vss
77 -----
78 Cell pin lists are equivalent.
79 Device classes trim and trim are equivalent.
80
81 Final result: Circuits match uniquely.
82 .

```

Plain Text Tab Width: 8

Open Save

trim.spice

Home ~/Desktop/EDA/SAR\_IPN/new\_layout/comparator

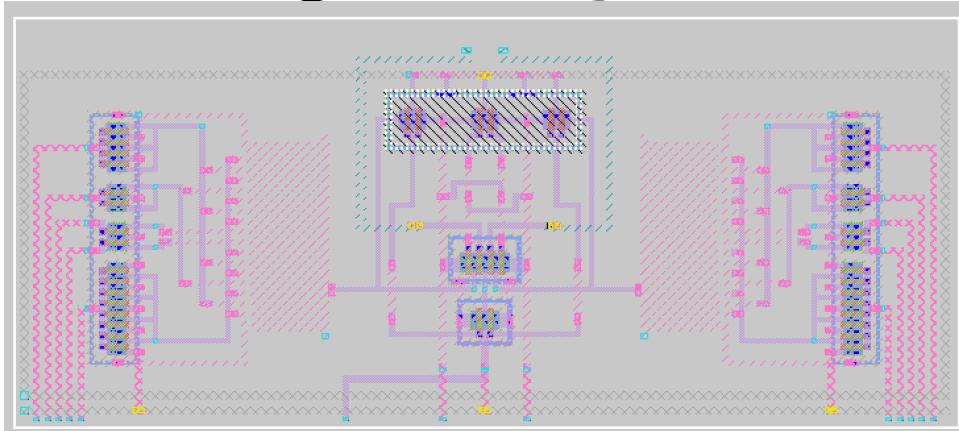
```

30 .AV a_09_11249m a_20_247m a_1129_11249m a_11249_11249m sky130_fd_pr_nfet_01v8_lvt ad=0.29 pd=2.50
as=0.145 ps=1.29 ws=1 l=0.3
39 X1 a_n29_n131# a_n92_91# a_n147_n131# a_n249_n243# sky130_fd_pr_nfet_01v8_lvt ad=0.145 pd=1.29
as=0.29 ps=2.58 w=1 l=0.3
40 .ends
41
42 .subckt trim drain d_4_ d_3_ d_2_ d_1_ d_0_ vss
43 Xsky130_fd_pr_nfet_01v8_lvt_763N5J_0 n1 vss d_1_ vss sky130_fd_pr_nfet_01v8_lvt_763N5J
44 Xtrimcap_12 n4 drain trimcap
45 Xtrimcap_11 n4 drain trimcap
46 Xsky130_fd_pr_nfet_01v8_lvt_763N5J_1 n0 vss d_0_ vss sky130_fd_pr_nfet_01v8_lvt_763N5J
47 Xtrimcap_13 n4 drain trimcap
48 Xtrimcap_14 n4 drain trimcap
49 Xtrimcap_15 n4 drain trimcap
50 Xsky130_fd_pr_nfet_01v8_lvt_3SNHZA_0 n4 d_4_ vss d_4_ d_4_ n4 n4 d_4_ vss vss vss
51 + n4 d_4_ d_4_ d_4_ d_4_ vss sky130_fd_pr_nfet_01v8_lvt_3SNHZA
52 Xsky130_fd_pr_nfet_01v8_lvt_FS2HZA_0 vss d_3_ n3 d_3_ vss n3 d_3_ n3 d_3_ vss
sky130_fd_pr_nfet_01v8_lvt_FS2HZA
53 Xsky130_fd_pr_nfet_01v8_lvt_THUHZA_0 vss d_2_ n2 vss d_2_ n2
sky130_fd_pr_nfet_01v8_lvt_THUHZA
54 Xtrimcap_0 n3 drain trimcap
55 Xtrimcap_2 n3 drain trimcap
56 Xtrimcap_1 n3 drain trimcap
57 Xtrimcap_3 n3 drain trimcap
58 Xtrimcap_4 n2 drain trimcap
59 Xtrimcap_5 n2 drain trimcap
60 Xtrimcap_6 n1 drain trimcap
61 Xtrimcap_7 n0 drain trimcap
62 Xtrimcap_8 n4 drain trimcap
63 Xtrimcap_9 n4 drain trimcap
64 Xtrimcap_10 n4 drain trimcap
65 .ends
66

```

# Comparator

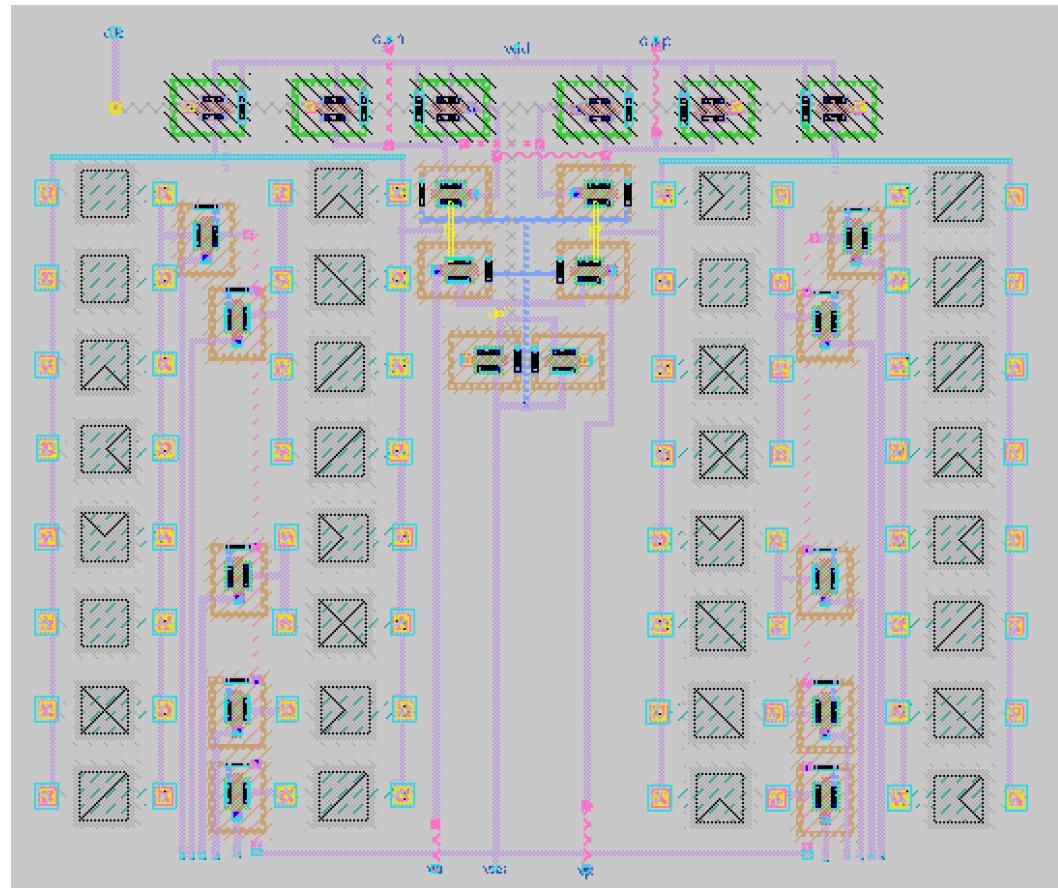
## Original layout



```
Root cell box:  
    width x height ( llx, lly ), ( urx, ury ) area (units^2)  
  
microns: 50.520 x 20.300 ( 0.000, -0.200 ), ( 50.520, 20.100 ) 1025.556  
lambda: 5052.00 x 2030.00 ( 0.00, -20.00 ), ( 5052.00, 2010.00 ) 10255560.00  
internal: 10104 x 4060 ( 0, -40 ), ( 10104, 4020 ) 41022240
```

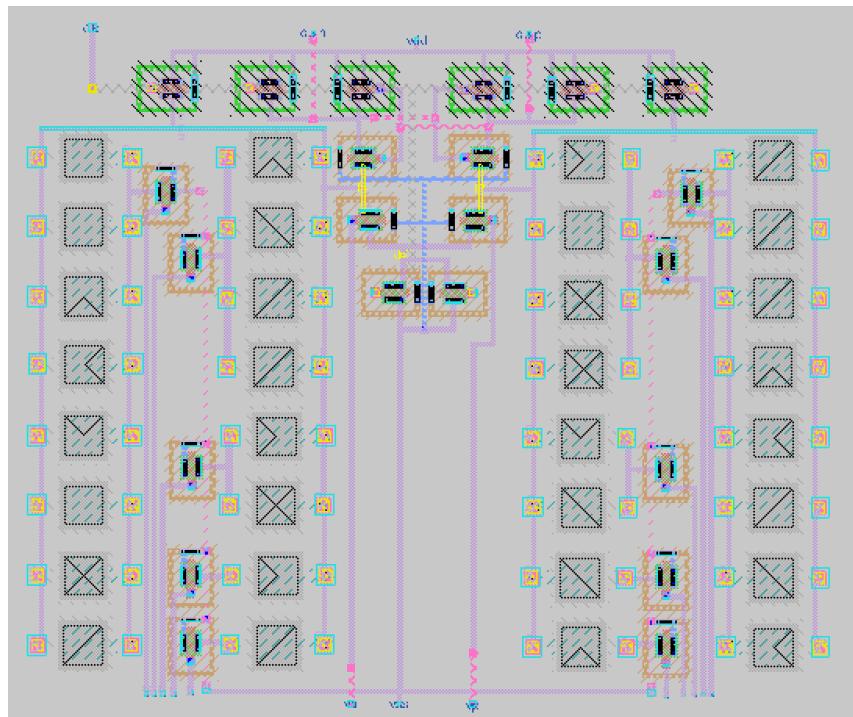
```
Root cell box:  
    width x height ( llx, lly ), ( urx, ury ) area (units^2)  
  
microns: 33.435 x 28.510 (-4.740, -20.385), ( 28.695, 8.125 ) 953.232  
lambda: 3343.50 x 2851.00 (-474.00, -2038.50), ( 2869.50, 812.50 ) 9532318.00  
internal: 6687 x 5702 ( -948, -4077 ), ( 5739, 1625 ) 38129274
```

## 1st redrawn layout



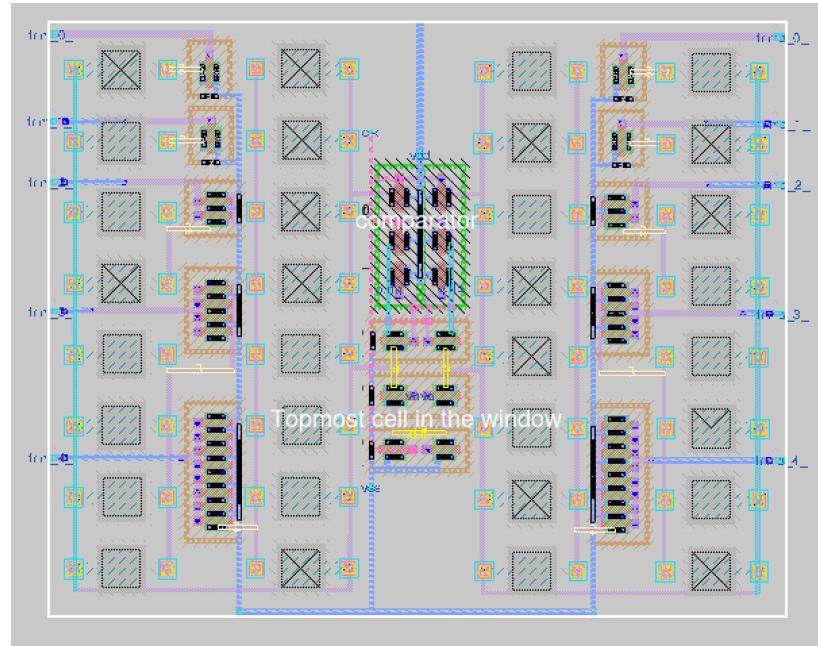
# Comparator

## 1st redrawn layout



```
Root cell box:  
    width x height ( llx, lly ), ( urx, ury ) area (units^2)  
microns: 33.435 x 28.510 (-4.740, -20.385), ( 28.695, 8.125) 953.232  
lambda: 3343.50 x 2851.00 (-474.00, -2038.50), ( 2869.50, 812.50) 9532318.00  
internal: 6687 x 5702 (-948, -4077), ( 5739, 1625) 38129274
```

## 2nd redrawn layout



```
Root cell box:  
    width x height ( llx, lly ), ( urx, ury ) area (units^2)  
microns: 31.260 x 25.150 (-8.845, -9.740), ( 22.415, 15.410) 786.189  
lambda: 3126.00 x 2515.00 (-884.50, -974.00), ( 2241.50, 1541.00) 7861890.00  
internal: 6252 x 5030 (-1769, -1948), ( 4483, 3082) 31447560
```

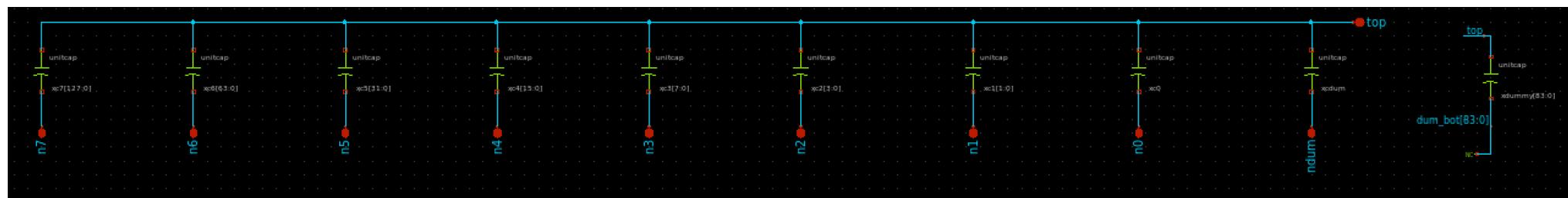
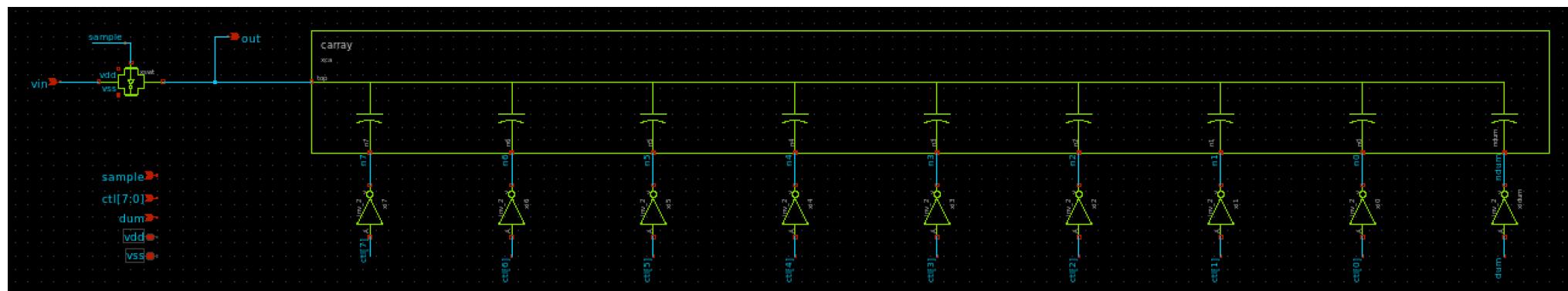
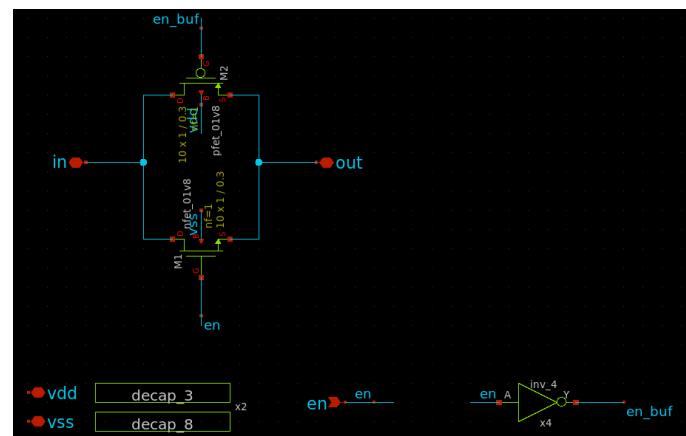
# Comparator LVS Output

```
● ○ ● alejandrojuarezlora — alex@alex-Parallels-Virtual-Platform: ~
```

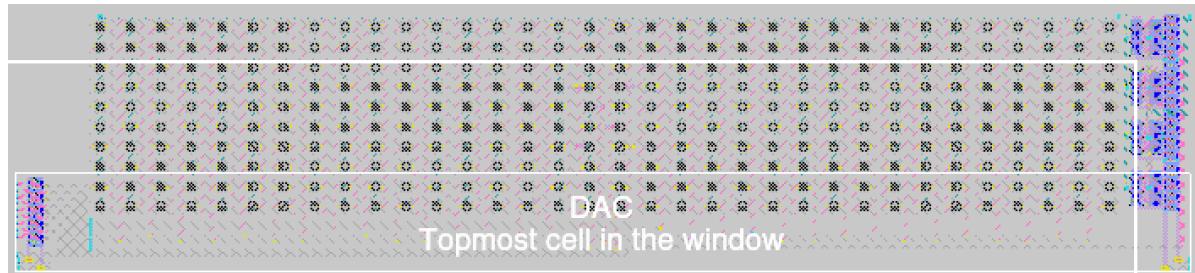
```
Circuit was modified by parallel/series device merging.
New circuit summary:
Contents of circuit 1: Circuit: 'comparator'
Circuit comparator contains 13 device instances.
  Class: sky130_fd_pr_nfet_01v8 instances: 5
  Class: sky130_fd_pr_pfet_01v8 instances: 6
  Class: trim_d_pr_nfet_01v8 instances: 5
Circuit contains 20 nets.
Contents of circuit 2: Circuit: 'comparator'
Circuit comparator contains 13 device instances.
  Class: sky130_fd_pr_nfet_01v8 instances: 5
  Class: sky130_fd_pr_pfet_01v8 instances: 6
  Class: trim instances: 2
Circuit contains 20 nets.
Circuit 1 contains 13 devices, Circuit 2 contains 13 devices.
Circuit 1 contains 20 nets, Circuit 2 contains 20 nets.
Final result: sky130_fd_pr_nfet_01v8_lvt_3SNHZA.mag
Circuits match uniquely.
Logging to file "comparator.out" disabled
LVS Done.
alex@alex-Parallels-Virtual-Platform:~/Desktop/EDA/SAR_IPN/my_lvs/comparator$
```

```
comparator.spice ×
Users > alejandrojuarezlora > EDA > SAR_IPN > new_layout > comparator > comparator.spice
64 Xtrimcap_3 n3 drain trimcap
65 Xtrimcap_4 n2 drain trimcap
66 Xtrimcap_5 n2 drain trimcap
67 Xtrimcap_6 n1 drain trimcap
68 Xtrimcap_7 n0 drain trimcap
69 Xtrimcap_8 n4 drain trimcap
70 Xtrimcap_9 n4 drain trimcap
71 Xtrimcap_10 n4 drain trimcap
72 .ends
73
74 .subckt sky130_fd_pr_nfet_01v8_7UX3DE a_n33_n87# a_30_117# a_30_n309# a_n88_n309#
75 + a_n88_117# a_n33_29# a_n190_n421#
76 X0 a_30_n309# a_n33_n87# a_n88_n309# a_n190_n421# sky130_fd_pr_nfet_01v8 ad=0.29 pd=2.58 as=0.29 ps=2.58 w=1
77 X1 a_30_117# a_n33_29# a_n88_117# a_n190_n421# sky130_fd_pr_nfet_01v8 ad=0.29 pd=2.58 as=0.29 ps=2.58 w=1 l=0
78 .ends
79
80 .subckt comparator vn vp clk vdd vss outp outn trim_4_ trim_3_ trim_2_ trim_1_ trim_0_
81 + trimb_4_ trimb_3_ trimb_2_ trimb_1_ trimb_0_
82 Xsky130_fd_pr_pfet_01v8_QE5SNW_0 outp outp clk vdd outn vdd clk vdd ip sky130_fd_pr_pfet_01v8_QE5SNW
83 Xsky130_fd_pr_pfet_01v8_QE5SNW_1 outn outn clk vdd outp vdd clk vdd vdd in sky130_fd_pr_pfet_01v8_QE5SNW
84 Xtrim_0 in trim_4_ trim_3_ trim_2_ trim_1_ trim_0_ vss trim
85 Xtrim_1 ip trimb_4_ trimb_3_ trimb_2_ trimb_1_ trimb_0_ vss trim
86 Xsky130_fd_pr_nfet_01v8_7UX3DE_0 clk vss vss diff diff clk vss sky130_fd_pr_nfet_01v8_7UX3DE
87 Xsky130_fd_pr_nfet_01v8_7UX3DE_1 outp ip in outn outp outn vss sky130_fd_pr_nfet_01v8_7UX3DE
88 Xsky130_fd_pr_nfet_01v8_7UX3DE_2 vn diff diff in ip vp vss sky130_fd_pr_nfet_01v8_7UX3DE
89 .ends
90
```

# Schematic of the DAC

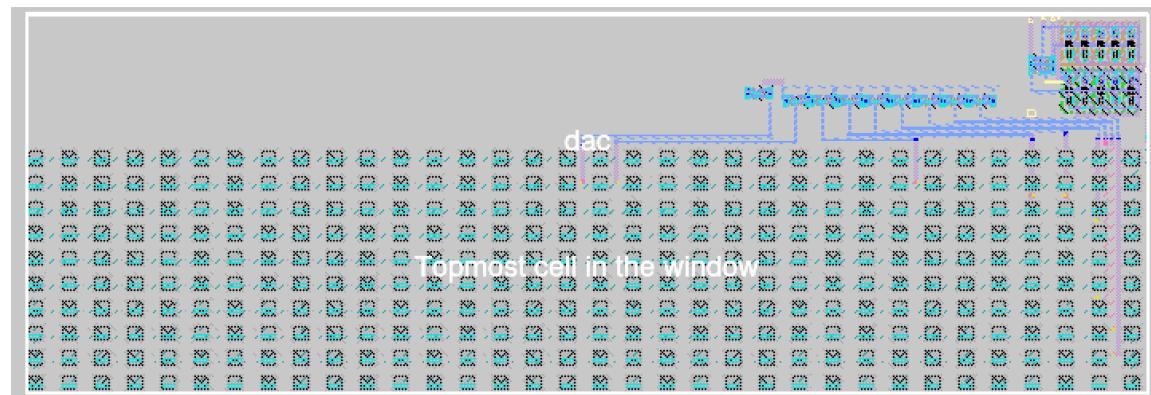


# DAC Original layout

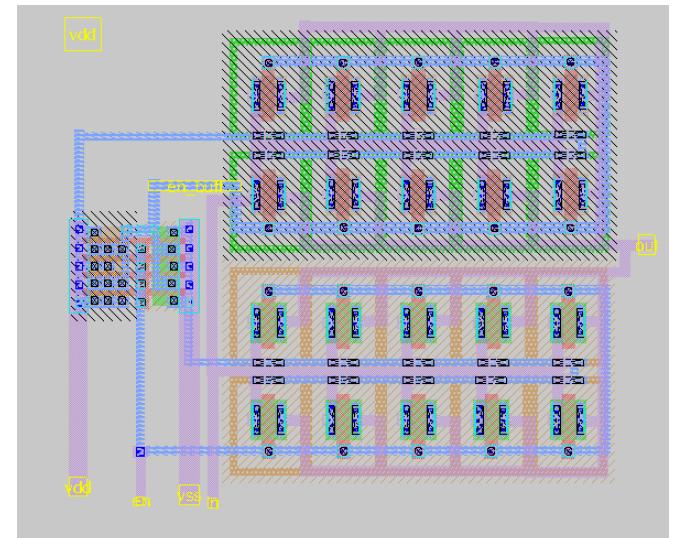


```
Root cell box:  
    width x height ( llx, lly ), ( urx, ury ) area (units^2)  
  
microns: 249.635 x 54.375 (-14.160, -4.275), ( 235.475, 50.100) 13573.902  
lambda: 24963.50 x 5437.50 (-1416.00, -427.50), ( 23547.50, 5010.00) 135739024.00  
internal: 49927 x 10875 (-2832, -855), ( 47095, 10020) 542956125
```

# DAC Redrawn layout



```
Root cell box:  
    width x height ( llx, lly ), ( urx, ury ) area (units^2)  
  
microns: 135.240 x 45.780 (-20.095, -16.705), ( 115.145, 29.075) 6191.287  
lambda: 13524.00 x 4578.00 (-2009.50, -1670.50), ( 11514.50, 2907.50) 61912872.00  
internal: 27048 x 9156 (-4019, -3341), ( 23029, 5815) 247651488
```



# Carry LVS output

The terminal window shows the LVS process for a circuit named 'carray'. It includes commit information, device instance counts, net counts, and a warning about automatically based nets. The text editor window shows the generated NGSPICE file, which contains subckt definitions for various components like 'unitcap' and 'carry'.

```
alejandrojuarezlora — alex@alex-Parallels-Virtual-Platform: ~/Desktop/EDA/SAR_IPN % zsh
Circuit unitcap contains 1 device instances.
  Class: sky130_fd_pr__cap_mim_m3_1 instances: 1
Circuit contains 2 nets.
  Committer: Jorge Alejandro Juárez Lora <alejandrojuarezlora@dhcp-172-31-157-162>
Circuit 1 contains 1 devices, Circuit 2 contains 1 devices.
Circuit 1 contains 2 nets, Circuit 2 contains 2 nets.
  You can suppress this message by setting them explicitly. Run the
    following command and follow the instructions in your editor to edit
  Contents of circuit 1: Circuit: 'carray'
  Circuit carray contains 340 device instances.
    Class: unitcap instances: 340
  Circuit contains 94 nets.
  Contents of circuit 2: Circuit: 'carray'
  Circuit carray contains 340 device instances.
    Class: unitcap instances: 340
  Circuit contains 94 nets.
  Circuit 1 contains 340 devices, Circuit 2 contains 340 devices.
  Circuit 1 contains 94 nets, Circuit 2 contains 94 nets.
  Enumerating objects: 17, done.
  Counting objects: 100% (17/17), done.
  Final result: compression using up to 4 threads
  Circuits match uniquely.ts: 100% (9/9), done.
  Writing objects: 100% (9/9), 980 bytes | 490.00 KiB/s, done.
  Logging to file "carray.out" disabled(delta 0), pack-reused 0
  LVS Done.
  alejandrojuarezlora — alex@alex-Parallels-Virtual-Platform: ~/Desktop/EDA/SAR_IPN/my_lvs/dac %
  7fbfe40..19eae82 main -> main
  (base) alejandrojuarezlora@dhcp-172-31-157-162 SAR_IPN %
```

carry\_lay.spice

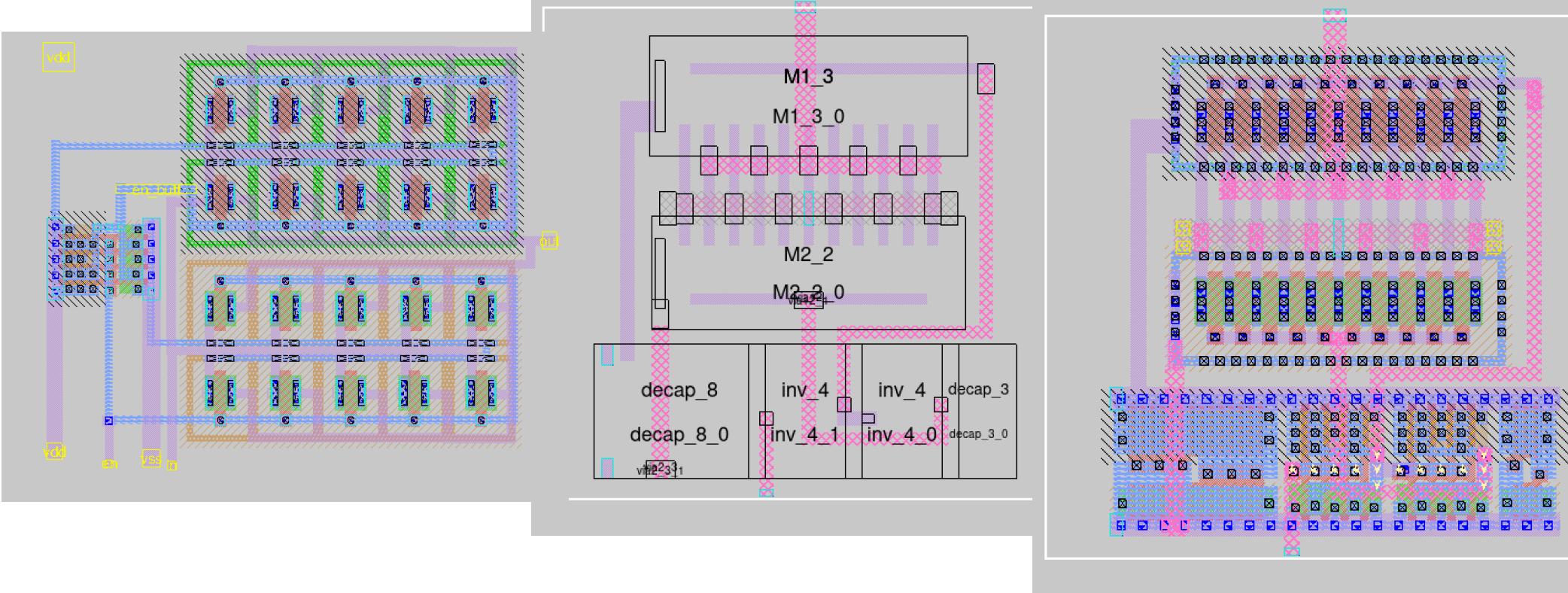
```
/* NGSPICE file created from carry.ext - technology: sky130B
2
3 .subckt sky130_fd_pr__cap_mim_m3_1_FJK8MD m3_n386_n240# c1_n346_n200#
4 X0 c1_n346_n200# m3_n386_n240# sky130_fd_pr__cap_mim_m3_1 l=2 w=2
5 .ends
6
7 .subckt unitcap cp cn
8 Xsky130_fd_pr__cap_mim_m3_1_FJK8MD_0 cn cp sky130_fd_pr__cap_mim_m3_1_FJK8MD
9 .ends
10
11 .subckt carry top ndum n0 n1 n2 n3 n4 n5 n6 n7
12 Xunitcap_190 top n5 unitcap
13 Xunitcap_191 top unitcap_191/cn unitcap
14 Xunitcap_180 top n6 unitcap
15 Xunitcap_181 top n6 unitcap
16 Xunitcap_170 top n6 unitcap
17 Xunitcap_192 top unitcap_192/cn unitcap
18 Xunitcap_330 top unitcap_330/cn unitcap
19 Xunitcap_182 top n6 unitcap
20 Xunitcap_171 top n6 unitcap
21 Xunitcap_160 top unitcap_160/cn unitcap
22 Xunitcap_193 top n6 unitcap
23 Xunitcap_183 top unitcap_183/cn unitcap
24 Xunitcap_150 top n6 unitcap
25 Xunitcap_331 top unitcap_331/cn unitcap
26 Xunitcap_172 top n6 unitcap
27 Xunitcap_194 top n6 unitcap
28 Xunitcap_161 top n6 unitcap
```

# Issues with sw\_top

```
● ● ● alejandrojuarezlora — alex@alex-Parallels-Virtual-Platform: ~/Desktop/EDA/S  
Circuit was modified by parallel/series device merging.  
New circuit summary:  
7fbfe40..19eae82 main -> main  
Contents of circuit 1: Circuit: 'sw_top' 72-31-157-162 SAR_IPN % cd sim  
Circuit sw_top contains 3 device instances: 72-31-157-162 sim % ls  
Class: sky130_fd_sc_hd_inv_4 instances: 1 tr_sar.spice  
Class: sky130_fd_sc_hd_pfet_01v8 instances: 1 tr_sar_digital.raw  
Class: sky130_fd_pr_pfet_01v8 instances: 2-1-157-162 sim % code comparator.  
Circuit contains 13 nets.  
Contents of circuit 2: Circuit: 'sw_top' 72-31-157-162 sim % ls  
Circuit sw_top contains 5 device instances,  
Circuit sw_top contains 5 device instances,  
Class: sky130_fd_sc_hd_inv_4 instances: 1-157-162 sim % cd .. /new_layout  
Class: sky130_fd_sc_hd_inv_4 instances: 1 72-31-157-162 dac % l  
Class: sky130_fd_sc_hd_decap_3 instances: 1  
Class: sky130_fd_sc_hd_decap_8 instances: 1 157-162 dac % sls  
Class: sky130_fd_pr_pfet_01v8 instances: 1  
Circuit contains 16 nets.  
(base) alejandrojuarezlora@dhcp-172-31-157-162: ~$  
Circuit 1 contains 3 devices, Circuit 2 contains 5 devices. *** MISMATCH ***_PGNH6  
Circuit 1 contains 13 nets, Circuit 2 contains 16 nets. *** MISMATCH ***_PGNH6  
carry.spice sky130_fd_sc_hd_inv_4  
dac.mag sky130_fd_sc_hd_pfet_01v8_67UB6  
Final result: d_pr_cap_mim_m3_1_FJK8MD.ext sky130_fd_sc_hd_inv_2.mag  
Netlists do not match. d_mtm_m3_1_FJK8MD.mag sky130_fd_sc_hd_inv_4.ext  
Logging to file "sw_top.out" disabled cp-172-31-157-162 dac % code sw_top.spic  
LVS Done.  
alex@alex-Parallels-Virtual-Platform: ~/Desktop/EDA/SAR_IPN/my_lvs/dac$
```

```
rs > alejandrojuarezlora > EDA > SAR_IPN > my_lvs > dac > └── sw_top.sch.spice  
** sch_path: /media/psf/Home/EDA/SAR_IPN/xschem/sar/sw/sw_top.sch  
.subckt sw_top out en vss vdd in  
.PININFO out:B en:I vss:B vdd:B in:B  
x2 vss vss vdd vdd sky130_fd_sc_hd_decap_8  
x4 en vss vss vdd vdd en_buf sky130_fd_sc_hd_inv_4  
x1 VGND VNB VPB VPWR sky130_fd_sc_hd_decap_3  
XM1 in en out vss sky130_fd_pr_nfet_01v8 L=0.3 W=1 nf=1 m=10  
XM2 in en_buf out vdd sky130_fd_pr_pfet_01v8 L=0.3 W=1 nf=1 m=10  
.ends  
.end  
  
21 .subckt sw_top out en vss vdd in  
22 Xsky130_fd_pr_pfet_01v8_67UB6S_0 in out en_buf vdd sky130_fd_pr_pfet_01v8_67UB6S  
23 Xsky130_fd_pr_pfet_01v8_67UB6S_2 in out en_buf vdd sky130_fd_pr_pfet_01v8_67UB6S  
24 Xsky130_fd_pr_pfet_01v8_67UB6S_1 in out en_buf vdd sky130_fd_pr_pfet_01v8_67UB6S  
25 Xsky130_fd_pr_pfet_01v8_67UB6S_3 in out en_buf vdd sky130_fd_pr_pfet_01v8_67UB6S  
26 Xsky130_fd_pr_pfet_01v8_67UB6S_4 in out en_buf vdd sky130_fd_pr_pfet_01v8_67UB6S  
27 Xsky130_fd_pr_pfet_01v8_67UB6S_5 in out en_buf vdd sky130_fd_pr_pfet_01v8_67UB6S  
28 Xsky130_fd_pr_pfet_01v8_67UB6S_6 in out en_buf vdd sky130_fd_pr_pfet_01v8_67UB6S  
29 Xsky130_fd_pr_pfet_01v8_67UB6S_7 in out en_buf vdd sky130_fd_pr_pfet_01v8_67UB6S  
30 Xsky130_fd_pr_pfet_01v8_67UB6S_8 in out en_buf vdd sky130_fd_pr_pfet_01v8_67UB6S  
31 Xsky130_fd_pr_pfet_01v8_67UB6S_9 in out en_buf vdd sky130_fd_pr_pfet_01v8_67UB6S  
32 Xsky130_fd_pr_nfet_01v8_PGNH6C_0 in out en_vss sky130_fd_pr_nfet_01v8_PGNH6C  
33 Xsky130_fd_pr_nfet_01v8_PGNH6C_1 in out en_vss sky130_fd_pr_nfet_01v8_PGNH6C  
34 Xsky130_fd_pr_nfet_01v8_PGNH6C_2 in out en_vss sky130_fd_pr_nfet_01v8_PGNH6C  
35 Xsky130_fd_pr_nfet_01v8_PGNH6C_3 in out en_vss sky130_fd_pr_nfet_01v8_PGNH6C  
36 Xsky130_fd_pr_nfet_01v8_PGNH6C_4 in out en_vss sky130_fd_pr_nfet_01v8_PGNH6C  
37 Xsky130_fd_pr_nfet_01v8_PGNH6C_5 in out en_vss sky130_fd_pr_nfet_01v8_PGNH6C  
38 Xsky130_fd_pr_nfet_01v8_PGNH6C_6 in out en_vss sky130_fd_pr_nfet_01v8_PGNH6C  
39 Xsky130_fd_pr_nfet_01v8_PGNH6C_7 in out en_vss sky130_fd_pr_nfet_01v8_PGNH6C  
40 Xsky130_fd_pr_nfet_01v8_PGNH6C_8 in out en_vss sky130_fd_pr_nfet_01v8_PGNH6C  
41 Xsky130_fd_pr_nfet_01v8_PGNH6C_9 in out en_vss sky130_fd_pr_nfet_01v8_PGNH6C  
42 Xsky130_fd_pr_nfet_01v8_PGNH6C_0 in out en_vss sky130_fd_pr_nfet_01v8_PGNH6C  
43 Xsky130_fd_pr_nfet_01v8_PGNH6C_1 in out en_vss sky130_fd_pr_nfet_01v8_PGNH6C  
44 .ends  
45
```

# Issues with sw\_top layout

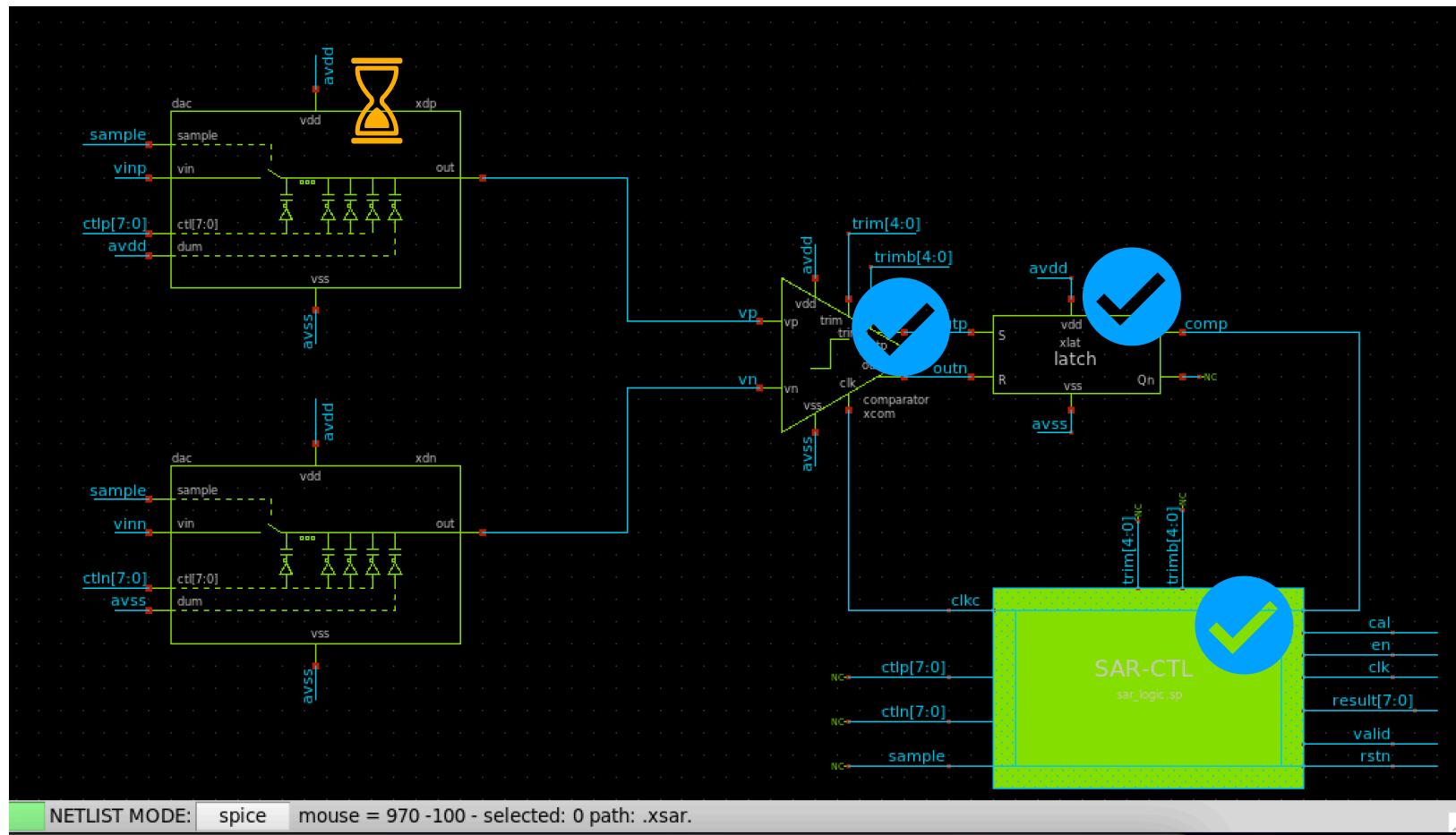


# **SAR-ADC**

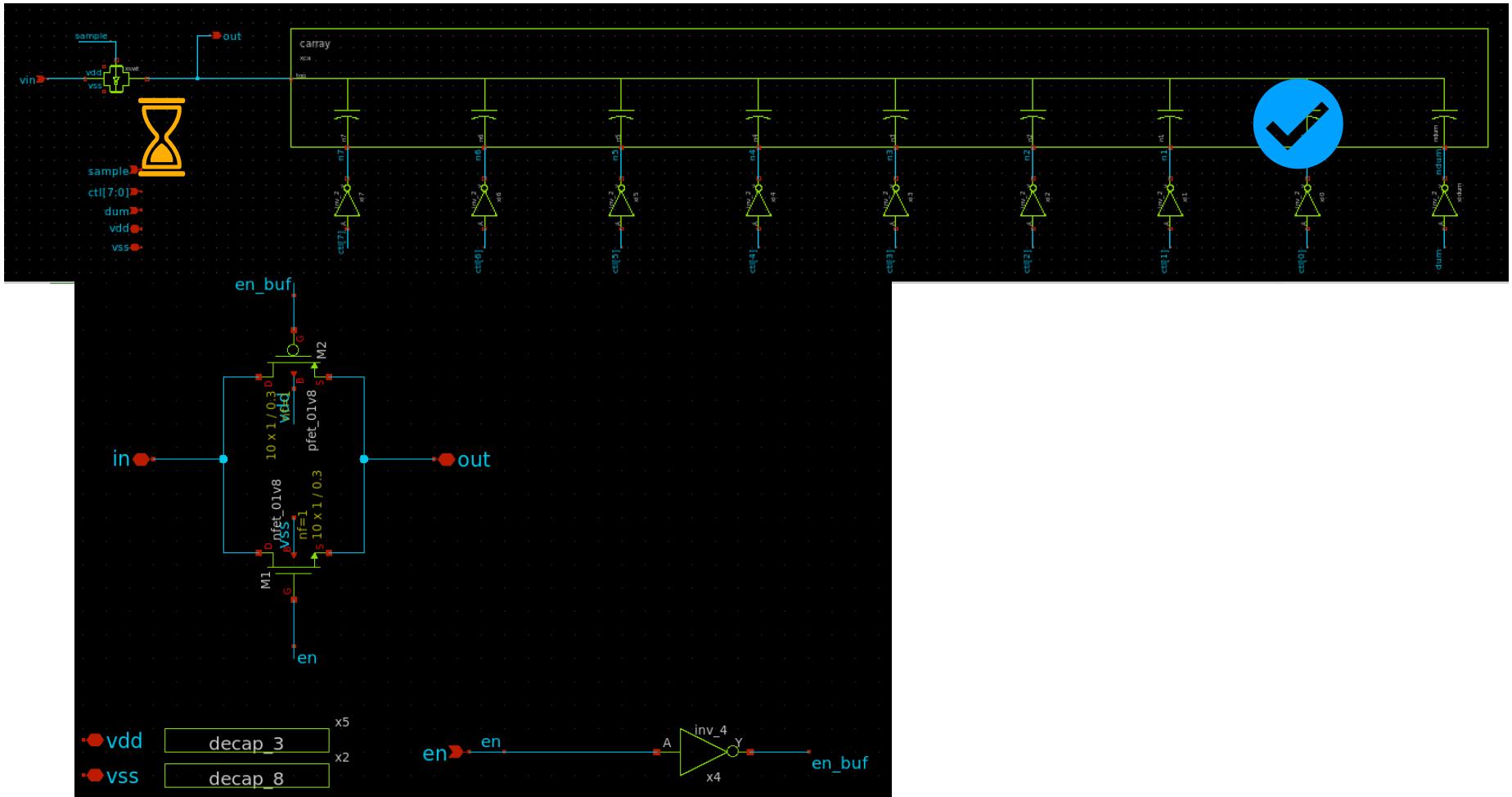
## **Activity Report**

**Alejandro Juárez Lora, Oct 13, 2023**

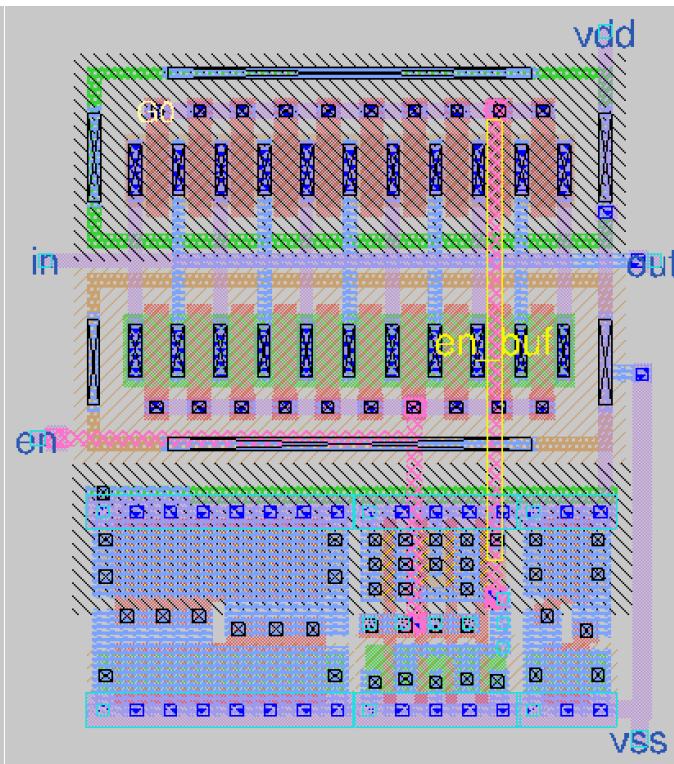
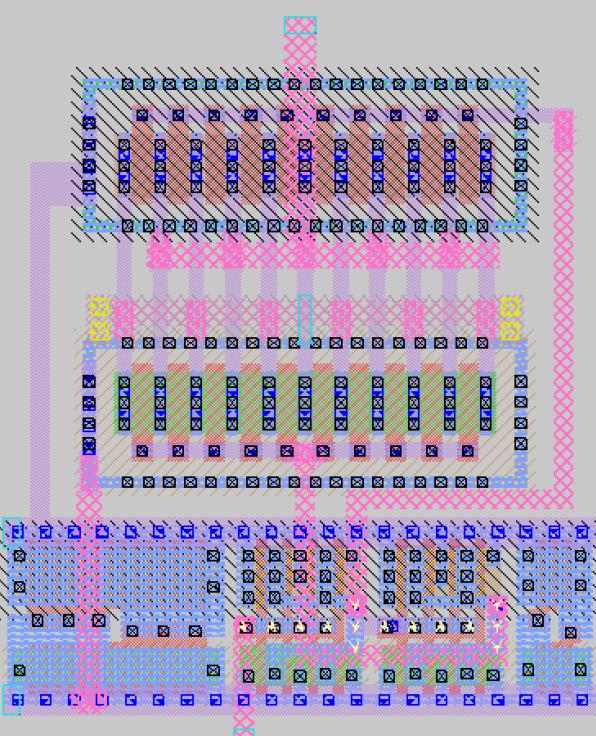
# LVS so far...



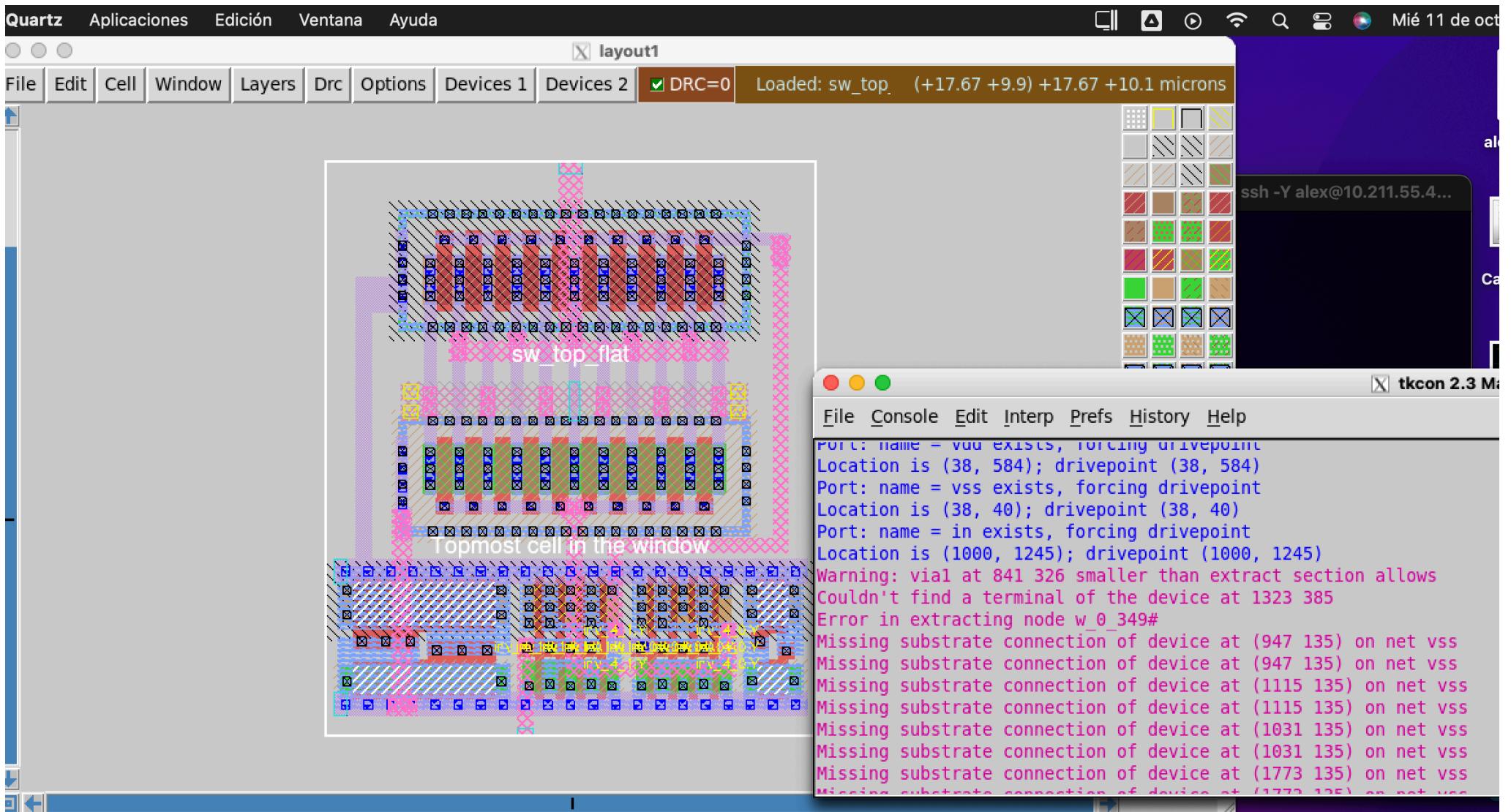
# DAC LVS so far...



# sw\_top redrawn, there are some differences



- Attaching the bulk in the decap\_8 and decap\_3
  - Original layout leaves it unattached
- My layout has one inverter, as schematic. Original layout has two inverters



# sw\_top (original) LVS output

./run\_lvs\_sw\_top\_original.sh

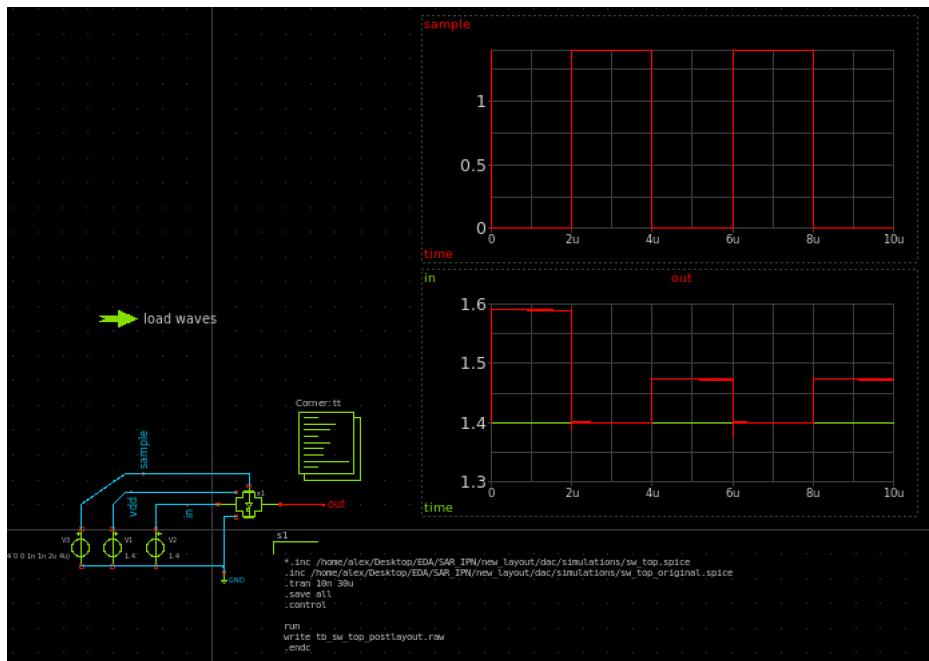
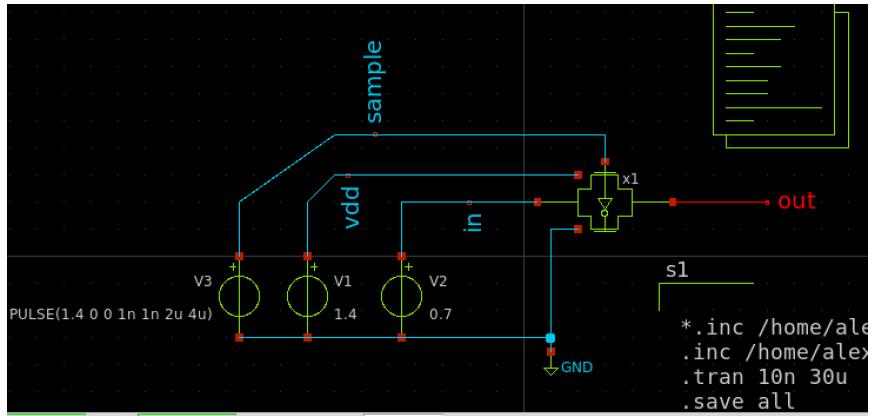
```
Circuit was modified by parallel/series device merging.  
New circuit summary:  
  
Contents of circuit 1: Circuit: 'sw_top'  
Circuit sw_top contains 6 device instances.  
  Class: sky130_fd_pr_nfet_01v8 instances: 1  
  Class: inv_4           instances: 2  
  Class: decap_3         instances: 1  
  Class: decap_8         instances: 1  
  Class: sky130_fd_pr_pfet_01v8 instances: 1  
Circuit contains 48 nets.  
Contents of circuit 2: Circuit: 'sw_top'  
Circuit sw_top contains 5 device instances.  
  Class: sky130_fd_pr_nfet_01v8 instances: 1  
  Class: sky130_fd_sc_hd_inv_4 instances: 1  
  Class: sky130_fd_sc_hd_decap_3 instances: 1  
  Class: sky130_fd_sc_hd_decap_8 instances: 1  
  Class: sky130_fd_pr_pfet_01v8 instances: 1  
Circuit contains 34 nets.  
  
Circuit 1 contains 6 devices, Circuit 2 contains 5 devices. *** MISMATCH ***  
Circuit 1 contains 48 nets,   Circuit 2 contains 34 nets. *** MISMATCH ***  
  
Final result:  
Netlists do not match.  
Logging to file "sw_top_original.out" disabled  
LVS Done.  
alex@alex-Parallels-Virtual-Platform:~/Desktop/EDA/SAR_IPN/my_lvs/dac$
```

Output during LVS running

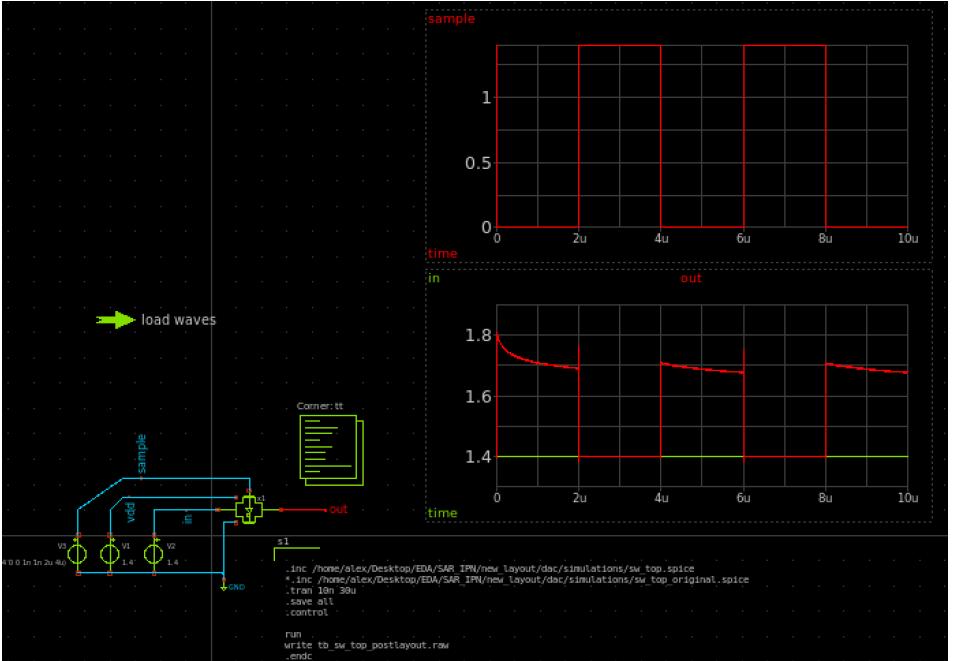
```
-----  
Instance: decap_8_0  
a_65_55# = 9  
a_65_331# = 5  
w_0_269# = 4  
VSUBS = 9  
proxy1 = 1  
proxy2 = 1  
proxy3 = 1  
proxy4 = 1  
proxypyroxa_65_55# = 1  
proxypyroxa_65_331# = 1  
proxypyroyw_0_269# = 1  
proxypyroxyVSUBS = 1  
-----  
| Instance: sky130_fd_sc_hd_decap_8:2  
| proxya_65_55# = 1  
| proxya_65_331# = 1  
| proxyw_0_269# = 1  
| proxyVSUBS = 1  
| 1 = 7  
| 2 = 7  
| 3 = 7  
| 4 = 7  
| proxya_65_55# = 1  
| proxya_65_331# = 1  
| proxyw_0_269# = 1  
| proxyVSUBS = 1  
-----  
Netlists do not match.  
  
Subcircuit pins:  
Circuit 1: sw_top  
Circuit 2: sw_top  
-----  
vss  
vdd  
en  
Cell pin lists are equivalent.  
Device classes sw_top and sw_top are equivalent.  
  
Final result: Netlists do not match.  
alex@alex-Parallels-Virtual-Platform:~/Desktop/EDA/SAR_IPN/my_lvs/dac$
```

Output file sw\_top\_original.out

# Post Layout sim with $V_{in} = 1.4V$

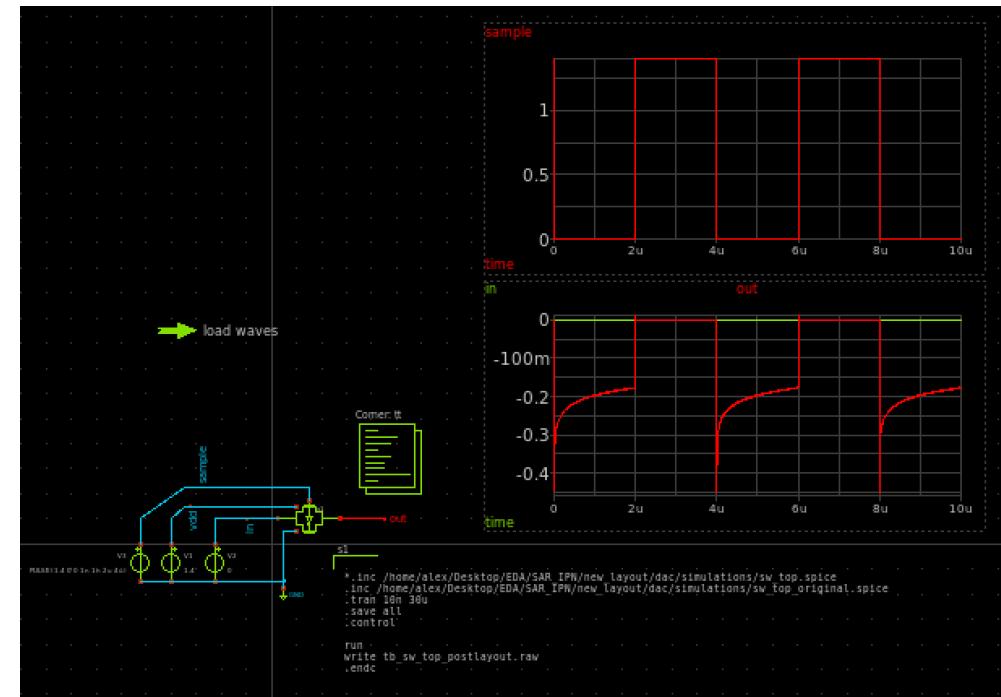


Original

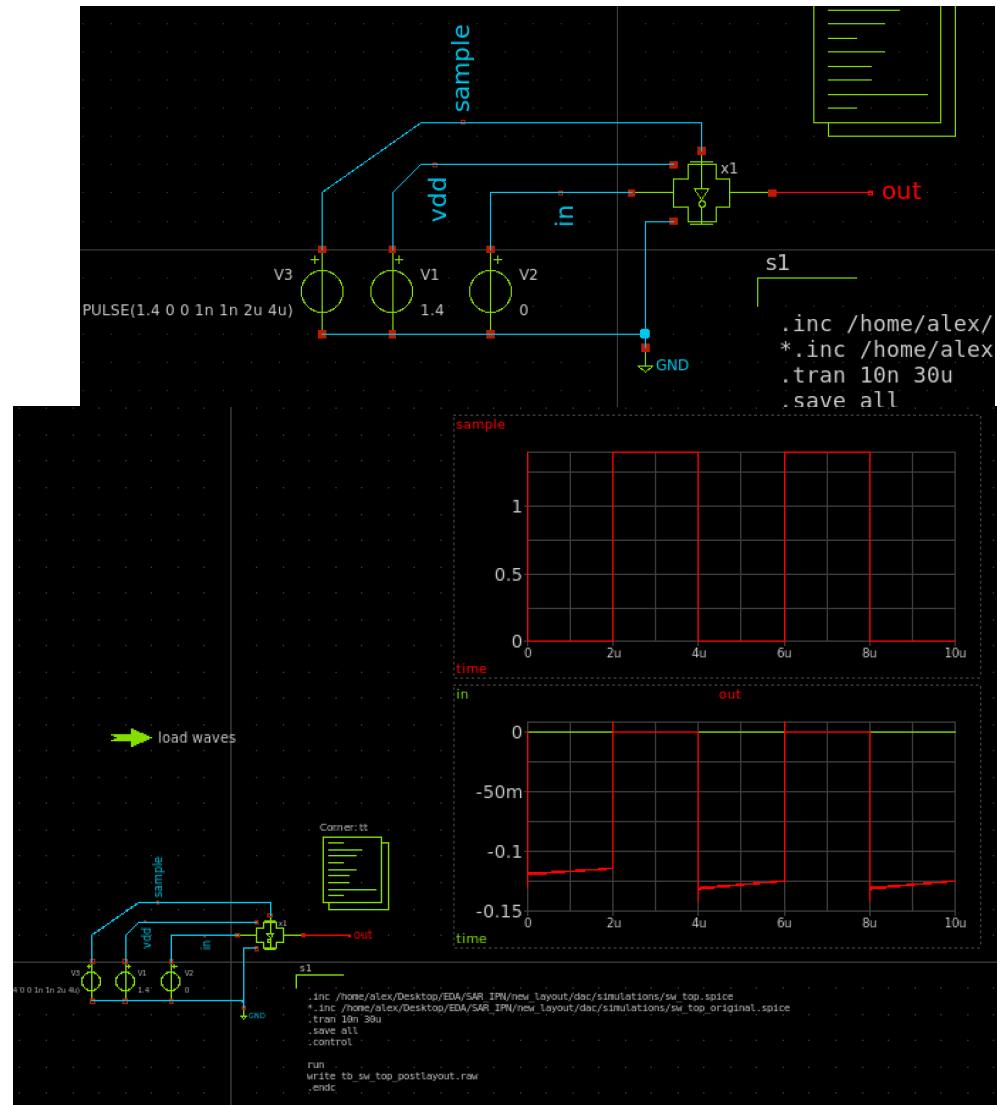


Redrawn

# Post Layout with $V_{in} = 0V$

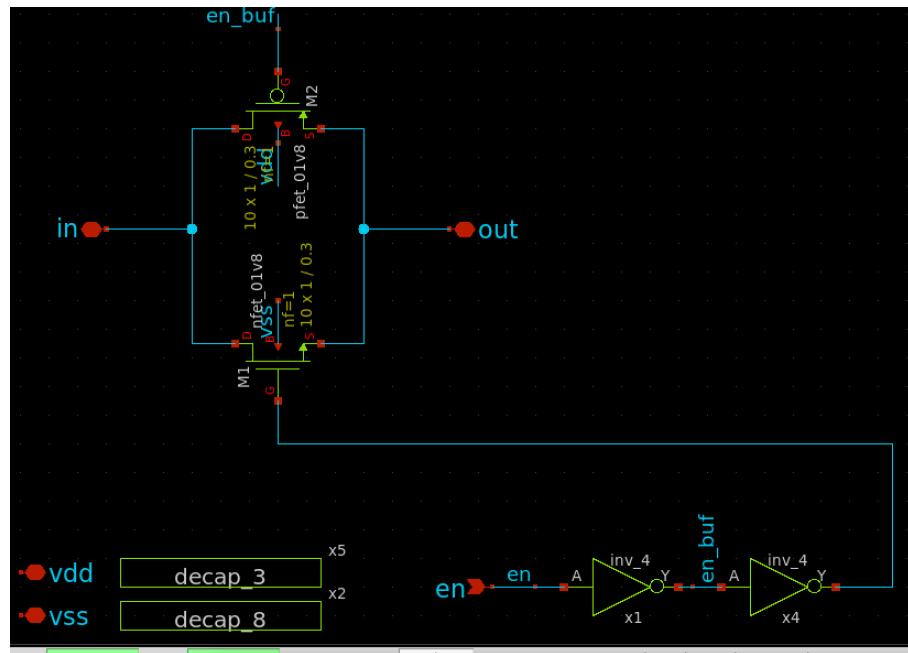


Original

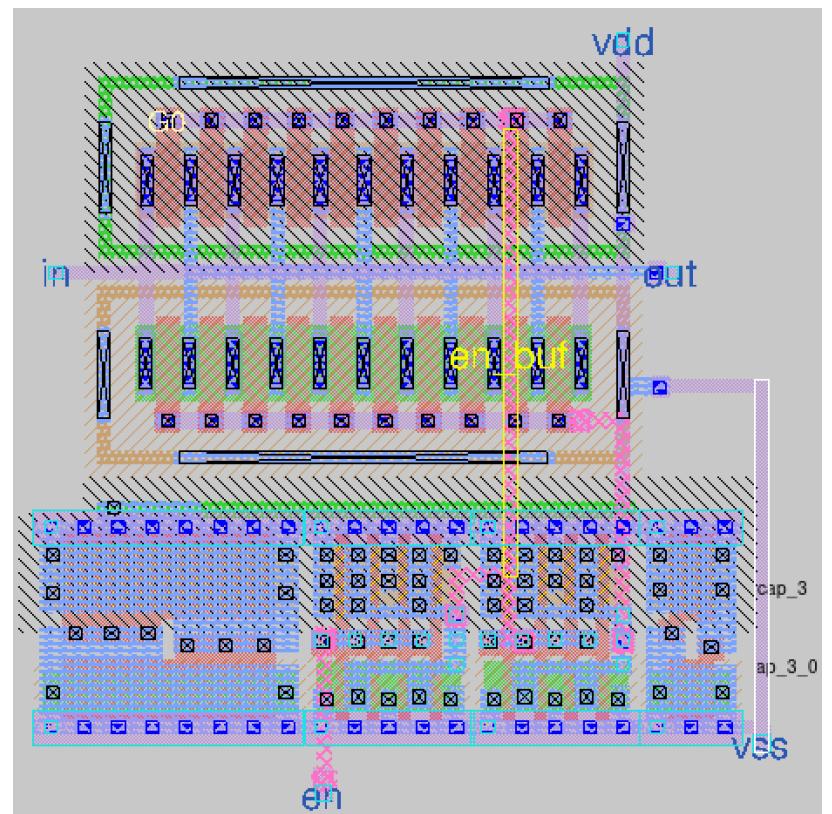


Redrawn

# Proceeding with two inverters



Modified schematic



Redrawn final

# sw\_top (final) LVS output

./run\_lvs\_sw\_top\_final.sh

```
alejandrojuarezlora — alex@alex-Parallels-Virtual-Platform: ~/Desktop/E...
Class: sky130_fd_sc_hd__inv_4 instances: 2
Class: sky130_fd_sc_hd__decap_3 instances: 1
Class: sky130_fd_sc_hd__decap_8 instances: 1
Class: sky130_fd_pr_pfet_01v8 instances: 1
Circuit contains 27 nets.
Contents of circuit 2: Circuit: 'sw_top'
Circuit sw_top contains 6 device instances.
Class: sky130_fd_pr_nfet_01v8 instances: 1
Class: sky130_fd_sc_hd_inv_4 instances: 2
Class: sky130_fd_sc_hd_decap_3 instances: 1
Class: sky130_fd_sc_hd_decap_8 instances: 1
Class: sky130_fd_pr_pfet_01v8 instances: 1
Circuit contains 27 nets.

Circuit 1 contains 6 devices, Circuit 2 contains 6 devices.
Circuit 1 contains 27 nets, Circuit 2 contains 27 nets.

Final result:
Top level cell failed pin matching.

Logging to file "sw_top_final.out" disabled
LVS Done.
alex@alex-Parallels-Virtual-Platform:~/Desktop/EDA/SAR_IPN/my_lvs/dac$
```

Output during LVS running

```
260 -----
261 261 Netlists do not match.
262
263 263 Subcircuit pins:
264 264 Circuit 1: sw_top |Circuit 2: sw_top
265 -----
266 266 en |en
267 267 vss |vdd **Mismatch**
268 268 vdd |vss **Mismatch**
269 269 in |in
270 270 out |out
271 -----
272 272 Cell pin lists for sw_top and sw_top altered to match.
273 273 Device classes sw_top and sw_top are equivalent.
274
275 275 Final result: Top level cell failed pin matching.
276
```

Output file sw\_top\_final.out

# sw\_top (final) LVS output

./run\_lvs\_sw\_top\_final.sh

```
Open + sw_top_sch_final.spice
Home ~/Desktop/EDA/SAR_IPN/xschem/sar/sw/sw_top.sch

1/** sch_path: /media/psf/Home/EDA/SAR_IPN/xschem/sar/sw/sw_top.sch
2 .subckt sw_top out en vss vdd in
3 *.PININFO out:B en:I vss:B vdd:B in:B
4 x2 vss vss vdd vdd sky130_fd_sc_hd_decap_8
5 x4 en_buf vss vss vdd vdd net1 sky130_fd_sc_hd_inv_4
6 x5 vss vss vdd vdd sky130_fd_sc_hd_decap_3
7 XM1 in net1 out vss sky130_fd_pr_nfet_01v8 L=0.3 W=1 nf=1 m=10
8 XM2 in en_buf out vdd sky130_fd_pr_pfet_01v8 L=0.3 W=1 nf=1 m=10
9 x1 en vss vss vdd en_buf sky130_fd_sc_hd_inv_4
10 .ends
11 .end
```

## Schematic

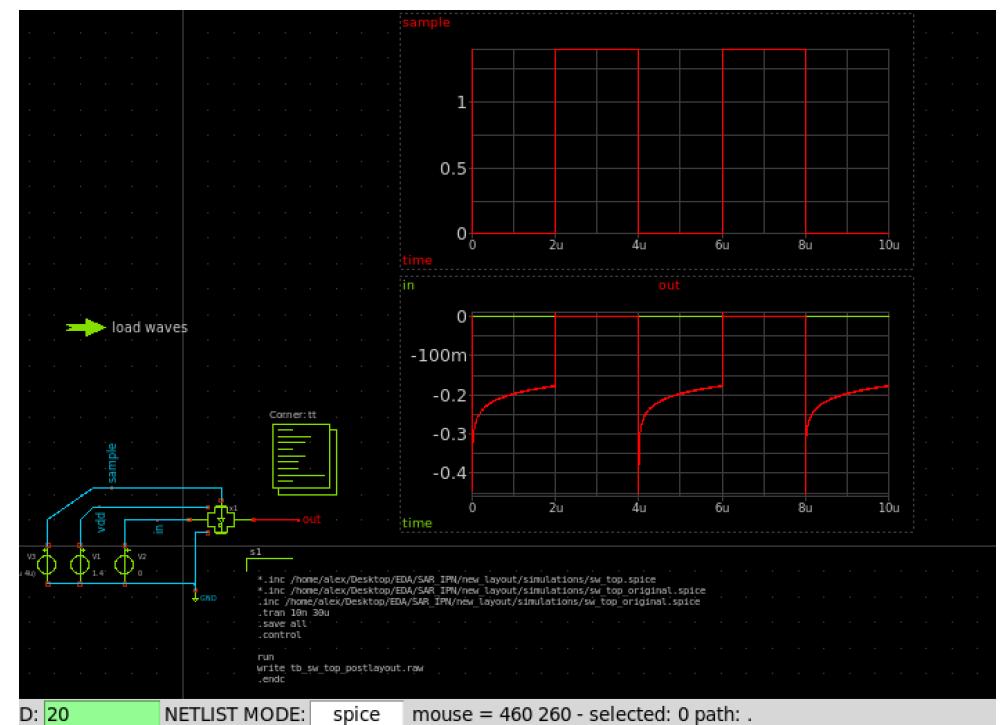
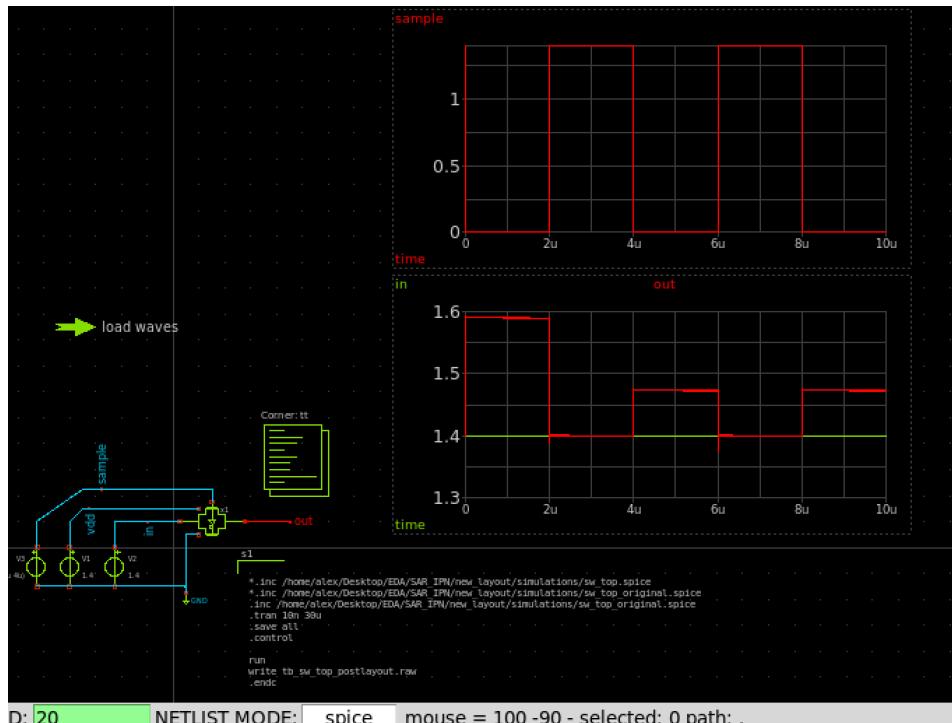
```
Open + sw_top_final_lay.spice
Home ~/Desktop/EDA/SAR_IPN/my_lvs/dac

55 .subckt sky130_fd_sc_hd_decap_8 VEND VNB VPB VPWR
56 X0 VPWR VGND VPWR VPB sky130_fd_pr_pfet_01v8_hvt ad=0.226 pd=2.26 as=0.452 ps=4.52 w=0.87 l=2.89
57 X1 VGND VPWR VGND VNB sky130_fd_pr_nfet_01v8 ad=0.143 pd=1.62 as=0.286 ps=3.24 w=0.55 l=2.89
58 .ends
59 .subckt sky130_fd_pr_nfet_01v8_JJRV6Y a_n501_n131# a_561_n131# a_26_91# a_n383_n131#
60 + a_n328_91# a_n446_91# a_n564_91# a_443_n131# a_n265_n131# a_n619_n131# a_n210_91#
61 + a_n721_n243# a_325_n131# a_n147_n131# a_498_91# a_207_n131# a_144_91# a_262_91#
62 + a_n29_n131# a_380_91# a_n92_91# a_89_n131#
63 X0 a_561_n131# a_498_91# a_443_n131# a_n721_n243# sky130_fd_pr_nfet_01v8 ad=0.29 pd=2.58 as=0.
64 X1 a_n265_n131# a_n328_91# a_n383_n131# a_n721_n243# sky130_fd_pr_nfet_01v8 ad=0.145 pd=1.29 a
65 X2 a_89_n131# a_26_91# a_n29_n131# a_n721_n243# sky130_fd_pr_nfet_01v8 ad=0.145 pd=1.29 as=0.1
66 X3 a_207_n131# a_144_91# a_89_n131# a_n721_n243# sky130_fd_pr_nfet_01v8 ad=0.145 pd=1.29 as=0.
67 X4 a_n501_n131# a_n564_91# a_n619_n131# a_n721_n243# sky130_fd_pr_nfet_01v8 ad=0.145 pd=1.29 a
68 X5 a_n147_n131# a_n210_91# a_n265_n131# a_n721_n243# sky130_fd_pr_nfet_01v8 ad=0.145 pd=1.29 a
69 X6 a_443_n131# a_380_91# a_325_n131# a_n721_n243# sky130_fd_pr_nfet_01v8 ad=0.145 pd=1.29 as=0
70 X7 a_n383_n131# a_n446_91# a_n501_n131# a_n721_n243# sky130_fd_pr_nfet_01v8 ad=0.145 pd=1.29 a
71 X8 a_n29_n131# a_n92_91# a_n147_n131# a_n721_n243# sky130_fd_pr_nfet_01v8 ad=0.145 pd=1.29 as=0
72 X9 a_325_n131# a_262_91# a_207_n131# a_n721_n243# sky130_fd_pr_nfet_01v8 ad=0.145 pd=1.29 as=0
73 .ends
74
75 .subckt sw_top out en vss vdd in
76 Xsky130_fd_pr_pfet_01v8_VVAZD4_0 in out en_buf in in en_buf en_buf vdd out out en_buf
77 + in en_buf in in en_buf en_buf out en_buf out en_buf en_buf sky130_fd_pr_pfet_01v8_VVAZD4
78 Xsky130_fd_sc_hd_decap_3_0 vss vss vdd sky130_fd_sc_hd_decap_3
79 Xsky130_fd_sc_hd_inv_4_0 en_buf vss vss vdd vdd net1 sky130_fd_sc_hd_inv_4
80 Xsky130_fd_sc_hd_inv_4_1 en vss vss vdd vdd en_buf sky130_fd_sc_hd_inv_4
81 Xsky130_fd_sc_hd_decap_8_0 vss vss vdd vdd sky130_fd_sc_hd_decap_8
82 Xsky130_fd_pr_nfet_01v8_JJRV6Y_0 out in net1 in net1 net1 net1 out out in net1 vss
83 + in in net1 out net1 net1 out net1 net1 in sky130_fd_pr_nfet_01v8_JJRV6Y
84 .ends
85
```

## Layout

# Post Layout simulation of sw\_top final

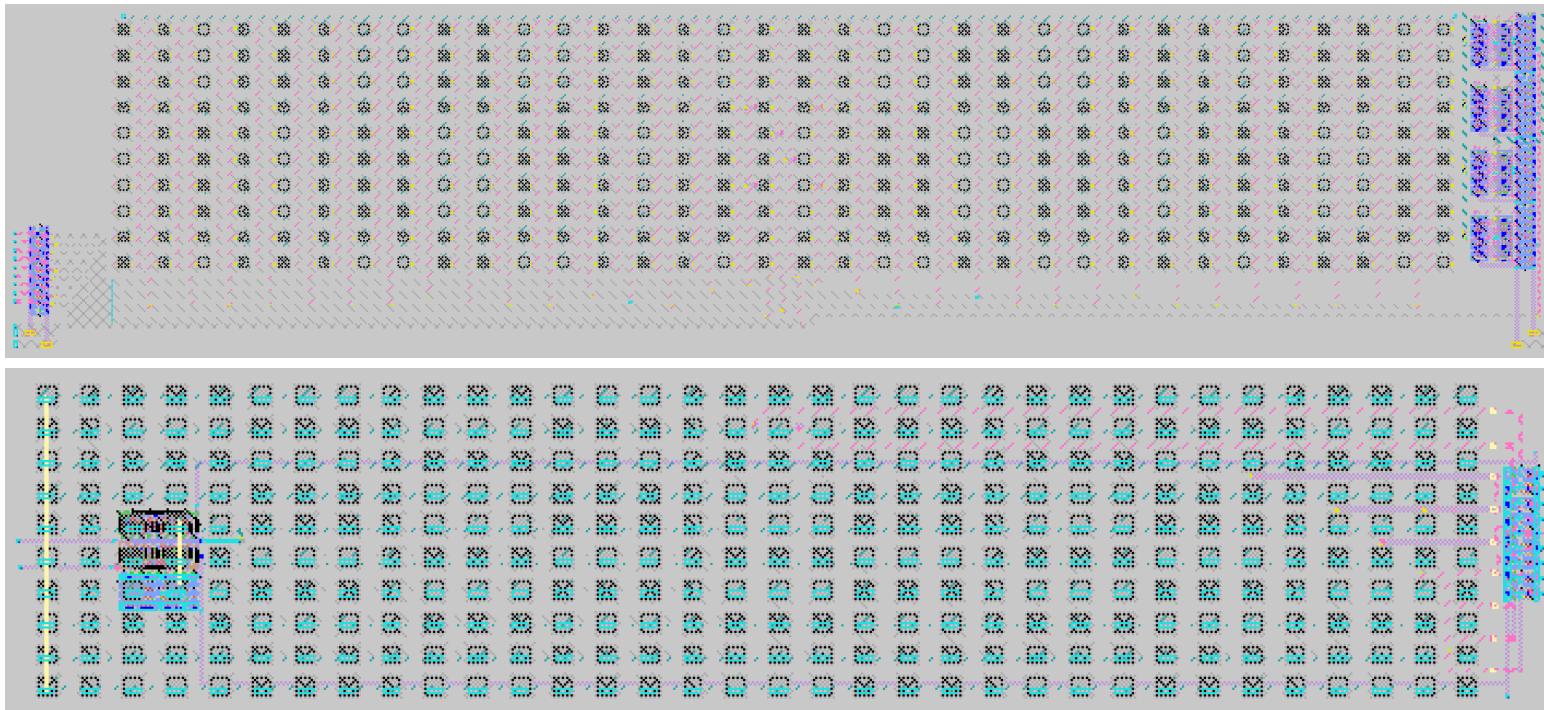
Redrawn layout with two inverters, behaves as expected



$$V_{in} = 1.4V$$

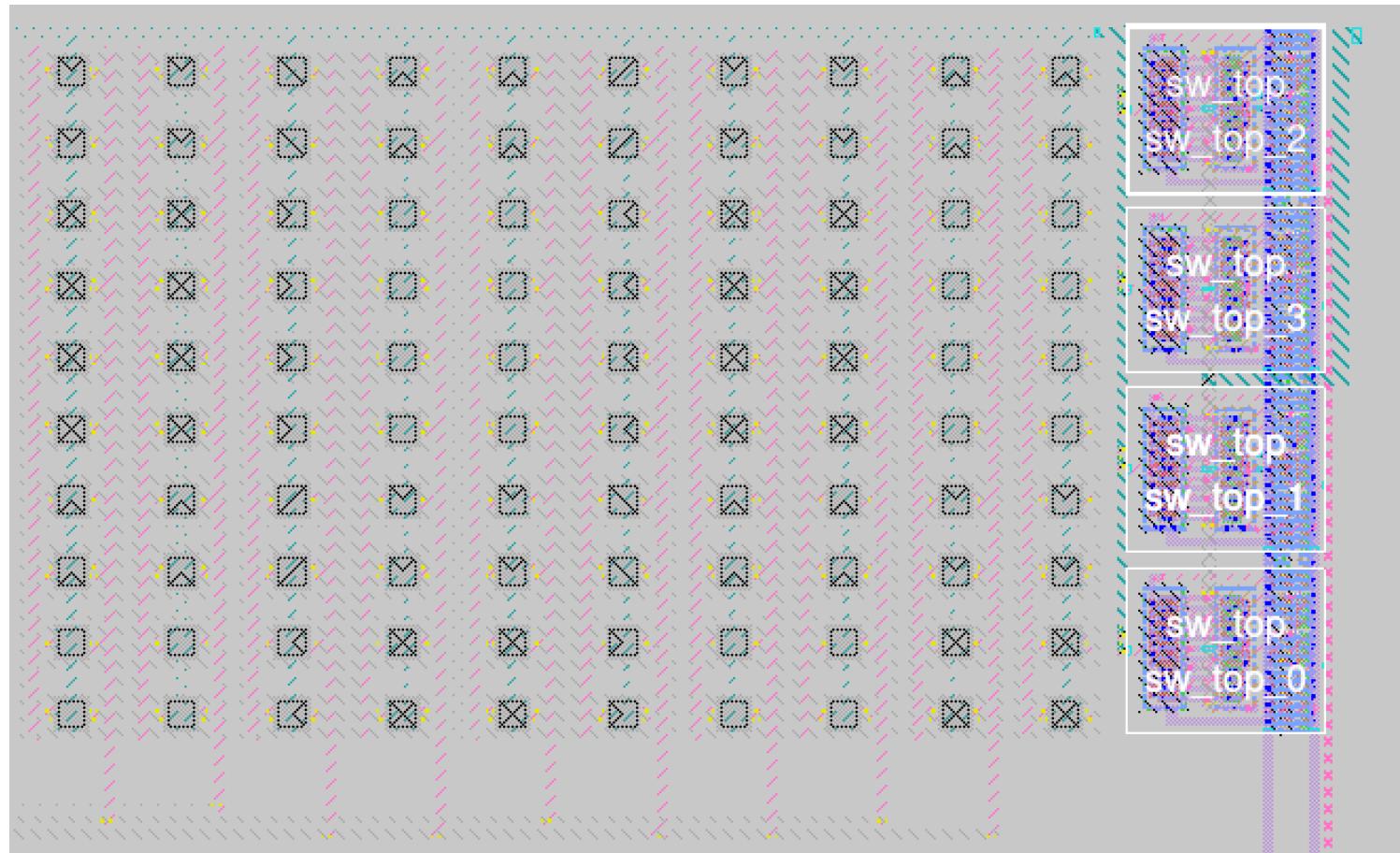
$$V_{in} = 0V$$

# DAC redrawn, there are some differences

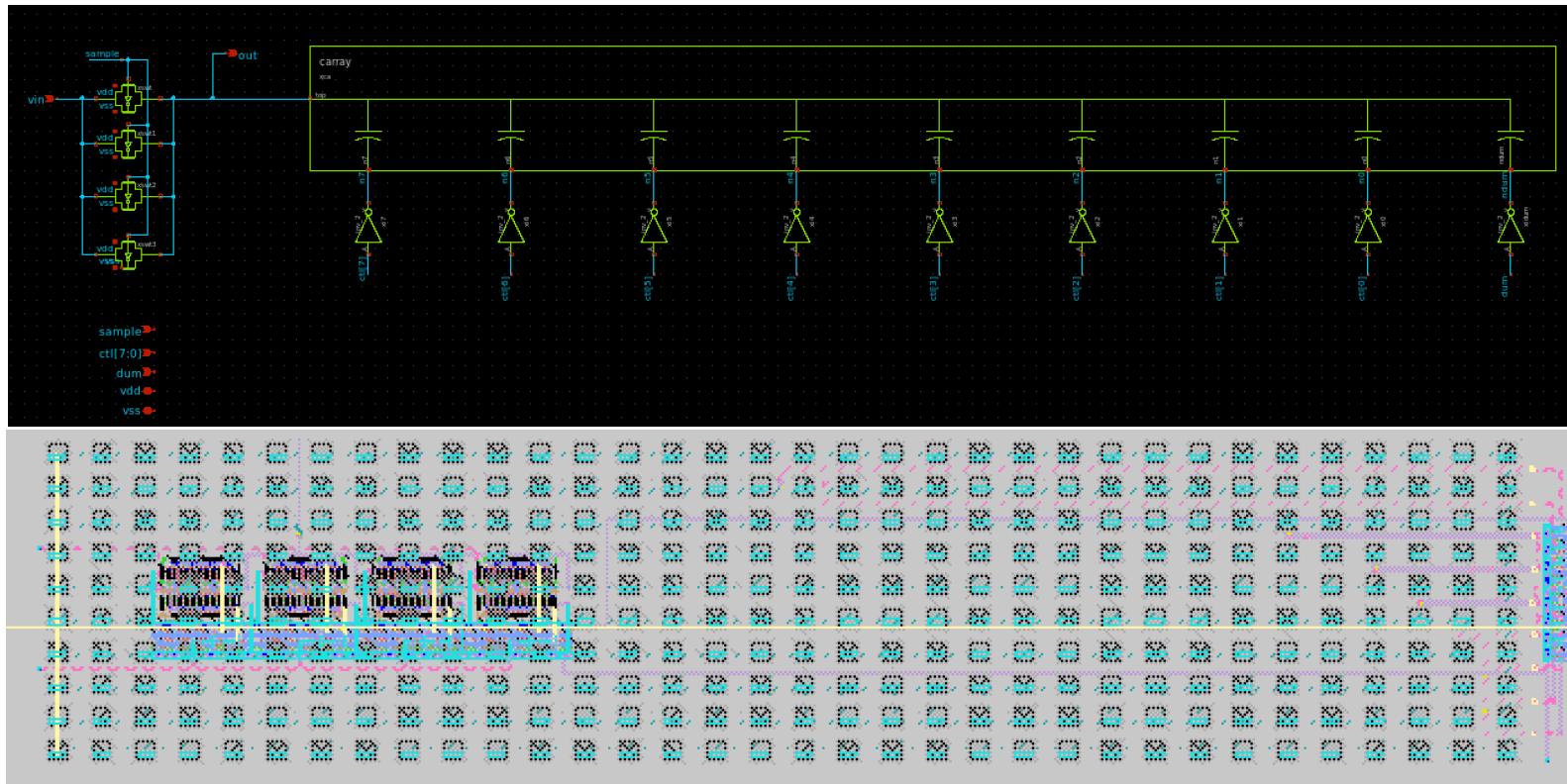


- Original Layout has 4 sw\_top in parallel (Why?)
- Redrawn Layout only has one switch
  - The sw\_top is drawn under the capacitor array to save space

# Original DAC with 4 sw\_top in parallel



# Redrawing schematic and layout with 4 sw\_top in parallel



# Redrawn DAC LVS output

```
● ○ ● alejandrojuarezlora — alex@alex-Parallels-Virtual-Platform: ~/Desktop/EDA/SAR_IPN/my_lvs/dac$ lvs -o dev,inst,dvname
Circuit dac contains 28 device instances.
Class: sky130_fd_pr_nfet_01v8 instances: 4
Class: carray instances: 1
Class: sky130_fd_sc_hd_inv_2 instances: 9
Class: sky130_fd_sc_hd_inv_4 instances: 8
Class: sky130_fd_sc_hd_decap_3 instances: 1
Class: sky130_fd_sc_hd_decap_8 instances: 1
Class: sky130_fd_pr_pfet_01v8 instances: 4
Circuit contains 166 nets.
Contents of circuit 2: Circuit: 'dac'
Circuit dac contains 28 device instances.
Class: sky130_fd_pr_nfet_01v8 instances: 4
Class: carray instances: 1
Class: sky130_fd_sc_hd_inv_2 instances: 9
Class: sky130_fd_sc_hd_inv_4 instances: 8
Class: sky130_fd_sc_hd_decap_3 instances: 1
Class: sky130_fd_sc_hd_decap_8 instances: 1
Class: sky130_fd_pr_pfet_01v8 instances: 4
Circuit contains 165 nets.

Circuit 1 contains 28 devices, Circuit 2 contains 28 devices.
Circuit 1 contains 142 nets,    Circuit 2 contains 141 nets. *** MISMATCH ***

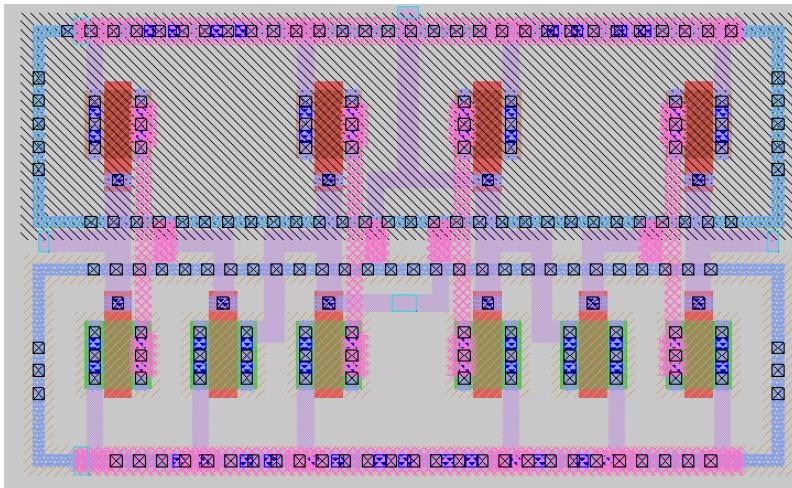
Final result:
Netlists do not match.
Logging to file "dac.out" disabled
LVS Done.
alex@alex-Parallels-Virtual-Platform:~/Desktop/EDA/SAR_IPN/my_lvs/dac$
```

# **SAR-ADC**

## **Activity Report**

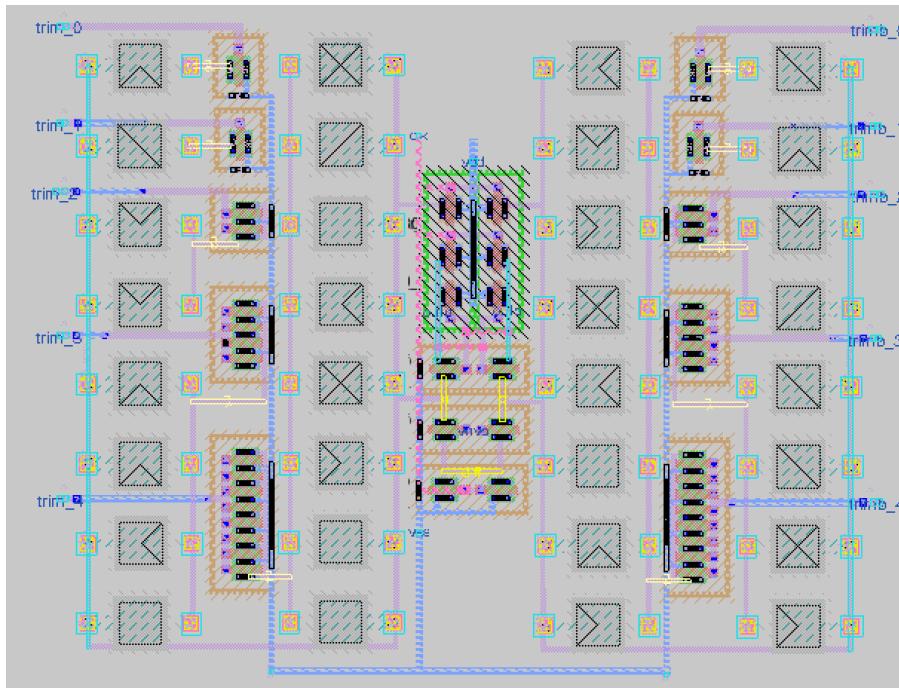
**Alejandro Juárez Lora, Oct 20, 2023**

# LVS so far...latch



```
Subcircuit summary:  
Circuit 1: latch  
-----  
sky130_fd_pr_pfet_01v8_lvt (4)  
sky130_fd_pr_nfet_01v8_lvt (6)  
Number of devices: 10  
Number of nets: 8  
  
Circuit 2: latch  
-----  
sky130_fd_pr_pfet_01v8_lvt (4)  
sky130_fd_pr_nfet_01v8_lvt (6)  
Number of devices: 10  
Number of nets: 8  
  
Resolving symmetries by property value.  
Resolving symmetries by pin name.  
Netlists match uniquely.  
  
Subcircuit pins:  
Circuit 1: latch  
-----  
S Ubicaciones  
R Google Drive - alejandr...  
vss  
vdd Google Drive - jjuarezl...  
Qn Google Drive - jjuarezl...  
Q  
  
Circuit 2: latch  
-----  
IS  
IR  
Ivss  
Ivdd  
IQn  
IQ  
  
Cell pin lists are equivalent.  
Device classes latch and latch are equivalent.  
  
Final result: Circuits match uniquely.  
alex@alex-Parallels-Virtual-Platform:~/Desktop/EDA/SAR_IPN/new_layout/lvs/latch$
```

# LVS so far... Comparator

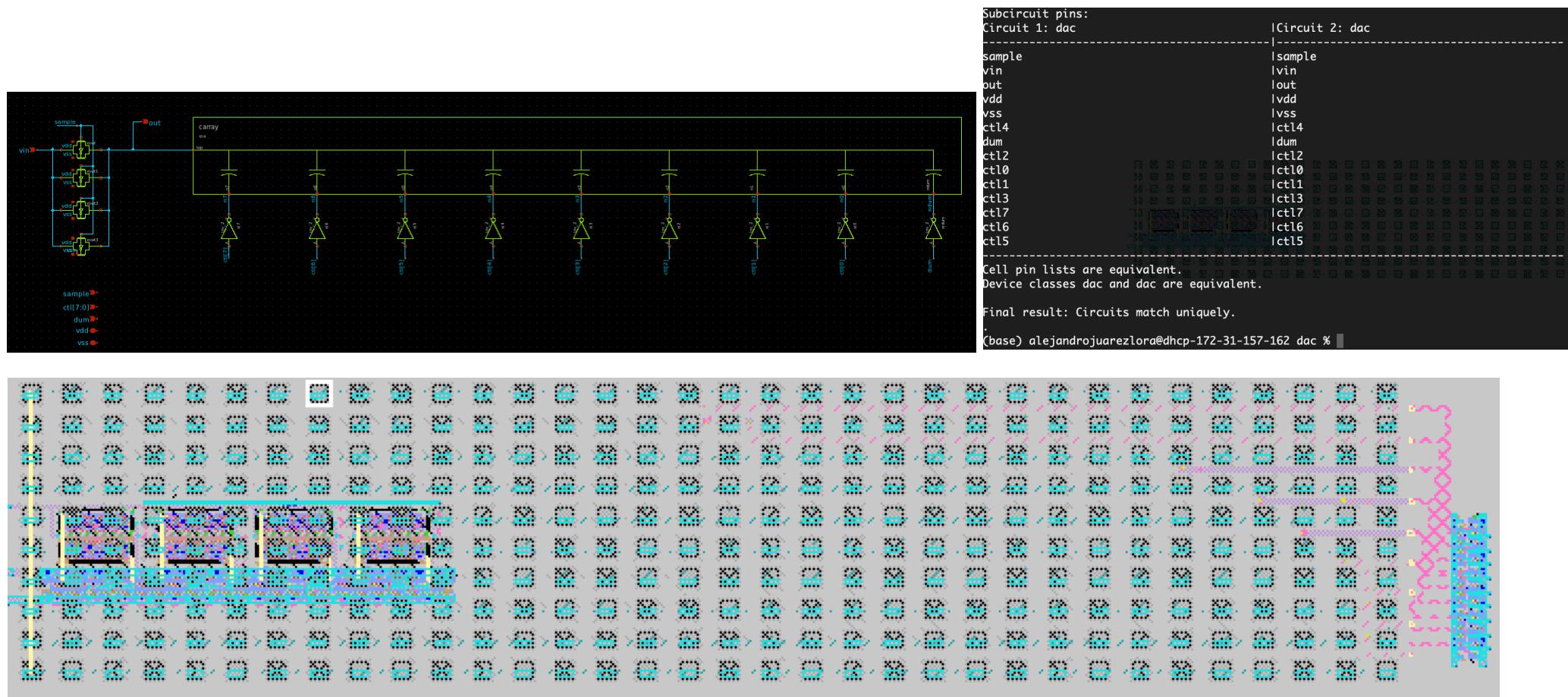


```
Documents
Subcircuit pins:
Circuit 1: comparator
-----
vss alejandrojuarezlora
trim_4_
trimb_4_sica
trim_3_
trimb_3_
trim_2_
trimb_2_Cloud Drive
trim_1_
trimb_1_compartido
trim_0_
trimb_0_
vn bicaciones
vp Google Drive - alejandr...
vdd
clk Google Drive - jjuarezl...
outn
outp

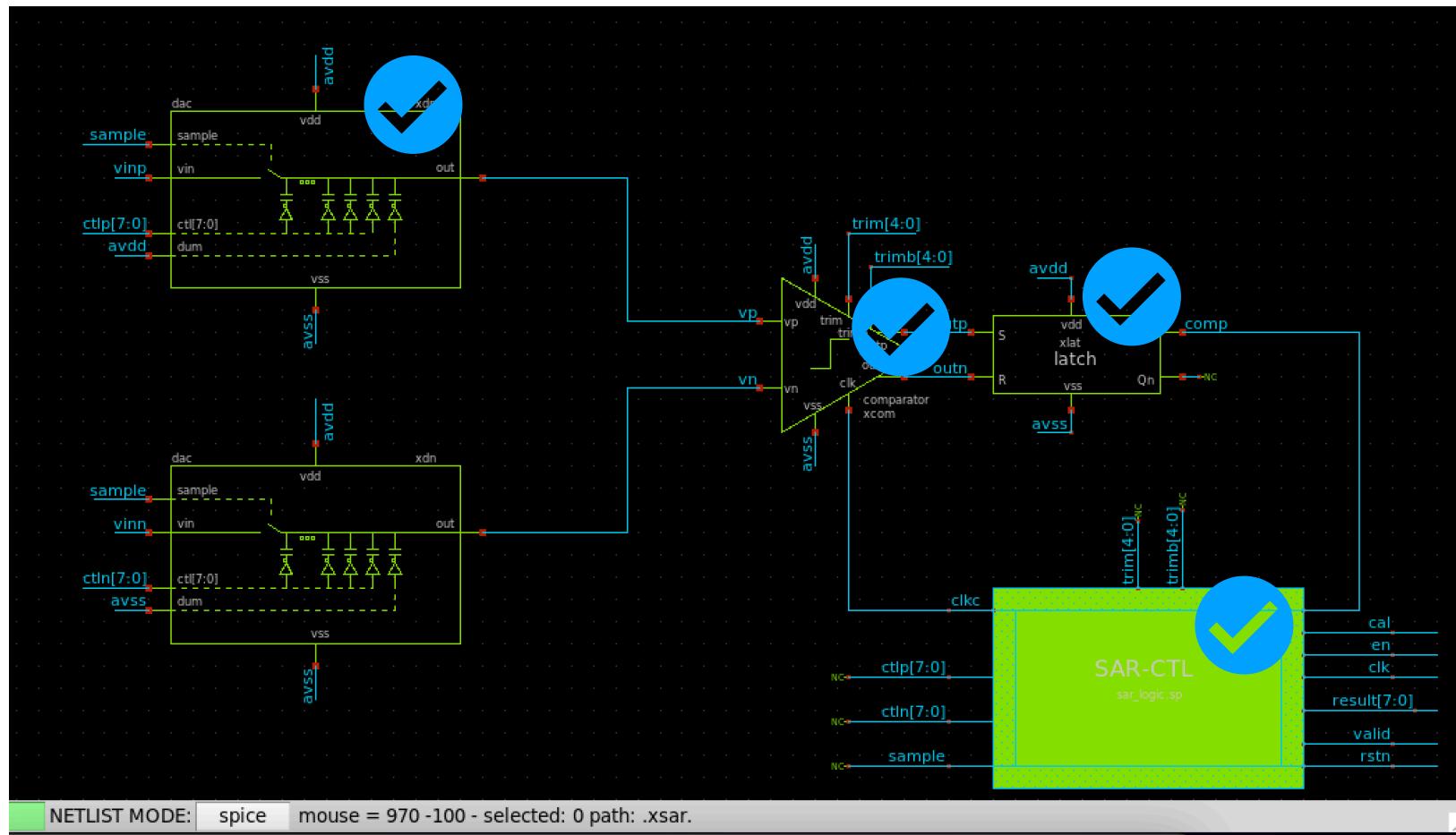
-----
Cell pin lists are equivalent.
Device classes comparator and comparator are equivalent.

Final result: Circuits match uniquely.
.
alex@alex-Parallels-Virtual-Platform:~/Desktop/EDA/SAR_IPN/new_layout/lvs/comparator$
```

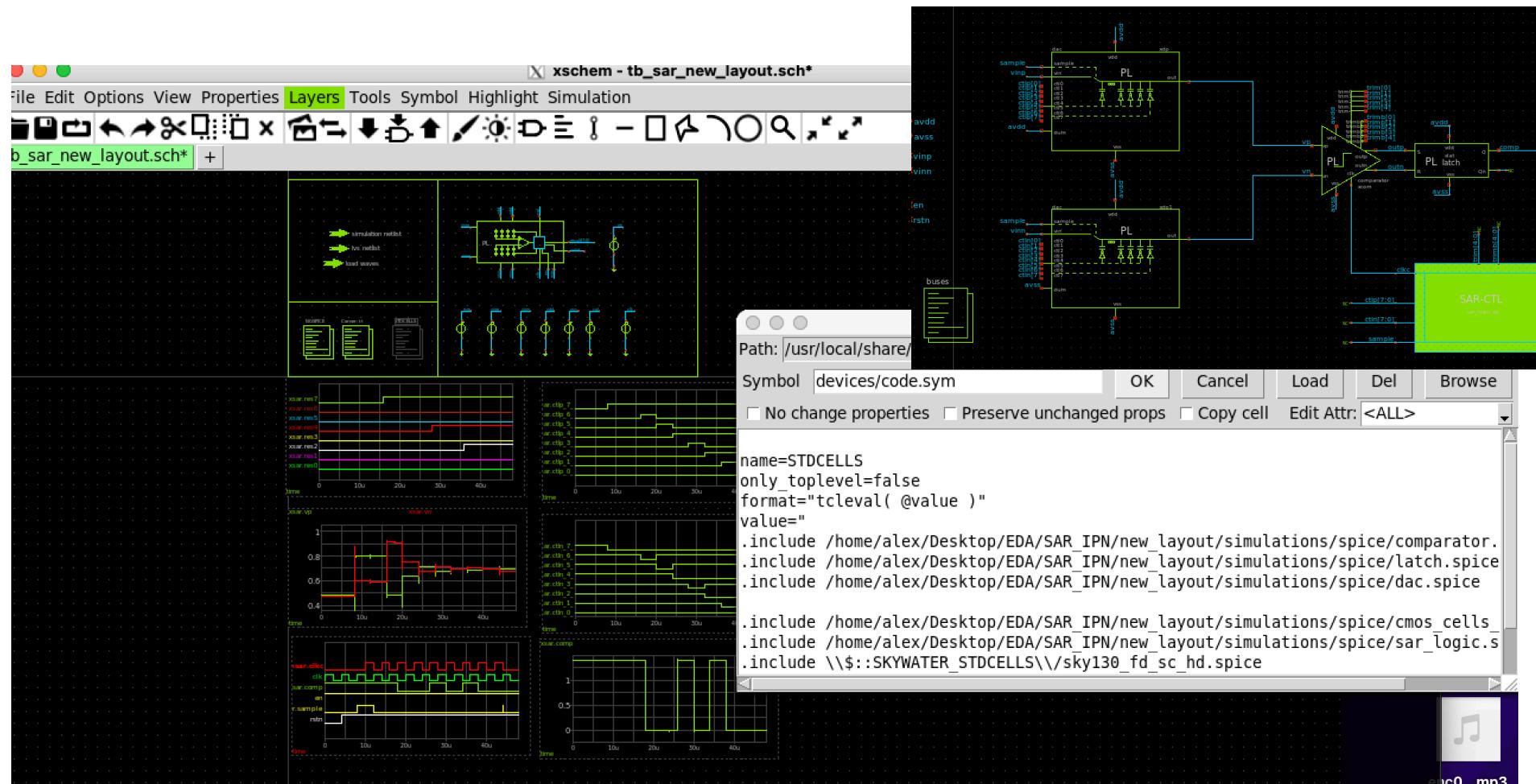
# LVS with 4 sw\_top in parallel



# LVS so far...



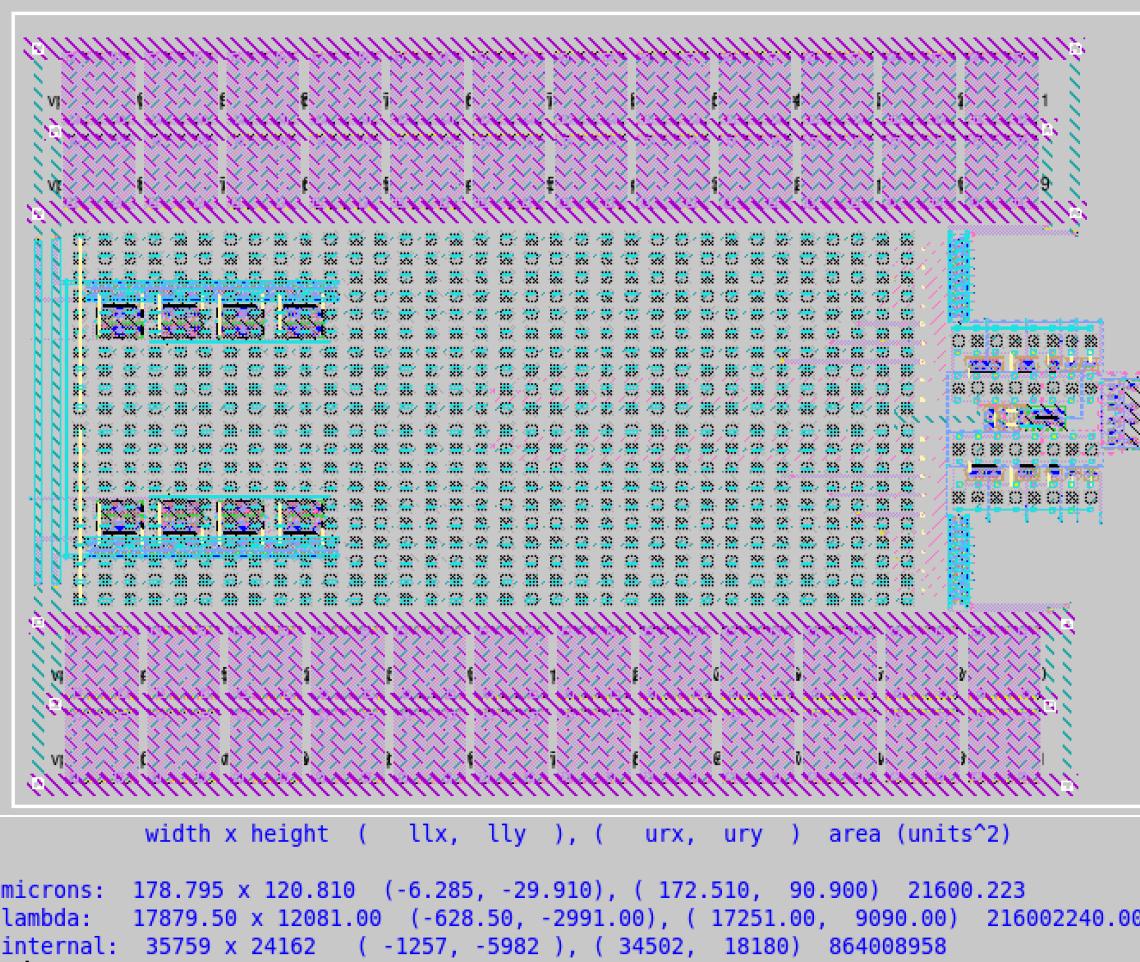
# Post Layout Simulation with new version



# Merging All into a single block

To do:

- Where should ports be located?
- Post layout simulation of the whole device
- Hardening of the macro
  - Set 0,0 x,y coordinates
  - Set dimensions of the block
  - Set several settings for the block to work with open lane

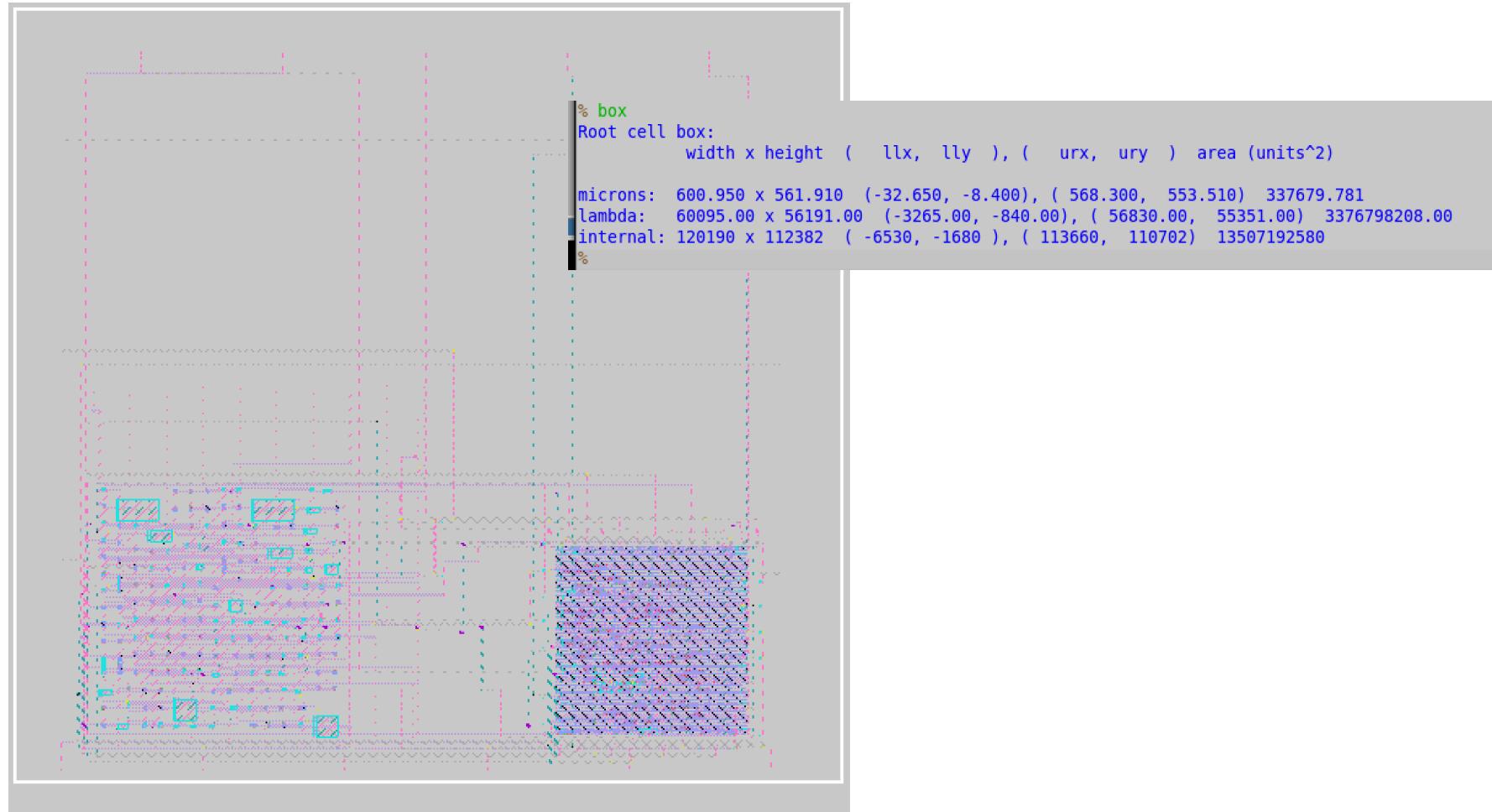


# **SAR-ADC**

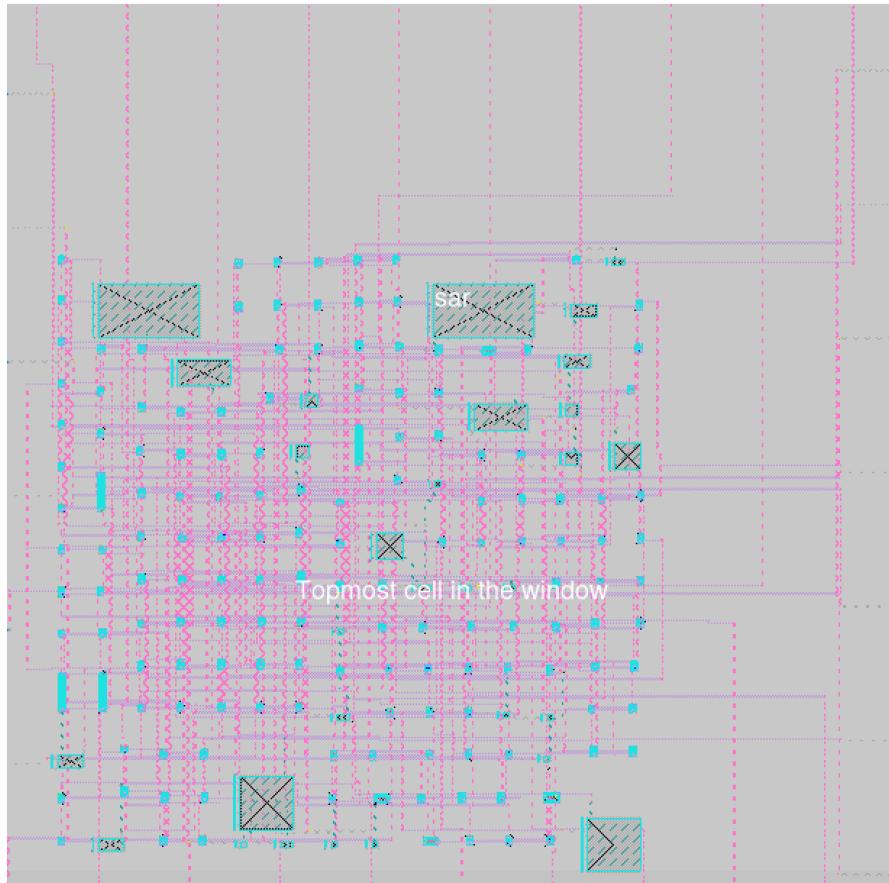
## **Activity Report**

**Alejandro Juárez Lora, Nov 6, 2023**

# Full SAR-ADC, Kevin's layout



# Testing Kevin's layout

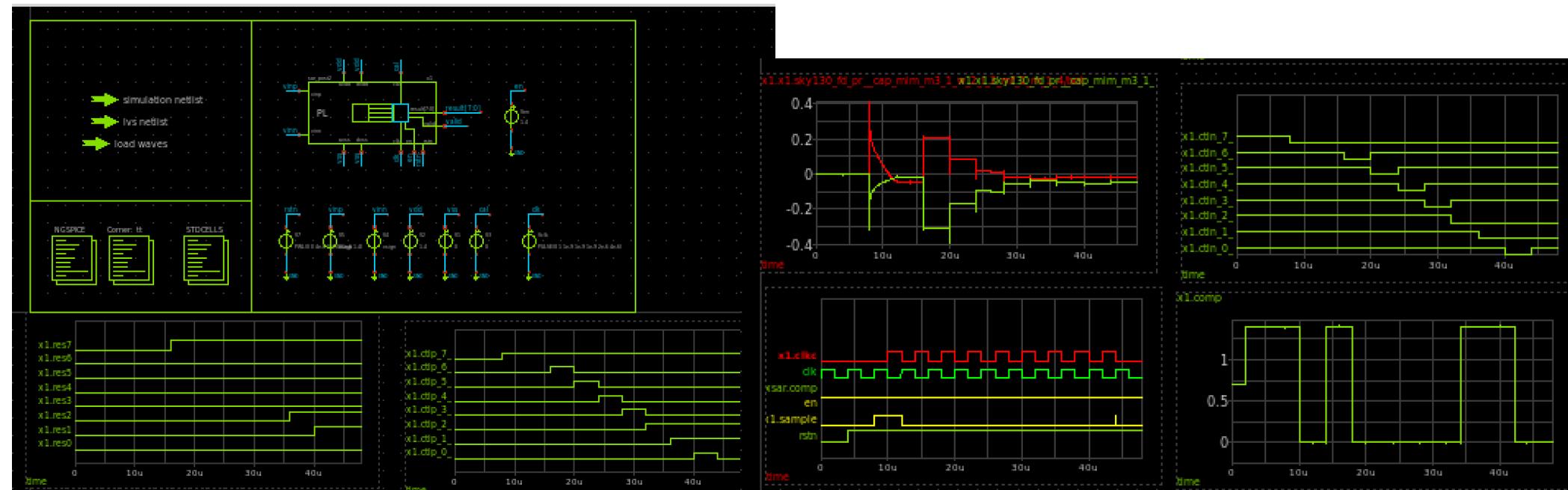


Resulting layout of the analog part

- Post layout simulation
- Space usage
  - What about the blank spaces
  - How smaller can we go

```
% box
Root cell box:
    width x height ( llx, lly ), ( urx, ury ) area (units^2)
microns: 264.000 x 264.000 ( 0.000, 0.000 ), ( 264.000, 264.000 ) 69696.000
lambda: 26400.00 x 26400.00 ( 0.00, 0.00 ), ( 26400.00, 26400.00 ) 696960000.00
internal: 52800 x 52800 ( 0, 0 ), ( 52800, 52800 ) 2787840000
%
```

# Post layout simulation results

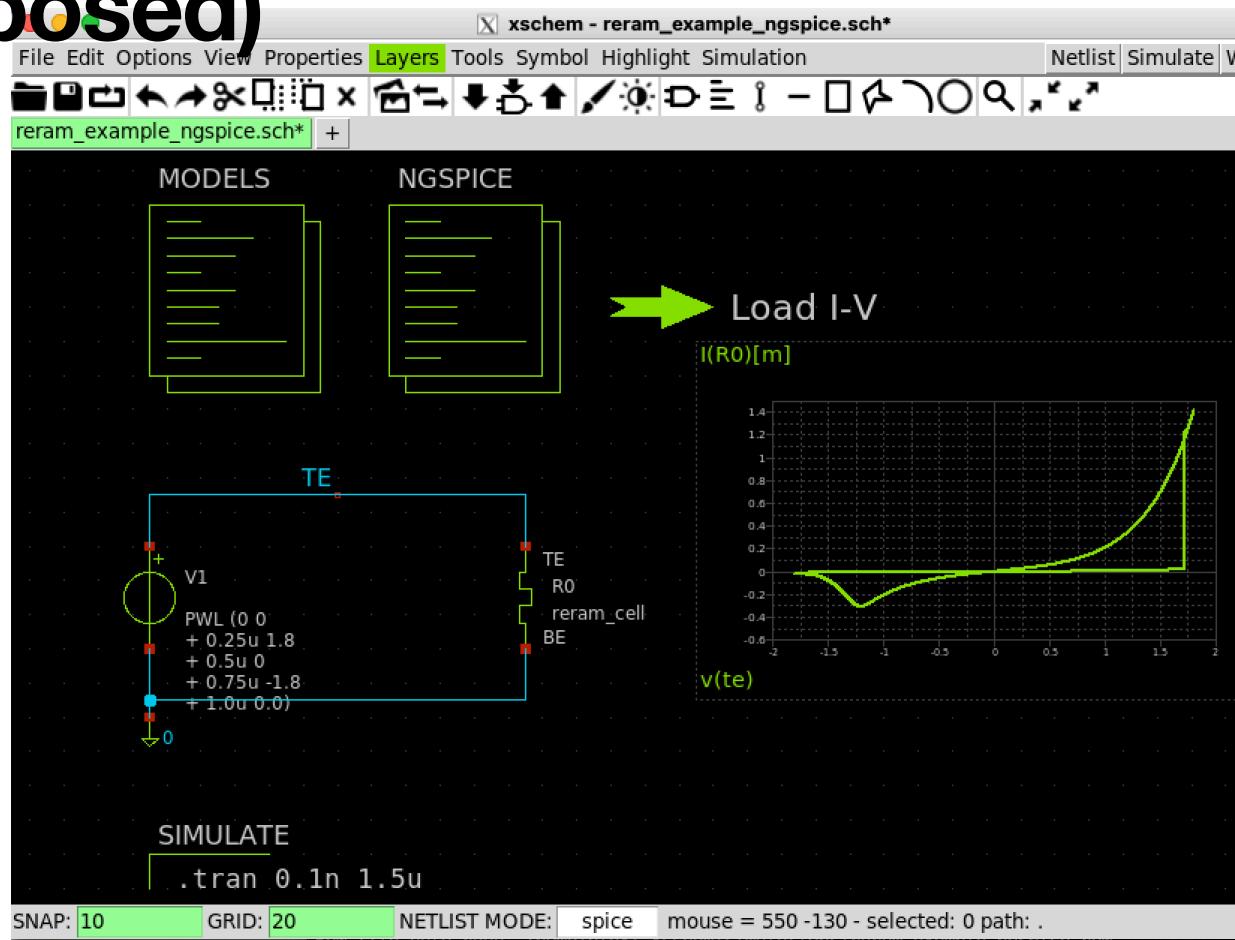


# **Associative Proc.**

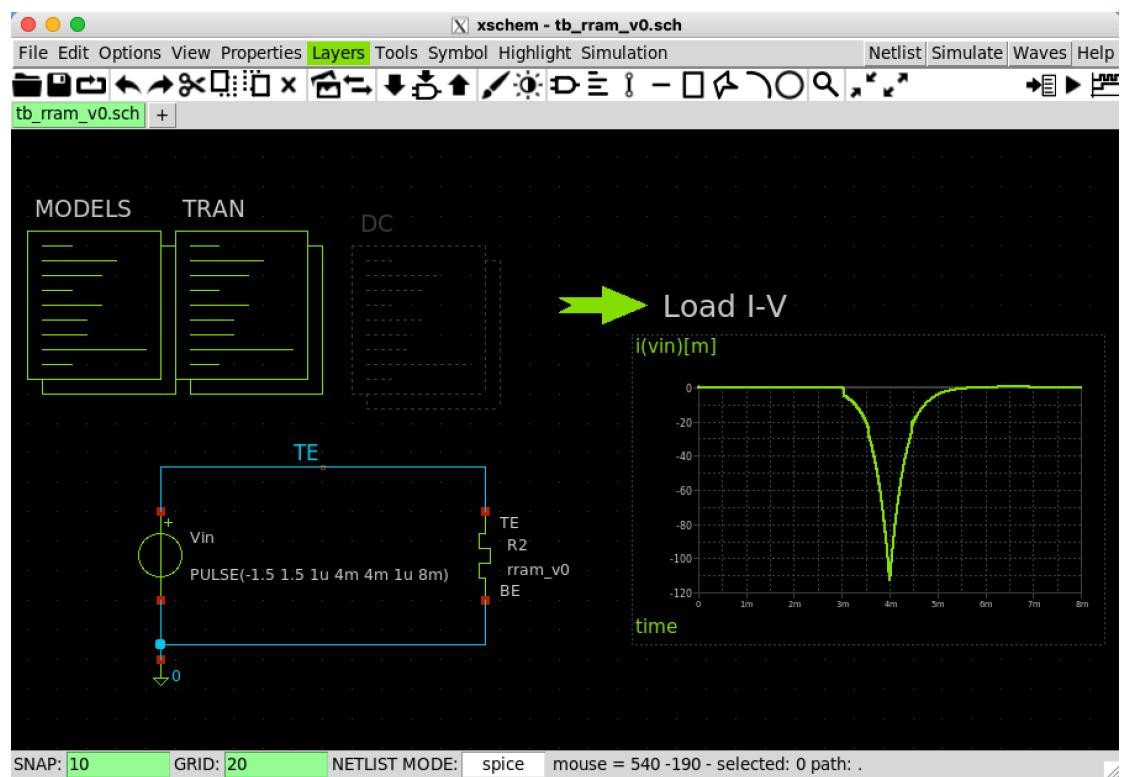
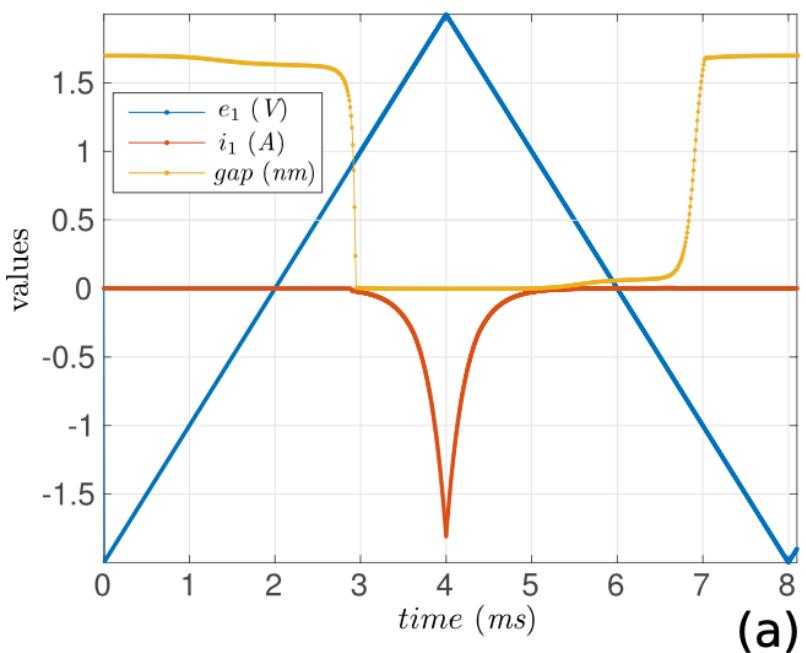
**Activity Report**

**Alejandro Juárez Lora, Nov 13, 2023**

# Stanford original Memristor model (Wellposed)

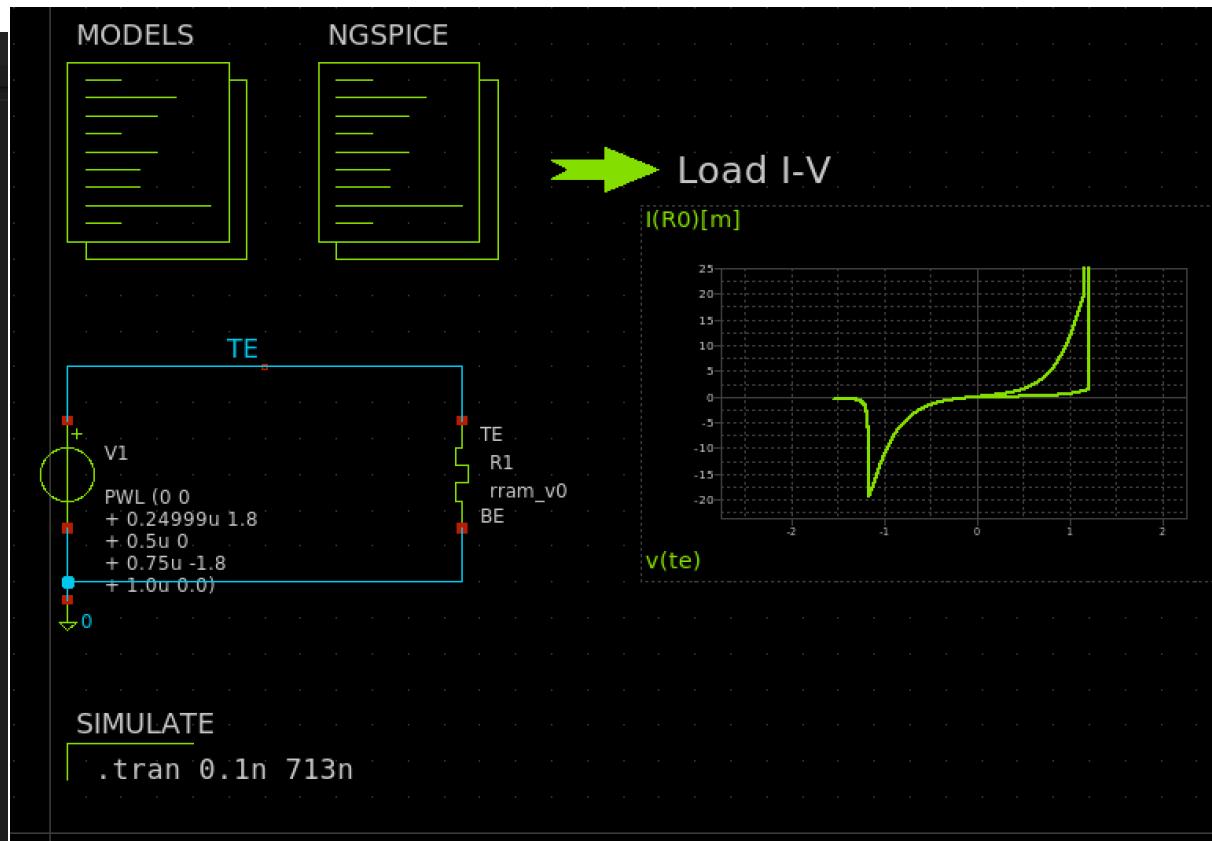


# Memristor model (Wellposed)



# Memristor model (Wellposed)

```
rram_v0.va
Users > alejandrojuarezlora > EDA > SNN_IPN > memristor_models > wellposed > rram_v0.va
1  include "constants.vams"
2  'include "disciplines.vams"
3
4 module rram_v0_va(t, b);
5   inout t, b;
6   electrical t, b, ns;
7   parameter real g0 = 0.25 from (0:inf);
8   parameter real V0 = 0.25 from (0:inf);
9   parameter real Vt0 = 10 from (0:inf);
10  parameter real I0 = 1e-3 from (0:inf);
11  parameter real Beta = 0.8 from (0:inf);
12  parameter real gamma0 = 16 from (0:inf);
13  parameter real Ea = 0.6 from (0:inf);
14  parameter real a0 = 0.25 from (0:inf);
15  parameter real tox = 12 from (0:inf);
16  parameter real maxGap = 1.7 from (0:inf);
17  parameter real minGap = 0.2 from (0:inf);
18  parameter real maxslope = 1e15 from (0:inf);
19  parameter real smoothing = 1e-8 from (0:inf);
20  parameter real GMIN = 1e-12 from (0:inf);
21  parameter real Kclip = 50 from (0:inf);
22  real s, f1, f2, Gap, Gamma, Fw1, Fw2, clip_maxGap, clip_minGap;
23
24 analog function real smoothstep;
25   input x, smoothing;
26   real x, smoothing;
27   begin
28     | smoothstep = 0.5*(x/sqrt(x*x + smoothing)+1);
29   end
30 endfunction // smoothstep
31
32 analog function real safeexp;
33   input x, maxslope;
34   real x, maxslope, breakpoint;
35   begin
36     | breakpoint = log(maxslope);
37     | safeexp = exp(x*(x <= breakpoint)*(x <= breakpoint) + (x>breakpoint)*(maxslope + maxslope*(x-breakpoint));
38   end
39 endfunction
40
41 analog function real safesinh;
42   input x, maxslope;
43   real x, maxslope;
44   begin
45     | safesinh = 0.5*(safeexp(x, maxslope) - safeexp(-x, maxslope));
46
```

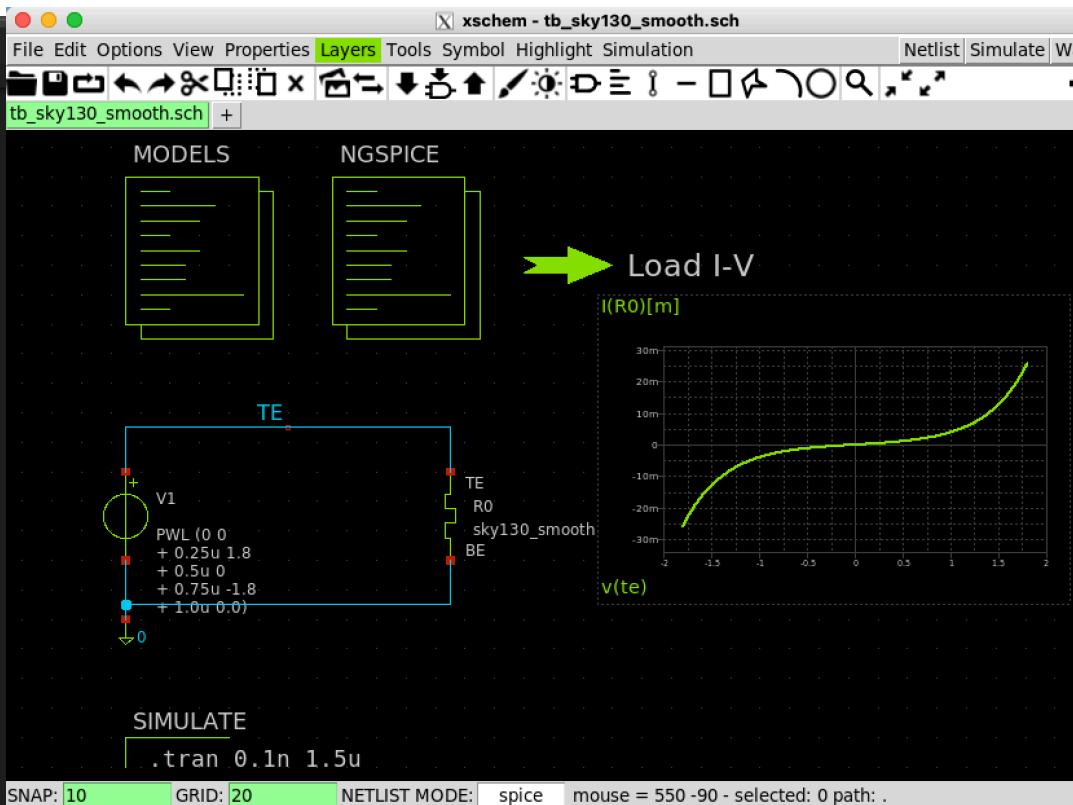


# Adding smooth functions

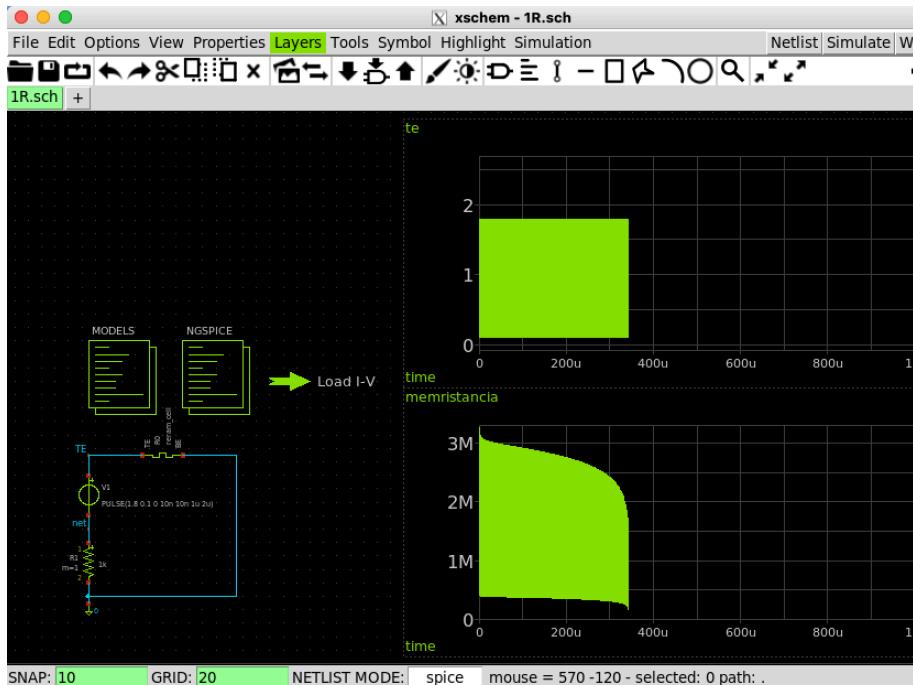
```

sky130_smooth.va x  sky130_smooth.spice
Users > alejandrojuarezlora > EDA > SNN_IPN > memristor_models > sky130_smooth > sky130_smooth.va
70      real t_delta;           // difference between current vs. previous time step
71
72
73
74      analog function real smoothstep;
75          input x, smoothing;
76          real x, smoothing;
77          begin
78              | smoothstep = 0.5*(x/sqrt(x*x + smoothing)+1);
79          end
80      endfunction // smoothstep
81
82      analog function real safeexp;
83          input x, maxslope;
84          real x, maxslope, breakpoint;
85          begin
86              | breakpoint = log(maxslope);
87              | safeexp = exp(x*(x <= breakpoint))*(x <= breakpoint) + (x>breakpoint)*(maxslope + maxslope*(x-breakpoint));
88          end
89      endfunction
90
91      analog function real safesinh;
92          input x, maxslope;
93          real x, maxslope;
94          begin
95              | safesinh = 0.5*(safeexp(x, maxslope) - safeexp(-x, maxslope));
96          end
97      endfunction
98
99      analog function real smoothabs;
100         input x, smoothing;
101         real x, smoothing;
102         begin
103             | smoothabs = sqrt(x*x + smoothing) - sqrt(smoothing);
104         end
105     endfunction // smoothabs
106
107

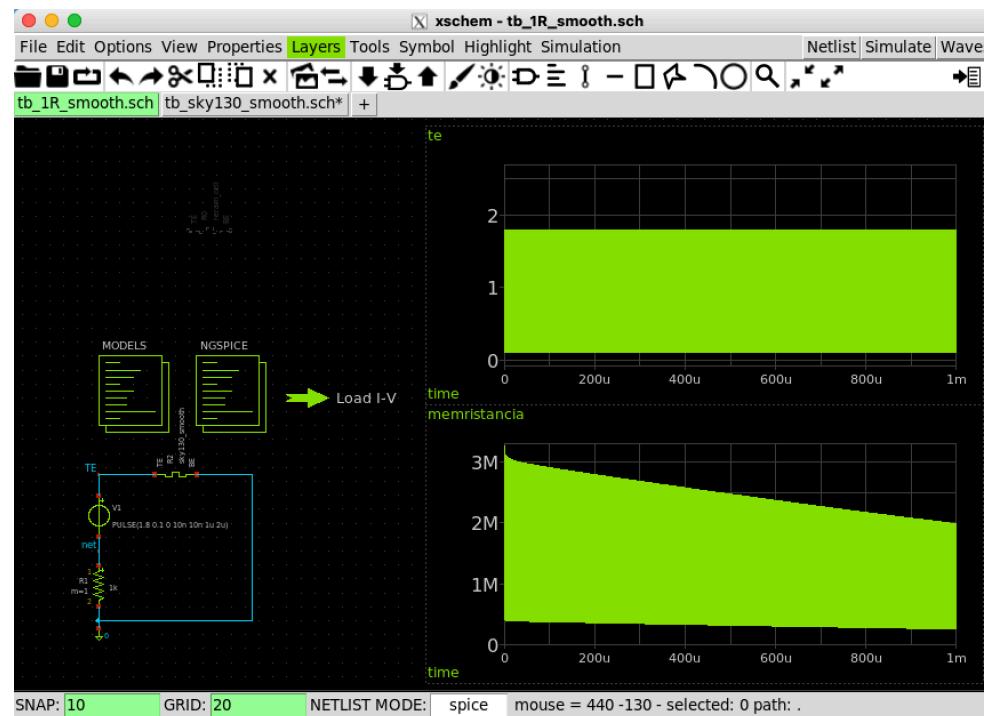
```



# Adding smooth functions and testing on same tb

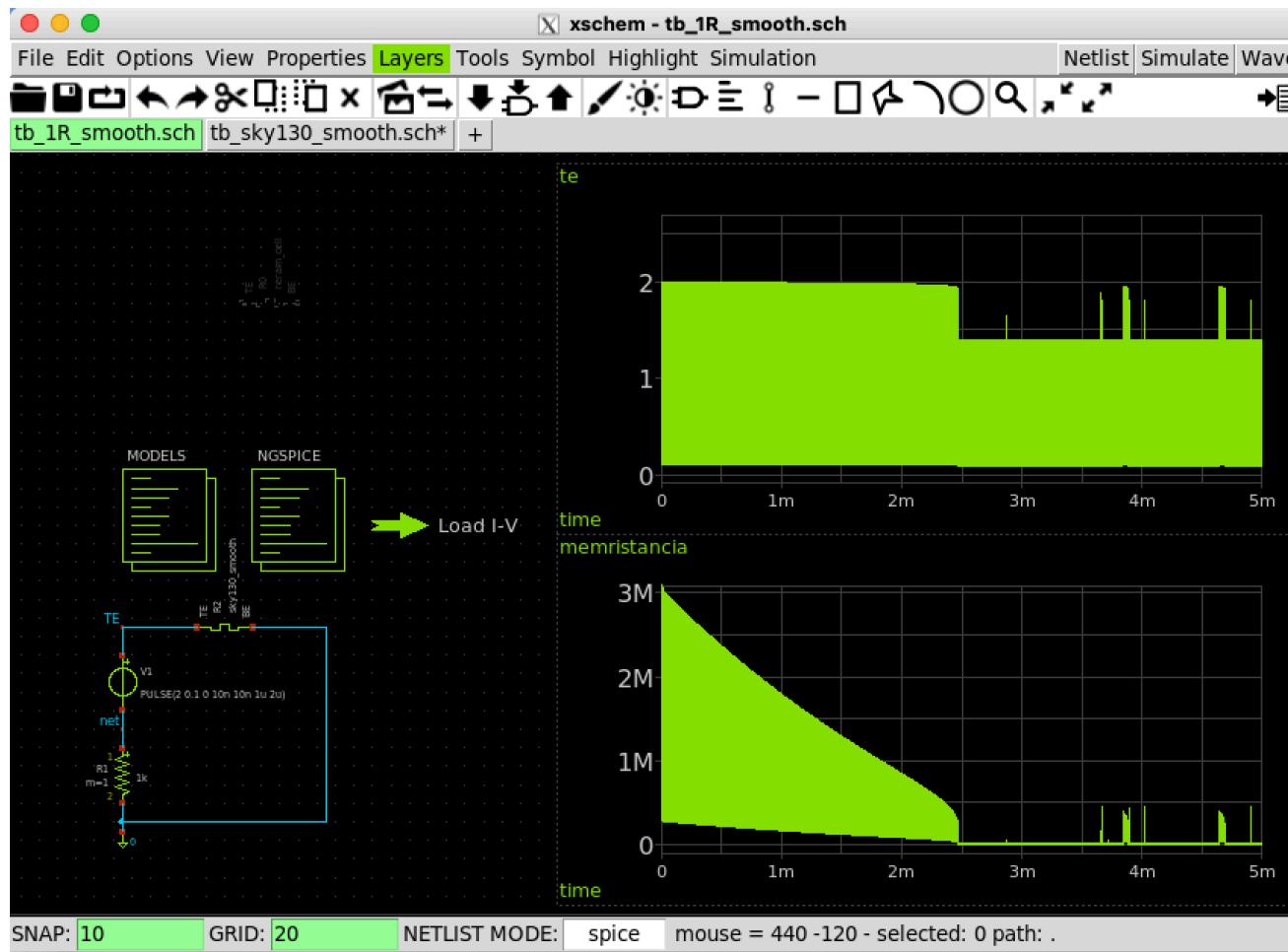


Original no smooth



Adding smoothing fn

# 2V spikes 5ms sim

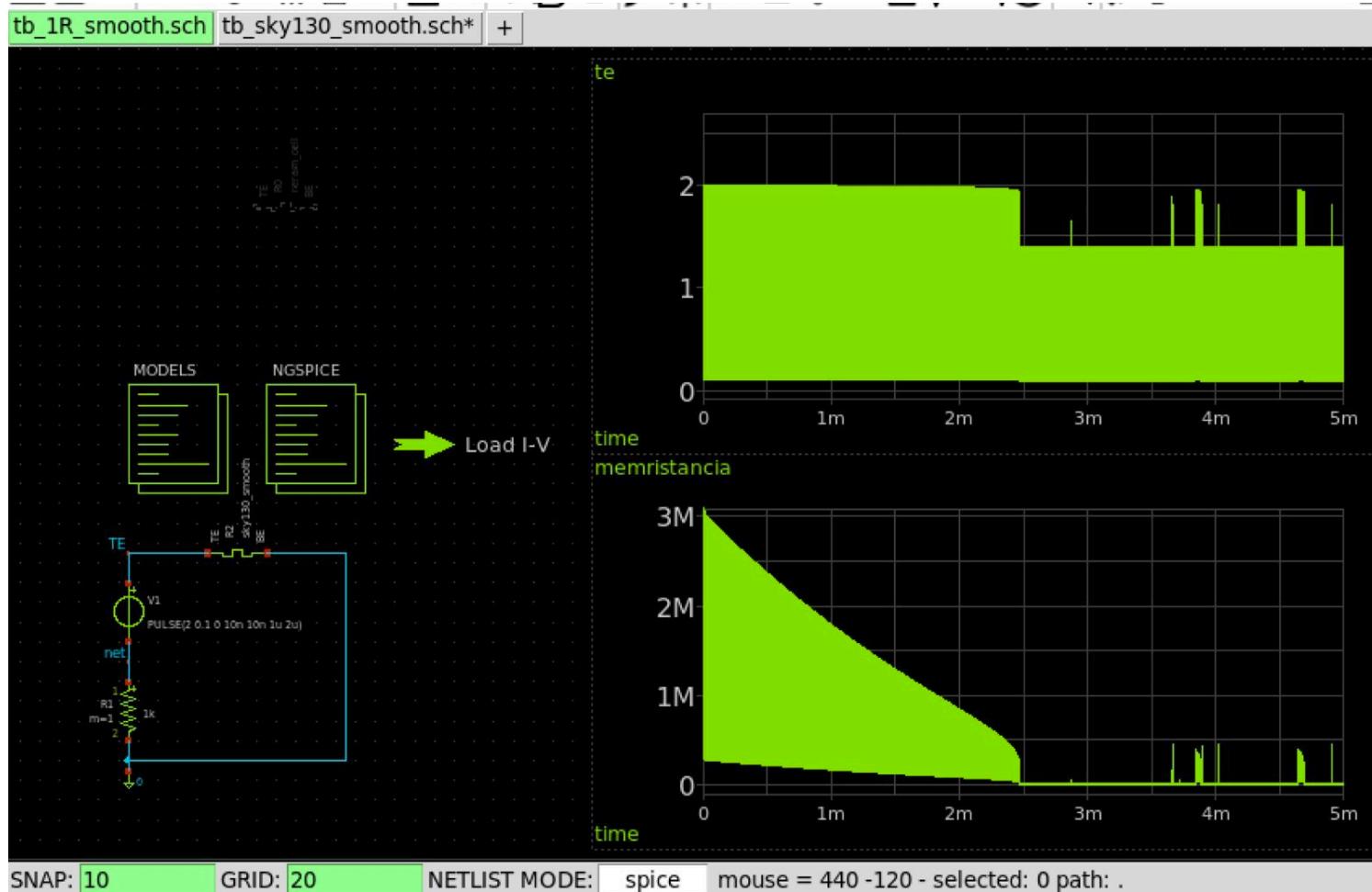


# **Associative Proc.**

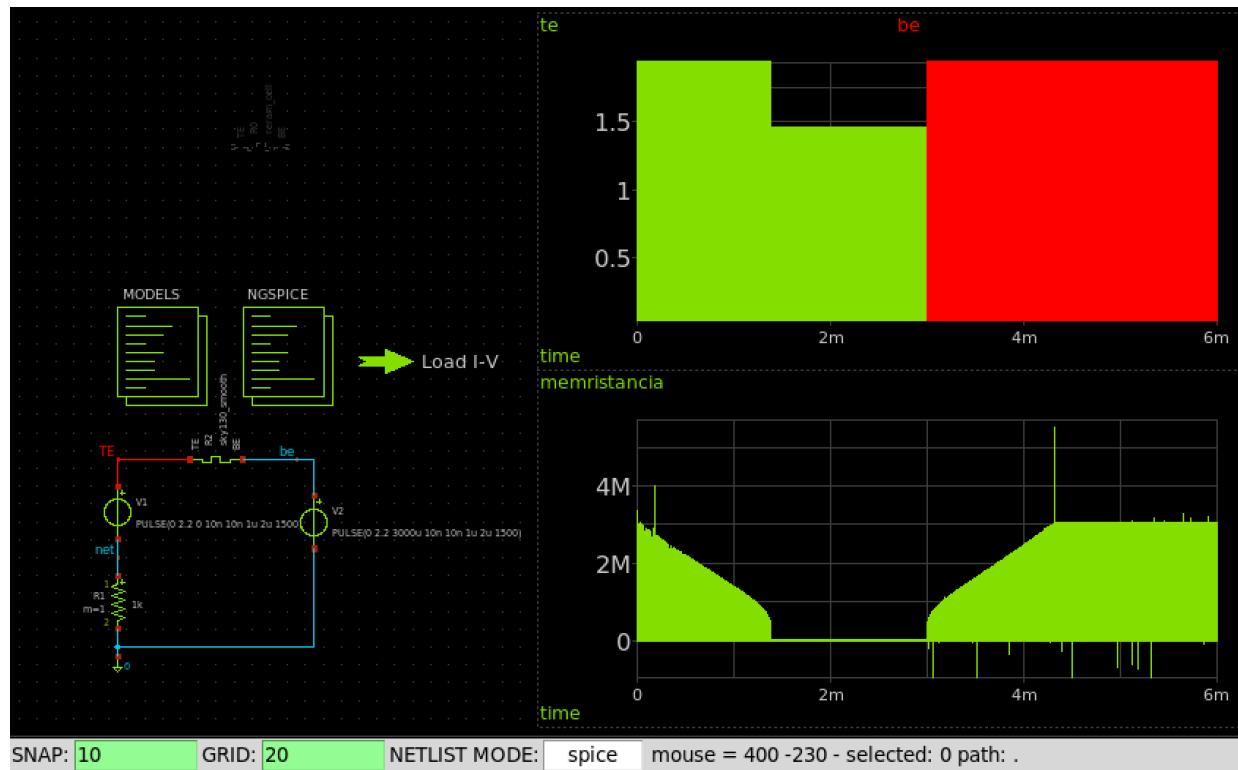
**Activity Report**

**Alejandro Juárez Lora, Nov 20, 2023**

# About the memristor



# sky130\_rram smooth



```

sky130_smooth.va x   rram_v0.spice
sky130_smooth >  sky130_smooth.va

82  analog function real safeexp;
83    input x, maxslope;
84    real x, maxslope, breakpoint;
85    begin
86      breakpoint = log(maxslope);
87      safeexp = exp(x*(x <= breakpoint))*(x <= breakpoint) + (x>breakpo
88    end
89  endfunction

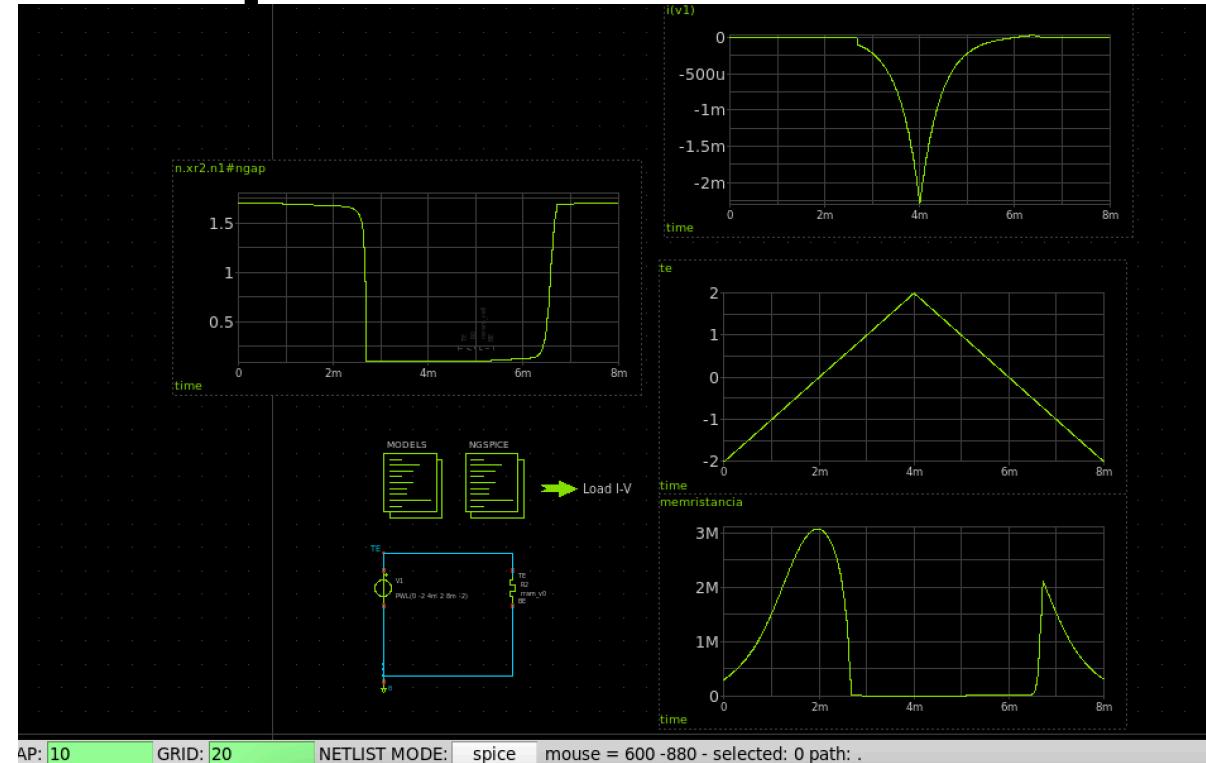
90
91  analog function real safesinh;
92    input x, maxslope;
93    real x, maxslope;
94    begin
95      safesinh = 0.5*(safeexp(x, maxslope) - safeexp(-x, maxslope));
96    end
97  endfunction

98
99  analog function real smoothabs;
100   input x, smoothing;
101   real x, smoothing;
102   begin
103     smoothabs = sqrt(x*x + smoothing) - sqrt(smoothing);
104   end
105 endfunction // smoothabs

106
107 // core equations
108 analog begin
109   $bound_step(t_step); // bound maximum time step
110   Tfilament_current = V(nFilament, BE);
111   Temperature_current = V(nT, BE);
112   gamma = gamma_k0 + gamma_k1 * pow((Tox - Tfilament_current), 3);
113   kT_over_q = (^P_K * Temperature_current) / ^P_Q;
114   Tfilament_dTdt = velocity_k1 * (safeexp(-Eact_generation / kT_over
115                                         -Eact_recombination / kT_over
116                                         -safeexp(-Eact_recombination / kT_over
117                                         Fw1 = smoothstep(Tfilament_min-Tfilament_current, smoothing);
118                                         Fw2 = smoothstep(Tfilament_current-Tfilament_max, smoothing);
119                                         I(nFilament, BE) <+ Tfilament_dTdt + (limexp(Kclip*(Tfilament_min-Tfi
120                                         I(nFilament, BE) <+ ddt(-1.0e-9*Tfilament_current);
121                                         I(TE,BE) <+ I_k1 * safeexp(-(Tox - Tfilament_current)/(Tox - Tfilamen
122                                         I(nT, BE) <+ smoothabs(V(TE,BE)*I(TE,BE), smoothing)/C_thermal + (Tem
123                                         I(nT, BE) <+ ddt(-Temperature_current);
124
125 end
ndmodule

```

# Wellposed model



Doesnt work with impulses

```

sky130_smooth.v
wellposed > rram_v0.va
wellposed > rram_v0.spice

28 analog function real smoothstep;
29   input x, smoothing;
30   real x, smoothing;
31   begin
32     | smoothstep = 0.5*(x/sqrt(x*x + smoothing)+1);
33   end
34 endfunction // smoothstep

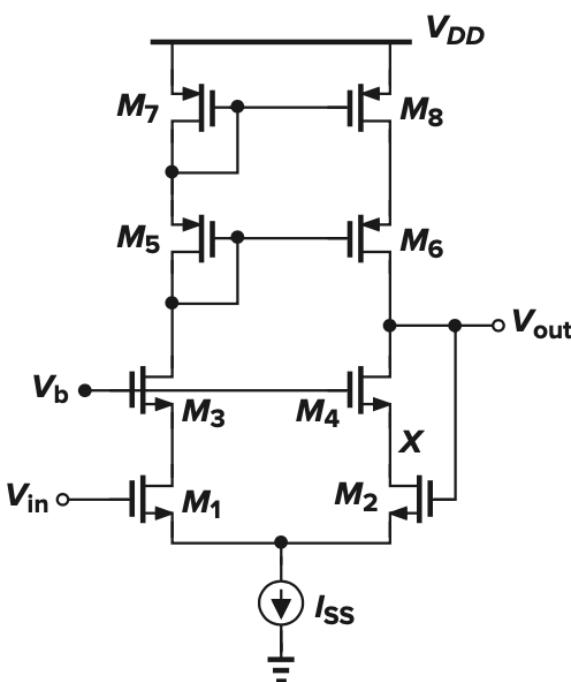
36 analog function real safeexp;
37   input x, maxslope;
38   real x, maxslope, breakpoint;
39   begin
40     | breakpoint = log(maxslope);
41     | safeexp = exp(x*(x <= breakpoint))*(x <= breakpoint) + (x>breakpoi
42   end
43 endfunction

45 analog function real safesinh;
46   input x, maxslope;
47   real x, maxslope;
48   begin
49     | safesinh = 0.5*(safeexp(x, maxslope) - safeexp(-x, maxslope));
50   end
51 endfunction

54 analog begin
55   Gap = V(nGap, b);
56   I(t, b) <- I0 * safeexp(-Gap/g0, maxslope) * safesinh(V(t, b)/V0, maxslo
57   Gamma = gamma0 - Beta0 * pow(Gap, 3);
58   ddt_gap = -Vel0*safeexp(-Ea/$vt, maxslope)*safesinh(V(t, b)*Gamma*a0/tox;
59   Fw1 = smoothstep(minGap-Gap, smoothing);
60   Fw2 = smoothstep(Gap-maxGap, smoothing);
61   clip_minGap = (safeexp(Kclip*(minGap-Gap), maxslope) - ddt_gap) * Fw1;
62   clip_maxGap = (-safeexp(Kclip*(Gap-maxGap), maxslope) - ddt_gap) * Fw2;
63   I(nGap, b) <- ddt_gap + clip_minGap + clip_maxGap;
64   I(nGap, b) <- ddt(-1e-9*Gap);
65 end
66 endmodule
67

```

# Telescope Opamp



Computing  $V_b$  for voltage output swing

-  $M_2$  and  $M_4$  must be in saturation

$$V_b - V_{th4} \leq V_{out} \leq V_x + V_{th2} \quad (1)$$

$$V_x = V_b - V_{gs4} \quad (2)$$

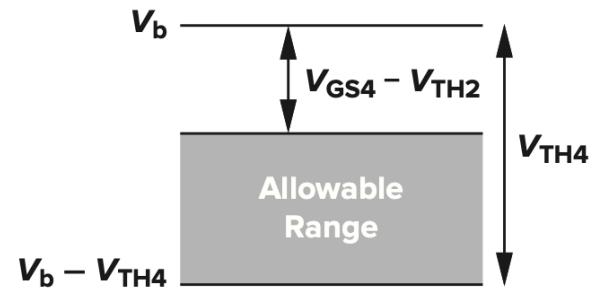
$$V_b - V_{th4} \leq V_{out} \leq V_b - V_{gs4} + V_{th2}$$

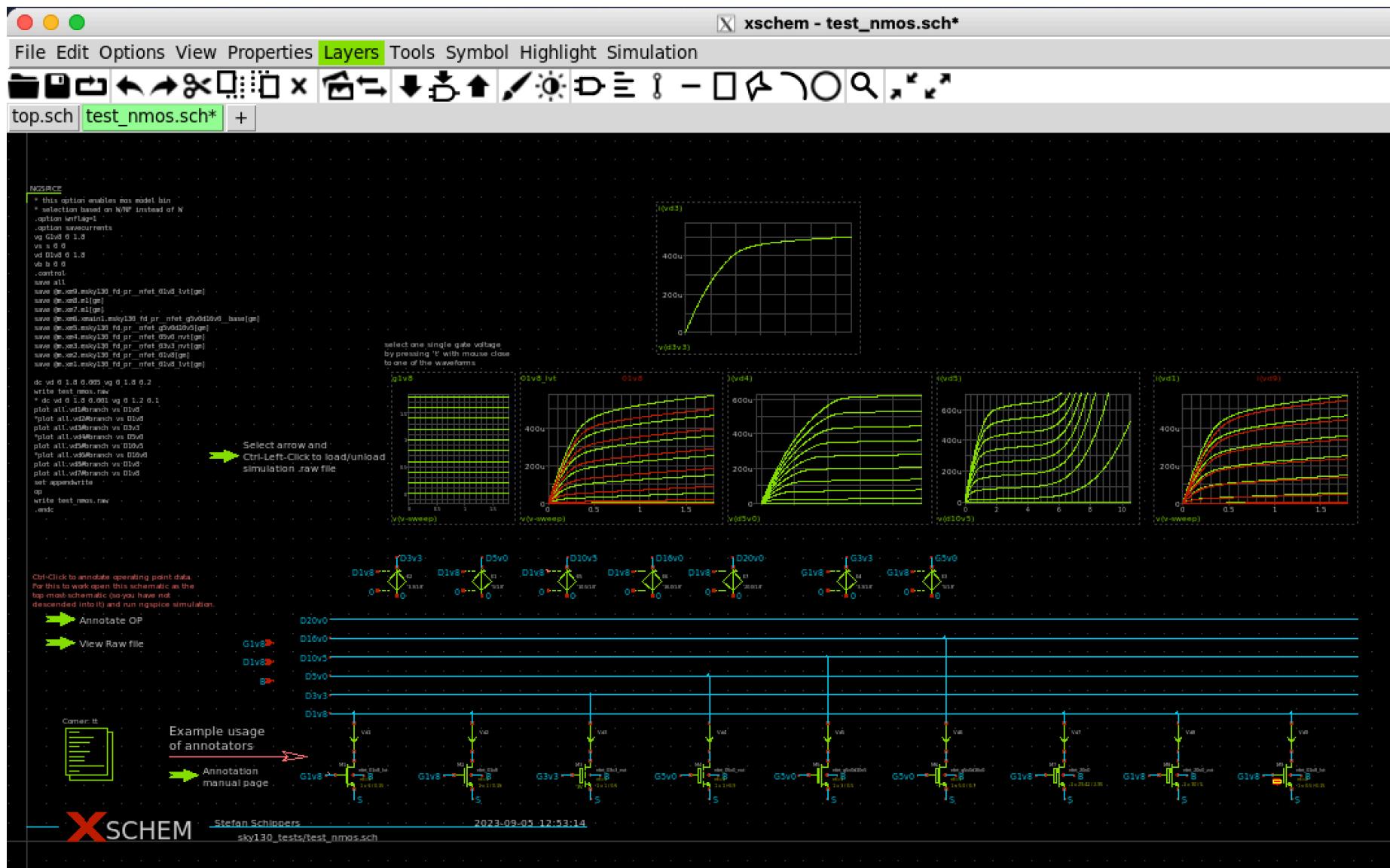
$V_{min}$  (3)                           $V_{max}$  (4)

Therefore

$$V_{max} - V_{min} = V_b - V_{gs4} + V_{th2} - (V_b - V_{th4})$$

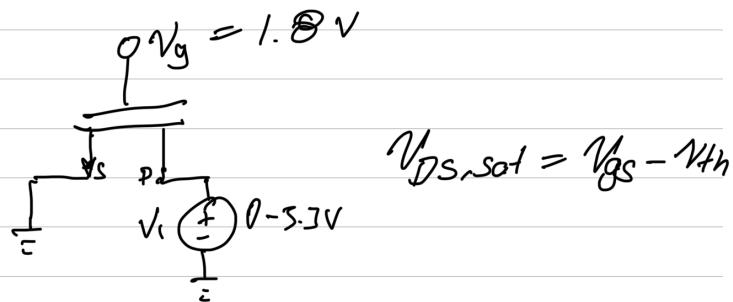
$$V_{max} - V_{min} = V_{th4} - (V_{gs4} - V_{th2}) \quad (5)$$





# Threshold voltage for sky130 is a problem!

For sky130\_nfet\_03v3\_nvt

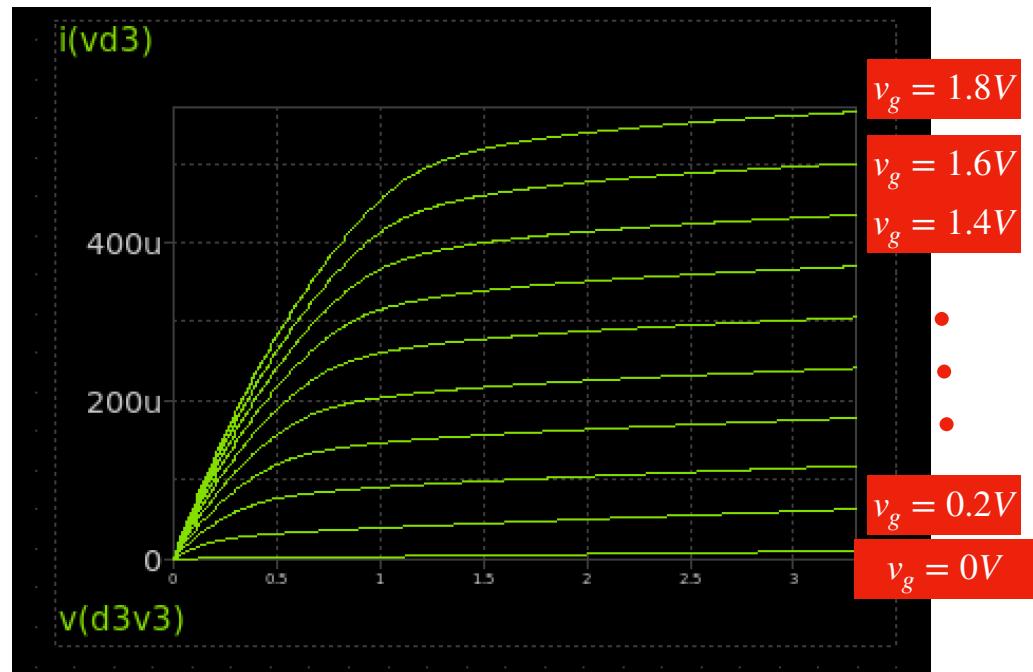


$$1.2V = 1.8V - V_{th}$$

$$\therefore V_{th} \approx 0.6$$

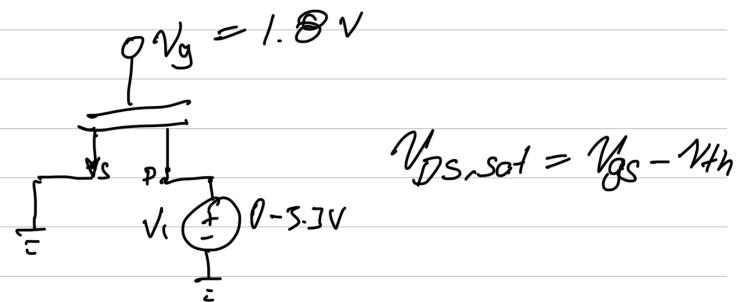
Operating Voltages where SPICE models are valid for `sky130_fd_pr_nfet_03v3_nvt`

- $V_{DS} = 0$  to 3.3V
- $V_{GS} = 0$  to 3.3V
- $V_{BS} = 0$  to -3.3V



# Larger transistors also does not help!

For sky130\_nfet\_05v0



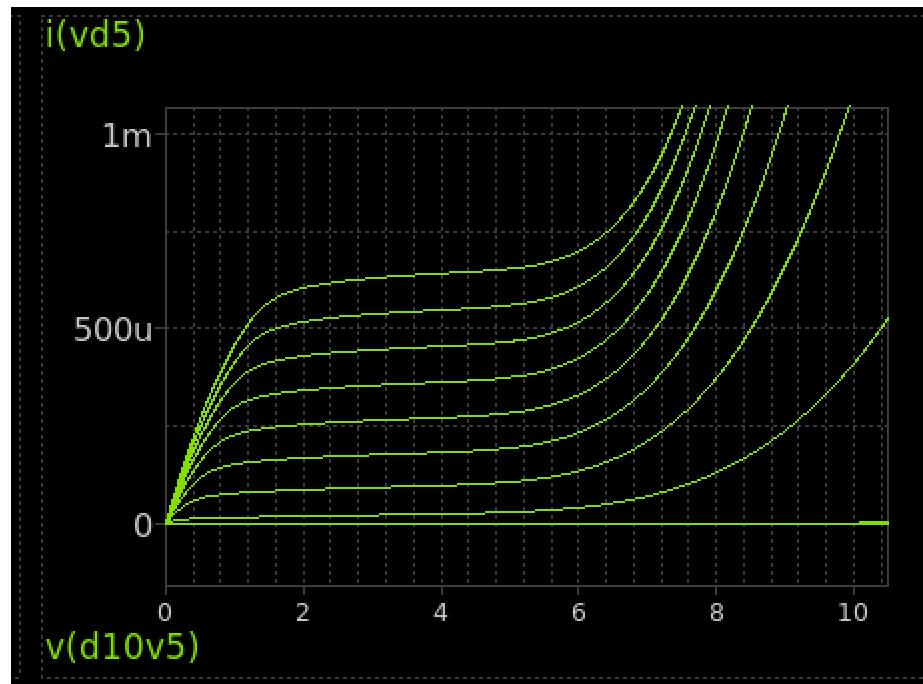
DC sweeping  $V_i$

$$1.2V = 1.8V - 0V - V_{th}$$

$$\therefore V_{th} \approx 0.6$$

Operating Voltages where SPICE models are valid, subject to SOA limitations:

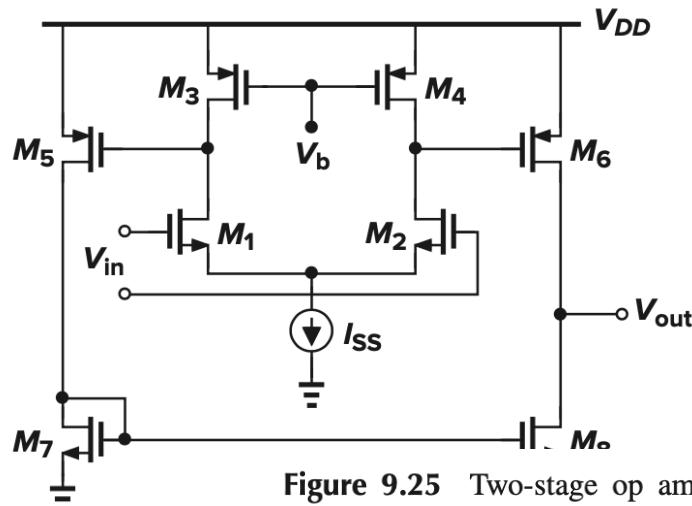
- $V_{DS} = 0$  to  $+22\text{V}$
- $V_{GS} = 0$  to  $5.5\text{V}$
- $V_{BS} = 0$  to  $-2.0\text{V}$



# Exploring options

**Table 9.1** Comparison of performance of various op amp topologies.

	Gain	Output Swing	Speed	Power Dissipation	Noise
Telescopic	Medium	Medium	Highest	Low	Low
Folded-Cascode	Medium	Medium	High	Medium	Medium
Two-Stage	High	Highest	Low	Medium	Low
Gain-Boosted	High	Medium	Medium	High	Medium

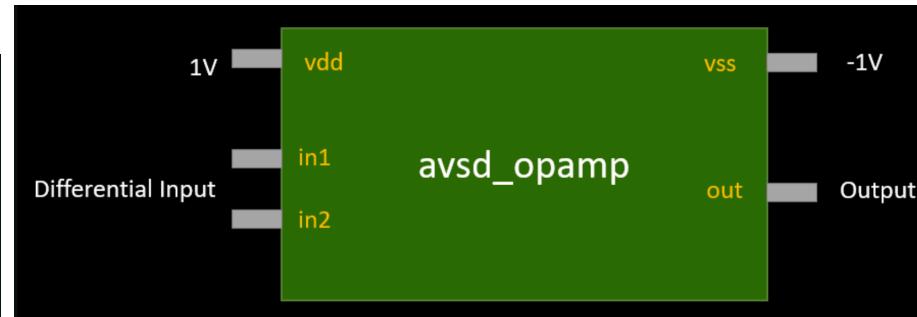
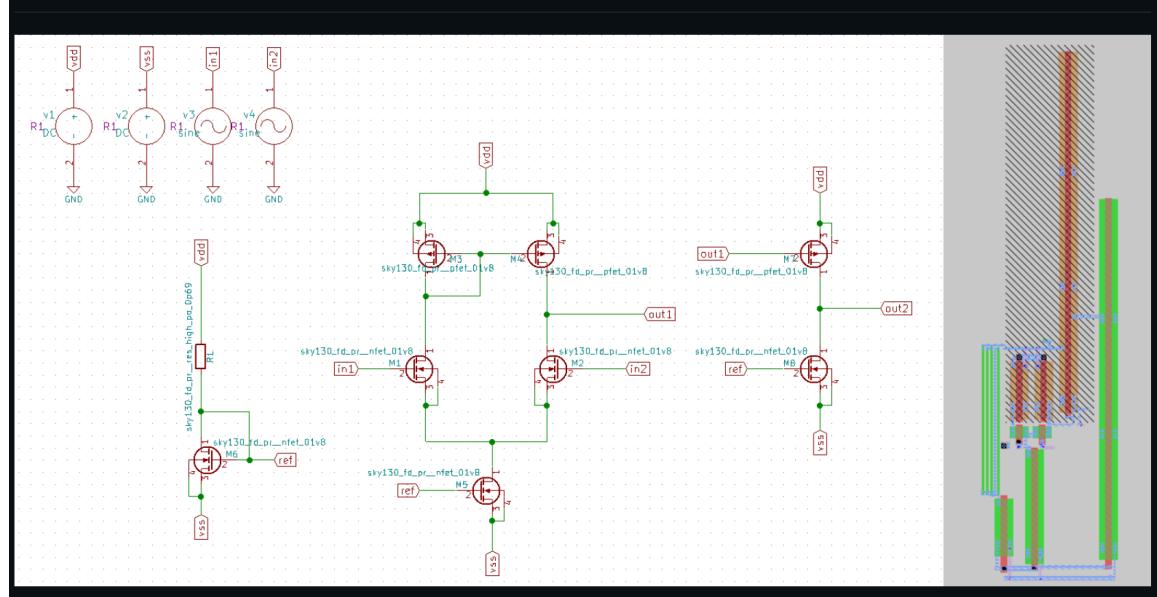


**Figure 9.25** Two-stage op amp with single-ended output.

[https://github.com/rohinthram/avsd\\_opamp](https://github.com/rohinthram/avsd_opamp)

# Exploring options pt1

## avsd\_opamp - IP Design



Specification	Value
Differential Gain	31.55dB
CMRR	41.4dB
Gain Bandwidth Product	46MHz
Phase Margin	101.93°
Input Offset Voltage	-24.55mV
Power Dissipation at 60Hz 1mV p-p sinusoid with 1kΩ	17µW
Slew Rate	180 V/µs

[https://github.com/rohinthram/avsd\\_opamp](https://github.com/rohinthram/avsd_opamp)

# Exploring options

Screenshot of a GitHub repository page for a General Purpose Open Source Operational Amplifier (OpAmp) project.

The page title is "General Purpose Open Source Operational Amplifier (OpAmp)".

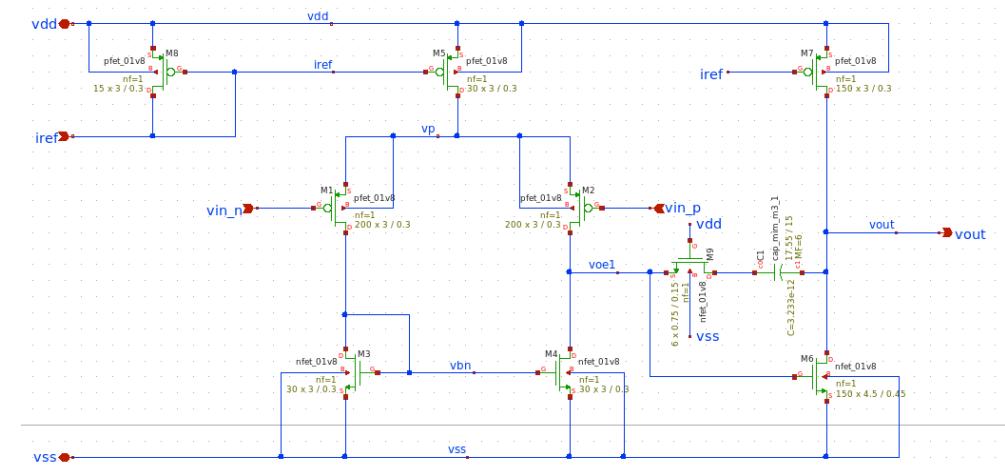
The description states: "This project is a test chip, which contains several two stages operational amplifiers with Miller compensation. This is an all analog design implemented on the [Google-Skywater 130nm Open Source PDK](#). It is an Open Source project under [Apache License 2.0] (LICENSE)."

The OpAmp design is located in an Open Source SoC Harness obtained from the [efabless Caravel Project](#).

## OpAmp Desing

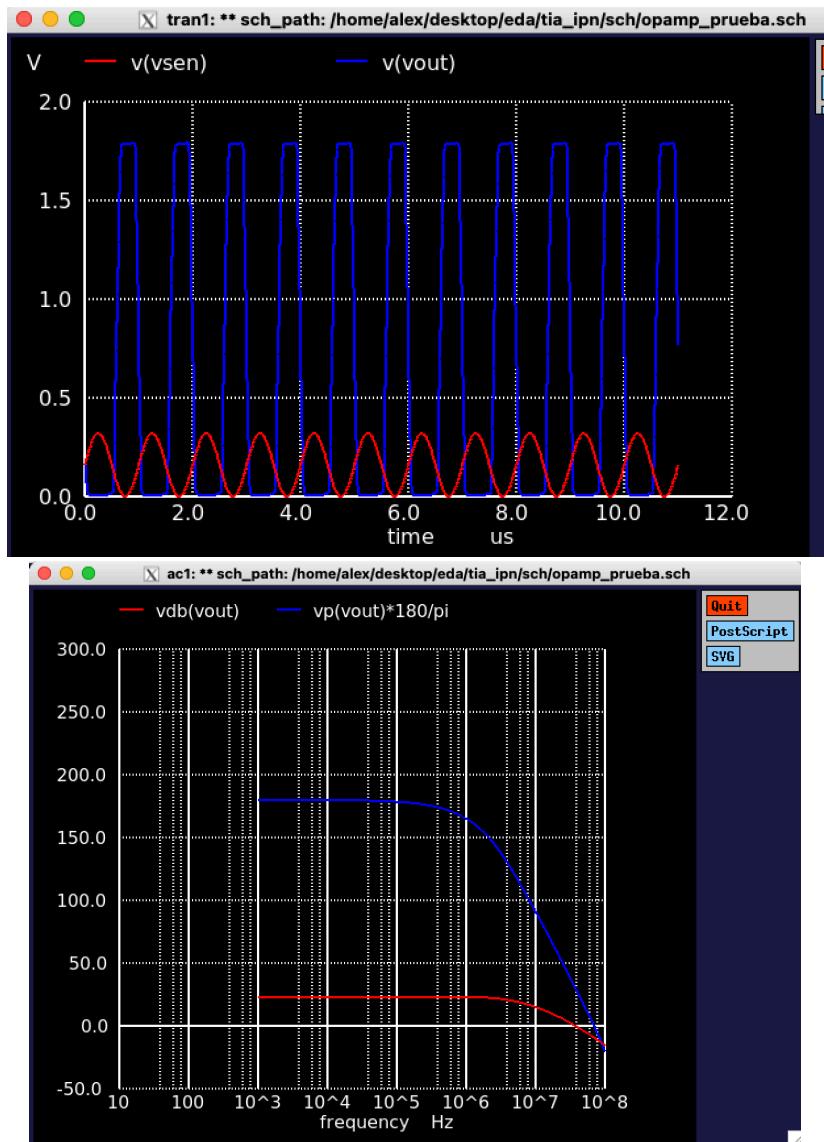
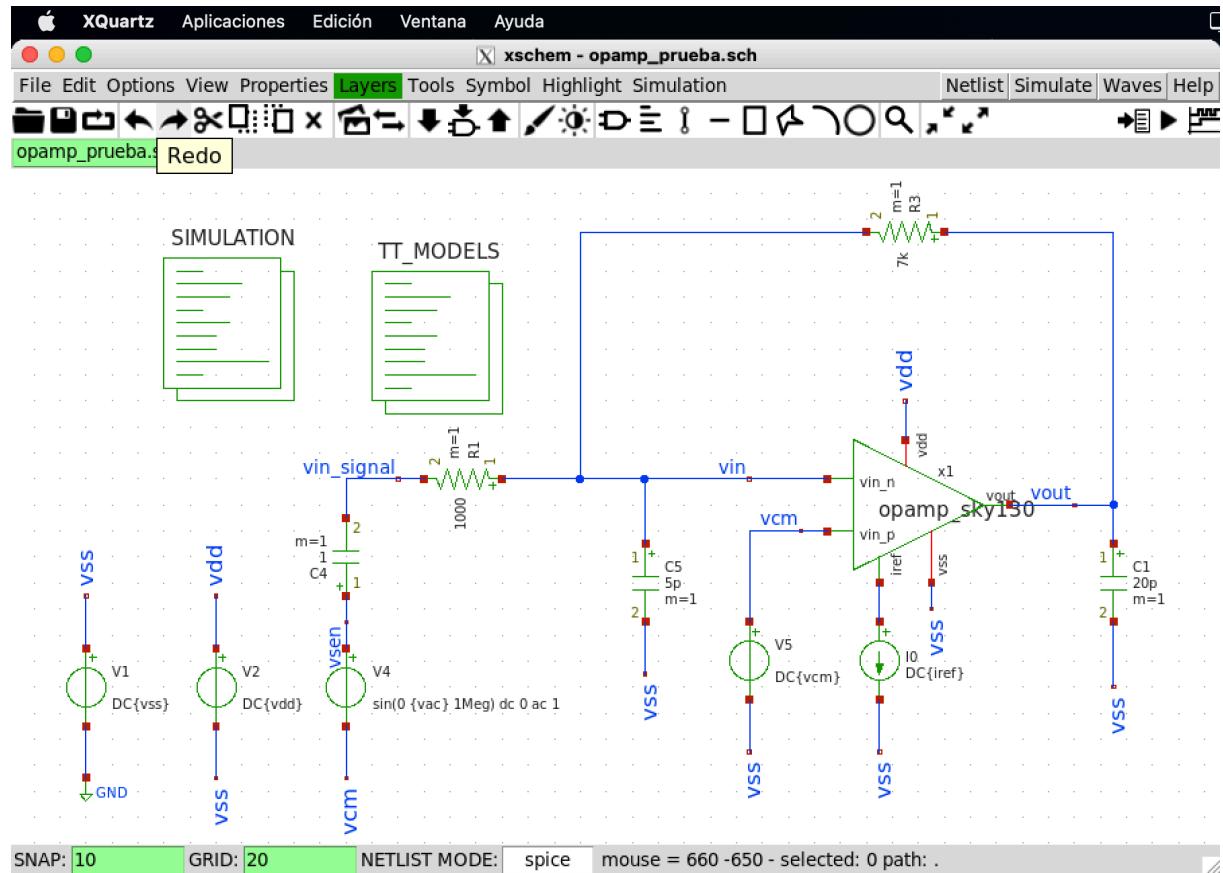
### General Specifications:

- V\_dd
- I\_ref
- Power Consumption
- DC Gain
- Bandwidth
- Chip Area



[https://github.com/JuliaAlva/caravel\\_fulgor\\_opamp/tree/master](https://github.com/JuliaAlva/caravel_fulgor_opamp/tree/master)

# Testing the device



# Redrawing into 3.3v...

The screenshot shows a web browser displaying the SkyWater SKY130 PDK documentation at [skywater-pdk.readthedocs.io](https://skywater-pdk.readthedocs.io). The page title is "Device Details". The left sidebar contains a navigation menu with items like "SkyWater SKY130 PDK", "Versioning Information", "Current Status", "Known Issues", "Design Rules", "PDK Contents", "Analog Design", "Digital Design", "Simulation", "Physical & Design Verification", "Python API", "Previous Nomenclature", "Glossary", "How to Contribute", "Partners", and "References". The main content area has two columns. The left column is titled "Spice Model Information" and lists operating voltages:  $V_{DS} = 0$  to 3.3V,  $V_{GS} = 0$  to 3.3V, and  $V_{BS} = 0$  to -3.3V. The right column is titled "Details" and lists various PMOS models: 1.8V accumulation-mode MOS varactors, 3.0V native NMOS FET, 5.0V native NMOS FET, 5.0V/10.5V NMOS FET, and 5.0V/10.5V PMOS FET. A table below shows device parameters for VTXNLNVH, VTXNS90NVH, and VTXNSN90NVH. The URL in the address bar is <https://skywater-pdk.readthedocs.io/en/main/rules/device-details.html#v-native-nmos-fet>.

Param	W/L	Units	MODEL	TT	FF	SS	FS	SF
VTXNLNVH	10/4.0	V		0.121	0.091	0.151	0.164	0.07
VTXNS90NVH	10/0.9	V		5.855	6.098	5.605	6.107	5.59
VTXNSN90NVH	0.42/0.9	V		0.075	0.017	0.129	0.152	-0.01

**There is no 3.3V PMOS!**

**There is a g05d10v5 PMOS and NMOS**

<https://skywater-pdk.readthedocs.io/en/main/rules/device-details.html#v-native-nmos-fet>