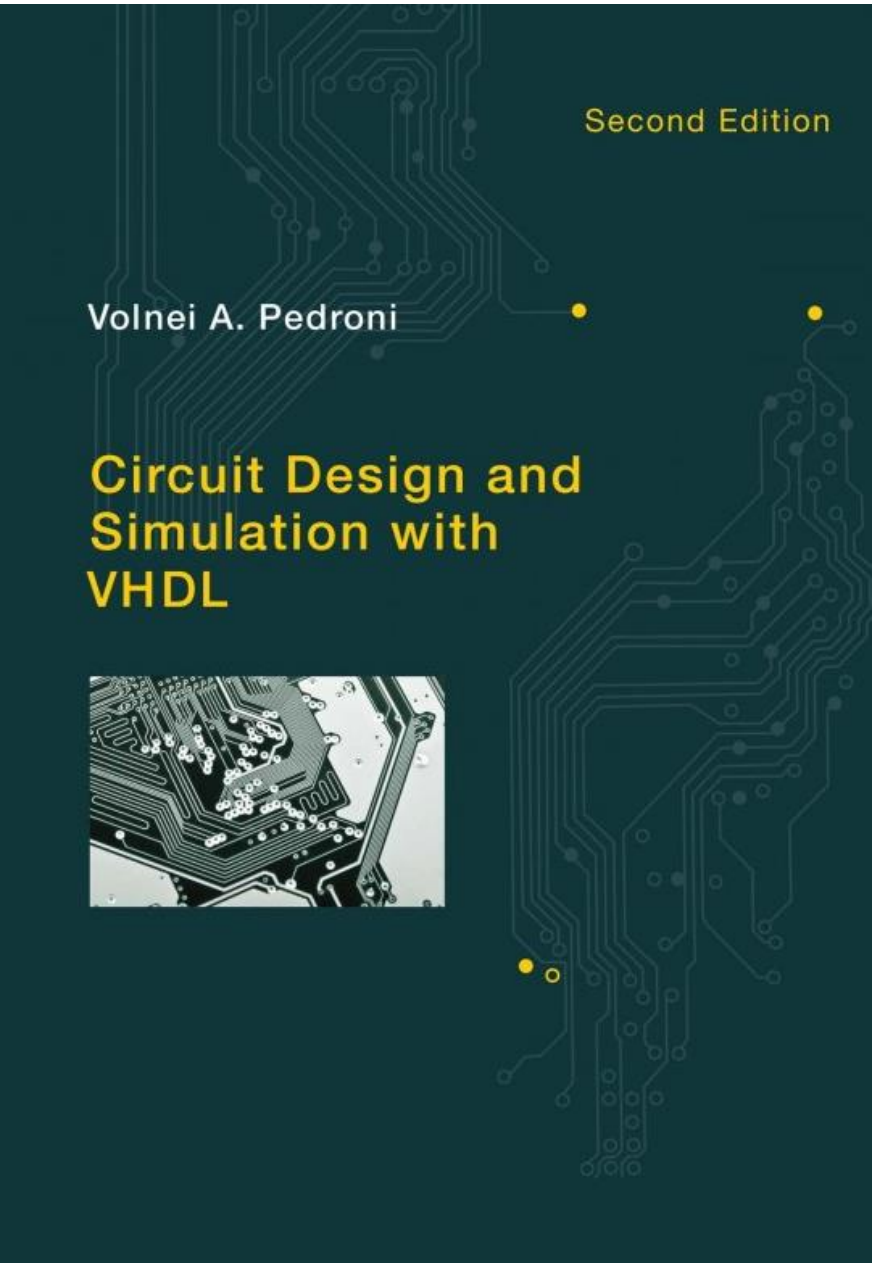
Session 6: September 7

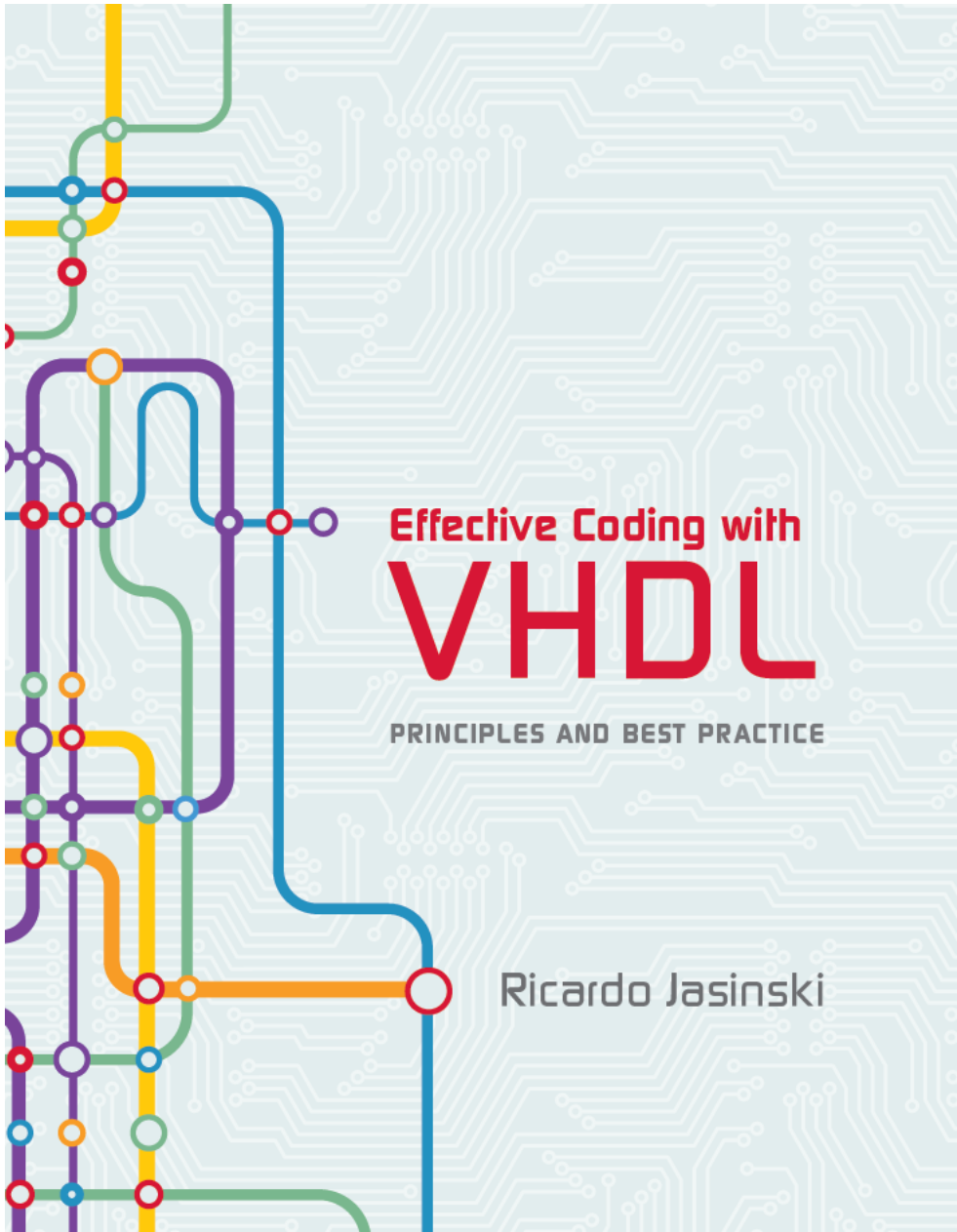
VHDL

Session 6: Outline

- Bibliography – Methodology
- Logic gates (homework).
- Boolean function
- When / Select
- Compare-Add Circuit
- Decoder
- Real application

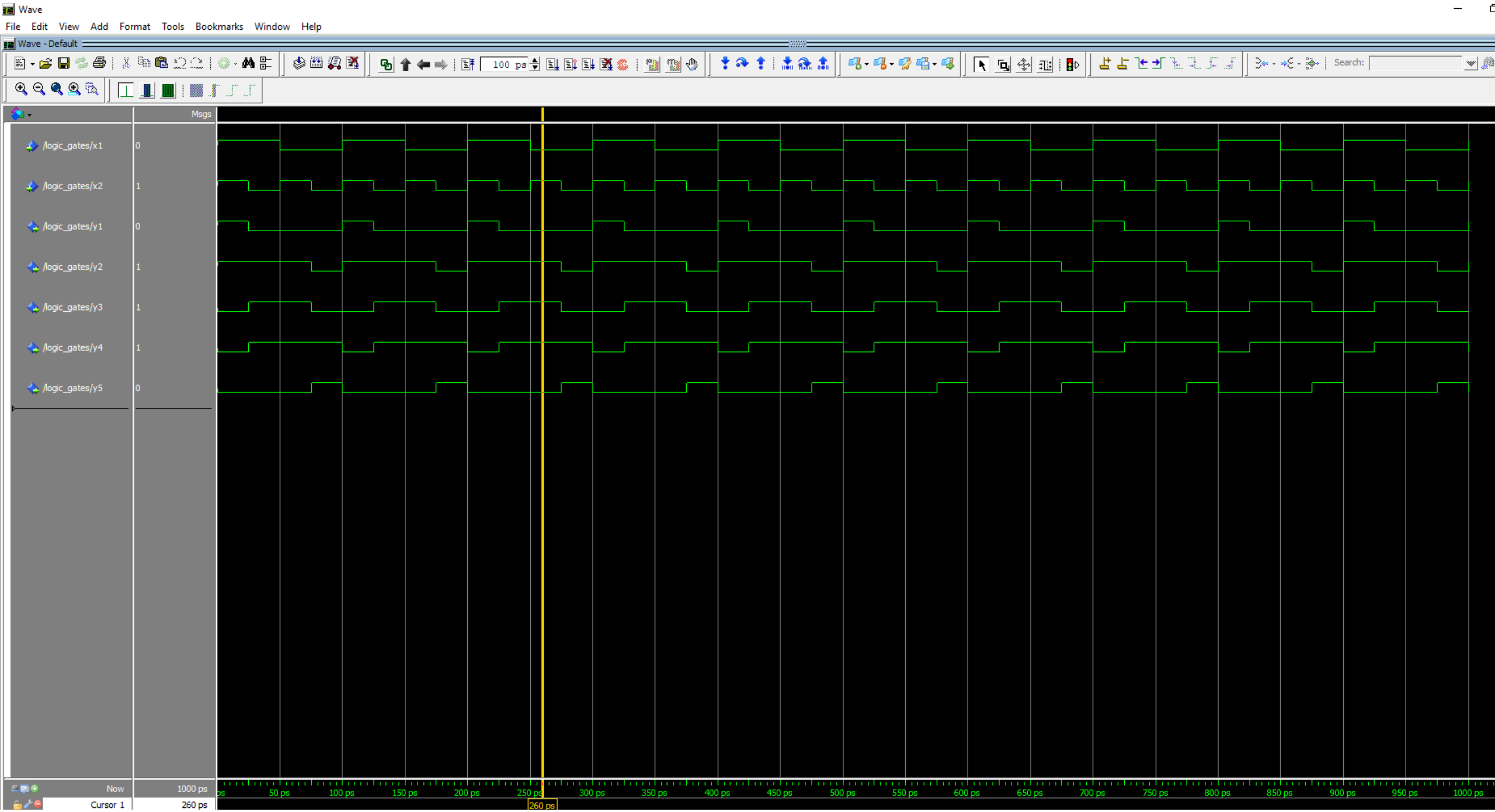
BIBLIOGRAPHY





Logic gates example

```
1  library ieee;
2  use ieee.std_logic_1164.all;
3
4  entity logic_gates is port(
5      x1, x2 : in std_logic;
6      y1,y2,y3,y4,y5: out std_logic);
7  end logic_gates;
8
9  /* esto es un comentario de múltiples
10 lineas*/
11 architecture logic_gates_arc of logic_gates is
12 begin
13     y1 <= x1 and   x2;
14     y2 <= x1 or x2;
15     y3 <= x1 xor x2;
16     y4 <= x1 nand x2;
17     y5 <= x1 nor x2;
18 end logic_gates_arc;
```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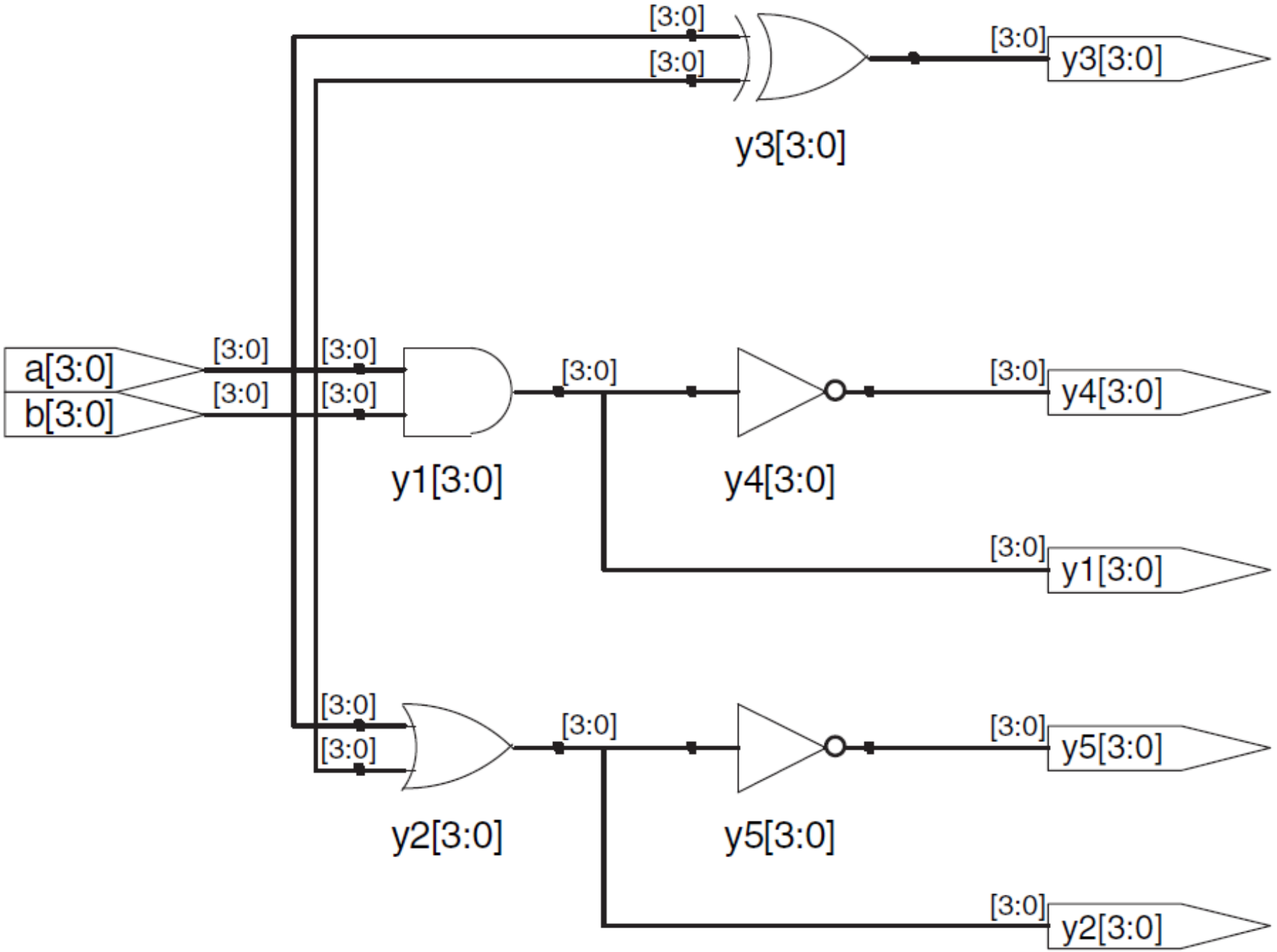
File Edit View Add Format Tools Bookmarks Window Help
Wave - Default
100 ps
Search:
Msgs
/logic_gates/x1 0
/logic_gates/x2 1
/logic_gates/y1 0
/logic_gates/y2 1
/logic_gates/y3 1
/logic_gates/y4 1
/logic_gates/y5 0
Now 1000 ps
Cursor 1 260 ps
50 ps 100 ps 150 ps 200 ps 250 ps 300 ps 350 ps 400 ps 450 ps 500 ps 550 ps 600 ps 650 ps 700 ps 750 ps 800 ps 850 ps 900 ps 950 ps 1000 ps
260 ps

Synthesized circuit



VHDL Design for any Boolean Function Written in Canonical Form

- *F* is 1 only when there are two 1s in each input combination *A B C*

$$F(A,B,C) = \Sigma m(3, 5, 6)$$

$$F(A,B,C) = \overline{A}\cdot B\cdot C + A\cdot\overline{B}\cdot C + A\cdot B\cdot\overline{C}$$

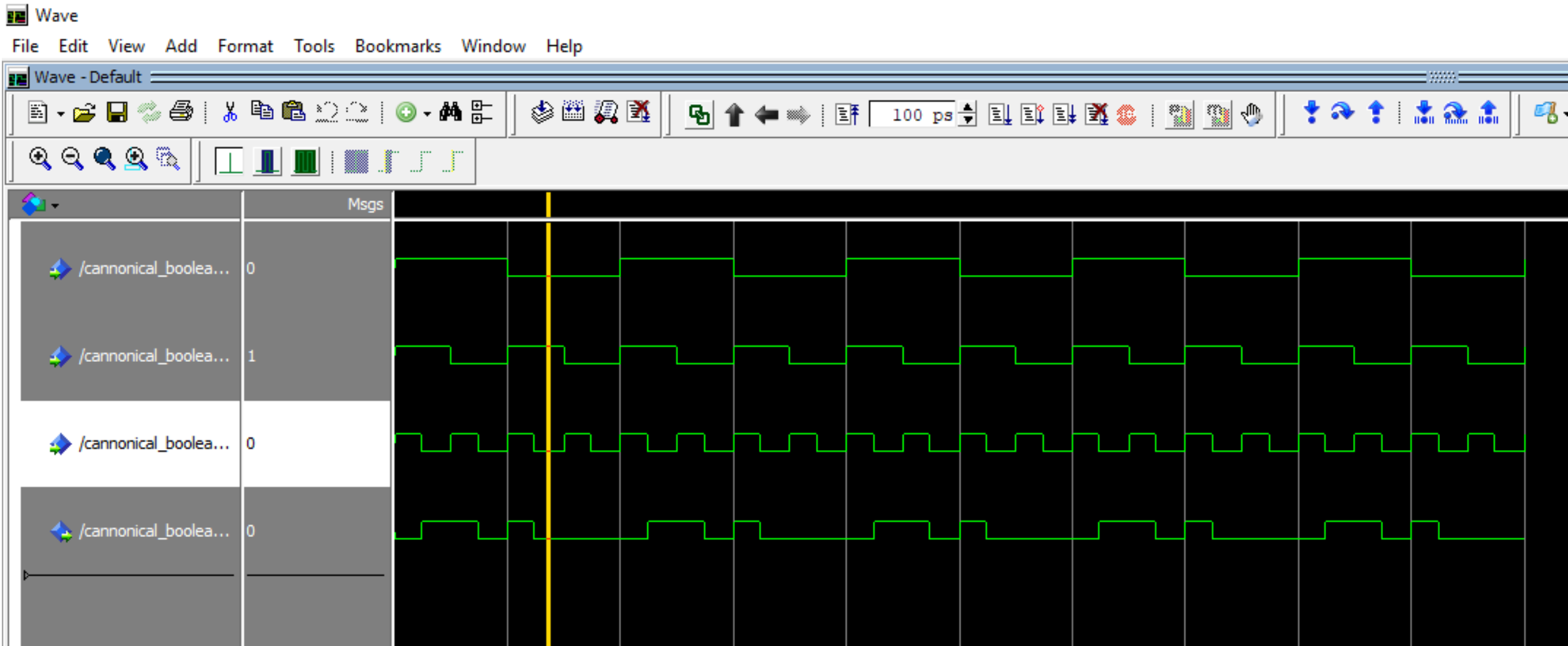
$F <=$ **(not** A **and** B **and** C**) or**
(A **and not** B **and** C**) or**
(A **and** B **and not** C**)**

(Decimal)	A	B	C	F
0	0	0	0	0
1	0	0	1	0
2	0	1	0	0
3	0	1	1	1
4	1	0	0	0
5	1	0	1	1
6	1	1	0	1
7	1	1	1	0

```vhdl
library ieee; use ieee.std_logic_1164.all;

entity cannonical_boolean_function is
port(a,b,c: in std_logic;
      f  :  out   std_logic);
end cannonical_boolean_function;

architecture cannonical_boolean_function_arc of cannonical_boolean_function is
begin
   f <= (not a and b and c) or (a and not b and c) or (a and b and not c);
end cannonical_boolean_function_arc;
```


Wave
File Edit View Add Format Tools Bookmarks Window Help
Wave - Default
100 ps
Msgs
/cannonical_boolea...
0
/cannonical_boolea...
1
/cannonical_boolea...
0
/cannonical_boolea...
0

Compare-Add Circuit

- The inputs are two unsigned 3-bit values (a and b, ranging from 0 to 7), while the outputs are comp (single bit) and sum (to avoid overflow, 4 bits are needed, hence ranging from 0 to 15).