



Res. 2333 del 2012

Vigilada Mineducación Resolución 12220 de 2016

ARQUITECTURA DE COMPUTADORES II: LABORATORY.

Professor: Roger Gomez Nieto, MSc

roger.gomez@javerianacali.edu.co

Subject: AC182_

Session 1.



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- IDE's installation.
- Presentation and mail list.
- Score, bibliography and course overview.
- Previous Knowledge.
- Introduction to ASM ARM.
- “Hello world” in ASM.

[Class Schedule](#)
[Request Info](#)

ARM ASSEMBLER PROGRAMMING LANGUAGE

OVERVIEW

This course introduces the student to low-level software development using ARM assembly language. The course will cover Arm Architecture, instruction set, data movement, various addressing modes, arithmetic and logic operations, using loop structures, basic data structures including tables, lists, stacks and strings. Course activities include setting up the development environment, using cross compilers and off-chip debugging techniques, writing new programs as well as reverse engineering and modifying existing programs without access to the source code.

PREREQUISITES

Some programming experience is required. Native programming experience in languages like C or C++ is highly recommended. Exposure to computer architecture or operating systems concepts like memory protection, kernel and user modes at least on a level of one undergraduate course is helpful.

DURATION

- 5-Day Class – \$2995.00
- 10-Day Class – \$3995.00



TOPICS

- Arm history and ecosystem
- ARM Architecture
- Instruction Set
- Addressing Modes
- Programs
- Data Movement
- Logic
- Arithmetic
- Barrel shifter
- Conditional execution
- Program Loops
- Strings
- Tables and Lists
- Stacks
- Subroutines
- Interrupts
- Code Conversion
- Cross compiling
- Reverse engineering

Course Evaluation.



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- Laboratory: 10%.
- Final Project: 25%.

Bibliografía



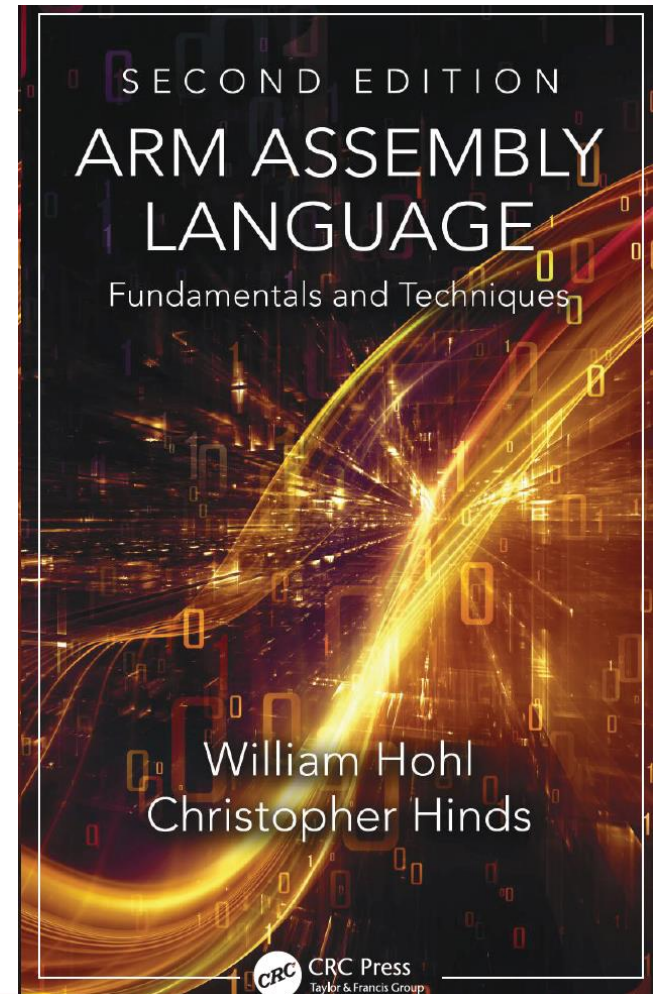
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Ata Elahi · Trevor Arjeski

ARM Assembly Language with Hardware Experiments

 Springer



Bibliografía

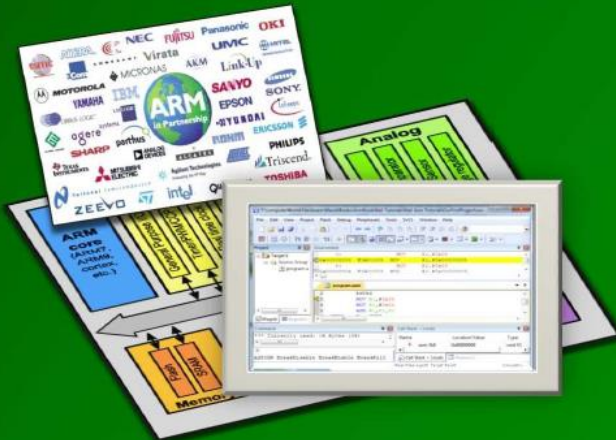


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ARM Assembly Language Programming & Architecture

Muhammad Ali Mazidi
Sarmad Naimi
Sepehr Naimi
Janice Mazidi



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THE DEFINITIVE GUIDE TO ARM® CORTEX®-M0 AND CORTEX-M0+ PROCESSORS



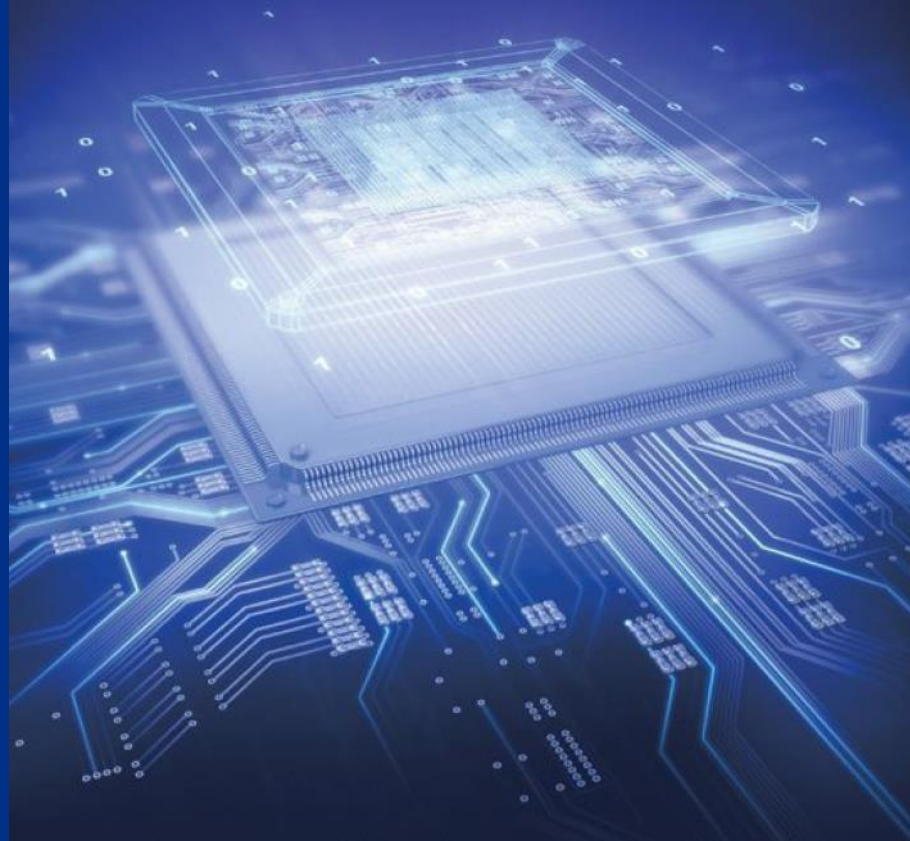
Second Edition

Joseph Yiu

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ARM® Microprocessor Systems

Cortex®-M Architecture, Programming, and Interfacing



Muhammad Tahir and Kashif Javed

 **CRC Press**
Taylor & Francis Group



COMPUTER ORGANIZATION AND DESIGN

THE HARDWARE/SOFTWARE INTERFACE

 **RISC-V EDITION**



MK
MORGAN KAUFMANN

DAVID A. PATTERSON
JOHN L. HENNESSY

Reasons to Learn Assembly



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- the first steps in booting the computer,
- code to handle interrupts,
- low-level locking code for multi-threaded programs,
- code for machines where no compiler exists,
- code which needs to be optimized beyond the limits of the compiler,
- on computers with very limited memory, and
- code that requires low-level access to architectural and/or processor features.

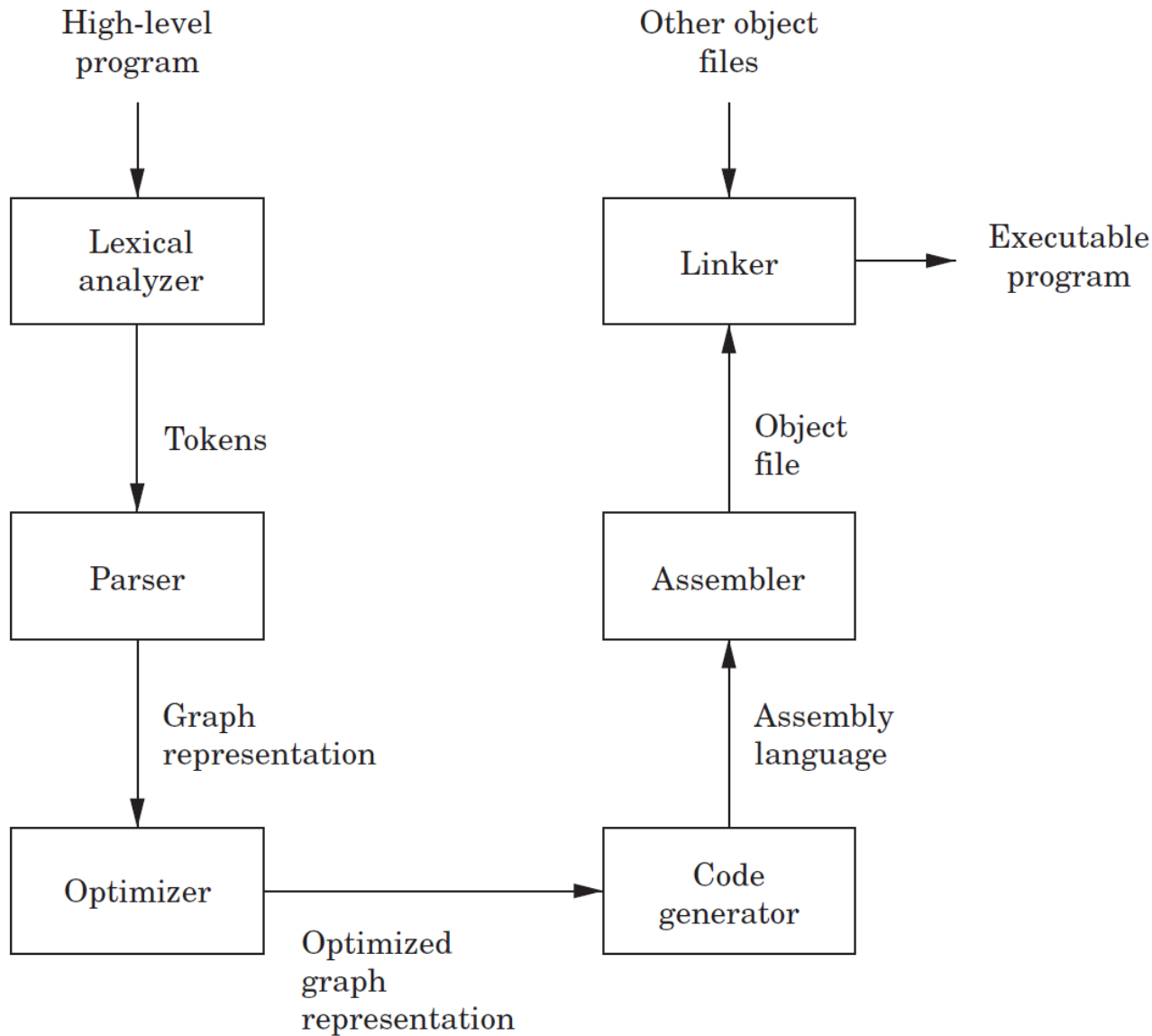


Figure 1.2
Stages of a typical compilation sequence.

Little Endian

Little-endian

32-bit integer

0A0B0C0D

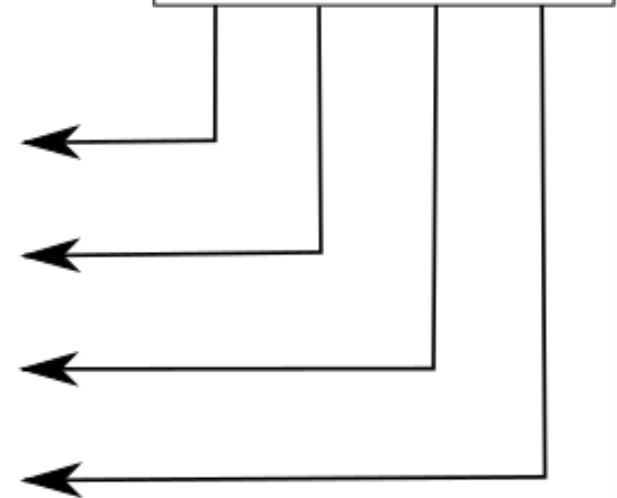
Memory

⋮		⋮
0D	a	0A
0C	$a+1$	0B
0B	$a+2$	0C
0A	$a+3$	0D
⋮		⋮

Big-endian

32-bit integer

0A0B0C0D



IDE.



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- <https://www.keil.com/download/product/> versión 5.25 MDK (Microcontroller Development Kit) (837 MB).
- Fill the required information.
- <http://www2.keil.com/mdk5/legacy/> Legacy Support for ARM7 (127 MB).

Select Device for Target 'Target 1'...

Device

Legacy Device Database [no RTE]

Vendor: ARM

Device: ARM7 (Little Endian)

Toolset: ARM

Search:

Description:

ARM7TDMI-S based high-performance 32-bit RISC Microcontroller with

- +
-
- Analog Devices
- ARM
 - ARM7 (Big Endian)
 - ARM7 (Little Endian)
 - ARM966E-S (Big Endian)
 - ARM966E-S (Little Endian)
 - ARM9E-S (Big Endian)
 - ARM9E-S (Little Endian)
 - Cortex-R4

OK

Cancel

[Help](#)

Instruction Set Cortex -M family

VSEL							VCVTA		VCVTN		VCVTP		VCVTM		VMAXNM		VMINNM		Cortex-M7 FPU (single and double precision floating point)																														
VRINTR							VRINTA		VRINTN		VRINTP		VRINTM		VRINTX		VRINTY																																
										Cortex-M4 FPU (single precision floating point)																																							
VABS		VADD		VCMP		VCMPPE		VCVT		VCVTR		VDIV		VLDM		VLDR																																	
VMLA		VMLS		VMOV		VMRS		VMSR		VMUL		VNEG		VNMLA		VMMLS		VFNMA																															
VNMUL		VPOP		VPUSH		VSQRT		VSTM		VSTR		VSUB		VFMA		VFMS		VFNMS																															
QDADD		QADD		QADD16		QADD8		SADD16		SADD8		UADD16		UADD8		UHADD16		UHADD8																															
QDSUB		QSUB		QSUB16		QSUB8		SSUB16		SSUB8		USUB16		USUB8		UHSUB16		UHSUB8																															
ADC							ADD		ADR		AND		ASR		B		BIC		SHADD16		SHADD8		SHSUB16																										
BFC							BFI		CLZ		CDP		CLREX		CMN		CMP		PKH		SEL		SHSUB8																										
CBNZ		CBZ		DBG		EOR		LDR		LDRH		LDRB		LDRD				SMULTT		SMULTB		UQADD16																											
LDMIA		LDMDB		LDRT		LDRHT		LDRBT		LDRSH		LDRSB						SMULBT		SMULBB		UQSUB16																											
LDRSBT		LDRSHT		LDREX		LDREXB		LDREXH		LSL		LSR						SMLATT		SMLATB		UQADD8																											
LDC		MCR		MRC		MCRR		MRRC		PLD		PLI						SMLABT		SMLABB		UQSUB8																											
MOV		MOVW		MOVT		MUL		MVN		MLS		MLA						SMLALT		SMLALTB		SMMUL																											
NOP		PUSH		POP		ORR		ORN		PLDW		RBIT						SMLALBT		SMLALBB		SMULWT																											
ADC		ADD		ADR		BKPT		BLX		BIC		REV		REV16		REVSH		ROR		USADA8		USAD8		SMULWB																									
AND		ASR		B		BX		CPS		CMN		RSB		RRX		SBC		SEV		QSAX		QASX		SMLAD																									
BL		MRS		MSR								SUB		STC		UBFX		SBFX		UQSAX		UQASX		SMLSD																									
DSB		DMB		ISB								STR		STRD		UDIV		SDIV		UASX		SASX		SMLALD																									
CMP		EOR		LDR		LDRH		LDRB		LDM		STRB		STRH		UMULL		SMULL		USAX		SSAX		SMLSDD																									
LDRSH		LDRSB		LSL		LSB		MOV		NOP		STMIA		STMDB		UMLAL		SMLAL		UHASX		SHASX		SMUAD																									
REV		REV16		REVSH		MUL		MVN		ORR		STREX		STREXB		UXTB		SXTB		UHSAX		SHSAX		SMUSD																									
PUSH		POP		ROR		RSB		SEV		SVC		STREXH		STRT		USAT		SSAT		UXTAB		SXTAB		SMLAWT																									
SBC		STR		STRH		STRB		STM		SUB		STRHT		STRBT		UXTH		SXTH		UXTAH		SXTAH		SMLAWB																									
SXTB		UXTB		SXTH		UXTH		TST		YIELD		TBB		TBH		WFI		WFE		UXTAB16		SXTAB16		SMMLA																									
WFE		WFI		Cortex-M0/M0+/M1 (ARMv6-M)								TST		TEQ		YIELD		IT		UXTB16		SXTB16		SMMLS																									
16-bit instructions										32-bit instructions										Cortex-M3 (ARMv7-M)										Cortex-M4 (ARMv7E-M)																			
																				USAT16										SSAT16										UMAAL									



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ARM Directives



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Directive	Description
AREA	Instructs the assembler to assemble a new code or data section
END	Informs the assembler that it has reached the end of a source file.
ENTRY	Declares an entry point to a program.
EQU	Gives a symbolic name to a numeric constant, a register-relative value or a PC-relative value.
INCLUDE	It adds the contents of a file to our program.

[label] mnemonic [operands] [;comment]

AREA



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Microprocessor programs often contain several AREA statements for the following purposes:

- Reset (startup) address
- Interrupt service addresses
- Trap (software interrupt) addresses
- RAM storage
- Stack
- Main program
- Subroutines
- Input/Output

The AREA statement at the start of an ARM program is required, and its absence will cause the assembly to fail.

END, marks the end of the assembly language source program. This must appear in the file or a “missing END directive” error will occur.

ENTRY is beginning of the code.

4.3.7. MOV and MVN

Move and Move Not.

Syntax

MOV{S}{cond} Rd, Operand2

MOV{cond} Rd, #imm16

MVN{S}{cond} Rd, Operand2

where:

S

is an optional suffix. If *S* is specified, the condition code flags are updated on the result of the operation (see [Conditional execution](#)).

cond

is an optional condition code (see [Conditional execution](#)).

Rd

is the destination register.

Operand2

is a flexible second operand. See [Flexible second operand](#) for details of the options.

imm16

is any value in the range 0-65535.

- Notice the # before immediate value.
- “immediate” is a constant value that must be provided right there with the instruction.



Certain 32-bit values cannot be represented as an immediate operand to a single 32-bit instruction, although you can load these values from memory in a single instruction.

MOV can load any 8-bit immediate value, giving a range of 0x0-0xFF (0-255). It can also rotate these values by any **even** number.

```
1          AREA PRUEBA1, CODE, READONLY
2  ENTRY
3          MOV R1, #0X23
4 HERE      B HERE
5          END
```