Alejandro Sherman, 862062898, Section 21, ENGR ID asherman, NET ID asher011
Partner Sec21 Group 1: Christopher Alexman calex025 (our reports and results are unique)

Lab 4 Part 2 Report

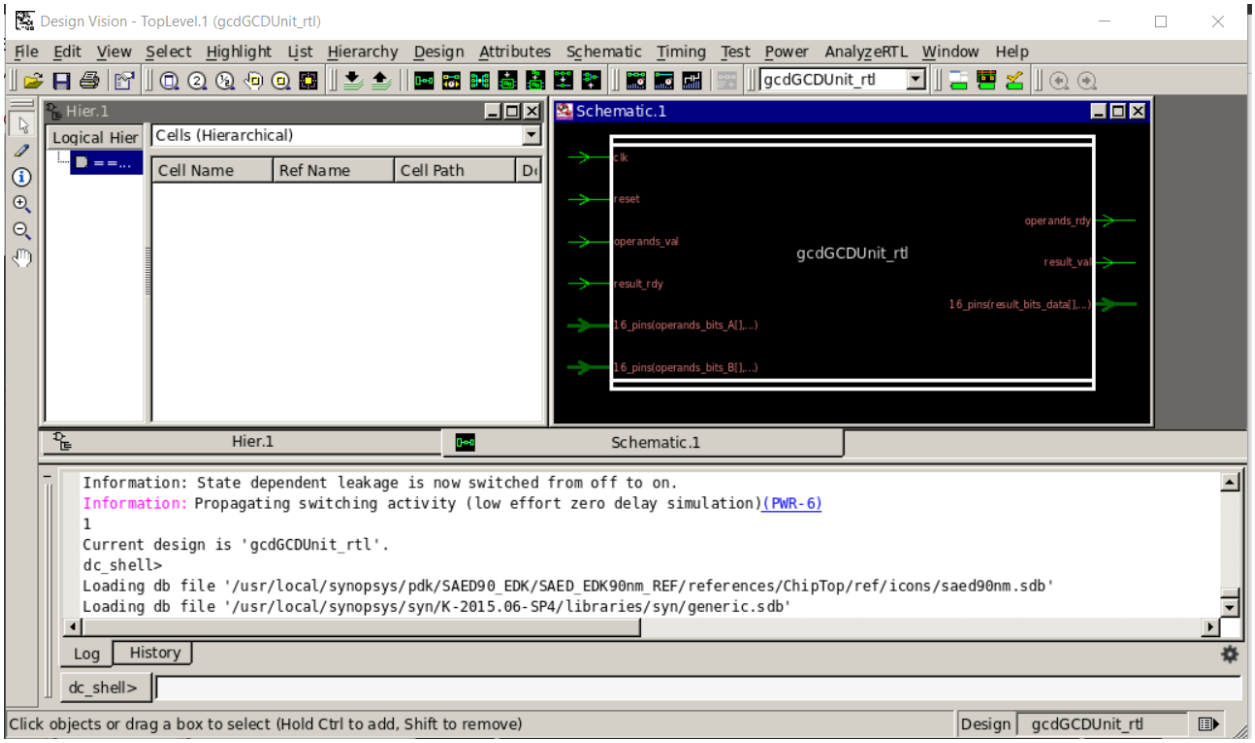
Video Checkoff

Video Checkoff Week 2 Part1:
https://www.youtube.com/watch?v=oOfRTjm-Ns4
(Includes gate level for gcd and compiler report location)
Video Checkoff Week 2 Part2:
https://www.youtube.com/watch?v=BajzzlxEvgQ
(Includes final layout in fig 51)

What I learned

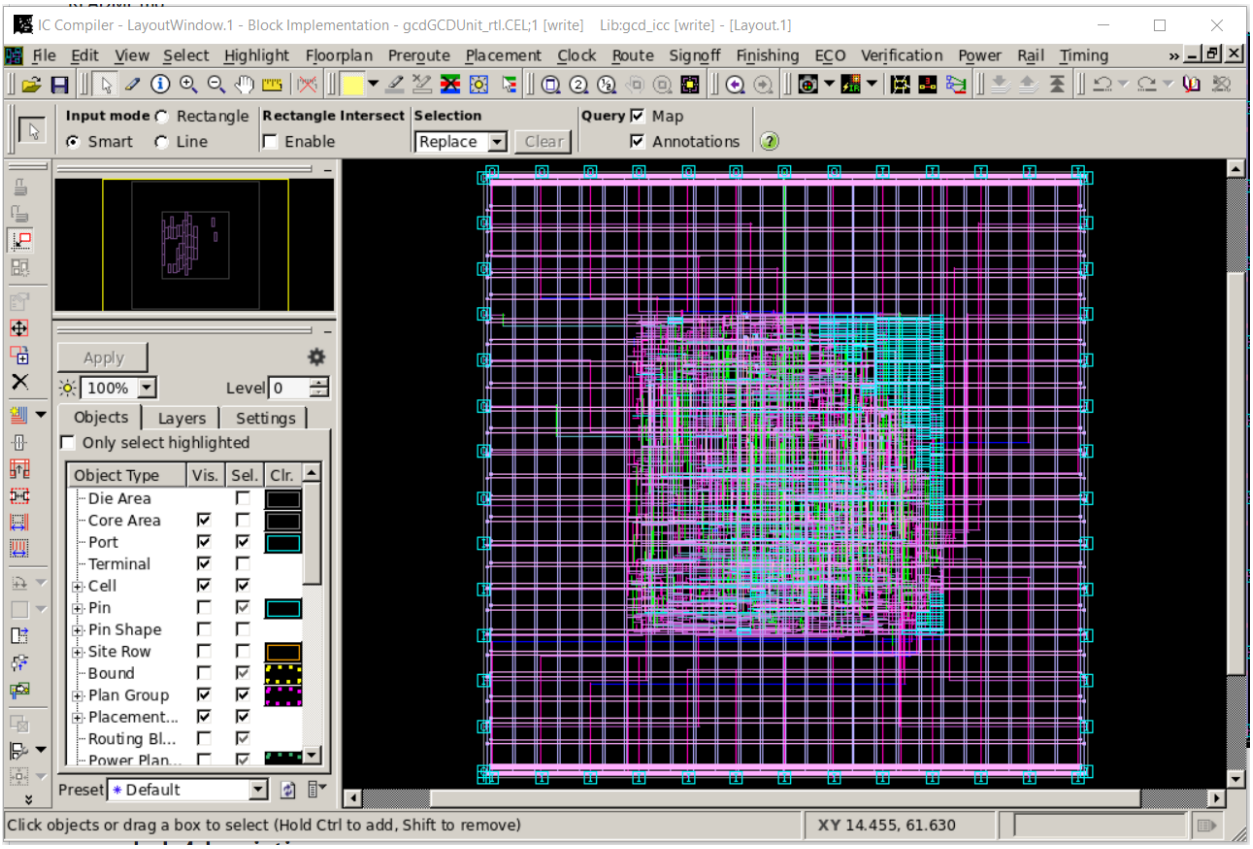
In today's lab I learned how to once again perform register level design and then create my hardware design with HDL for electric designs. This time, I learned how to do so with a more complex verilog design. Additionally, I learned how to generate meaningful data reports from dc_shell. Also, when running icc_shell I learned how to modify a floorplan for a larger layout. Finally, I learned how to continue routing after enabling filters and I also learned how to generate the post place and route netlist, the constraint file, and parasitics files to generate power estimates.

Gate Level for GCD



Final Layout

Fig 51



Timing Report

```
****************************************
Report : timing
        -path full
        -delay max
        -nets
        -max_paths 1
        -transition_time
Design : gcdGCDUnit_rtl
Version: K-2015.06-SP4
Date   : Sat Feb 26 20:33:56 2022
****************************************

Operating Conditions: TYPICAL   Library: saed90nm_typ
Wire Load Model Mode: top

  Startpoint: GCDdpath0/A_reg_reg[4]
              (rising edge-triggered flip-flop clocked by ideal_clock1)
  Endpoint: GCDdpath0/A_reg_reg[9]
            (rising edge-triggered flip-flop clocked by ideal_clock1)
  Path Group: ideal_clock1
```

Path Type: max

Attributes:
d - dont_touch
u - dont_use
mo - map_only
so - size_only
i - ideal_net or ideal_network
inf - infeasible path

Point	Fanout	Trans	Incr	Path	Attributes
clock ideal_clock1 (rise edge)			0.00	0.00	
clock network delay (ideal)			0.00	0.00	
GCDdpath0/A_reg_reg[4]/CLK (DFFARX1)			0.00	0.00	0.00 r
GCDdpath0/A_reg_reg[4]/Q (DFFARX1)			0.04	0.24	0.24 f
result_bits_data[4] (net)	5		0.00	0.24 f	
U153/QN (NAND2X1)		0.04	0.03	0.28 r	
n294 (net)	2		0.00	0.28 r	
U251/QN (INVX0)		0.03	0.03	0.31 f	
n183 (net)	2		0.00	0.31 f	
U133/QN (NAND2X0)		0.06	0.04	0.35 r	
n149 (net)	1		0.00	0.35 r	
U252/QN (NAND2X1)		0.05	0.04	0.39 f	
n314 (net)	3		0.00	0.39 f	
U253/QN (NAND2X2)		0.03	0.02	0.41 r	
n153 (net)	1		0.00	0.41 r	
U258/QN (NAND2X1)		0.03	0.03	0.44 f	
n154 (net)	1		0.00	0.44 f	
U259/Q (AO21X1)		0.04	0.08	0.52 f	
n227 (net)	4		0.00	0.52 f	
U177/Q (LSDNX1)		0.04	0.08	0.60 f	
n308 (net)	2		0.00	0.60 f	
U320/Q (AO21X1)		0.03	0.09	0.69 f	
n233 (net)	1		0.00	0.69 f	
U322/Q (XOR2X1)		0.04	0.12	0.81 r	
n234 (net)	1		0.00	0.81 r	
U140/QN (NAND2X0)		0.05	0.04	0.84 f	
n238 (net)	1		0.00	0.84 f	
U324/QN (NAND4X0)		0.07	0.04	0.88 r	
n91 (net)	1		0.00	0.88 r	
GCDdpath0/A_reg_reg[9]/D (DFFARX1)			0.07	0.00	0.88 r
data arrival time				0.88	

clock ideal_clock1 (rise edge)			1.00	1.00	
clock network delay (ideal)			0.00	1.00	
GCDdpath0/A_reg_reg[9]/CLK (DFFARX1)			0.00	1.00 r	
library setup time		-0.12	0.88		
data required time			0.88		

```
  ----------------------------------------------------------------------------------------------------
  data required time                                                                          0.88
  data arrival time                                                                          -0.88
  ----------------------------------------------------------------------------------------------------
  slack (MET)                                                                                 0.00
```

Area Report

```
****************************************
Report : area
Design : gcdGCDUnit_rtl
Version: K-2015.06-SP4
Date   : Sat Feb 26 20:38:09 2022
****************************************

Library(s) Used:

    saed90nm_typ (File:
/usr/local/synopsys/pdk/SAED90_EDK/SAED_EDK90nm_REF/references/ChipTop/ref/saed90nm_fr/LM/s
aed90nm_typ.db)

Number of ports:                        54
Number of nets:                        384
Number of cells:                       317
Number of combinational cells:         283
Number of sequential cells:             34
Number of macros/black boxes:            0
Number of buf/inv:                      34
Number of references:                   30

Combinational area:            1995.864012
Buf/Inv area:                   199.999007
Noncombinational area:         1081.958015
Macro/Black Box area:             0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:               3077.822028
Total area:                 undefined

Hierarchical area distribution
------------------------------

                           Global cell area          Local cell area
                           ------------------  ----------------------------
Hierarchical cell                Absolute   Percent  Combi-     Noncombi-  Black-
                           Total      Total    national   national   boxes   Design
-------------------------------  ---------  -------  ---------  ---------  ------  ---------
gcdGCDUnit_rtl                   3077.8220    100.0  1995.8640  1081.9580  0.0000  gcdGCDUnit_rtl
-------------------------------  ---------  -------  ---------  ---------  ------  ---------
```

Total 1995.8640 1081.9580 0.0000

Power Analysis

```
****************************************
Report : power
        -hier
        -analysis_effort low
Design : gcdGCDUnit_rtl
Version: K-2015.06-SP4
Date   : Sat Feb 26 20:39:31 2022
****************************************

Library(s) Used:

    saed90nm_typ (File:
/usr/local/synopsys/pdk/SAED90_EDK/SAED_EDK90nm_REF/references/ChipTop/ref/saed90nm_fr/LM/saed90nm_typ.db)

Operating Conditions: TYPICAL   Library: saed90nm_typ
Wire Load Model Mode: top

Global Operating Voltage = 1.2
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1pW

--------------------------------------------------------------------------------
                                   Switch   Int      Leak     Total
Hierarchy                          Power    Power    Power    Power    %
--------------------------------------------------------------------------------
gcdGCDUnit_rtl                      0.128    1.124 9.51e+06    1.262 100.0
```

Standard Cell-Area Reference Analysis

```
****************************************
Report : reference
Design : gcdGCDUnit_rtl
Version: K-2015.06-SP4
Date   : Sat Feb 26 20:40:56 2022
****************************************

Attributes:
```

b - black box (unknown)
bo - allows boundary optimization
d - dont_touch
mo - map_only
h - hierarchical
n - noncombinational
r - removable
s - synthetic operator
u - contains unmapped logic

Reference	Library	Unit Area	Count	Total Area	Attributes
AND2X1	saed90nm_typ	7.445000	1	7.445000	
AO21X1	saed90nm_typ	10.138000	2	20.275999	
AO222X1	saed90nm_typ	14.746000	16	235.936005	
AOINVX1	saed90nm_typ	6.451000	1	6.451000	
AOINVX2	saed90nm_typ	6.451000	1	6.451000	
DFFARX1	saed90nm_typ	32.256001	32	1032.192017	n
DFFX1	saed90nm_typ	24.882999	2	49.765999	n
INVX0	saed90nm_typ	5.530000	28	154.840006	
INVX2	saed90nm_typ	6.451000	1	6.451000	
INVX8	saed90nm_typ	14.746000	1	14.746000	
ISOLANDX1	saed90nm_typ	7.373000	1	7.373000	
ISOLORX1	saed90nm_typ	7.387000	4	29.548000	
LSDNX1	saed90nm_typ	5.530000	1	5.530000	
NAND2X0	saed90nm_typ	5.443000	88	478.983986	
NAND2X1	saed90nm_typ	5.501000	9	49.508999	
NAND2X2	saed90nm_typ	8.798000	4	35.192001	
NAND2X4	saed90nm_typ	14.501000	1	14.501000	
NAND3X0	saed90nm_typ	7.373000	2	14.746000	
NAND4X0	saed90nm_typ	8.294000	16	132.703995	
NBUFFX2	saed90nm_typ	5.530000	1	5.530000	
NOR2X0	saed90nm_typ	5.530000	71	392.630015	
NOR2X1	saed90nm_typ	6.005000	6	36.030001	
NOR2X2	saed90nm_typ	9.216000	2	18.431999	
NOR2X4	saed90nm_typ	14.731000	2	29.462000	
NOR3X0	saed90nm_typ	8.294000	1	8.294000	
OA21X1	saed90nm_typ	9.216000	5	46.079998	
OA22X1	saed90nm_typ	11.059000	1	11.059000	
OR4X1	saed90nm_typ	10.152000	2	20.304001	
XNOR2X1	saed90nm_typ	13.824000	8	110.592003	
XOR2X1	saed90nm_typ	13.824000	7	96.768003	
Total 30 references				3077.822028	

RTL Design Resources Report

****

Report : resources

```
Design : gcdGCDUnit_rtl
Version: K-2015.06-SP4
Date   : Sat Feb 26 20:43:14 2022
****************************************

Resource Report for this hierarchy in file ./gcd_dpath.v
===============================================================================
| Cell          | Module         | Parameters | Contained Operations       |
===============================================================================
| sub_x_2       | DW01_sub       | width=16   | GCDdpath0/sub_45 (gcd_dpath.v:45) |
| lt_x_3        | DW_cmp         | width=16   | GCDdpath0/lt_51 (gcd_dpath.v:51) |
===============================================================================

Implementation Report
===============================================================================
|                |                | Current          | Set            |
| Cell           | Module         | Implementation   | Implementation |
===============================================================================
| sub_x_2        | DW01_sub       | pparch (area,speed)               |
| lt_x_3         | DW_cmp         | pparch (area,speed)               |
===============================================================================
```

Some Issues I had

Unlike the week 1 portion of lab 4, I didn't encounter much of any issues in week 2. Since I had played with dc_shell and icc_shell quite a bit in week 1, week 2 was much smoother as a result. Due to this, I didn't have any issues in week 2. The only thing I'd like to mention was that the layout step for week 2 took a lot longer to load before I could configure my options, but that wasn't an issue as I could continue just fine when it loaded.