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Partner Sec21 Group 1: Christopher Alexman calex025 (our reports and results are unique)

Lab 2 Report

Video Checkoff

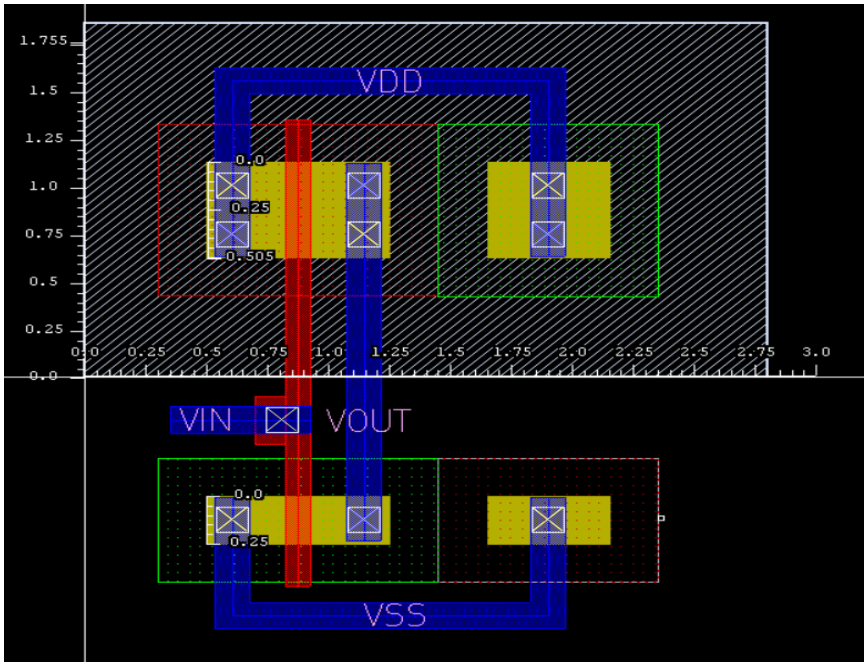
Video 1:
https://www.youtube.com/watch?v=rxLPVS0YvcM
(Includes Inverter layout, DRC pass, and LVS pass)
Video 2:
https://www.youtube.com/watch?v=GniTRf-LgQE
(Includes Nand schematic, symbol, testbench, and waveform)
Video 3:
https://www.youtube.com/watch?v=pqngl-7VWvg
(Includes Nand layout, DRC, and LVS)
*If image clarity is an issue, please increase the quality and increase window size of video

What I learned

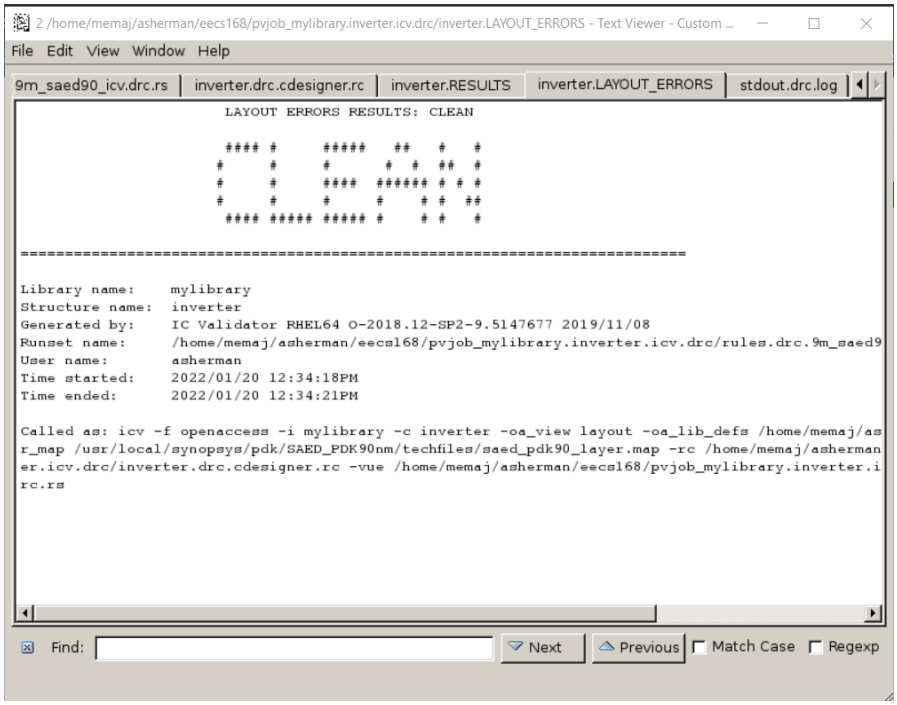
In today's lab I learned how to continue to operate many tools that can be used in this course to aid in the design of digital circuits. Specifically, I learned how to create layouts for existing schematics and match the layout to the schematic. Additionally, I learned how to adjust and move components within that layout. Furthermore, I learned how to run DRC on a layout. I also learned how to debug DRC. I also learned how to run LVS and what LVS is looking for. I also learned how to debug LVS. Finally, in this lab, I learned how to design a gate schematic and testbench from scratch, as well as how to design a layout in the same way. In the end, I learned how to perform all of these steps in a non-tutorial capacity.

Inverter Layout View

An inverter layout view as seen in Fig 11. (on next page)



DRC Result for Inverter Layout



LAYOUT ERRORS RESULTS

CLEAN

Model: Intel(R) Xeon(R) Silver 4214 CPU @ 2.20GHz

DRC Error Statistics

```
Library name:     mylibrary
Structure name:   inverter
Generated by:     IC Validator RHEL64 0-2018.12-SP2-9.5147677 2019/11/08
Runset name:      /home/memaj/asherman/eecs168/pvjob_mylibrary.inverter.icv.drc/rules.drc.9m_saed90_icv.drc.rs
User name:        asherman
Time started:     2022/01/20 12:34:18PM
Time ended:       2022/01/20 12:34:21PM

Called as: icv -f openaccess -i mylibrary -c inverter -oa_view layout -oa_lib_defs /home/memaj/asherman/eecs168/lib.defs -oa_layer_map /usr/local/synopsys/pdk/SAED_PDI
```

LVS Result for Inverter Layout

Fig 25.

VUE: [/home/memaj/asherman/eecs168/pvjob_mylibrary.inverter.icv.lvs/inverter.vue]

File View Tools Classification Windows Help

Execution | Load Results | Run Summary | LVS Errors

TOP BLOCK COMPARE RESULTS

PASS

[inverter, inverter]

Model: Intel(R) Xeon(R) Silver 4214 CPU @ 2.20GHz

Netlist Extraction Statistics

```
Library name:     mylibrary
Structure name:   inverter
Generated by:     IC Validator RHEL64 0-2018.12-SP2-9.5147677 2019/11/08
Runset name:      /home/memaj/asherman/eecs168/pvjob_mylibrary.inverter.icv.lvs/rules.lvs.9m_saed90_lvs.lvs.rs
User name:        asherman
Time started:     2022/01/20 09:25:15PM
Time ended:       2022/01/20 09:25:18PM

Called as: icv -f openaccess -i mylibrary -c inverter -oa_view layout -oa_lib_defs /home/memaj/asherman/eecs168/lib.defs -oa_layer_map /usr/local/synopsys/pdk/SAED_PDK
```

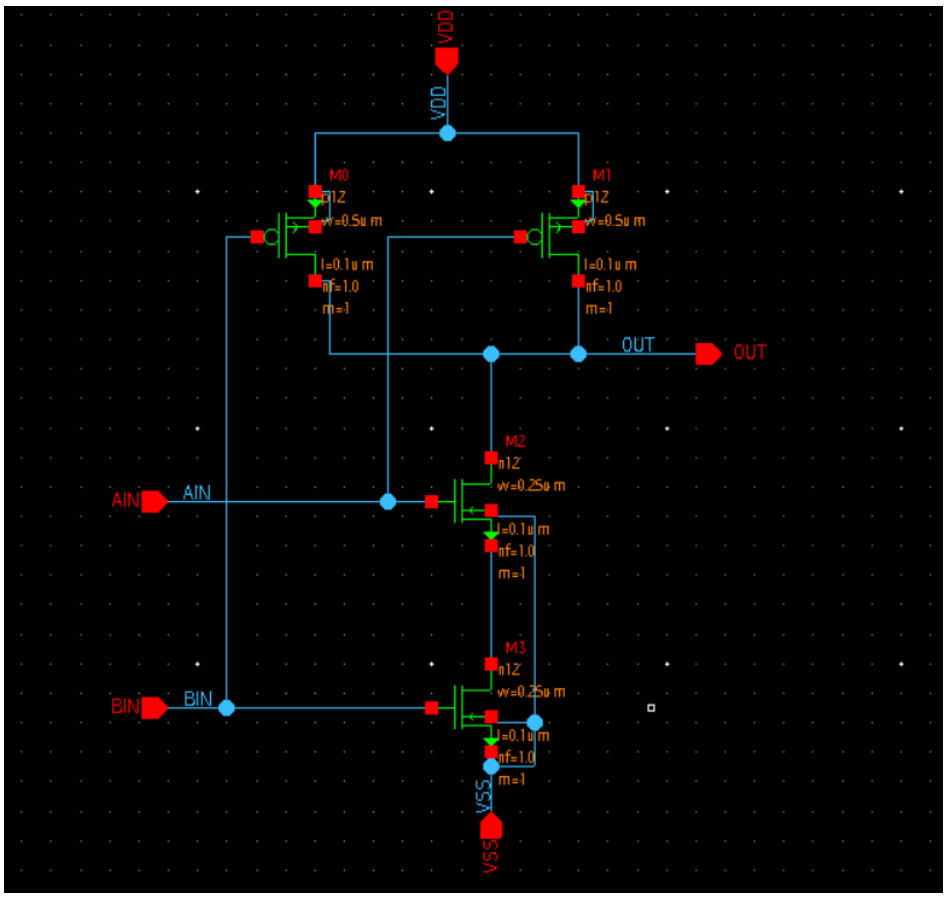
Layout vs. Schematic Statistics

```
Schematic:  /home/memaj/asherman/eecs168/pvjob_mylibrary.inverter.icv.lvs/inverter.sch_out
```

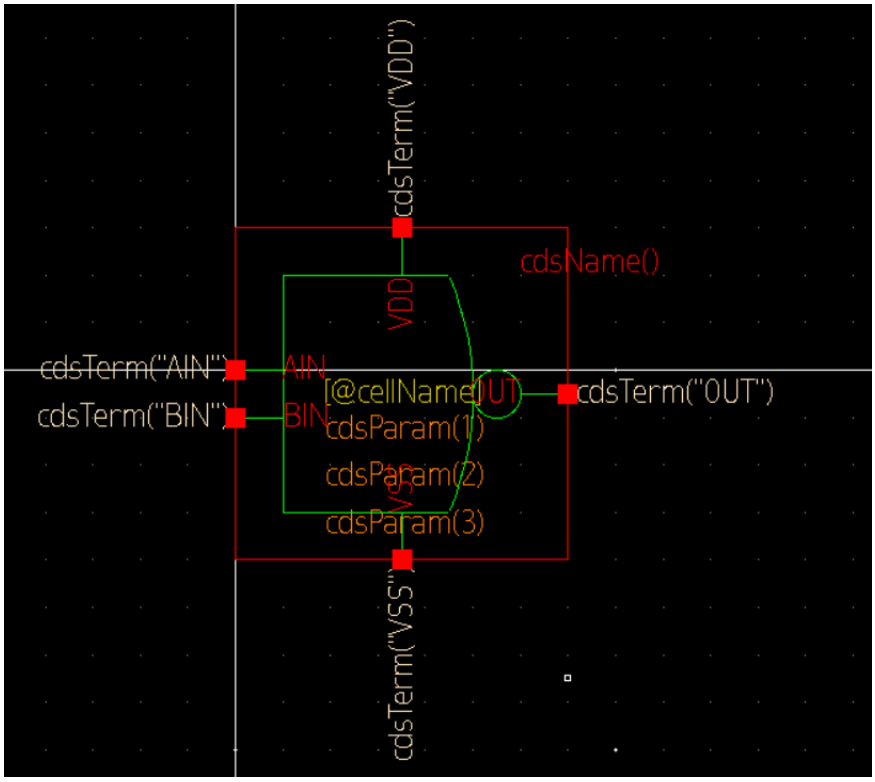
LVS Errors:

```
    1 successful equivalencies
    0 failed equivalencies
```

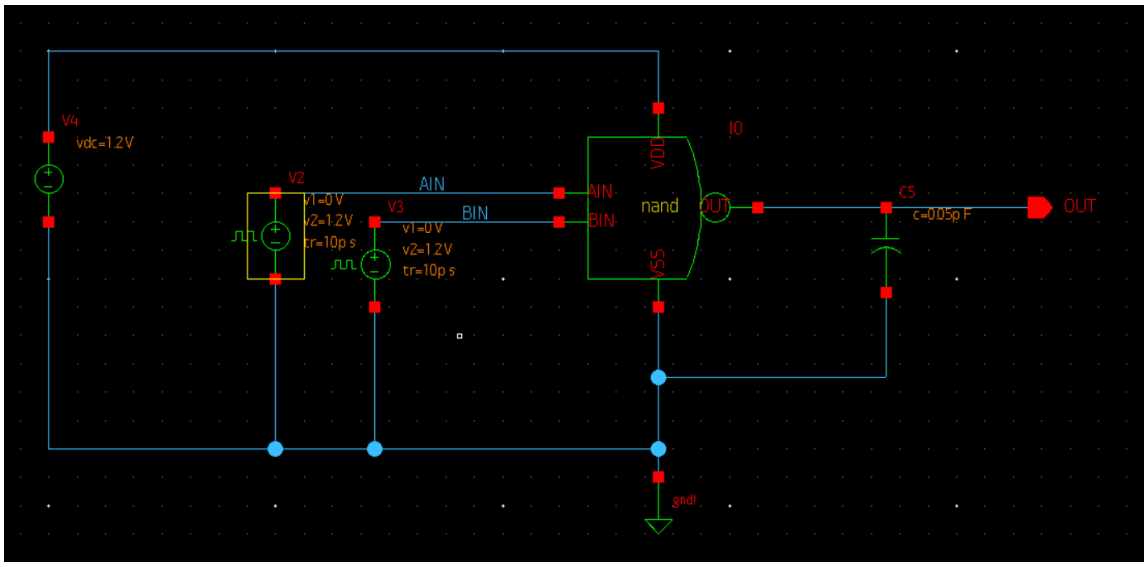
NAND Gate Schematic



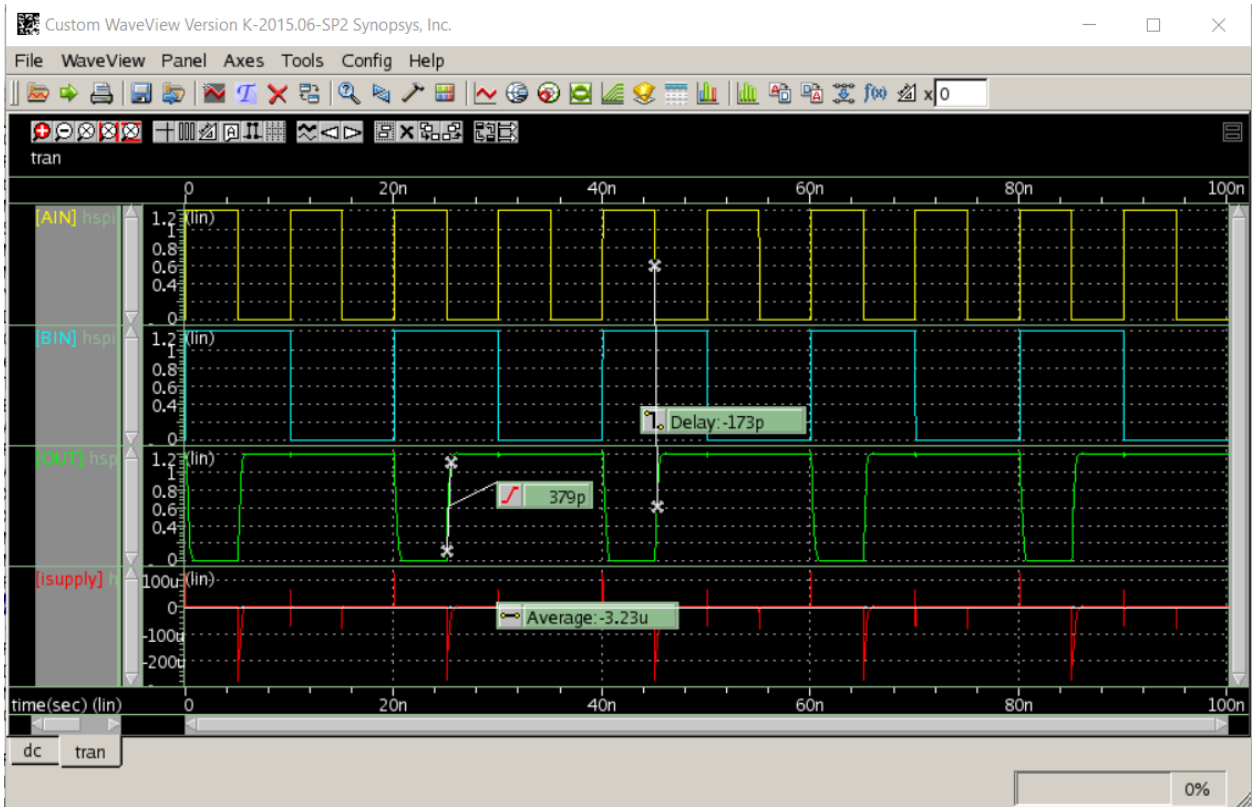
NAND Gate Symbol



NAND Gate Testbench Schematic

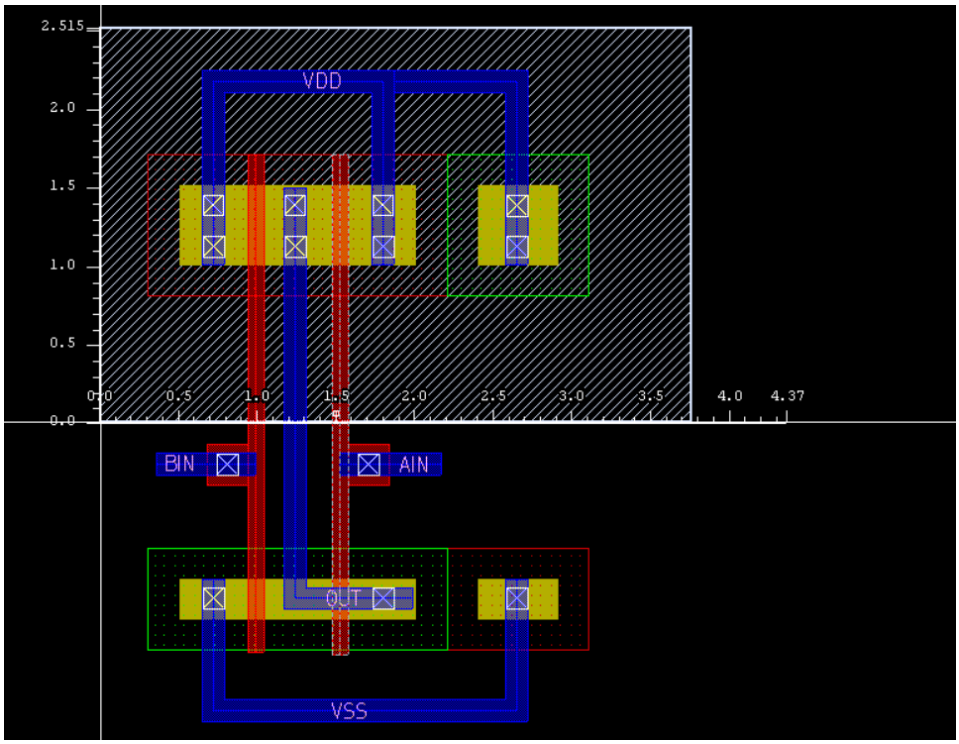


NAND Gate Waveform with measurements

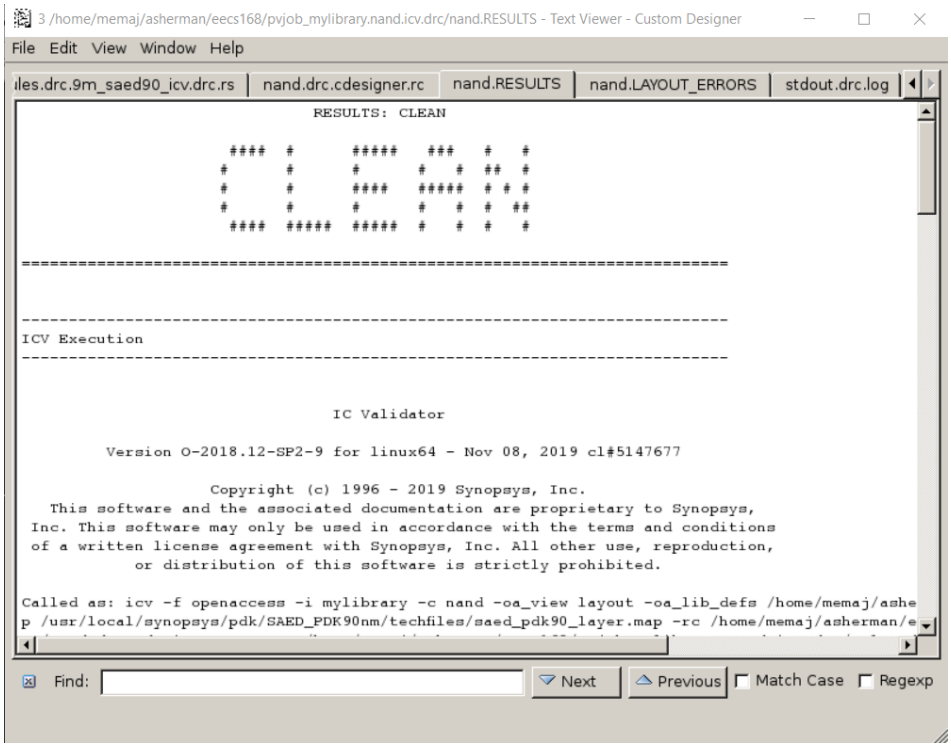


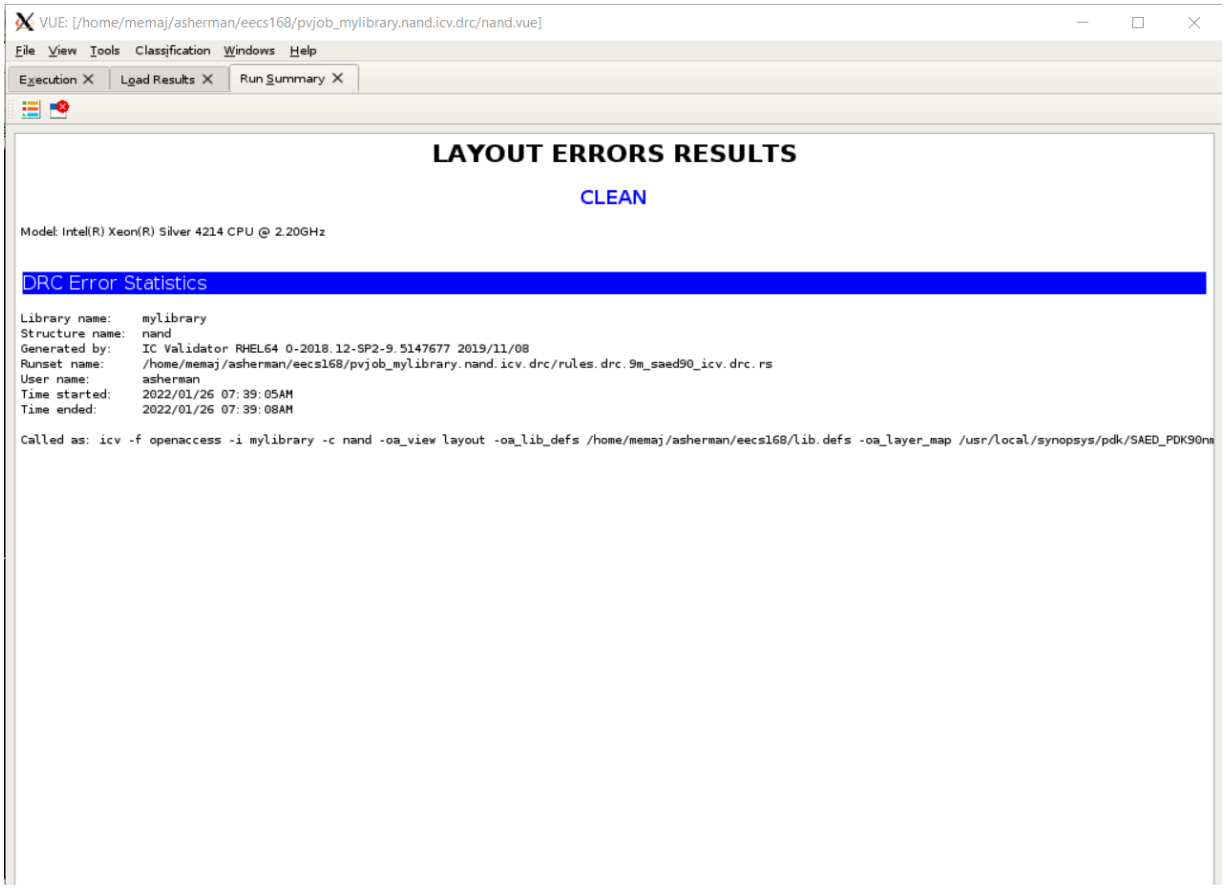
As seen in Fig 26.

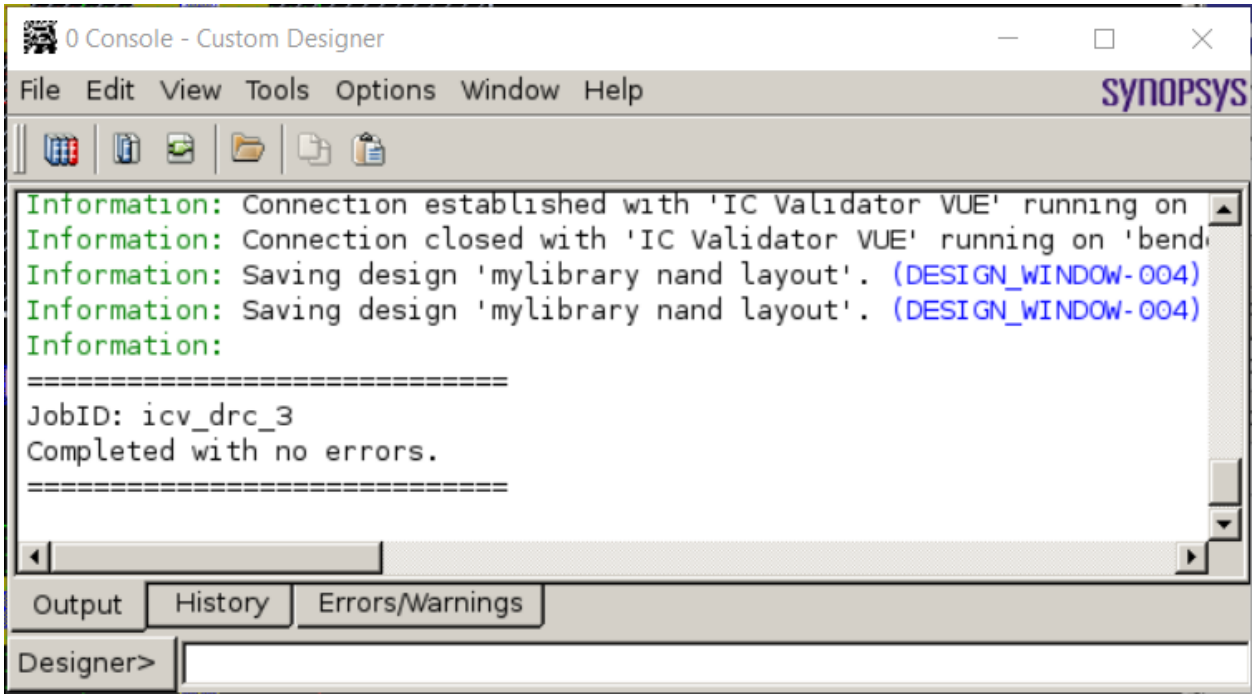
NAND Gate Layout



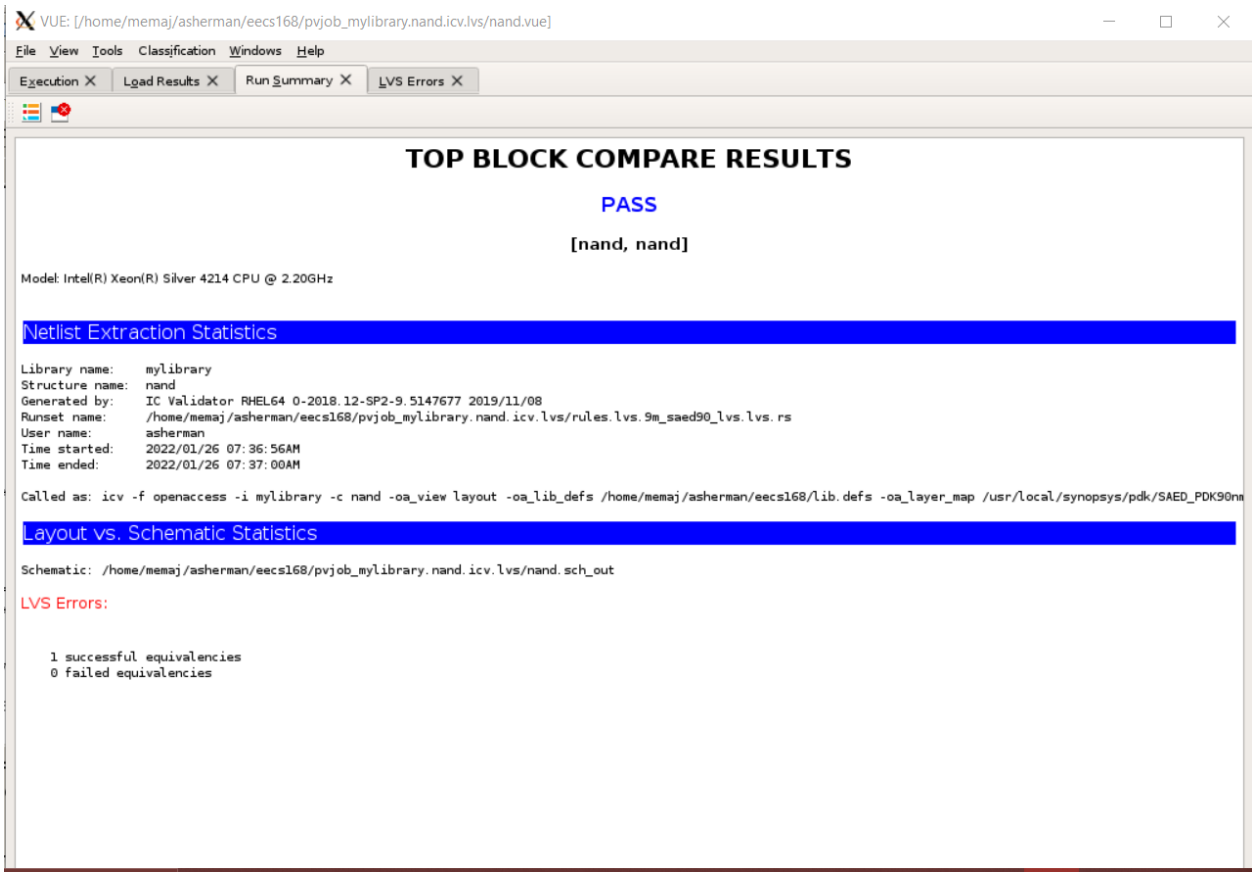
NAND Gate DRC Result

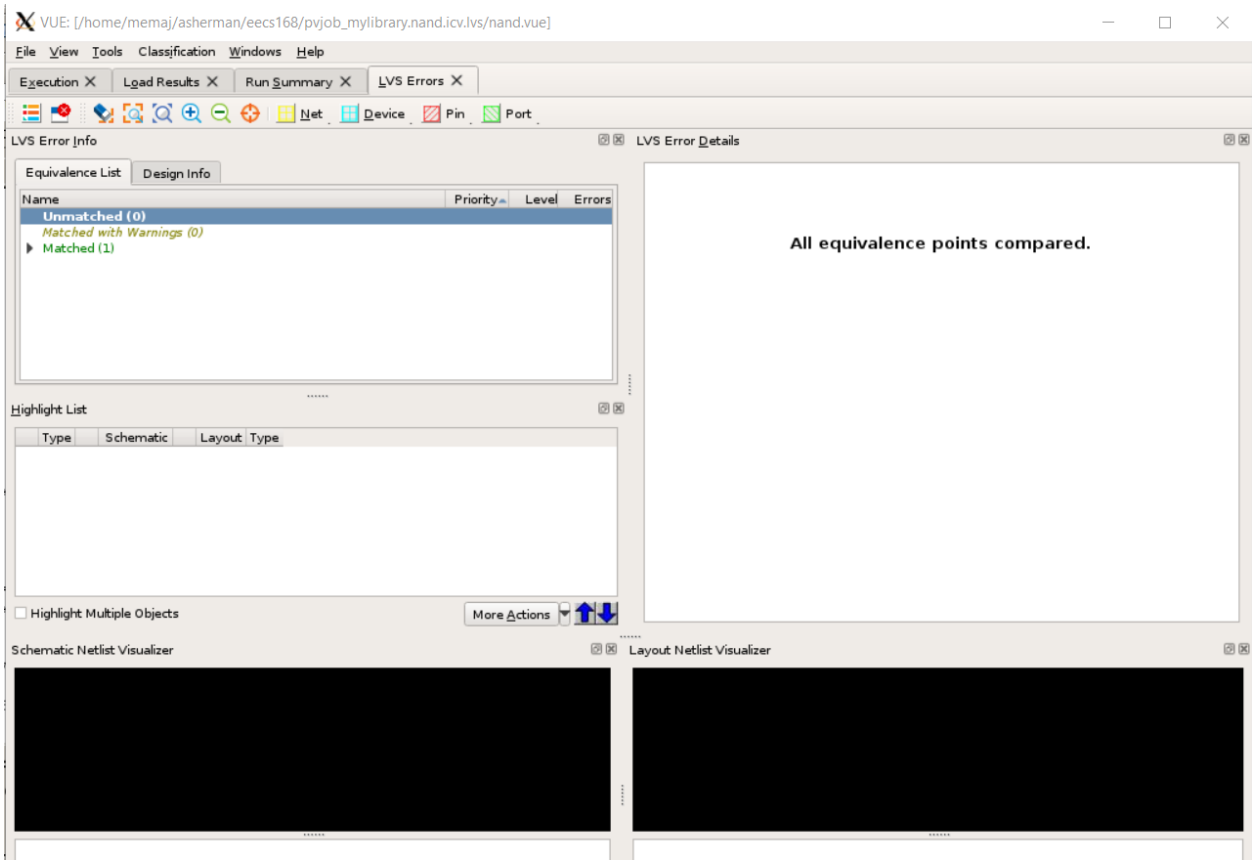


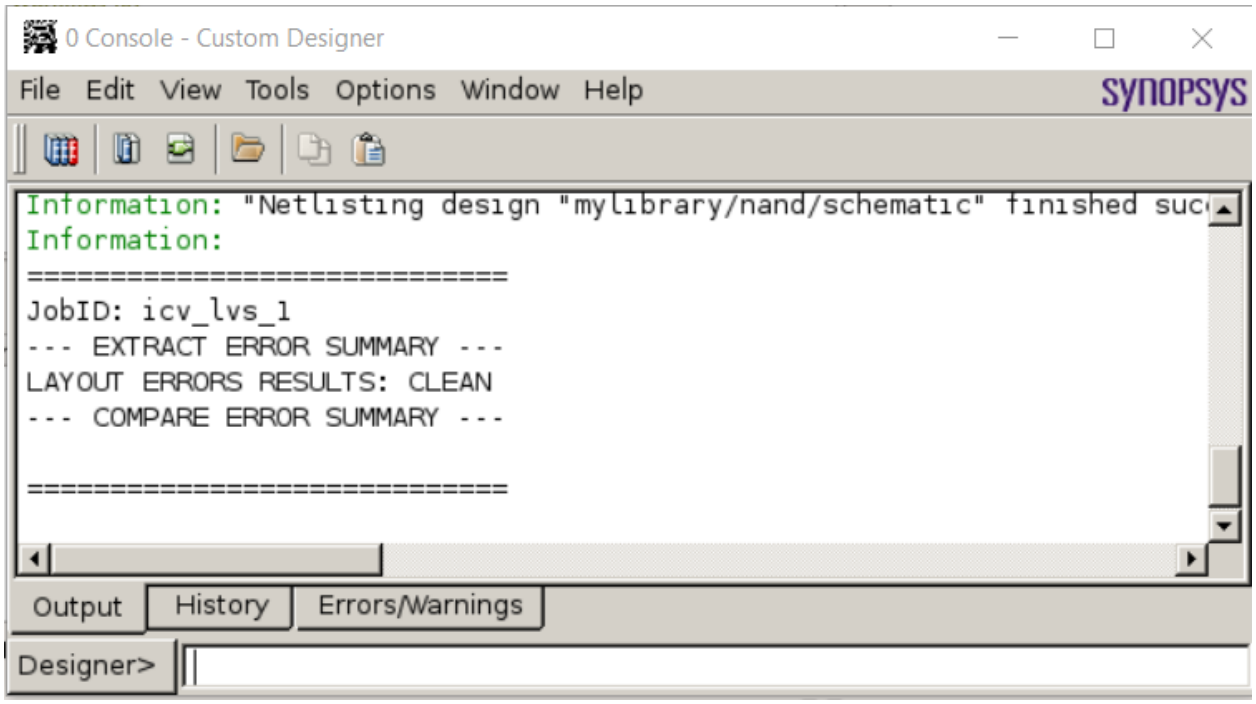




NAND Gate LVS Result




VUE: [/home/memaj/asherman/eecs168/pvjob_mylibrary.nand.icv.lvs/nand.vue]
File View Tools Classification Windows Help
Execution
Load Results
Run Summary
LVS Errors
Net
Device
Pin
Port
LVS Error Info
LVS Error Details
Equivalence List
Design Info
Name
Priority
Level
Errors
Unmatched (0)
Matched with Warnings (0)
Matched (1)
All equivalence points compared.
Highlight List
Type
Schematic
Layout Type
Highlight Multiple Objects
More Actions
Schematic Netlist Visualizer
Layout Netlist Visualizer


0 Console - Custom Designer
File Edit View Tools Options Window Help
SYNOPSYS
Information: "Netlisting design "mylibrary/nand/schematic" finished suc
Information:
==========
JobID: icv_lvs_1
--- EXTRACT ERROR SUMMARY ---
LAYOUT ERRORS RESULTS: CLEAN
--- COMPARE ERROR SUMMARY ---
==========
Output
History
Errors/Warnings
Designer>

Some Issues I had

Throughout the course of this lab, I had the most issues with the layout components of these designs. First for the inverter, I had many issues with my component placements that I needed to fix for DRC. After solving, my LVS didn't pass due to my labels not matching. After asking the TA, I realized that the issue was that I didn't set my labels as M1PIN material. The next main issue was with my NAND gate layout. My first issue was visualizing how the layout should look. I solved this through trial and error. Next was getting LVS to pass for the NAND layout. This part took me a long time. Ultimately, after speaking with my lab partner (who had a similar issue) we realized that the issue stemmed from my NAND gate schematic specifically. There had been a wire that was meant to go to VSS instead of a joining wire. After this fix, all of my issues were solved.