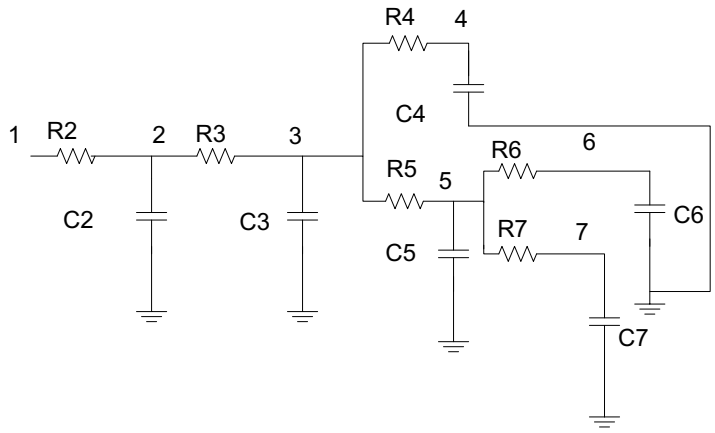
EECS 168 Introduction to VLSI Design Sheldon Tan

Homework 3

Please use the 180 nm process parameters shown at the end of homework for all the homework questions. For NMOS as $R_n = 6.47K\Omega$, for PMOS as $R_p = 29.6K\Omega$, and $C_l = 0.89f\ F$)

1. (10pt) Draw the transistor-level schematics for domino gates that implement these functions:
   (a) a+b+c
   (b) (abc)'
   (c) ((a+b)c)'

2. (10 pts) For the RC circuit shown below, compute the Elmore delays of from
   (a) from node 1 to node 4;
   (b) from node 1 to node 7;
   (c) from node 4 to node 7;



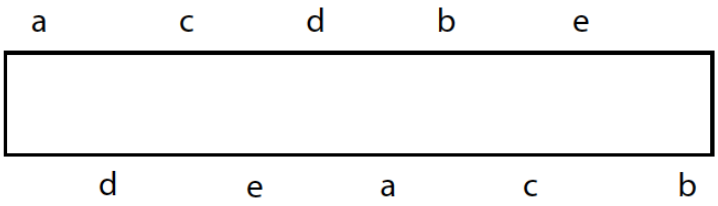
3. (20pt) Compute the Elmore delay for these wires assuming each wire is divided into 100 sections:

a) Poly wire of width 2 λ, length 1,000 λ.
b) Metal 1 wire of width 3 λ, length 1,000 λ.
c) Metal 1 wire of width 3 λ, length 10,000 λ.

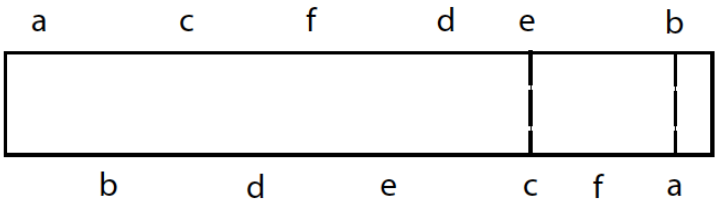
4. (20pt) Compute the optimal number of buffers and buffer sizes for these RC wires when driven by a minimum-size inverter:
   a) Poly wire of width 3 λ, length 1,000 λ.
   b) Metal 2 wire of width 3 λ, length 10,000 λ.

5. (15pt) Compute the density of these channels. Vertically aligned pins are shown with dotted lines.

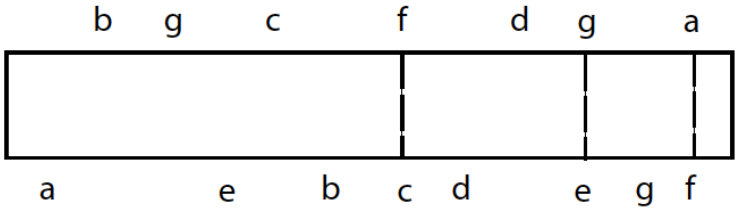
a)



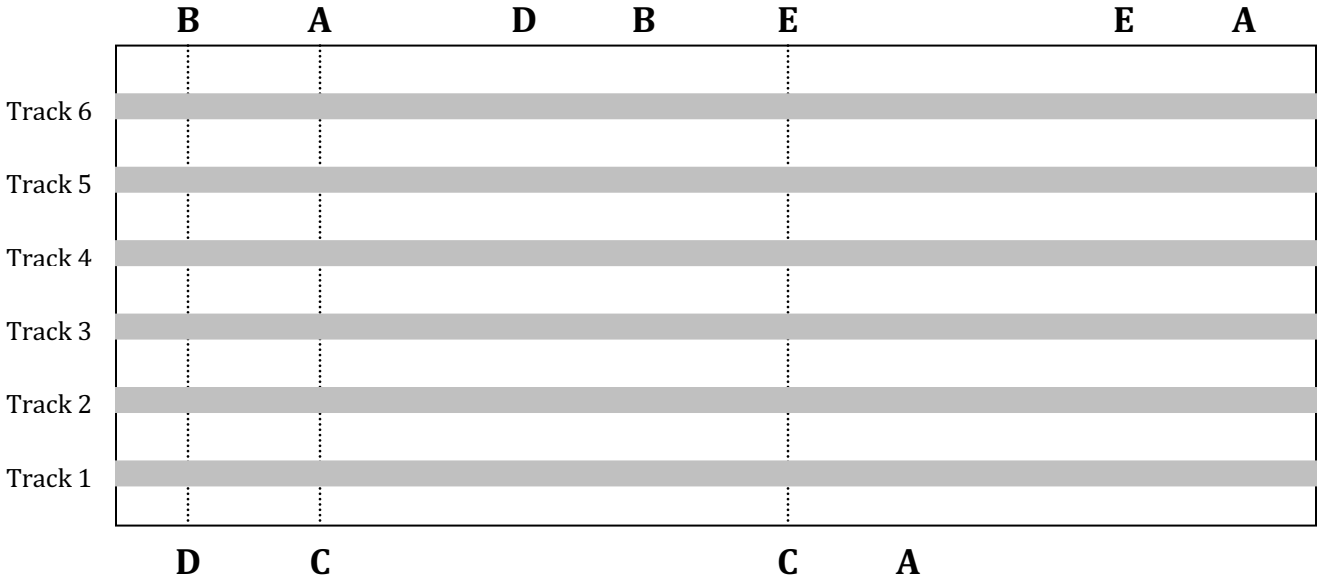
b)



c)



6. (15 pts) For the provided channel (dotted lines show the vertically aligned pins), route the channel using the left-edge algorithm.



7. (10) For each of these logic networks, draw the logic diagram and find the critical path, assuming that the delay through all *n*-input gates are *n*, delay through an inverter is 1.

   (a) NAND2(NAND2(a,b),NAND2(c,d)).
   (b) AOI21(NAND3(a,b,c), NOR2(d,e), INV(NAND2(f,g)))

8. A string of inverters drives a load of 50 pF. Assuming gate capacitance of the input inverter is 18 fF and P_{inv} is 1. To get minimal delay, you are asked to determine the number of inverter stages and sizes following the steps:

1) Use $\widehat{N} \approx \log_{\tilde{f}} F$ to estimate the number of stages N (Let $\hat{f} = 4$)
2) Calculate **path delay** and **inverter sizes** (in terms of gate capacitance) using the estimated N.
3) Calculate path delay respectively using $N + 1$ and $N - 1$. Evaluate the estimation accuracy in step 1)

n-type transconductance	k'_n	$170\mu A/V^2$
p-type transconductance	k'_p	$-30\mu A/V^2$
n-type threshold voltage	V_{tn}	0.5V
p-type threshold voltage	V_{tp}	-0.5V
n-diffusion bottomwall capacitance	$C_{ndiff,bot}$	$940aF/\mu m^2$
n-diffusion sidewall capacitance	$C_{ndiff,side}$	$200aF/\mu m$
p-diffusion bottomwall capacitance	$C_{pdiff,bot}$	$1000aF/\mu m^2$
p-diffusion sidewall capacitance	$C_{pdiff,side}$	$200aF/\mu m$
n-type source/drain resistivity	R_{ndiff}	$7\Omega/\square$
p-type source/drain resistivity	R_{pdiff}	$7\Omega/\square$
poly-substrate plate capacitance	$C_{poly,plate}$	$63aF/\mu m^2$
poly-substrate fringe capacitance	$C_{poly,fringe}$	$63aF/\mu m$
poly resistivity	R_{poly}	$8\Omega/\square$
metal 1-substrate plate capacitance	$C_{metal1,plate}$	$36aF/\mu m^2$
metal 1-substrate fringe capacitance	$C_{metal1,fringe}$	$54aF/\mu m$
metal 2-substrate capacitance	$C_{metal2,plate}$	$36aF/\mu m^2$
metal 2-substrate fringe capacitance	$C_{metal2,fringe}$	$51aF/\mu m$
metal 3-substrate capacitance	$C_{metal3,plate}$	$37aF/\mu m^2$
metal 3-substrate fringe capacitance	$C_{metal3,fringe}$	$54aF/\mu m$
metal 1 resistivity	R_{metal1}	$0.08\Omega/\square$
metal 2 resistivity	R_{metal2}	$0.08\Omega/\square$
metal 3 resistivity	R_{metal3}	$0.03\Omega/\square$
metal current limit	$I_{m,max}$	$1mA/\mu m$

Typical 180 nm process parameters