

Alejandro Sherman

Question #1: Assuming an n-type transistor with  $v_{ds}$  of 1.8V and  $V_t$  of 0.7V find the ranges of  $V_{gs}$  to put the transistor in cutoff, linear, and saturation regions.

Answer: n-type  $v_{ds} = 1.8V$   $V_t = 0.7V$

Cutoff region:  $V_{gs} < V_t$

$$V_{gs} < 0.7V$$

From lecture: 2.1

$$\text{Cutoff} = V_{gs} < V_t$$

$$\text{Linear} = V_{gs} \geq V_t$$

$$\text{Saturation} = V_{gs} \geq V_t$$

$$v_{ds} < v_{gs} - V_t$$

$$v_{ds} \geq v_{gs} - V_t$$

Linear region:  $V_{gs} \geq 0.7V$

$$1.8V < v_{gs} - 0.7V$$

$$2.5V < v_{gs}$$

still holds!

$$V_{gs} > 2.5V$$

Saturation region:  $V_{gs} \geq 0.7$

$$1.8V \geq v_{gs} - 0.7$$

$$2.5 \geq v_{gs}$$

$$0.7 \leq v_{gs} \leq 2.5$$



## Question 2

Assume a NMOS has  $V_t = 0.6V$  and  $\frac{W}{L} = \frac{5}{2}$ ,  $K_n = \frac{73\mu A}{V^2}$

Find  $I_{ds}$

From lecture 2.1:

Cutoff =  $v_{gs} < V_t$

Linear =  $v_{gs} \geq V_t$   $v_{ds} < v_{gs} - V_t$

Saturation =  $v_{gs} \geq V_t$   $v_{ds} \geq v_{gs} - V_t$

a)  $v_{ds} = 1.5V$ ,  $v_{gs} = 1V$   $\lambda = 0$

$$\begin{matrix} 1 > 0.6 \\ v_{gs} & V_t \end{matrix} \quad \& \quad \begin{matrix} 1.5 > 0.4 \\ v_{ds} & v_{gs} - V_t \end{matrix}$$

Saturation mode

$$I_{ds} = \frac{1}{2} K_n \left( \frac{W}{L} \right) (v_{gs} - V_t)^2$$

$$= \frac{1}{2} \left( \frac{73\mu A}{V^2} \right) \cdot \frac{5}{2} \cdot (1 - 0.6)^2$$

$$I_{ds} = 14.6 \mu A$$

b)  $v_{ds} = 1V$ ,  $v_{gs} = 0.5V$

$$\begin{matrix} 0.5 < 0.6 \\ v_{gs} & V_t \end{matrix} \quad \text{Cutoff mode}$$

$$I_{ds} = 0$$

c)  $v_{ds} = 0.2V$  and  $v_{gs} = 1V$

$$\begin{matrix} 1 > 0.6 \\ v_{gs} & V_t \end{matrix} \quad \begin{matrix} 0.2 < 0.4 \\ v_{ds} & v_{gs} - V_t \end{matrix}$$

Linear mode

$$I_{ds} = K_n \left( \frac{W}{L} \right) \left( (v_{gs} - V_t) v_{ds} - 0.5 v_{ds}^2 \right)$$

$$I_{ds} = \frac{73\mu A}{V^2} \left( \frac{5}{2} \right) \left( (0.4) \cdot 0.2 - 0.5 (0.2)^2 \right)$$

$$I_{ds} = 10.95 \mu A$$



Question 3 Compute the parasitic resistance of the following metal 1 wire, where the sheet resistance ( $R_{\square}$ ) of metal 1 is  $0.08 \frac{\Omega}{\square}$

$$\text{Resistance} = R_{\square} \cdot \frac{L_1}{W} + R_{\text{corner}} + R_{\square} \cdot \frac{L_2}{W}$$

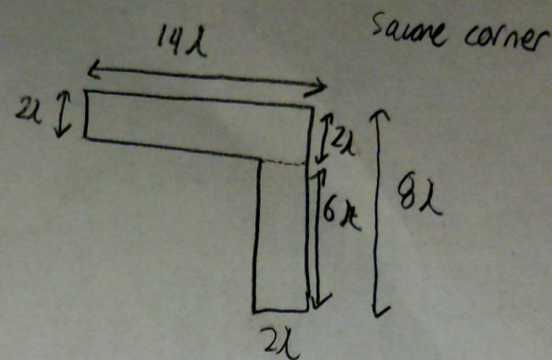
$$R_{\text{corner}} = 0.5 \cdot 0.08 \frac{\Omega}{\square} \quad W = 2\lambda$$

$$L_1 = 12\lambda$$

$$L_2 = 6\lambda$$

$$R = 0.08 \frac{\Omega}{\square} \cdot \frac{12\lambda}{2\lambda} + 0.5 \cdot 0.08 \frac{\Omega}{\square} + 0.08 \frac{\Omega}{\square} \cdot \frac{6\lambda}{2\lambda}$$

$$R = 0.76 \Omega$$



Question 4 Predict how interconnect resistance, interconnect capacitance and RC delay would change for a 90nm process from the 180nm process: Table omitted

a) Ideal scaling  $S = 0.5$

resistance:  $R' = \frac{R}{S^2} = \frac{R}{(0.5)^2} = 4R$  - Resistance increases by 4 times

capacitance:  $C' = C$  - capacitance has no change

RC delay:  $RC' = \frac{RC}{S} = 8RC$  - RC delay increases by 8 times

b) Constant dimension scaling

resistance:  $R' = R$  - Resistance has no change

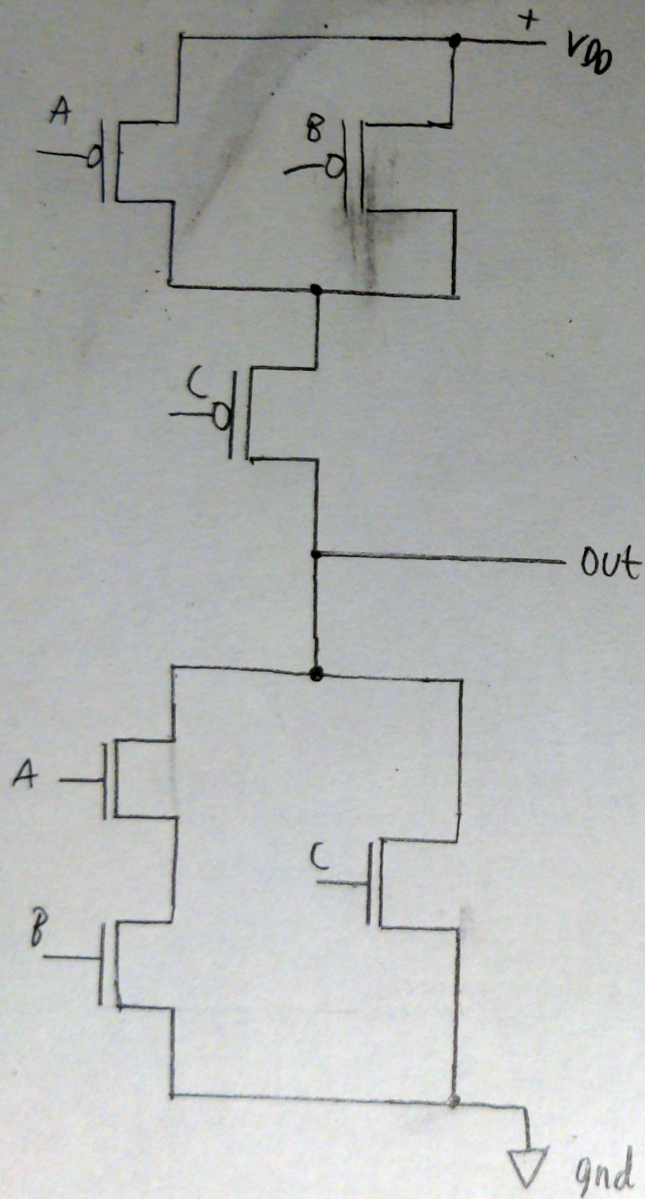
capacitance:  $C' = C$  - capacitance has no change

RC delay:  $RC' = \frac{RC}{S} = \frac{RC}{0.5} = 2RC$  - RC delay increases by 2 times



Question 5 Consider the following stick diagram. Draw the electrically equivalent transistor-level schematic. Stick diagram omitted

Identify transistor locations and route wires.  
Match pmos and nmos with pdiff and ndiff

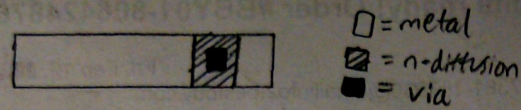




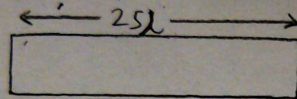
Questions Draw layouts for:

a) A metal-1 wire to n-diffusion wire through a via

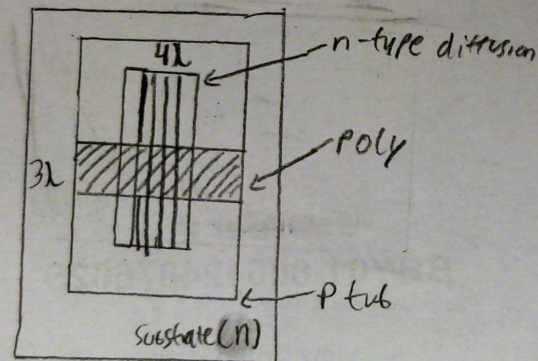
2D Topview



b) A poly wire with width of  $25\lambda$



c) A  $\frac{W}{L} = \frac{4}{3}$  n-type MOSFET transistor



d) A  $\frac{W}{L} = \frac{6}{2}$  p-type MOSFET transistor

