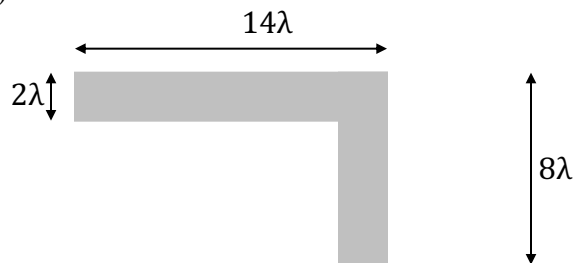


## Homework 1

- (10 pts). Assuming an n-type transistor with  $V_{ds}$  of 1.8V and  $V_t$  of 0.7V, find the ranges of  $V_{gs}$  to put the transistor in cutoff, linear, and saturation regions.
- (10 pt). Assume a NMOS has  $V_t = 0.6V$  and  $W/L = 5/2$ ,  $k_n = 73\mu A/V^2$ . Calculate the drain current  $I_{ds}$  for the given  $V_{ds}$  and  $V_{gs}$ . Assume  $\lambda = 0$ 
  - $V_{ds} = 1.5V$ ,  $V_{gs} = 1V$
  - $V_{ds} = 1V$ ,  $V_{gs} = 0.5V$
  - $V_{ds} = 0.2V$ ,  $V_{gs} = 1V$
- (15 pts). Compute the parasitic resistance of the following metal wire, where the sheet resistance ( $R_\square$ ) of metal1 is  $0.08\Omega/\square$ .

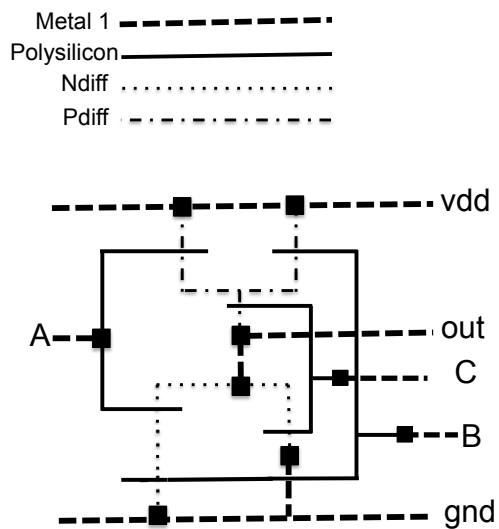


- (20 pts). Predict how interconnect resistance, interconnect capacitance and RC delay would change for a 90nm processing from the 180nm process: (a) Ideal scaling and (b) Constant dimension scaling. (tip: the scaling factor  $S=0.5$ ).

Table: Interconnect scaling trends ( $S$ : scaling factor)

	ideal scaling	constant dimension scaling
line width and spacing	$S$	1
wire thickness	$S$	1
interlevel dielectric thickness	$S$	1
wire length	$1/\sqrt{S}$	$1/\sqrt{S}$
resistance per unit length	$1/S^2$	1
capacitance per unit length	1	1
RC delay	$1/S^3$	$1/S$
current density	$1/S$	$S$

5. (20 pts). Consider the following stick diagram. Draw the electrically equivalent transistor-level schematic.



- 6.. (15pt). Draw layouts for:

- A metal-1 wire to n-diffusion wire through a via
- A poly wire with width of  $25 \lambda$
- A  $W/L = 4/3$  n-type MOSFET transistor
- A  $W/L = 6/2$  p-type MOSFET transistor