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Partner Sec21 Group 1: Christopher Alexman calex025 (our reports and results are unique)

Lab 3 Part 1 Report

Video Checkoff

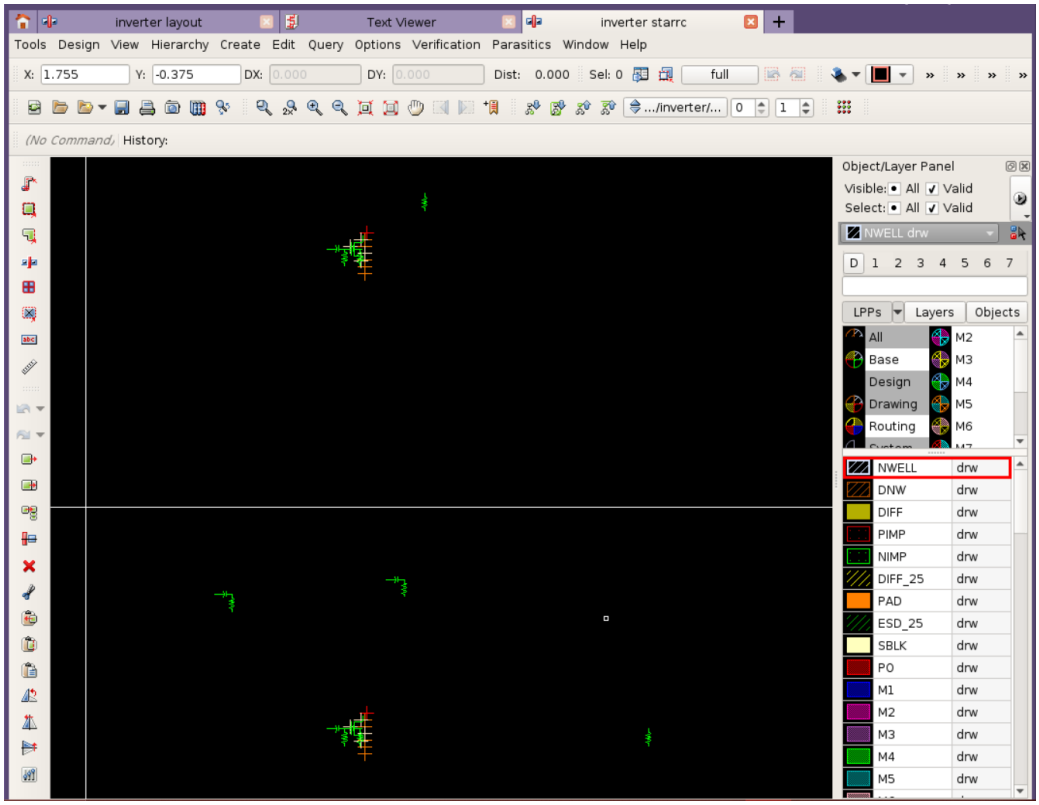
Video Checkoff 1:
https://www.youtube.com/watch?v=2M-6-hjAQQE
(Includes Ring Oscillator Schematic(hierarchical design), Ring Oscillator Layout, Testbench, and post simulation result)
*If image clarity is an issue, please increase the quality and increase window size of video

What I learned

In today's lab I learned how to create design configs from component layouts and schematics and how to run LPE to generate a parasitic view of the testbench of a design after running DRC and LVS to ensure all placements match. Additionally, I learned how to generate a waveform that applies parasitics. Furthermore, by building my ring oscillator, I learned how to use previously created components in a new cell view, in this case, reusing my inverter design. This reusing applies both to schematic creation and layout connection as five instances of my inverter layout were used in my ring oscillator layout. Additionally, I learned how to perform all the needed tasks for this part under the new cdesigner layout after the license update.

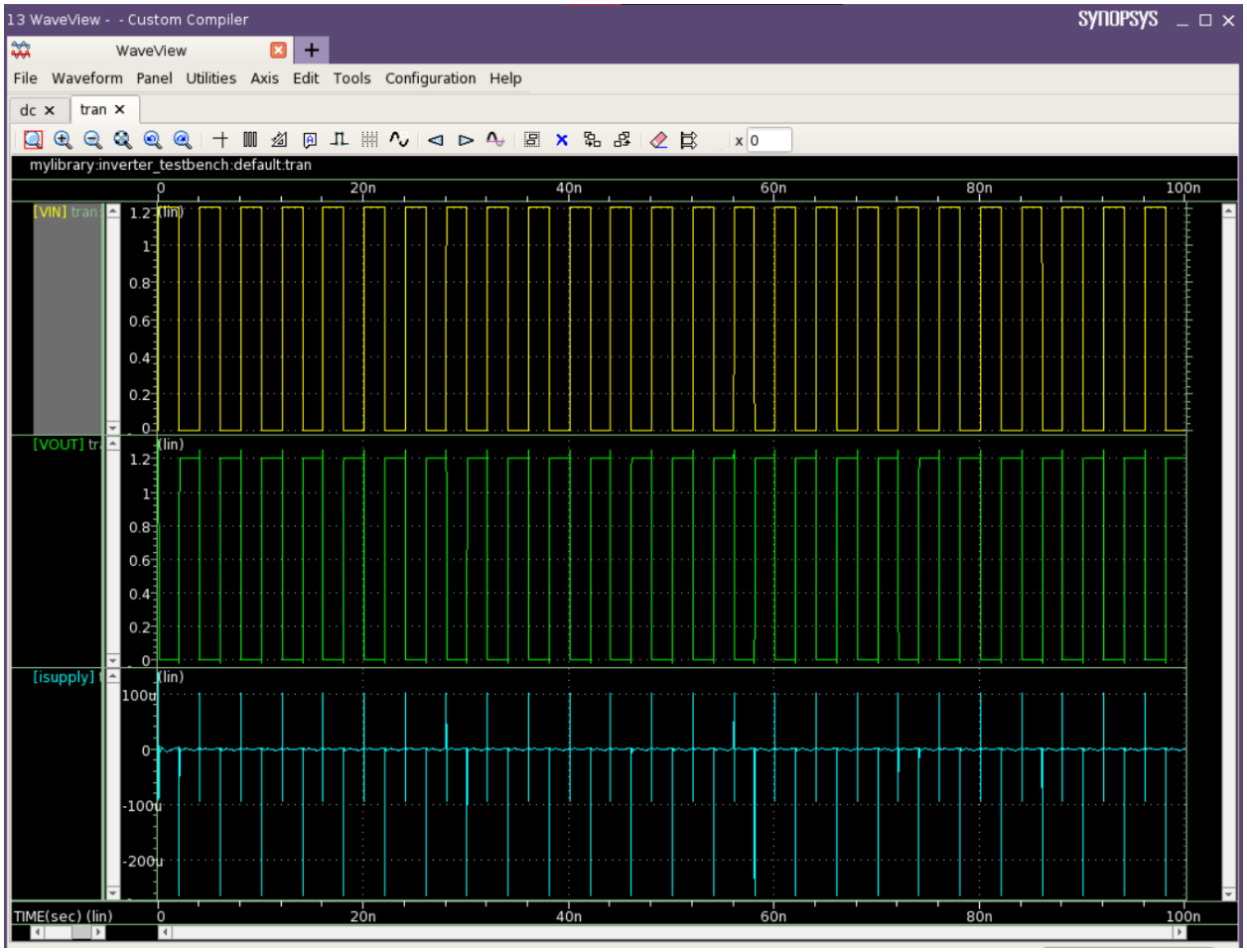
Inverter Parasitic View

Fig 9

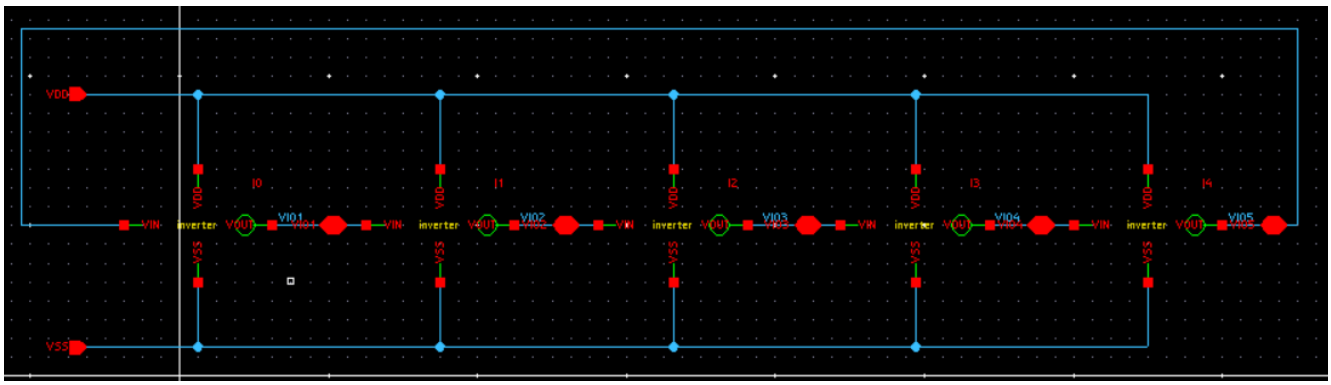


Inverter Simulation result with parasitic extraction

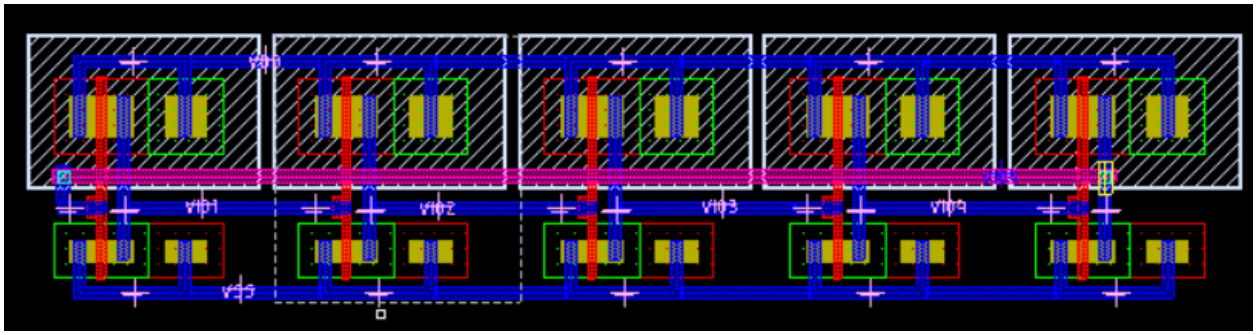
Fig 18



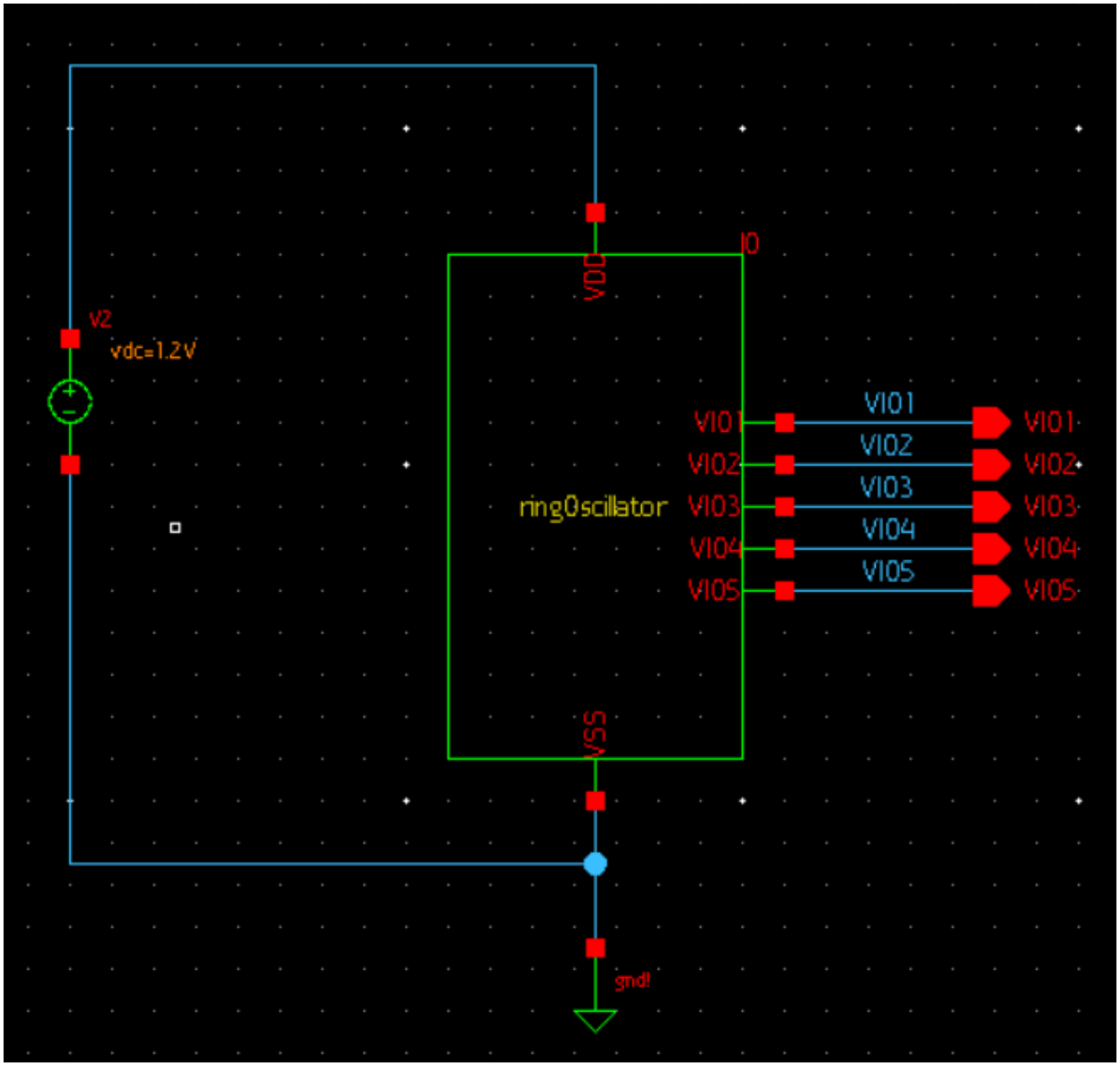
Ring Oscillator Schematic



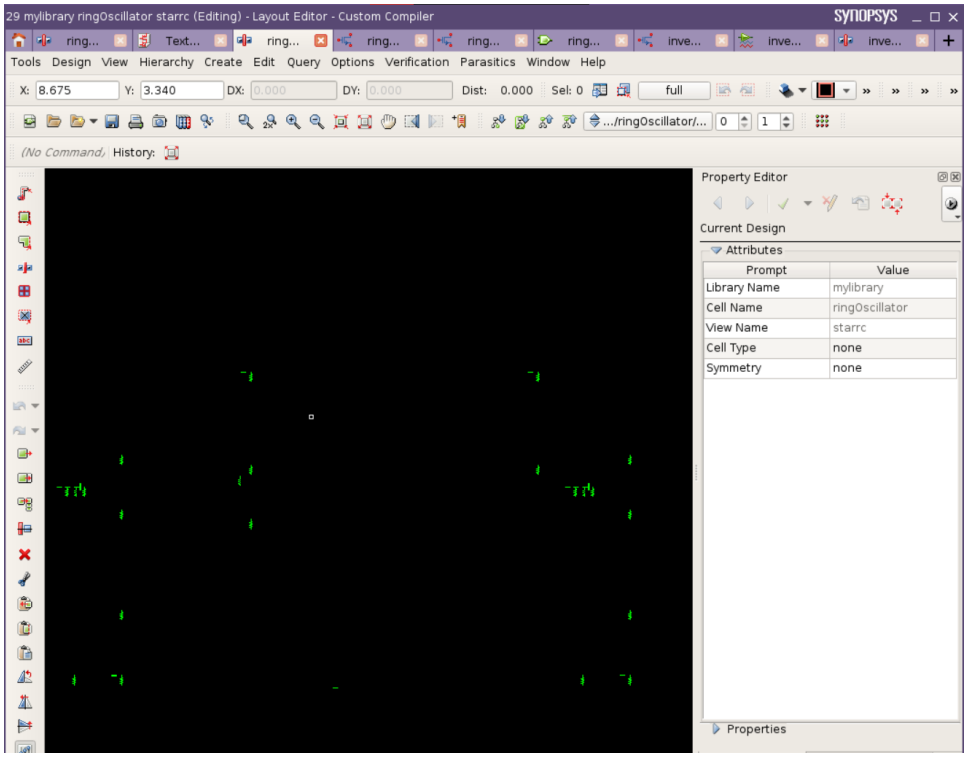
Ring Oscillator Layout



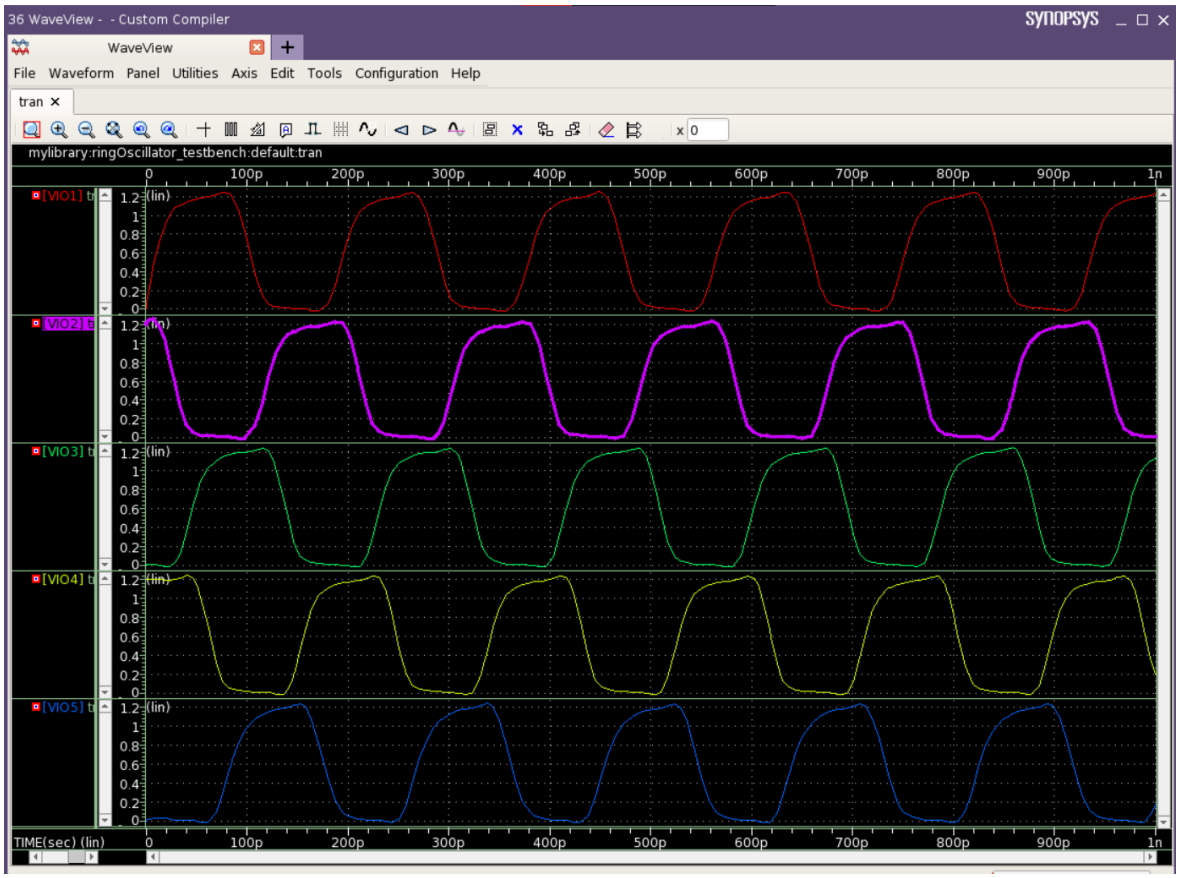
Ring Oscillator Testbench



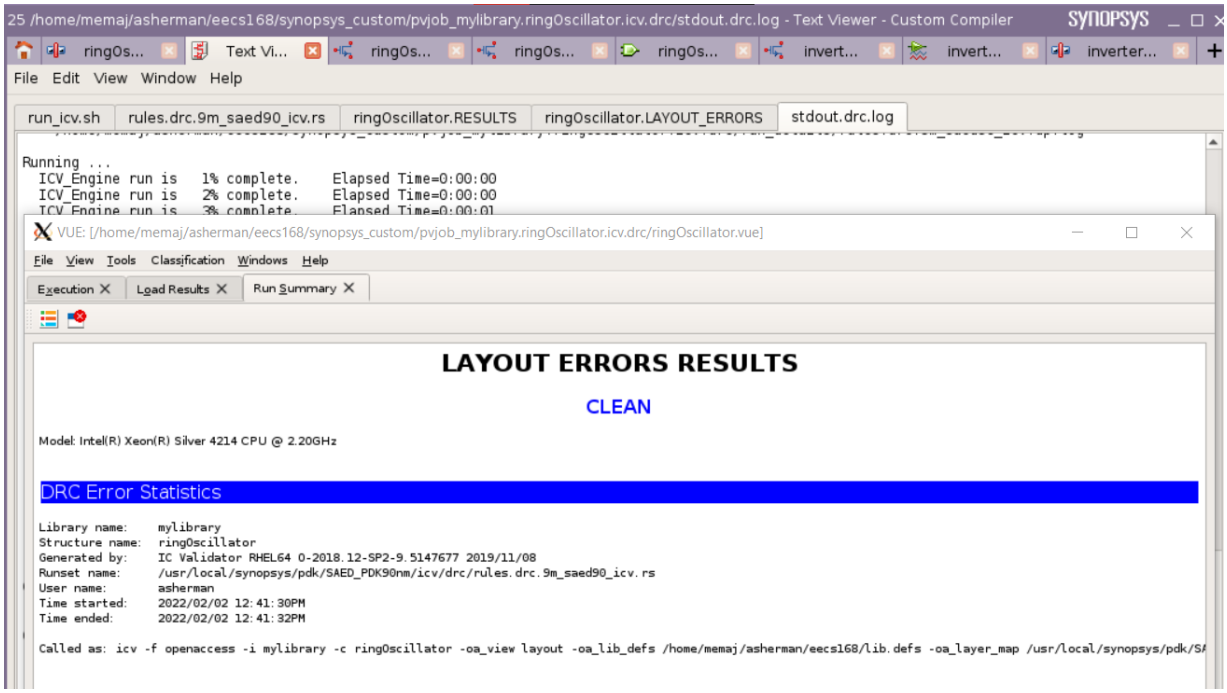
Ring Oscillator Parasitic View



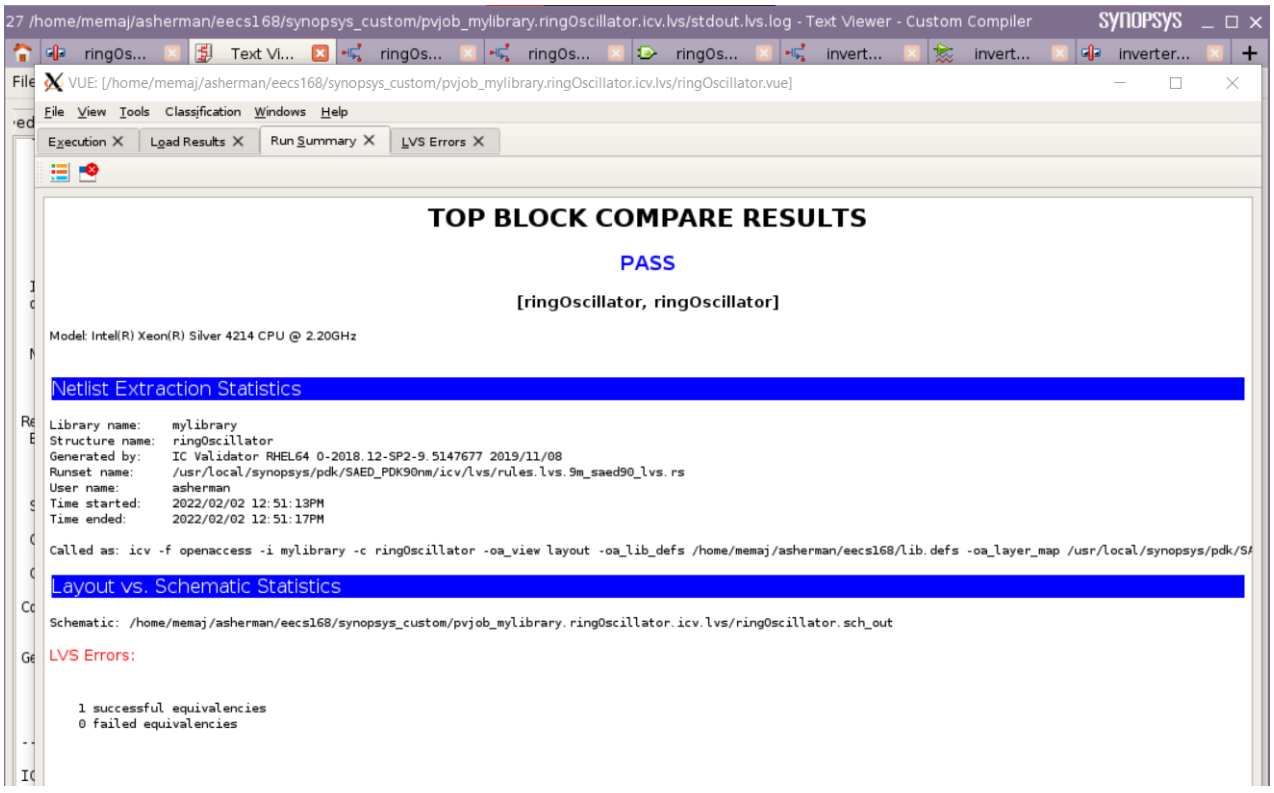
Ring Oscillator POST (Layout) SIMULATION result



Ring Oscillator DRC Pass



Ring Oscillator LVS Pass



Some Issues I had

The biggest issue I encountered while working on this part of lab 3 was one that many other students encountered. This issue was an incorrect inverter waveform with parasitics applied. In the generated waveform, the output signal of the inverter was not inverted at all, and the isupply was a solid negative line. This issue was brought up to the TA's and with their help we realized that a few settings were no longer set by default when running LPE when compared to the previous cdesigner program. So to fix this, we set LPE to extract power nets and provide the "-clean" argument. These changes worked for both the parasitic waveform of the inverter and ring oscillator. Any other issues in this lab were related to version changes present between the current newer version of cdesigner and the older version we used before. Such as some options being renamed (SAE -> PrimeWave) and the property editor being relocated, but these issues were minimal overall.