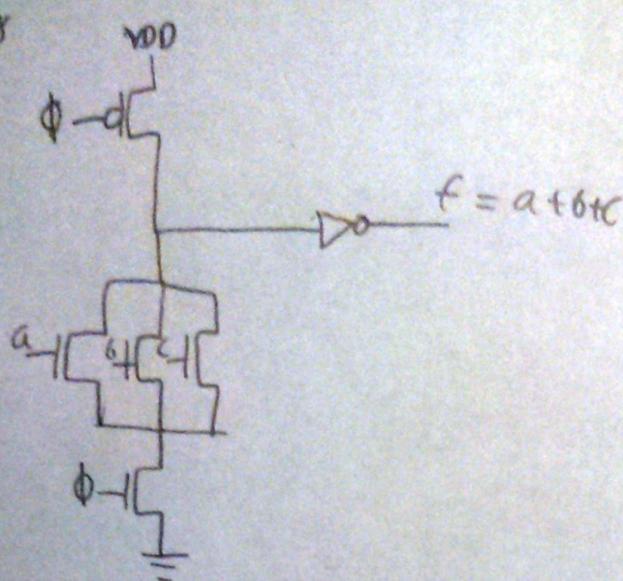


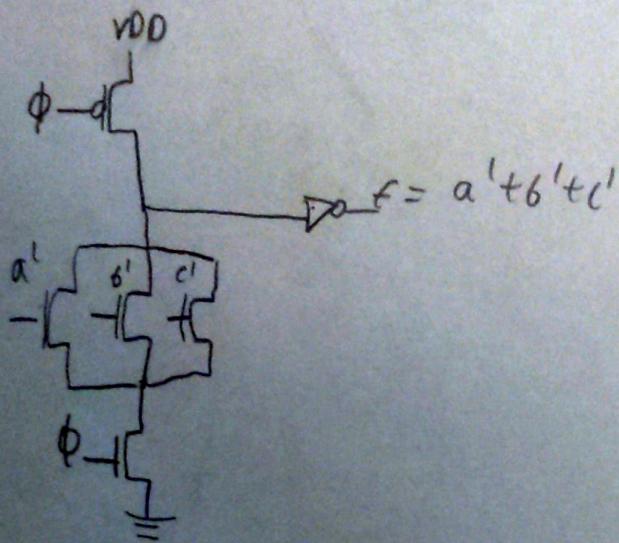
1) Draw the transistor-level schematics for dominoes that implement

these functions

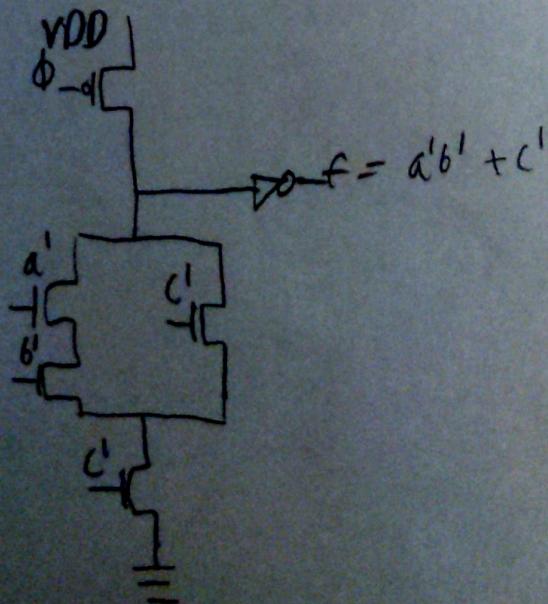
$$c) a + b + c$$



$$d) (a'b'c')' = a' + b' + c'$$



$$e) ((a+b)c)' = a'b' + c'$$



2) For the RC circuit below complete the Elmore delays

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a) node 1 to node 4

$$D_{14} = R_2(C_2 + C_3 + C_4 + C_5 + C_6 + C_7) + R_3(C_3 + C_4 + C_5 + C_6 + C_7) + R_4(C_4)$$

b) node 1 to node 7

$$D_{17} = R_2(C_2 + C_3 + C_4 + C_5 + C_6 + C_7) + R_3(C_3 + C_4 + C_5 + C_6 + C_7) + R_5(C_5 + C_6 + C_7) + R_7(C_7)$$

c) node 4 to node 7

$$D_{47} = D_{37} - D_{34}$$

$$= (R_5(C_5 + C_6 + C_7) + R_7(C_7)) - (R_4(C_4))$$

3) Compute Elmore delay for tree under assuming
each wire is divided into 100 regions

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a) Poly wire of width 2λ , length 1000λ

$$R = \frac{L}{w} \times \frac{R_{Poly}}{D} = \frac{1000\lambda}{2\lambda} \times 8 = 4000\Omega$$

$$C = C_{plate} + C_{fringe}$$

$$C_{plate} = A_C + C_{Poly,p}$$

$$= 1000\lambda \times 2 \times 0.09^2 \times 63 \times 10^{-18} F$$

$$= 1.02 \times 10^{-15} F$$

$$C_{fringe} = P_C \times C_{Poly,f}$$

$$= (100\lambda + 2\lambda) \times 2 \times 63 \times 10^{-18} F$$

$$= 1.136 \times 10^{-14} F$$

$$(= 1.238 \times 10^{-14} F)$$

For each section

$$R_{sec} = \frac{R}{100} = \frac{4000}{100} = 40\Omega$$

$$C_{sec} = \frac{C}{100} = 1.238 \times 10^{-16} F$$

Elmore delay is

$$D = R_{sec} \times (sec \times \frac{n(n-1)}{2})$$

$$= 40 \times 1.238 \times 10^{-16} \times \frac{100(100-1)}{2}$$

$$= 2.45 \times 10^{-11} S$$

b) Metal 1 of width 3λ , length 1000λ

$$R = \frac{L}{w} \times \frac{R_{M1}}{D} = \frac{1000\lambda}{3\lambda} \times 0.08 = 26.667\Omega$$

$$C = C_{plate} + C_{fringe}$$

$$C_{plate} = A_C + C_{M1,p}$$

$$= 1000\lambda \times 3 \times 0.09^2 \times 36 \times 10^{-18} F$$

$$= 8.740 \times 10^{-16} F$$

$$C_{fringe} = P_C \times C_{M1,f}$$

$$= (100\lambda + 3\lambda) \times 2 \times 54 \times 10^{-18} F$$

$$= 9.749 \times 10^{-15} F$$

$$C = 10.6 \times 10^{-15} F$$

For each section

$$R_{sec} = \frac{R}{100} = \frac{26.667}{100} = 0.26667\Omega$$

$$C_{sec} = \frac{C}{100} = 10.6 \times 10^{-17} F$$

Elmore delay is

$$D = R_{sec} \times (sec \times \frac{n(n-1)}{2})$$

$$= 0.26667 \times 10.6 \times 10^{-17} \times \frac{100(100-1)}{2}$$

$$= 1.399 \times 10^{-13} S$$

Q) Metal 2 wire of width 3λ , length $10,000\lambda$

$$R = \frac{L}{A} \times \frac{R_{M2}}{\square} = \frac{10,000\lambda}{3\lambda} \times 0.08 = 266.667 \Omega$$

$$C = C_{plate} + C_{trace}$$

$$\begin{aligned}C_{plate} &= \lambda C + C_{M2,P} \\&= 10,000 \times 3 \times 0.09^2 \times 36 \times 10^{-18} F \\&= 8.748 \times 10^{-15} F\end{aligned}$$

$$C_{trace} = \rho C \times C_{M2}$$

$$\begin{aligned}&= (10,000 \lambda + 3\lambda) \times 2 \times 54 \times 10^{-18} F \\&= 9.723 \times 10^{-14} F\end{aligned}$$

$$C = 10.5978 \times 10^{-14} F$$

For each section:

$$R_{sec} = \frac{R}{100} = 2.667 \Omega$$

$$C_{sec} = \frac{C}{100} = 10.5978 \times 10^{-16} F$$

Extra delay is

$$\begin{aligned}D &= R_{sec} \times C_{sec} \times \frac{n(n-1)}{2} \\&= 2.667 \times 10.5978 \times 10^{-16} \times \frac{100(100-1)}{2} \\&= \boxed{1.399 \times 10^{-11} S}\end{aligned}$$

4) Compute the optimal number of buffers and buffer sizes for three RC units driven by a minimum-size inverter.

a) Poly wire of width 32, length 1,000 λ

Consider the fall time:

$$t_{\text{fall}} = R_n = 6.47 \text{ k}\Omega$$

$$C_0 = 2CL = 2 \times 0.89 \text{ fF} = 1.78 \times 10^{-15}$$

$$R_{\text{int}} = \frac{L}{w} \times \frac{R_{\text{ain}}}{D} = \frac{1,000\lambda}{32} \times 8 = 2666.67 \text{ }\Omega$$

$$C_{\text{int}} = C_{\text{plate}} + C_{\text{fringe}}$$

$$C_{\text{plate}} = 1000 \times 3 \times 0.09^2 \times 63 \times 10^{-18} \text{ F}$$

$$C_{\text{fringe}} = (1000\lambda + 32) \times 2 \times 63 \times 10^{-18} \text{ F}$$

$$C = 1.29 \times 10^{-14} \text{ F}$$

$$K = \sqrt{\frac{0.4 \times R_{\text{int}} \times C_{\text{int}}}{0.7 \times R_n C_0}}$$

$$= \sqrt{\frac{0.4 \times 2666.67 \times 1.29 \times 10^{-14}}{0.7 \times 6.47 \times 10^3 \times 1.78 \times 10^{-15}}} =$$

$$= \sqrt{1.707} = 1.306 \approx 1 \text{ section}$$

$$h = \sqrt{\frac{R_n C_0}{R_{\text{int}} C_0}} = \sqrt{\frac{6.47 \times 10^3 \times 1.29 \times 10^{-14}}{2666.67 \times 1.78 \times 10^{-15}}} =$$

$$h = \sqrt{17.58}$$

$$h = 4.19$$

b) Metal2 wire of width 32, length 10,000 λ

Consider the fall time:

$$R_{\text{dian}} = R_n = 6.47 \text{ k}\Omega$$

$$C_0 = 2CL = 2 \times 0.89 \text{ fF} = 1.78 \times 10^{-15}$$

$$R_{\text{int}} = \frac{L}{w} \times \frac{R_{\text{ain}}}{D} = \frac{10,000\lambda}{32} \times 0.08 = 266.67 \text{ }\Omega$$

$$C_{\text{int}} = C_{\text{plate}} + C_{\text{fringe}}$$

$$C_{\text{plate}} = 10000 \times 3 \times 0.09^2 \times 36 \times 10^{-18} \text{ F}$$

$$C_{\text{fringe}} = (10,000\lambda + 32) \times 0.09 \times 51 \times 10^{-18} \text{ F}$$

$$C = 1.006 \times 10^{-13} \text{ F}$$

$$K = \sqrt{\frac{0.4 \times R_{\text{int}} \times C_{\text{int}}}{0.7 \times R_n C_0}}$$

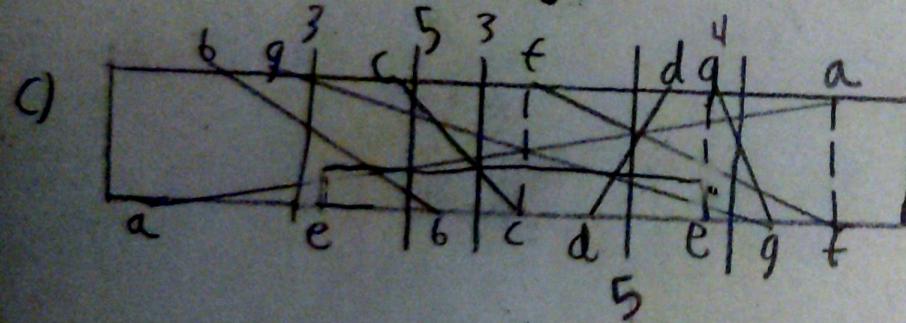
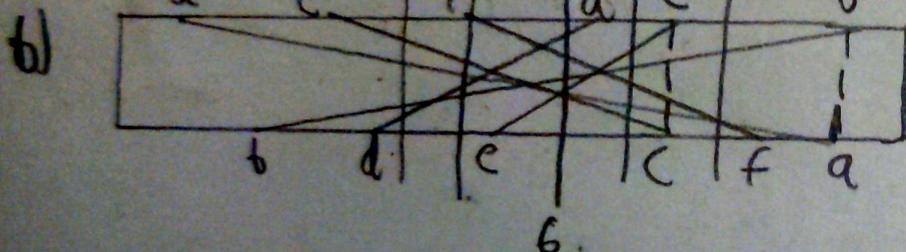
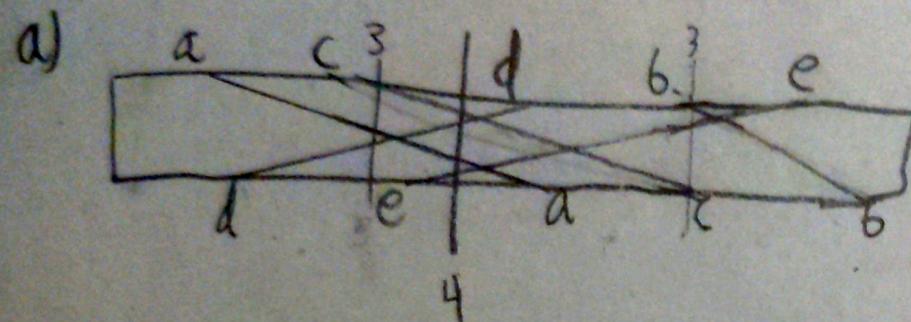
$$= \sqrt{\frac{0.4 \times 266.67 \times 1.006 \times 10^{-13}}{0.7 \times 6.47 \times 10^3 \times 1.78 \times 10^{-15}}} =$$

$$= \sqrt{1.33} = 1.1537 \approx 1 \text{ section}$$

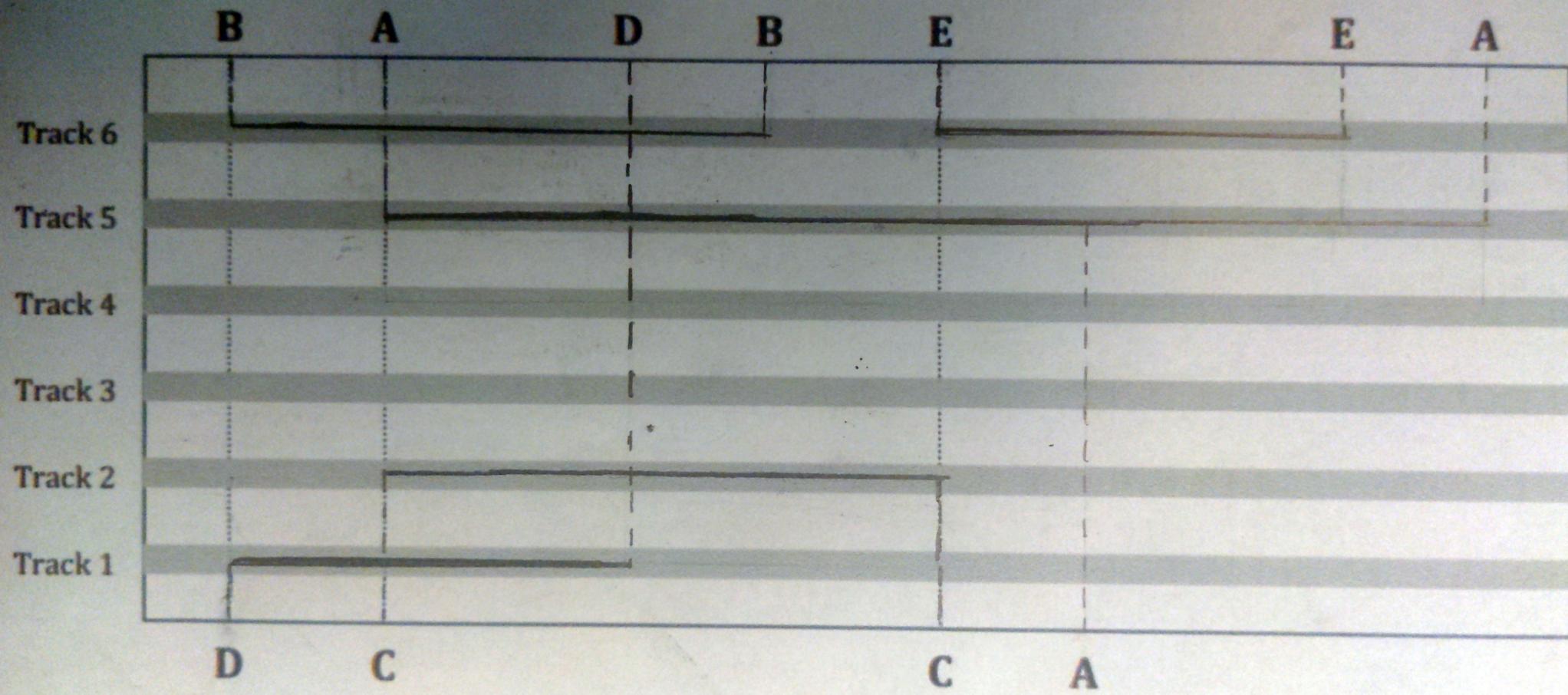
$$h = \sqrt{\frac{R_n C_0}{R_{\text{int}} C_0}} = \sqrt{\frac{6.47 \times 10^3 \times 1.006 \times 10^{-13}}{266.67 \times 1.78 \times 10^{-15}}} =$$

$$= \sqrt{1371.2} = 37.03$$

5) Compute the density of these channels. Vertically aligned pins are shown with dotted lines.



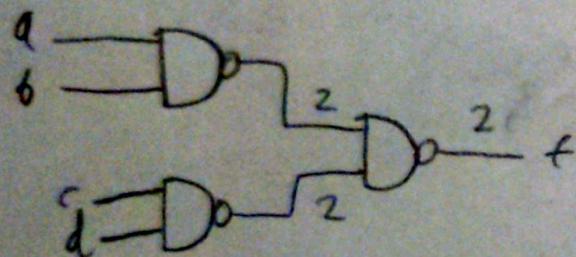
6. (15 pts) For the provided channel (dotted lines show the vertically aligned pins), route the channel using the left-edge algorithm.



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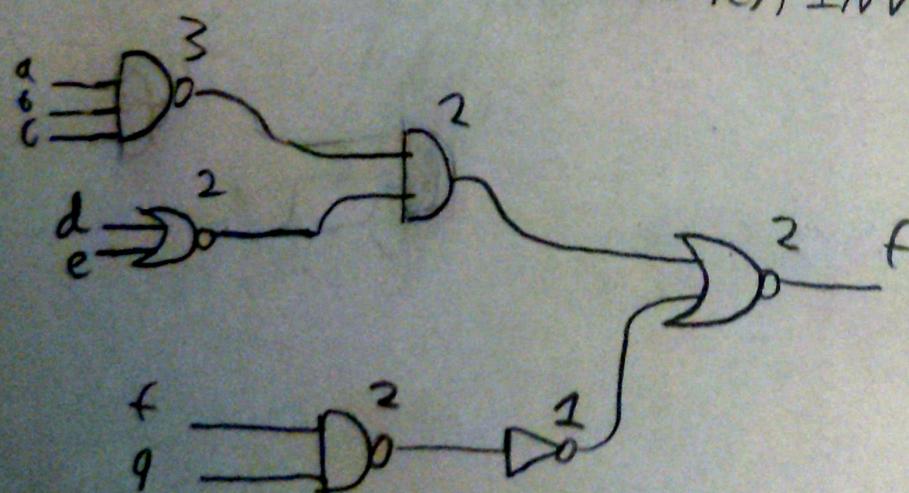
7) for each of these logic networks, draw the logic diagram and find the critical path, assuming that the delay through all n-input gates are n , delay through an inverter is 1.

a) $NAND_2(NAND_2(a,b), NAND_2(c,d))$



$$\begin{aligned} \text{critical path} &= a \rightarrow f \\ &\quad b \rightarrow f \\ &\quad c \rightarrow f \\ &\quad d \rightarrow f \\ \text{critical delay} &= 4 \end{aligned}$$

b) $AOI_2((NAND_3(a,b,c), NOR_2(d,e)), INV(NAND_2(f,g)))$



$$\text{critical delay} = 7$$

$$\begin{aligned} \text{critical path} &= a \rightarrow f \\ &\quad b \rightarrow f \\ &\quad c \rightarrow f \end{aligned}$$

8) A string of inverters drives a load of 50pf. Assuming gate capacitance to input node is 18ff and $P_{inv} = 1$. To get minimal delay you need to determine number of inverter stages and retiming the path.

1) Use $\bar{N} \approx 18FF$ to estimate number of stages N (let $f = 4$)

$$f = 6BH$$

$$f = 2777.78 \times 1 \times 1$$

$$G = g_i = 1$$

$$\beta = 1$$

$$H = \frac{50pf}{\underbrace{18ff}_{\text{Cin}}} \text{ (Out Cin)}$$

$$\hat{N} = \log_4 2777.78 = 5.719 \text{ Round to } \underline{\underline{N=6}}$$

2) Calculate path delay and inverter sizes using the estimated N .

$$f = f^{\frac{1}{N}} = 2777.78^{\frac{1}{6}} = 3.75$$

$$P = N * f$$

$$P = 6 * 1$$

$$f_i = g_i * h_i = g_i \frac{C_{out}}{C_{in}}$$

$$D = N * F^{\frac{1}{N}} + P$$

$$6 + 3.75 + 6$$

$$D = \underline{\underline{28.5 \tau}}$$

$$\begin{aligned} C_{in} &= \frac{C_{out}}{f} \\ &\xrightarrow{18FF} C_{in} = 0.2667 C_{out} \end{aligned}$$

3) Calculate path delay respectively using $N+1$ and $N-1$.

$$D = N * F^{\frac{1}{N}} + P$$

$$N-1 = 5$$

$$N+1 = 7$$

$$D = 7 * 2777.78^{\frac{1}{7}} + 7$$

$$D = 5 * 2777.78^{\frac{1}{5}} + 5$$

$$D = \underline{\underline{28.72 \tau}}$$

$$D = \underline{\underline{29.4 \tau}}$$

o This delay is more than the delay from 2)

This means our estimation was accurate!