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Lab 4 Part 1 Report

Video Checkoff

Video Checkoff Week 1 Part1:
https://www.youtube.com/watch?v=rI8vzzavx5Q
(Includes Simulation result of example counter and gate level for four bit full adder)
Video Checkoff Week 1 Part2:
https://www.youtube.com/watch?v=K4adaFIjN3I
(Includes final layout in fig 49)

What I learned

In today's lab I learned how to perform register level design and then create my hardware design with HDL for electric designs. Additionally, I learned how to use dc_shell, and icc_shell. Furthermore, I learned how verilog files are created and how to debug them in the event of an issue. Finally, I learned how to make use of verilog files to generate a hardware layout.

Simulation Result of Example Counter

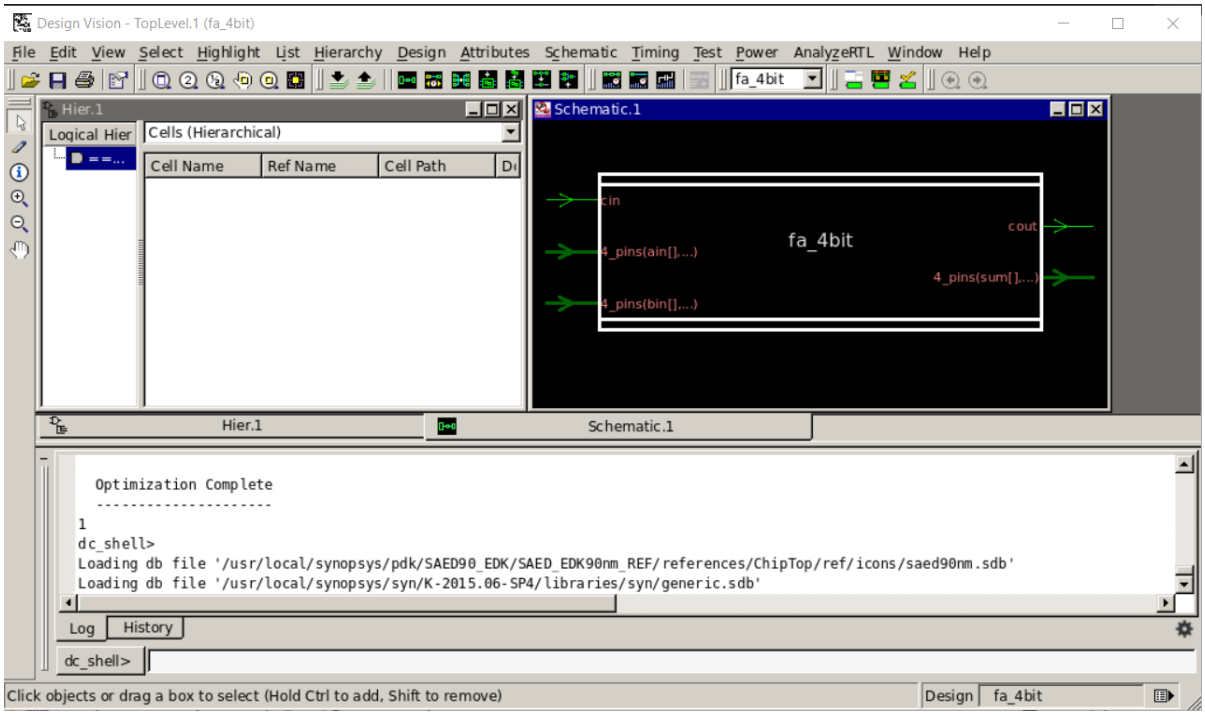
```
bender /home/memaj/asherman/eecs168/lab4-rtl/counter $ ./simv
Chronologic VCS simulator copyright 1991-2015
Contains Synopsys proprietary information.
Compiler version K-2015.09-SP1-1; Runtime version K-2015.09-SP1-1;  Feb 24 15:38 2022
time=   0 ns, clk=0, reset=0, out=xxxx
time=  10 ns, clk=1, reset=0, out=xxxx
time=  11 ns, clk=1, reset=1, out=xxxx
time=  20 ns, clk=0, reset=1, out=xxxx
time=  30 ns, clk=1, reset=1, out=xxxx
time=  31 ns, clk=1, reset=0, out=0000
time=  40 ns, clk=0, reset=0, out=0000
time=  50 ns, clk=1, reset=0, out=0000
time=  51 ns, clk=1, reset=0, out=0001
time=  60 ns, clk=0, reset=0, out=0001
time=  70 ns, clk=1, reset=0, out=0001
time=  71 ns, clk=1, reset=0, out=0010
time=  80 ns, clk=0, reset=0, out=0010
time=  90 ns, clk=1, reset=0, out=0010
time=  91 ns, clk=1, reset=0, out=0011
time= 100 ns, clk=0, reset=0, out=0011
time= 110 ns, clk=1, reset=0, out=0011
time= 111 ns, clk=1, reset=0, out=0100
time= 120 ns, clk=0, reset=0, out=0100
time= 130 ns, clk=1, reset=0, out=0100
time= 131 ns, clk=1, reset=0, out=0101
time= 140 ns, clk=0, reset=0, out=0101
time= 150 ns, clk=1, reset=0, out=0101
```

```
time=  151 ns, clk=1, reset=0, out=0110
time=  160 ns, clk=0, reset=0, out=0110
time=  170 ns, clk=1, reset=0, out=0110
All tests completed sucessfully


$finish called from file "counter_tb.v", line 55.
$finish at simulation time  171.0 ns
        V C S   S i m u l a t i o n   R e p o r t
Time: 171000 ps
CPU Time:      0.300 seconds;       Data structure size:   0.0Mb
Thu Feb 24 15:38:40 2022
bender /home/memaj/asherman/eecs168/lab4-rtl/counter $ ls
counter.dump  counter_tb.v  counter.v  csrc  simv  simv.daidir  ucli.key
bender /home/memaj/asherman/eecs168/lab4-rtl/counter $
```

```
time=  160 ns, clk=0, reset=0, out=0110
time=  170 ns, clk=1, reset=0, out=0110
All tests completed sucessfully


$finish called from file "counter_tb.v", line 55.
$finish at simulation time  171.0 ns
          V C S   S i m u l a t i o n   R e p o r t
Time: 171000 ps
CPU Time:      0.300 seconds;       Data structure size:   0.0Mb
Thu Feb 24 15:38:40 2022
bender /home/memaj/asherman/eecs168/lab4-rtl/counter $ ls
counter.dump  counter_tb.v  counter.v  csrc  simv  simv.daidir  ucli.key
bender /home/memaj/asherman/eecs168/lab4-rtl/counter $ ^C
bender /home/memaj/asherman/eecs168/lab4-rtl/counter $
```

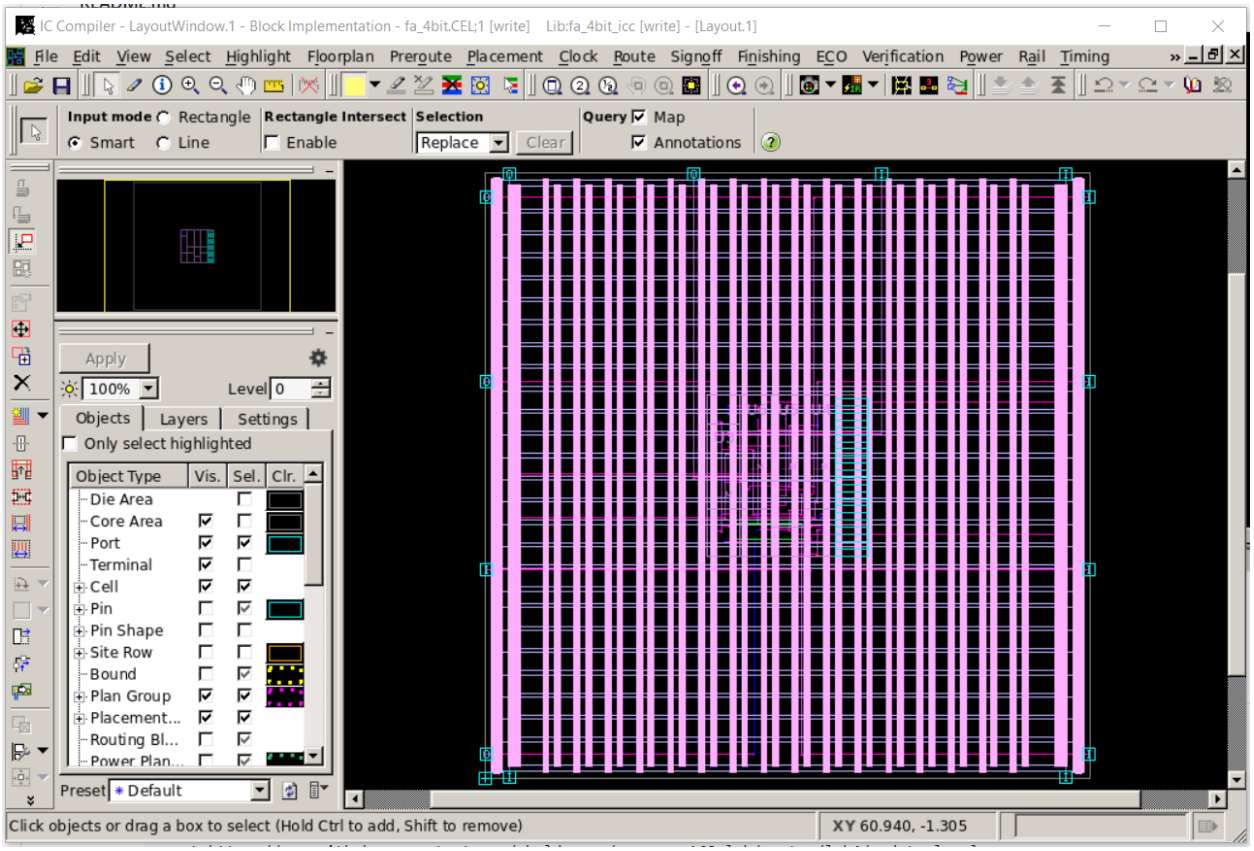
Gate Level Synthesized Schematic for Four Bit Full Adder

Fig 50



Final Layout

Fig 49



Some Issues I had

One Issue I had during the course of this lab was during the creation of my gate-level verilog synthesized file fa_4bit_synthesized.v. During this part of the lab, I was experiencing a lot of warnings that the "my_library.db" file couldn't be found. Then when I reached the "compile" step I encountered an error that halted my progress. I was perplexed as I had changed the library file to what was expected. Then I realized that the first line included in the library setup was a "*" meaning that it went through all listed libraries instead of only the selected one. This was causing my issue. So then I removed the default value for my link, target, and symbol libraries and ran my instructions again, and solved the issue. Other than that, I didn't encounter many issues during this lab.