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Partner Sec21 Group 1: Christopher Alexman calex025 (our reports and results are unique and we shared concepts and structures but not files)

Lab 3 Part 2/3 Report

Video Checkoff

Video 1 Week 2 Checkoff:
https://www.youtube.com/watch?v=SJPpIAXq8c4
(Includes 1-bit full adder layout (DRC, LVS) and post-simulation)

Video 2 Week 3 Checkoff:
https://www.youtube.com/watch?v=4eEA75wIUOY
(Includes 4-bit full adder layout (DRC, LVS) and post-simulation)
*If image clarity is an issue, please increase the quality and increase window size of video

Week 2 What I learned

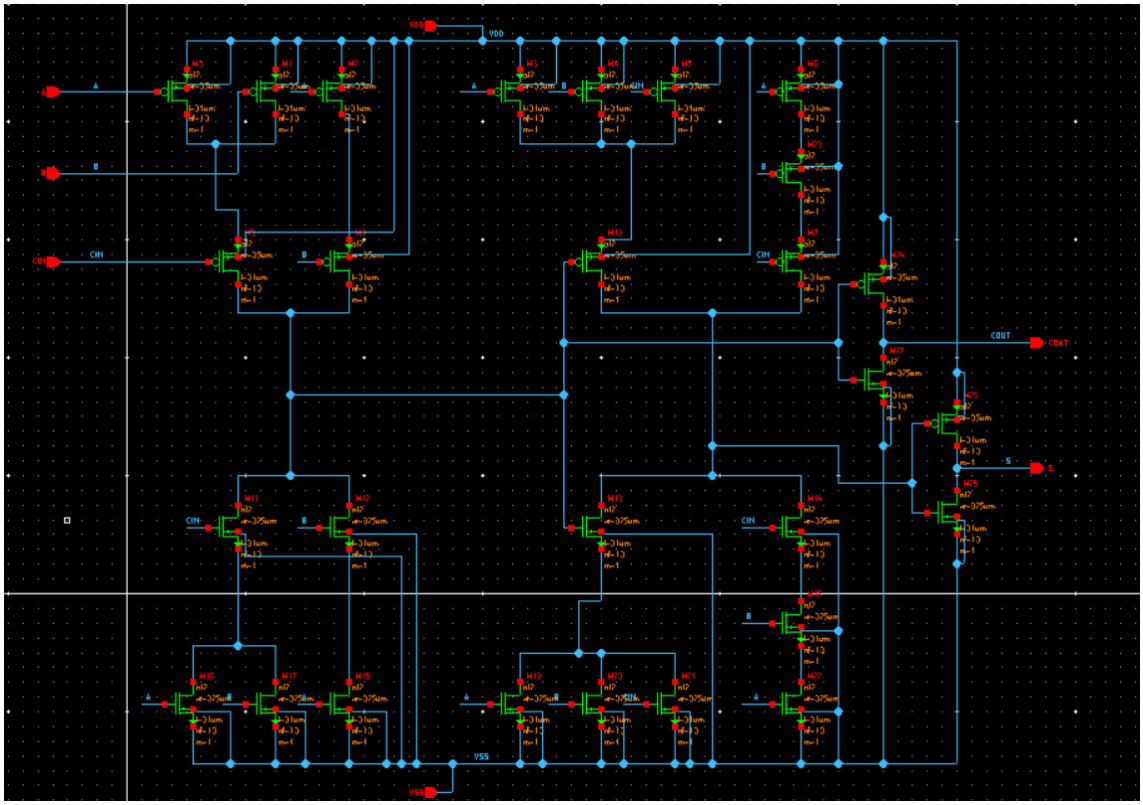
In today's lab I learned how to create a chip design from scratch. In other words, I learned how to complete the whole process of creating a design from schematic to final design with parasitic extraction and waveform in an unguided manner. Lab 3 was the first lab that had no lab video, and this was the first assignment with no guidance except certain hints. Week 2 required the most skill in layout building thus far.

Week 3 What I learned

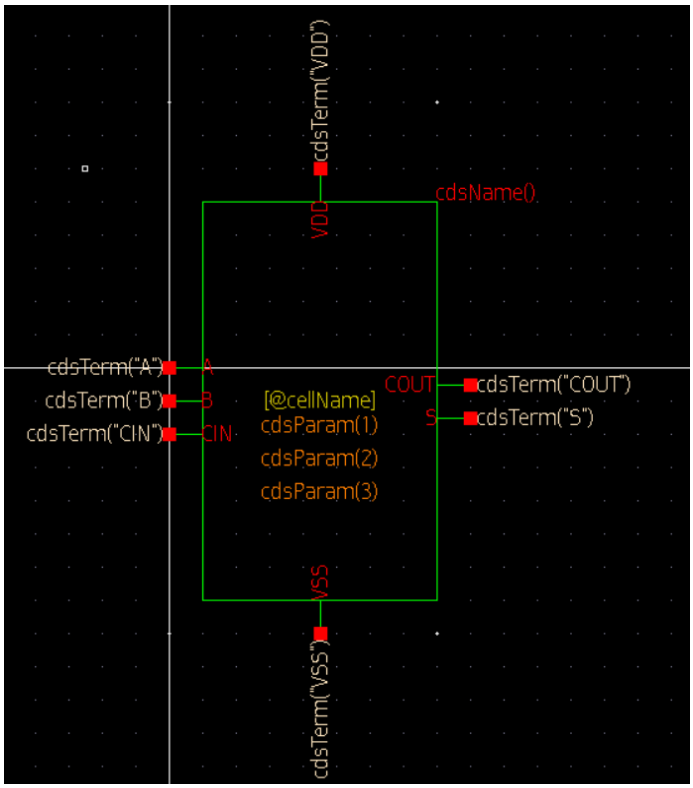
By the end of the last checkoff for lab3, I know how to not only create a design from scratch and complete all steps along the way, but also how to then use a previous design to implement a further design. This way, a hierarchical design can allow for the functionality of a chip to be reused in symbol form, as well as creating a new layout for the complicated chip by using a string of the previous chip's layout (4 in this case).This too, was done with no guidance, other than TA answers and hints. By the end of this week, I have created the toughest hierarchical design yet.

See next page.

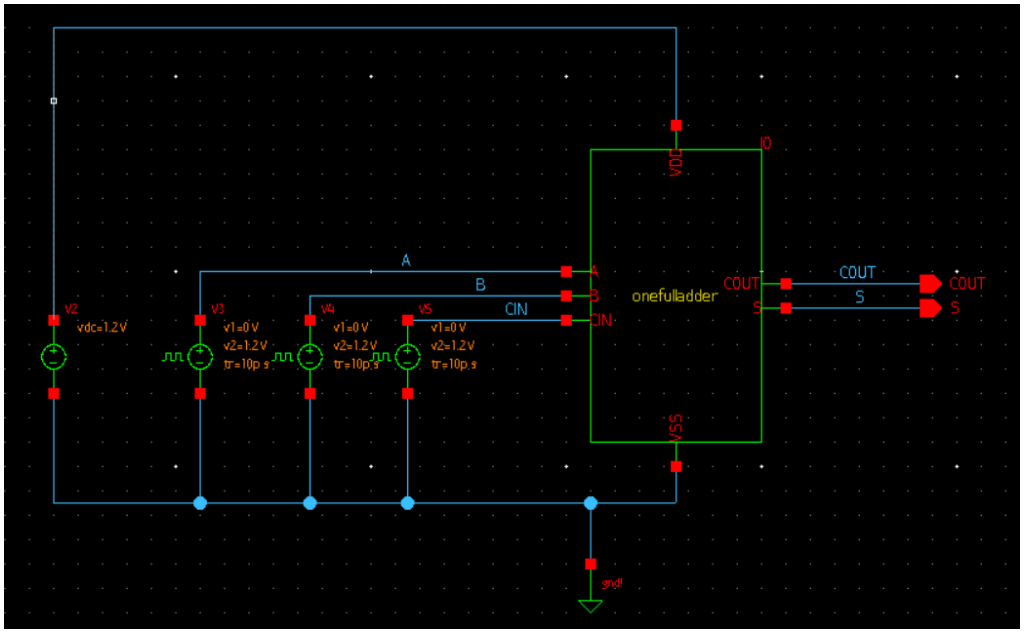
1 Bit Full Adder Schematic



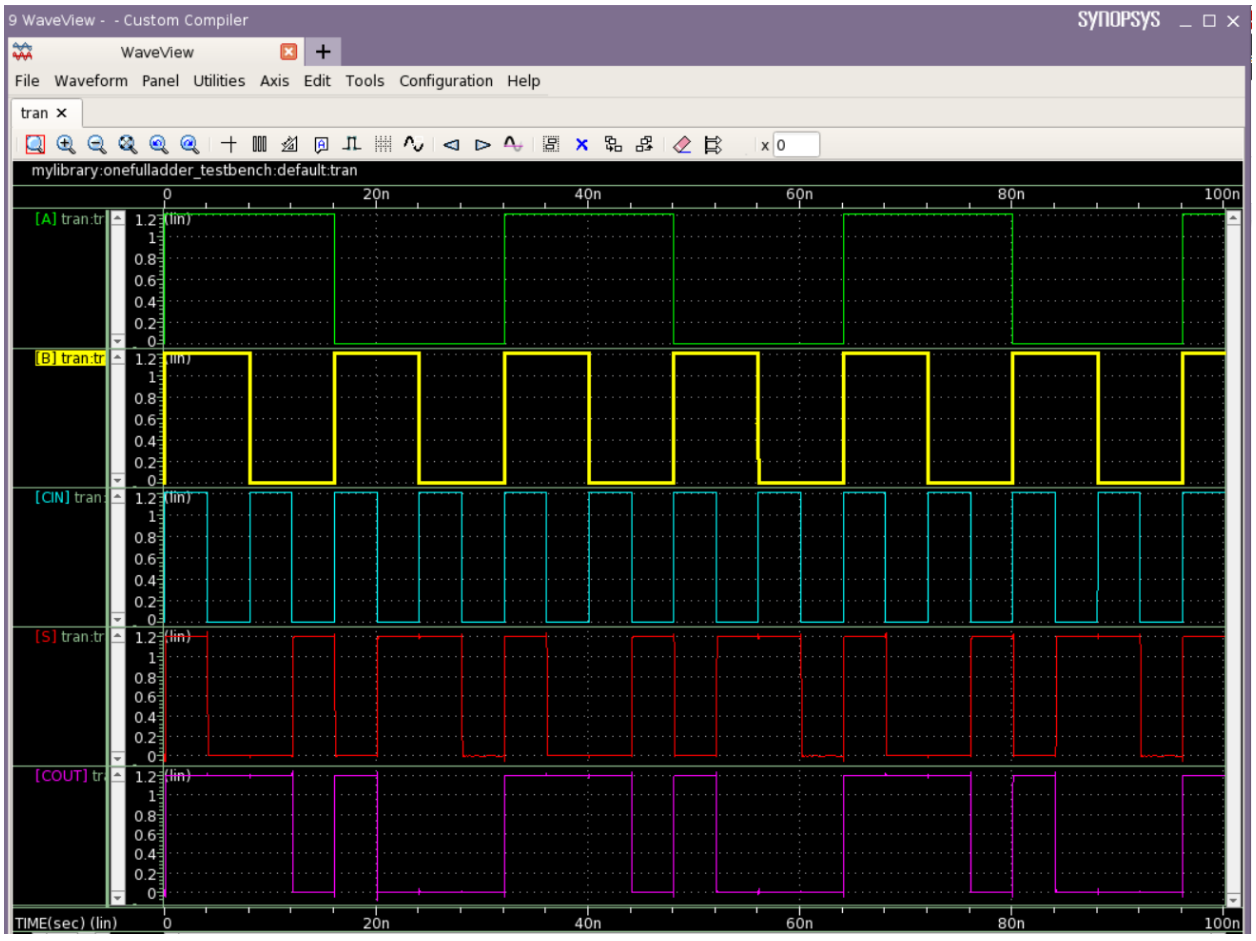
1 Bit Full Adder Symbol



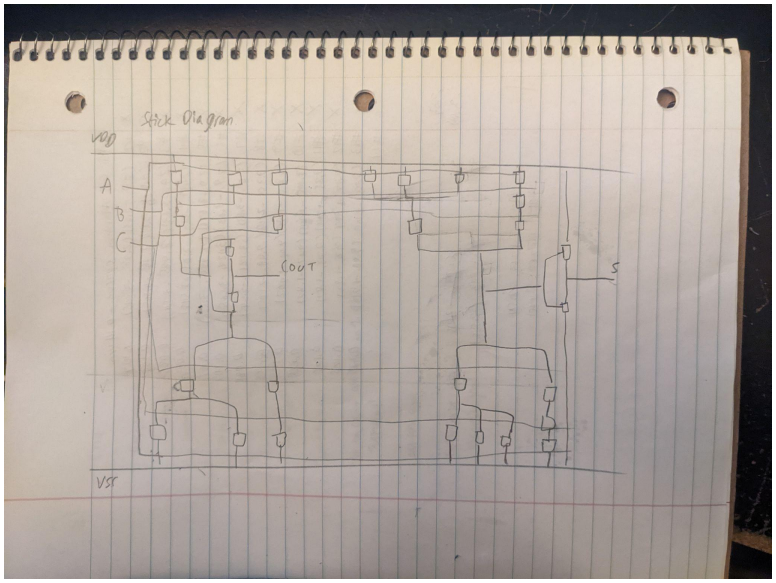
1 Bit Full Adder Testbench



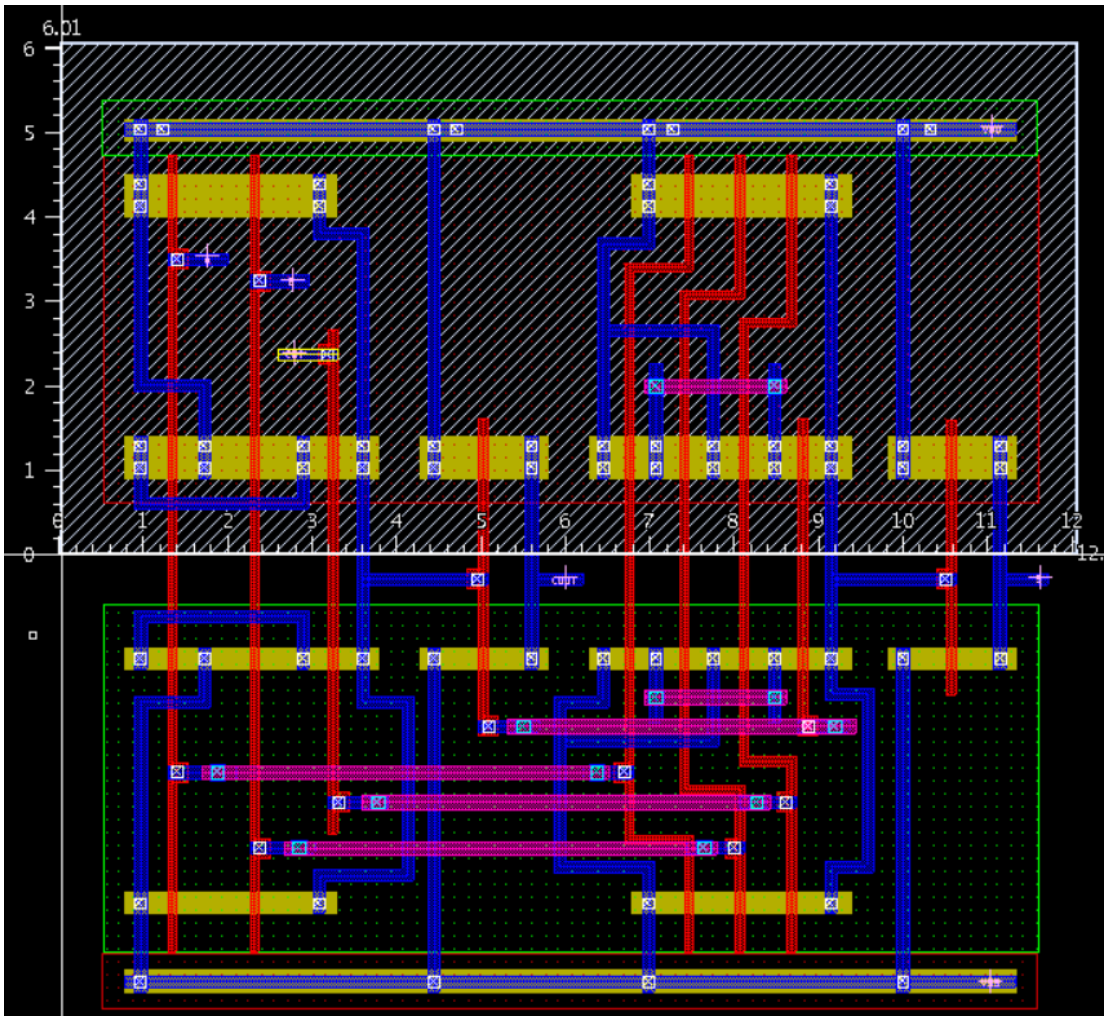
1 Bit Full Adder Pre-parasitic Waveform



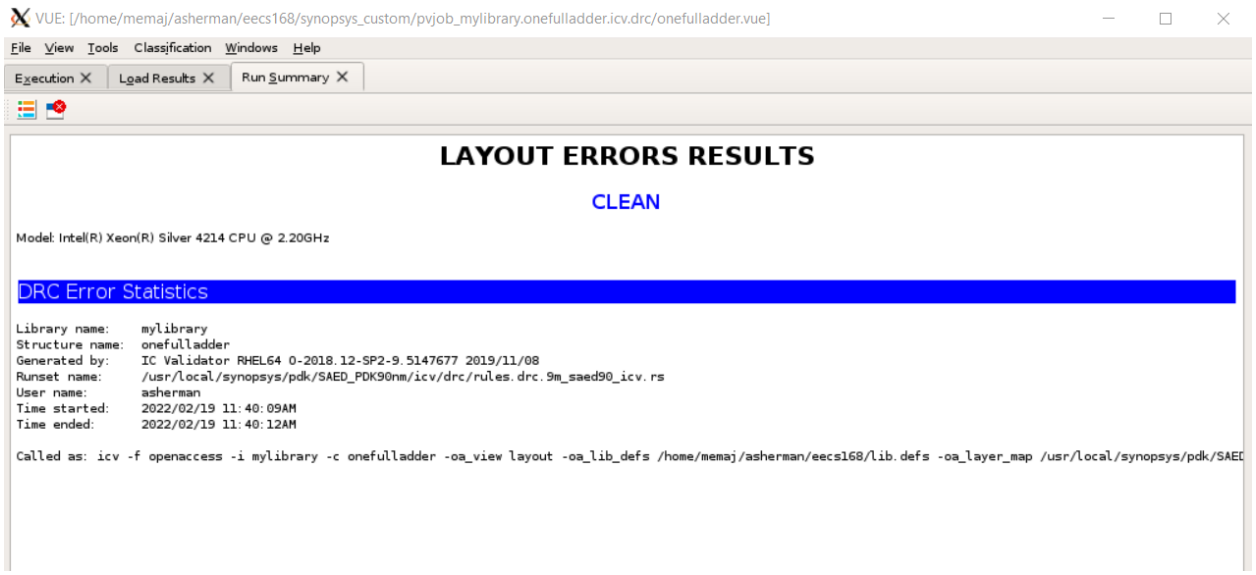
1 Bit Full Adder Stick Diagram



1 Bit Full Adder Layout

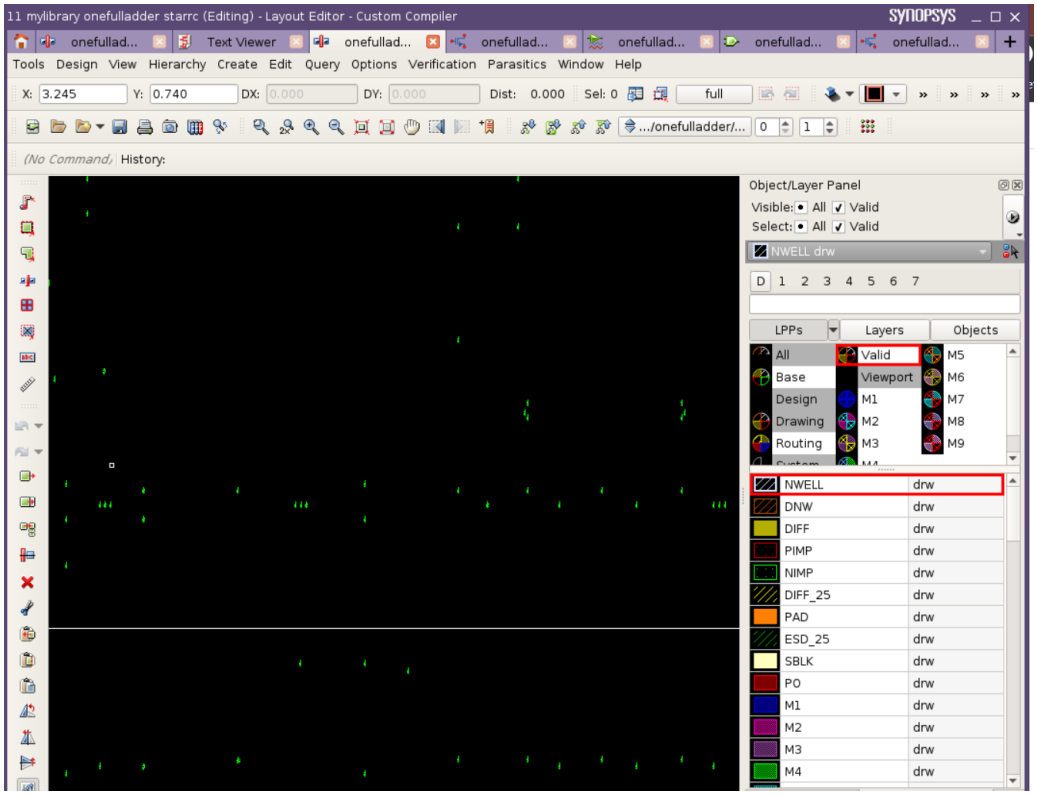


1 Bit Full Adder DRC Pass

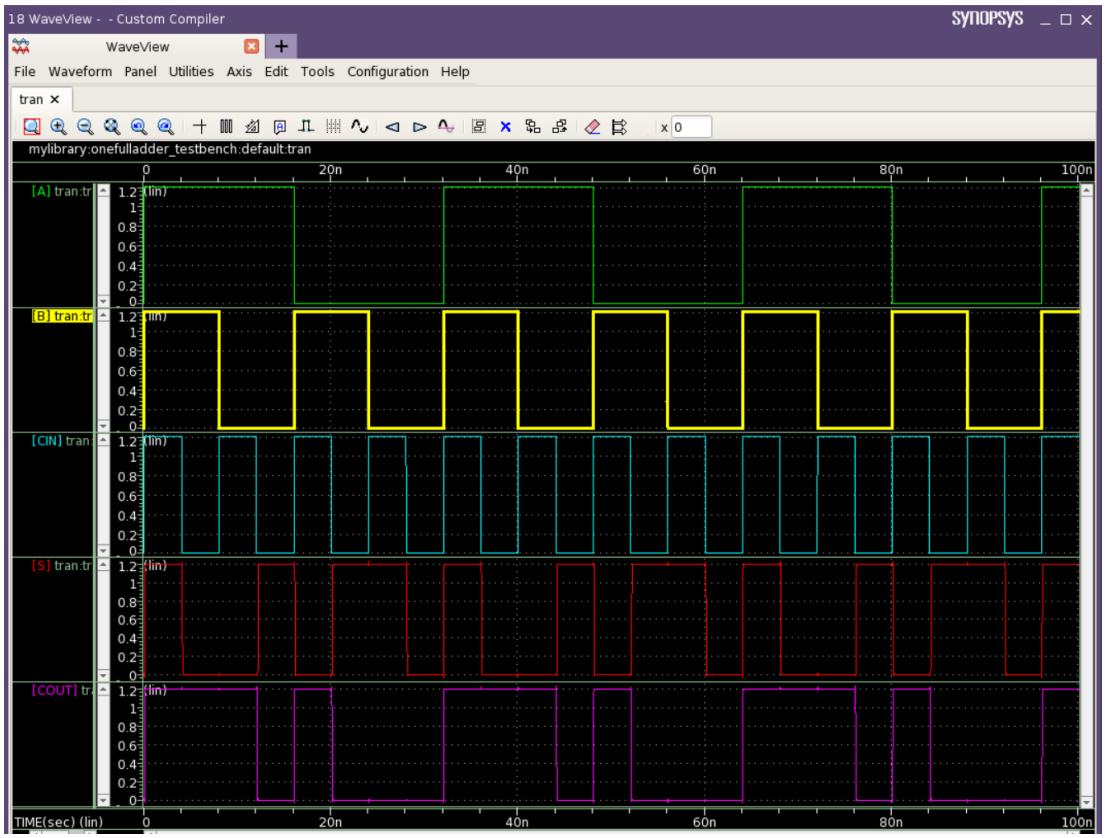


1 Bit Full Adder LVS Pass

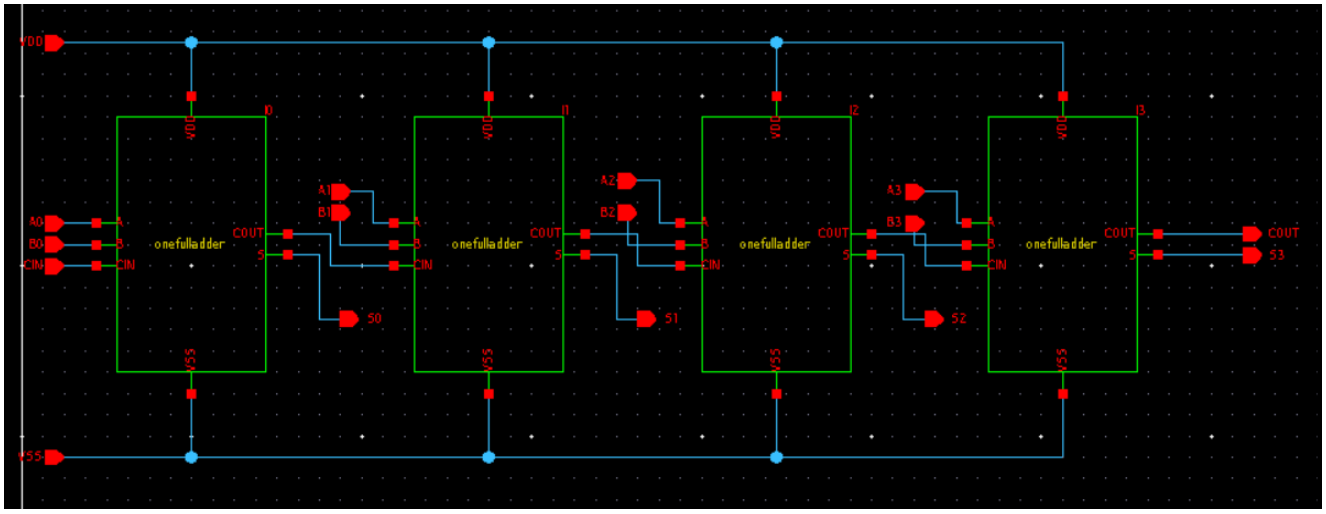
1 Bit Full Adder Parasitic view



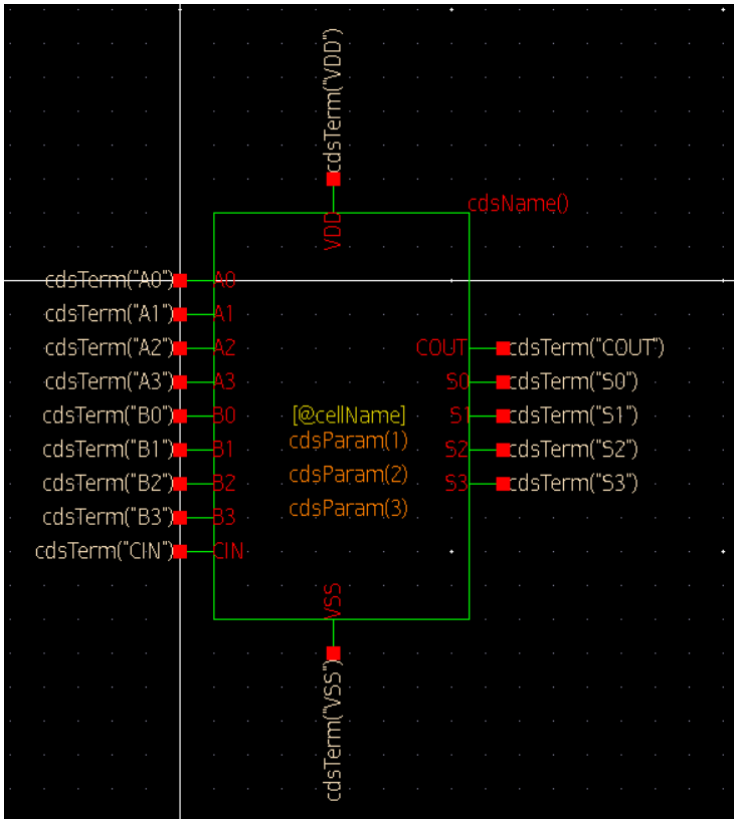
1 Bit Full Adder Waveform With Parasitics i.e POST (Layout) SIMULATION result



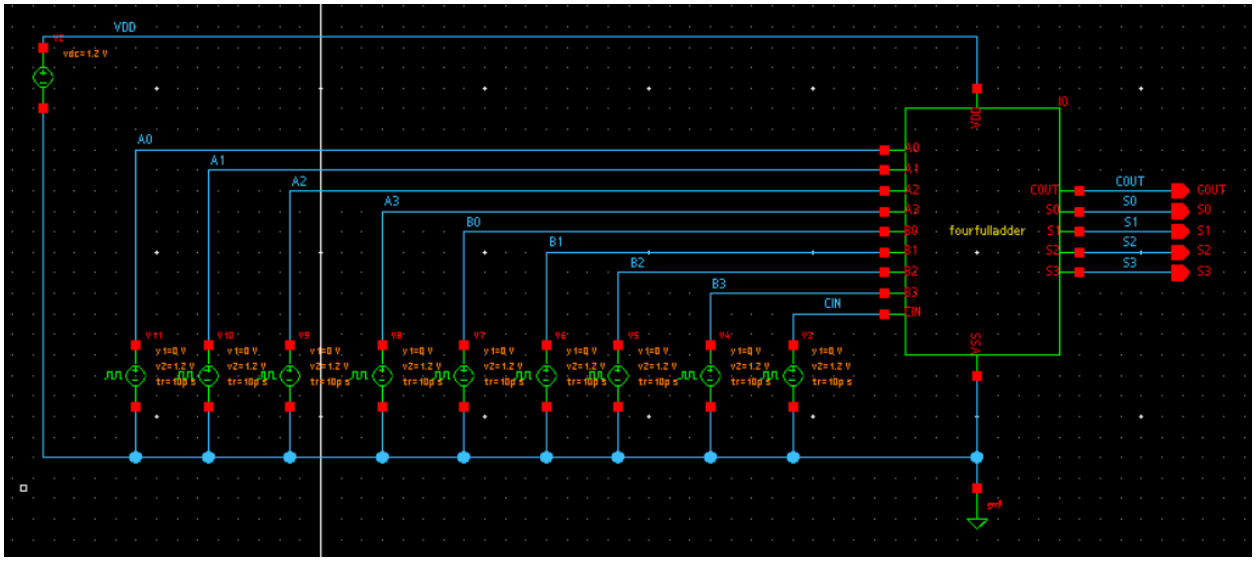
4 Bit Full Adder Schematic (Hierarchical)



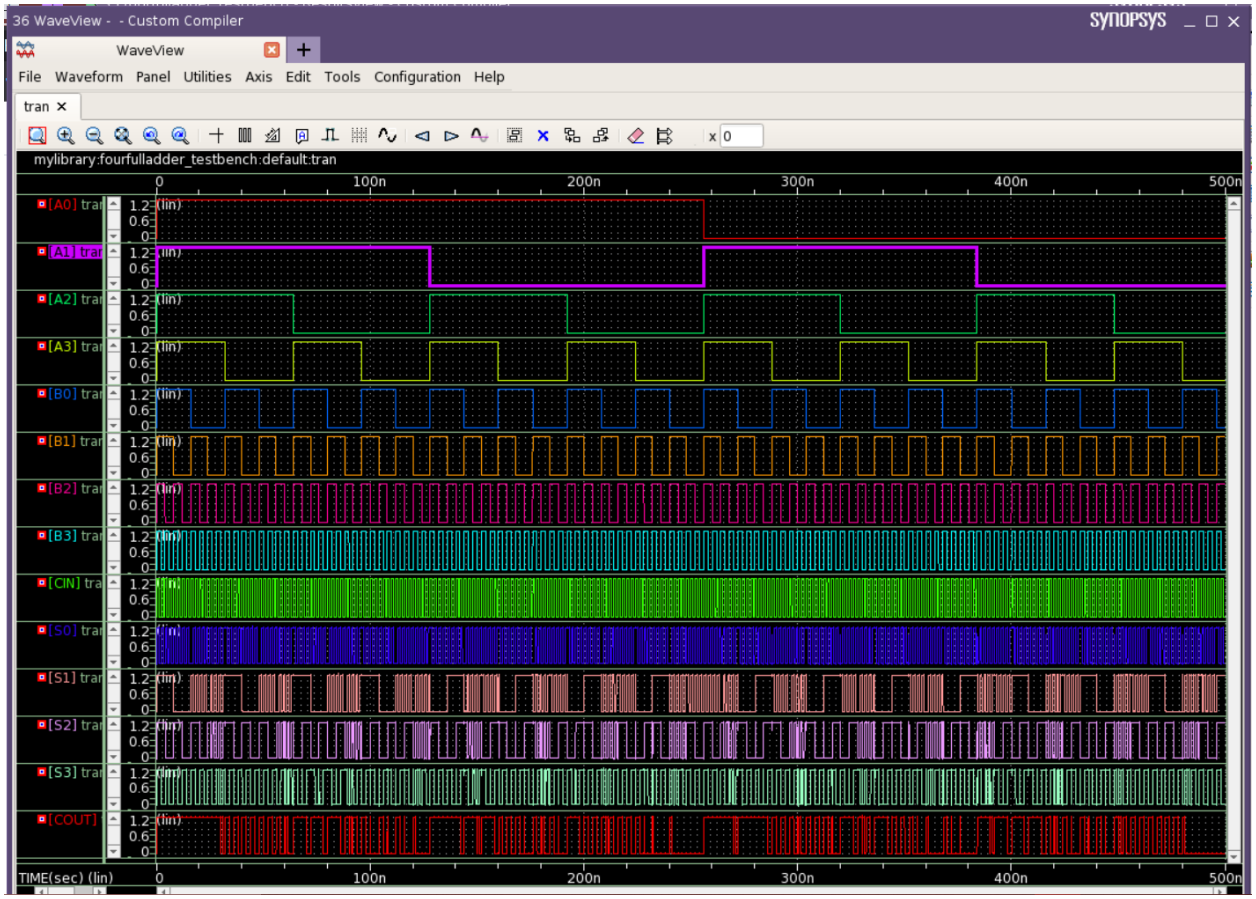
4 Bit Full Adder Symbol



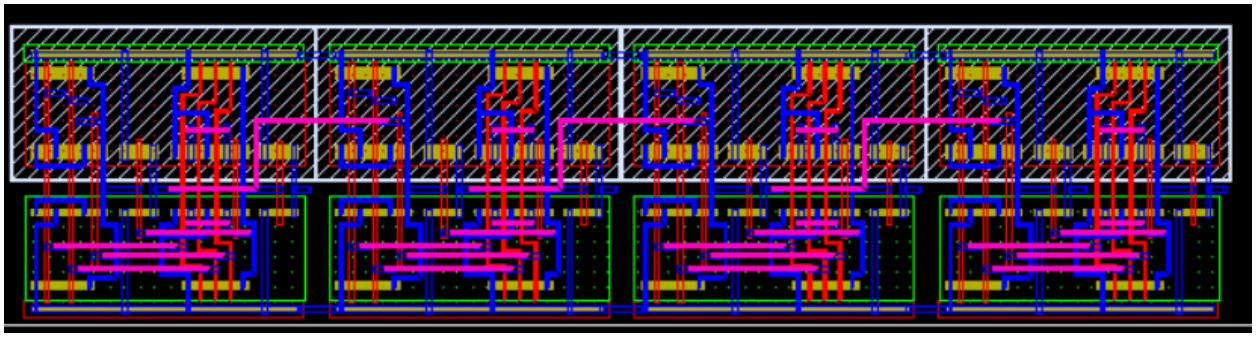
4 Bit Full Adder Testbench



4 Bit Full Adder Pre-parasitic Waveform



4 Bit Full Adder Layout (Hierarchical)



4 Bit Full Adder DRC Pass

VUE: [/home/memaj/asherman/eecs168/synopsys_custom/pvjob_mylibrary.fourfulladder.icv.drc/fourfulladder.vue]

File View Tools Classification Windows Help

Execution | Load Results | Run Summary

LAYOUT ERRORS RESULTS

CLEAN

Model: Intel(R) Xeon(R) Silver 4214 CPU @ 2.20GHz

DRC Error Statistics

```
Library name:     mylibrary
Structure name:   fourfulladder
Generated by:     IC Validator RHEL64 0-2018.12-SP2-9.5147677 2019/11/08
Runset name:      /usr/local/synopsys/pdk/SAED_PDK90nm/icv/drc/rules.drc.9m_saed90_icv.rs
User name:        asherman
Time started:     2022/02/19 07:21:51PM
Time ended:       2022/02/19 07:21:54PM

Called as: icv -f openaccess -i mylibrary -c fourfulladder -oa_view layout -oa_lib_defs /home/memaj/asherman/eecs168/lib.defs -oa_layer_map /usr/local/synopsys/pdk/SAE
```

4 Bit Full Adder LVS Pass

VUE: [/home/memaj/asherman/eecs168/synopsys_custom/pvjob_mylibrary.fourfulladder.icv.lvs/fourfulladder.vue]

File View Tools Classification Windows Help

Execution | Load Results | Run Summary | LVS Errors

TOP BLOCK COMPARE RESULTS

PASS

[fourfulladder, fourfulladder]

Model: Intel(R) Xeon(R) Silver 4214 CPU @ 2.20GHz

Netlist Extraction Statistics

```
Library name:     mylibrary
Structure name:   fourfulladder
Generated by:     IC Validator RHEL64 0-2018.12-SP2-9.5147677 2019/11/08
Runset name:      /usr/local/synopsys/pdk/SAED_PDK90nm/icv/lvs/rules.lvs.9m_saed90_lvs.rs
User name:        asherman
Time started:     2022/02/19 07:23:18PM
Time ended:       2022/02/19 07:23:23PM

Called as: icv -f openaccess -i mylibrary -c fourfulladder -oa_view layout -oa_lib_defs /home/memaj/asherman/eecs168/lib.defs -oa_layer_map /usr/local/synopsys/pdk/SAE
```

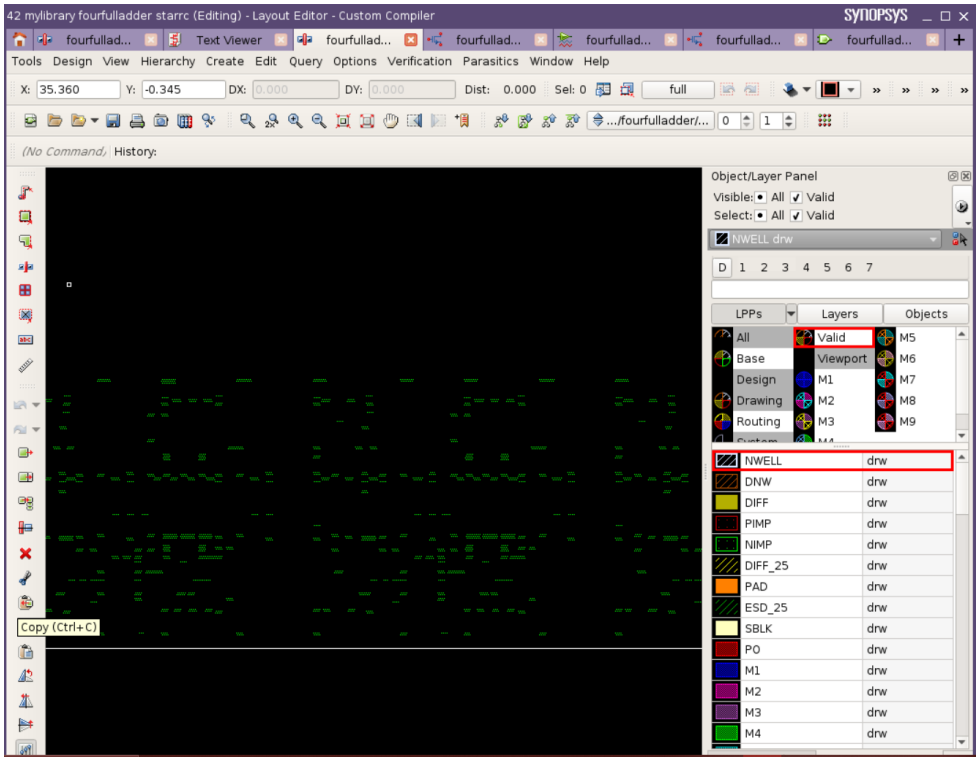
Layout vs. Schematic Statistics

```
Schematic:  /home/memaj/asherman/eecs168/synopsys_custom/pvjob_mylibrary.fourfulladder.icv.lvs/fourfulladder.sch_out
```

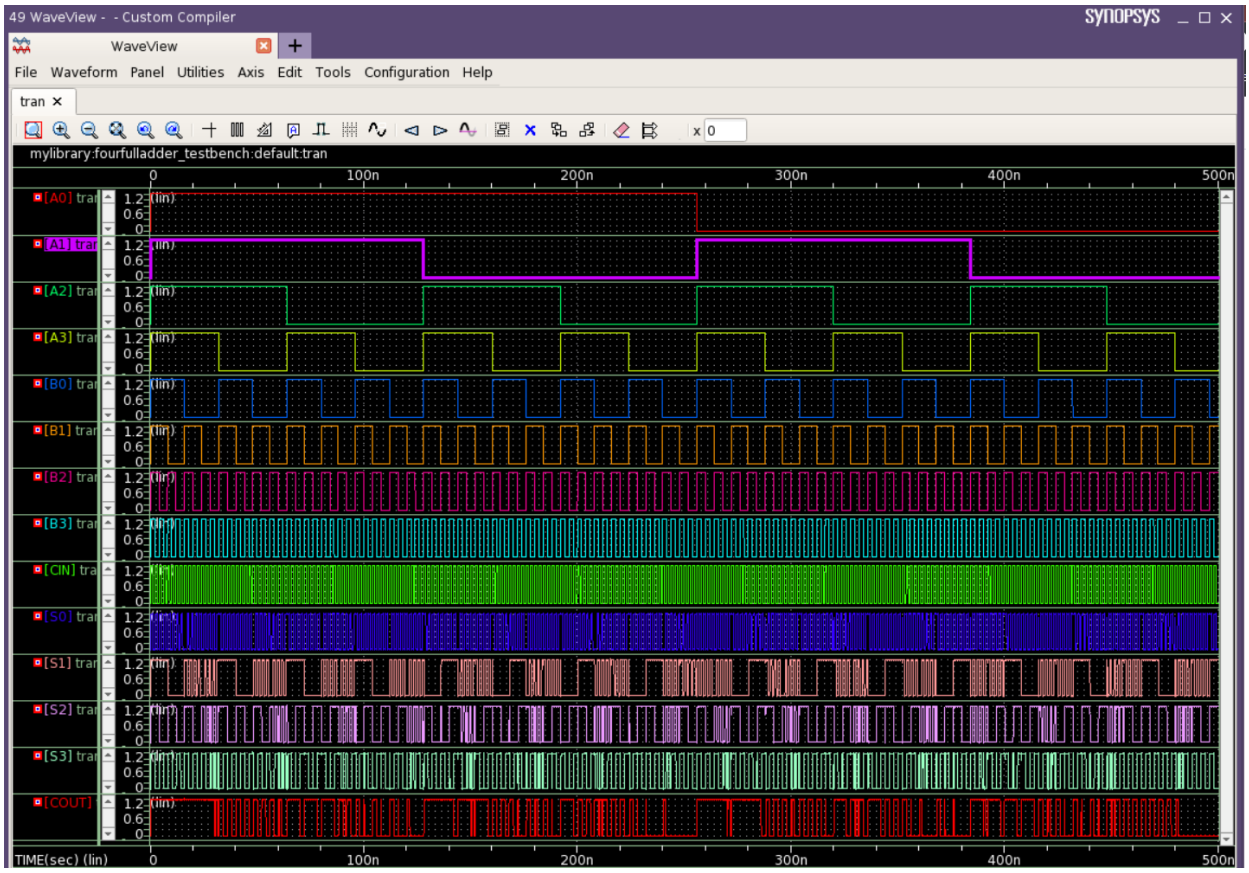
LVS Errors:

```
    1 successful equivalencies
    0 failed equivalencies
```

4 Bit Full Adder Parasitic view



4 Bit Full Adder Waveform With Parasitics i.e POST (Layout) SIMULATION result



Some Issues I had - Week 2

Out of all weeks of lab 3, week 2 was the most difficult for me. The most time consuming portion of this lab overall was creating the first initial layout for the 1 bit full adder. The reason this was the case was due to the fact that other than the hints, we were on our own. Eventually, I was able to come up with a design after discussing it with my partner. However, even with an idea of the design, the layout was so large that passing DRC was a massive headache. In fact, once I had finished most of my DRC errors, I still had a number of "layout grid" errors. I had never encountered such an error and had to ask the TA. Ultimately, the issue laid in decimal values being too specific such as (3.078, -3.656) needing to be changed to something like (3.08, -3.66). Ultimately I was able to solve my issues and pass DRC, LVS and generate my parasitic view after running LPE.

Some Issues I had - Week 3

In comparison to week 2, week 3 didn't have as many issues. Since week 3 mainly builds off of week 2, and the layout structure from week 2 could be reused, there were far less DRC or LVS issues so I was able to solve these aspects without much issue. I did have one small issue in my testbench but it was simply that I had forgotten to include units on one of my pulse and width values on a vpulse. Once I realized this, the fix was simple.