Title: **Hoja\_Master**

Author: \*

Size: A4

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Revision: \*

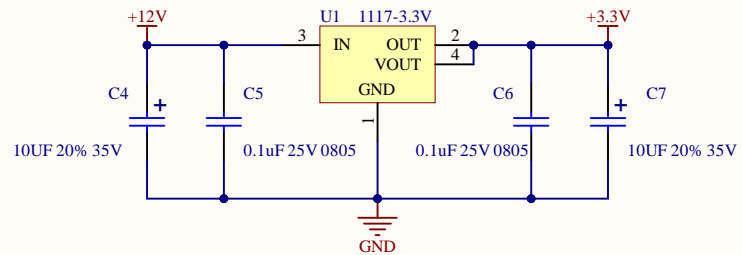
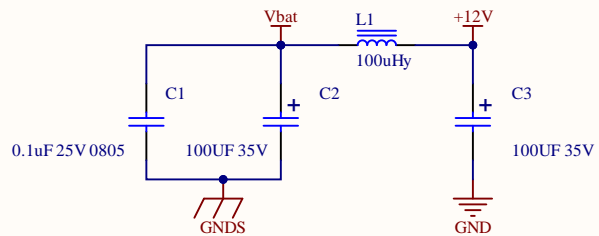
File: Hoja\_Master.SchDoc

Date: 27/10/2022



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\*



1

2

3

4

A

A

B

B

C

C

D

D

U2

RESETn

P0\_0/FC0\_RXD\_SDA\_FC3\_CTS\_SDA\_SSELN0/CT0CAP0/SCT0\_OUT3  
 P0\_1/FC0\_TXD\_SCL\_MISO/FC3\_RTS\_SCL\_SSELN1/CT0CAP1/SCT0\_OUT1  
 P0\_2/FC0\_CTS\_SDA\_SSELN0/FC2\_SSELN3/CT2CAP1  
 P0\_3/FC0\_RTS\_SCL\_SSELN1/FC2\_SSELN2/CT1MAT3  
 P0\_4/FC0\_SCK/FC3\_SSELN2/CT0CAP2  
 P0\_6/FC6\_TXD\_SCL\_MISO/CT0MAT1/UTICK\_CAP0  
 P0\_8/FC2\_RXD\_SDA\_MOSI/CT0\_OUT1/CT0MAT3  
 P0\_9/FC2\_TXD\_SCL\_MISO/CT0\_OUT2/CT3CAP0/FC3\_CTS\_SDA\_SSELN0  
 P0\_10/FC2\_SCK/CT0\_OUT3/CT3MAT0  
 P0\_11/FC3\_SCK/FC6\_RXD\_SDA\_MOSI/CT2MAT1  
 P0\_12/FC3\_RXD\_SDA\_MOSI/FC6\_TXD\_SCL\_MISO/CT2MAT3  
 P0\_13/FC3\_TXD\_SCL\_MISO/CT0\_OUT4/CT2MAT0  
 P0\_14/FC3\_CTS\_SDA\_SSELN0/CT0\_OUT5/CT2MAT1/FC1\_SCK//SPIFI  
 P0\_15/FC3\_RTS\_SCL\_SSELN1/SWO/CT2MAT2/FC4\_SCK//SPIFI\_IO2  
 P0\_21/CLKOUT/FC0\_TXD\_SCL\_MISO/CT3MAT0//SPIFI\_CLK  
 P0\_22/CLKIN/FC0\_RXD\_SDA\_MOSI/CT3MAT3  
 P0\_23/FC1\_RTS\_SCL\_SSELN1//CT0CAP0/UTICK\_CAP1  
 P0\_24/FC1\_CTS\_SDA\_SSELN0//CT0CAP1/CT0MAT0  
 P0\_31/PDM0\_CLK/FC2\_CTS\_SDA\_SSELN0/CT2CAP2/CT0CAP3/CT0MAT3

P0\_16/FC3\_SSELN2/FC6\_CTS\_SDA\_SSELN0/CT3MAT1/SWCLK//SPIFI\_1  
 P0\_17/FC3\_SSELN3/FC6\_RTS\_SCL\_SSELN1/CT3MAT2/SWDIO//SPIFI\_0  
 P0\_25/FC4\_RTS\_SCL\_SSELN1/FC6\_CTS\_SDA\_SSELN0/CT0CAP2/CT1CP1  
 P0\_26/FC4\_CTS\_SDA\_SSELN0//CT0CAP3

P0\_18/FC5\_TXD\_SCL\_MISO/CT0\_OUT0/CT0MAT0  
 P0\_19/FC5\_SCK/CT0\_OUT1/CT0MAT1//SPIFI\_CSN  
 P0\_20/FC5\_RXD\_SDA\_MOSI/FC0\_SCK/CT3CAP0

P0\_29/FC1\_RXD\_SDA\_MOSI/CT0\_OUT2/CT0MAT3/CT0CAP1//CT0MAT1  
 P0\_30/FC1\_TXD\_SCL\_MISO/CT0\_OUT3/CT0MAT2/CT0CAP2  
 P1\_0/PDM0\_DATA/FC2\_RTS\_SCL\_SSELN1/CT3MAT1//CT0CAP0  
 P1\_1/SWO/CT0\_OUT4/FC5\_SSELN2/FC4\_TXD\_SCL\_MISO  
 P1\_2/MCLK/FC7\_SSELN3/CT0\_OUT5/FC5\_SSELN3/FC4\_RXD\_SDA\_MOSI

LPC5441

RST\_TGTMCU

PWM\_2\_BUCK

PWM\_3

SWD\_CLK

SWD\_IO

R1

R2

R3

R4

R5

ADC\_Vo  
 ADC\_Icc  
 ADC\_Vcc  
 ADC\_I\_Buck2  
 ADC\_V\_Buck2

10K 5% 0805  
 10K 5% 0805  
 10K 5% 0805  
 10K 5% 0805  
 10K 5% 0805

D1

R7

1K 5% 0805

R8

1K 5% 0805

R9

1K 5% 0805

R

G

B

Lcd RGB

RGB\_R

RGB\_G

RGB\_B

+3.3V

P1\_3/FC7\_SSELN2/CT0\_OUT6/FC3\_SCK/CT0CAP1/USB0\_LEDN  
 P1\_4/PDM1\_CLK/FC7\_RTS\_SCL\_SSELN1/CT0\_OUT7//FC3\_TXD\_SCL\_MISO/  
 P1\_5/PDM1\_DATA/FC7\_CTS\_SDA\_SSELN0/CT1CAP0//CT1MAT3/PVT\_AM0\_ALERT/  
 P1\_6/FC7\_SCK/CT1CAP2//CT1MAT2/PVT\_RED0\_ALERT/USB0\_VBUS  
 P1\_7/FC7\_RXD\_SDA\_MOSI/CT1MAT2//CT1CAP2/PVT\_AMBER1\_ALERT  
 P1\_8/FC7\_TXD\_SCL\_MISO/CT1MAT3//CT1CAP3/PVT\_RED1\_ALERT  
 P1\_11/FC6\_RTS\_SCL\_SSELN1/CT1CAP0/FC4\_SCK//USB0\_VBUS  
 P1\_12/FC5\_RXD\_SDA\_MOSI/CT1MAT0/FC7\_SCK/UTICK\_CAP2  
 P1\_13/FC5\_TXD\_SCL\_MISO/CT1MAT1/FC7\_RXD\_SDA\_MOSI  
 P1\_14/FC2\_RXD\_SDA\_MOSI/CT0\_OUT7/FC7\_TXD\_SCL\_MISO  
 P1\_15/PDM0\_CLK/CT0\_OUT5/CT1CAP3/FC7\_CTS\_SDA\_SSELN0  
 P1\_16/PDM0\_DATA/CT0MAT0/CT0CAP0/FC7\_RTS\_SCL\_SSELN1  
 P1\_17//MCLK/UTICK\_CAP3  
 USB\_DP  
 USB\_DM  
 VDD\_0  
 VDD\_1  
 VDD\_2  
 VDD\_3  
 VDDA  
 VREFP  
 VSS\_0  
 VSS\_1  
 VSS\_2  
 VSSA  
 VREFN  
 P1\_9/FC3\_RXD\_SDA\_MOSI/CT0CAP2//USB0\_LEDN/USB0\_CONNECTN  
 P1\_10/FC6\_TXD\_SCL\_MISO/CT0\_OUT4/FC1\_SCK//USB0\_FRAME  
 P0\_5/FC6\_RXD\_SDA\_MOSI/CT0\_OUT6/CT0MAT0  
 P0\_7/FC6\_SCK/CT0\_OUT0/CT0MAT2/CT0CAP2

ASM1  
FiducialASM2  
FiducialASM3  
FiducialASM4  
Fiducial

RTCXIN

RTCXOUT

C8

18pF

Y1

32.768 kHz

C9

18pF

GND

GND

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J1

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9

10

SWD\_IO

SWD\_CLK

RST\_TGTMCU

JTAG/SWD Programmer

J2

JUMPER

C15

0.1uF

GND

GND

GND

GND

GND

GND

GND

GND

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