27.6 Single-Chip 3072ch 2D Array IC with RX Analog and All-Digital TX Beamformer for 3D Ultrasound Imaging

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A diagnostic ultrasound (US) system transmits acoustic waves at several to tens of MHz into the human body for clinical purposes and detects the reflected waves to observe the internal organs without having a medical operation or radiation exposure. The system is composed of a main unit and probe connected via coaxial cables. The probe is very small because medical technicians laboriously grab and manipulate it for a long time. To avoid image obscurity depending on medical technicians, high-speed and high-resolution 3D/4D imaging is necessary. For this reason, several thousands of lead bulk piezoelectric material transducers (TD) need to be squeezed into the small probe. Since the number of cables is limited to several hundreds, the probe needs to include beamforming functionality and a 2D array IC [1-6], which includes thousands of US transceivers.

Figure 27.6.1 shows a block diagram of the diagnostic US system and the proposed 2D array IC, which includes 3,072 US transceivers. Since a TD pillar is 300×300μm^2, each US transceiver size needs to be the same pitch. The TD is connected to an IC via a low-temperature co-fired ceramic (LTCC) interposer to alleviate fabrication difficulties. On the other side of the pillars, there is an acoustic impedance matching layer and a lens. The 2D array IC bilaterally interfaces from the 3,072-ch TD to the 128-ch coaxial cables. The 24 TD and US transceivers are grouped to coherently execute transmitter and receiver US signal processing. The main unit digitizes the signal to perform beamforming and image rendering.

The subarray block diagram is shown in Fig. 27.6.2. The transmitter is an all-digital architecture, and is composed of a digital beamformer, a switched-capacitor delayer (SCD), and a tunable amplitude 3-level pulser (TA3LP). Therefore, it is free from waveform distortion and timing error caused by cable propagation between the main unit and the probe. The pulser power consumption is generally far less than that of linear amplifiers, but the pulser's constant amplitude leads to limited image quality. TA3LP in this work has a built-in amplitude control function, and the TX and RX chain share the SCD to squeeze all the necessary blocks in a die. The TD TRX signal I/Os include zero-power-TRX-isolation switches (ZTRSW) to protect subsequent blocks with ordinal rating elements. Although conventional ZTRSW uses a zener diode as a floating switch gate bias and inherently needs a lot of power, ZTRSW in this work only consumes 10μW during RX mode using MOSFET active floating-gate bias topology. The next stage is a programmable gain-and-input-impedance low-noise amplifier (PGZLNA). PGZLNA boosts the weak signal to a reasonable level for the next stage. The programmable input impedance is used to achieve >85dB dynamic range. The charge-domain adders (CDADDs) perform, in the charge domain, correlated-signal summation of 24 SCD outputs, and the CDADDs are placed in a subarray without signal headroom concerns. If each SCD setting is ideal, and their correlation is ideal, RX SNR is √24 times better. It means the noise level is √24 times lower. Therefore, the next stage block, which is the low-noise cable buffer (LNCBUF), needs to be low noise and have heavy coaxial cable drivability. Finally, the main unit digitizes the signal to perform beamforming and image rendering.

Figure 27.6.3 shows the SCD circuit, which is composed of a capacitor ring memory (CRM), an operational amplifier (OPA), and a CDADD. Since CRM occupies most of the area, TX and RX chain share the CRM. While the RX chain uses CRM as an analog memory, the TX chain uses them as a 2b D-latch. During TX mode, the OPA operates as a comparator. The switches, being carefully placed and deployed, achieve the optimal metamorphosis to avoid signal distortions. The CRM, which is composed of 32 capacitors, controls the time differences of write (charge) and read timing to make the necessary delay. The write and read signals are non-overlapped 40MHz pulse trains and cover the 25-to-750ns delay range. During RX mode, dynamically changing the focal points leads to fast image rendering. For this reason, duplicated write pulse or doubling the read pulse width can increase the delay time. Adversely doubling the write pulse width or skipping read pulse can shorten it. Figure 27.6.4 shows the TA3LP circuits, which can launch plus, zero, and minus level signals. The output stage takes on the source follower push-pull topology (PP). PP consumes a lot of power only during the pulse transition durations and alleviates the previous inverter (INV) stage bias current and transistor sizes. The INV output has grounding switches to make zero level (RZ: return to zero circuit). PP and INV will operate within a safe operating area to avoid device destruction. Since TA3LP does not use feedback topology, rise and fall time adjustment is necessary. As previously noted, TA3LP has a 256 level amplitude adjustment module to compete with a linear amplifier system and cover many diagnostic modes necessary for the US system. The amplitude transition can settle to <4.4μs.

The 2D array IC is assembled and implemented in the probe and main unit with a real-time rendering engine that is optimized and caters for the probe. The system can capture 3D tissue images with several arbitrary 2D cutting planes within the angle of view (AoV) of this system. Arbitrary 2D cutting plane images are easily extracted from the full-volume 3D dataset. The System AoV is more than 90°×90°, and it can look over the whole human heart during echo-cardiography. Figure 27.6.5 shows the 2D and 3D image of a phantom (white ball: agar / black ball: agar and graphite mixture) as an example. Figure 27.6.6 shows the performance comparisons. Our work is only a 2D array IC that includes the RX analog, all-digital TX beamformer, and related peripheral blocks. The silicon area occupies 0.09mm^2/ch and consumes 0.7mW/ch during B-mode capture. Regardless of the 138V_{pp} US launch capability, 0.7mW/ch power consumption is also the lowest in the table.

A die micrograph of the 2D array IC implemented in a 0.18μm HV SOI CMOS process is shown in Fig. 27.6.7. The total area is 417mm^2 including the digital beamformer and the other control and the interface circuits.

References:

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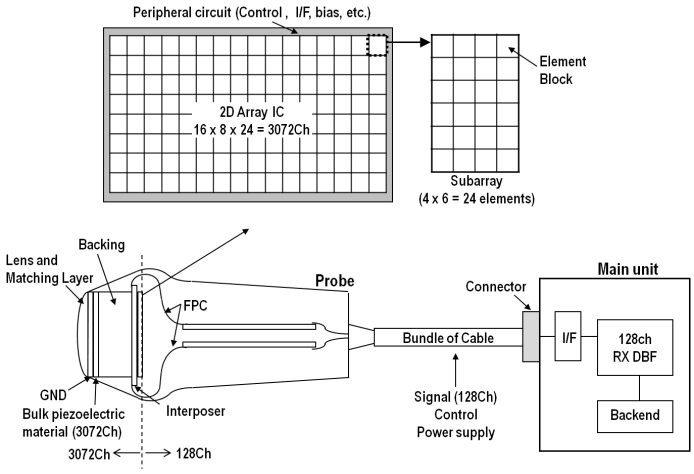

Figure 27.6.1: Block diagram of diagnostic ultrasound system with 3,072-ch 2D array IC.

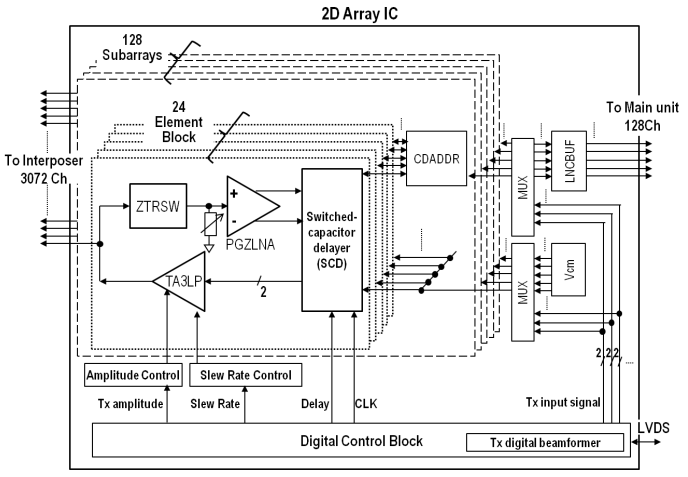

Figure 27.6.2: Block diagram of 2D array IC.

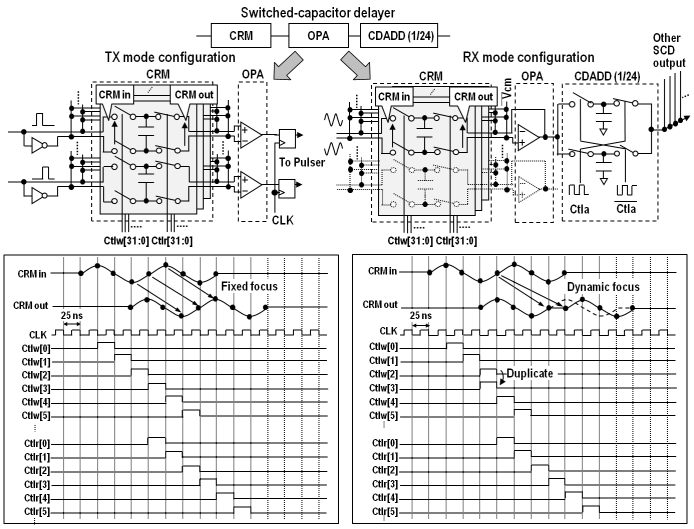

Figure 27.6.3: Switched-capacitor delayer circuit (top). Timing chart of fixed focus (bottom left) and dynamic focus (bottom right).

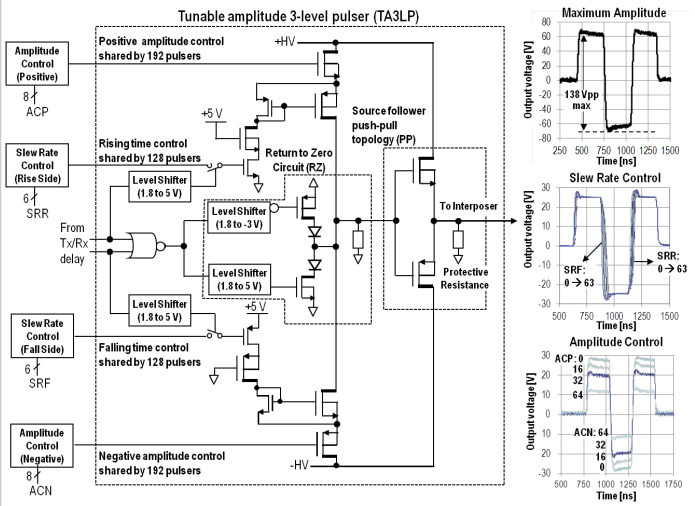

Figure 27.6.4: Circuit diagram of tunable amplitude 3-level pulser and its control block.

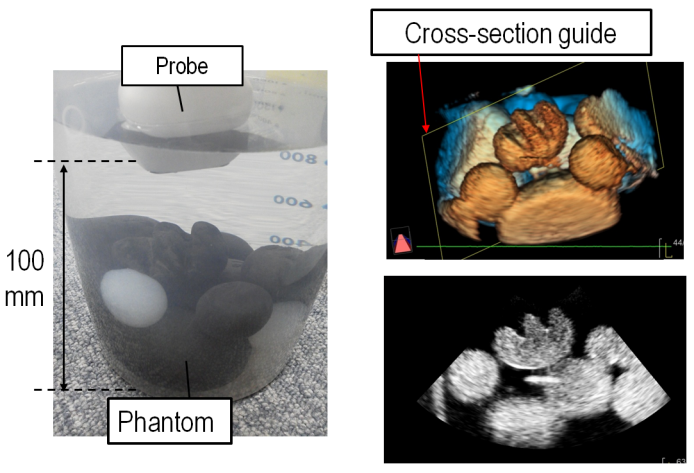

Figure 27.6.5: Evaluated 3D image (top right) and 2D cutting plain images from the full-volume 3D dataset (bottom right).

	This work	ISSCC2015 [1]	ISSCC2014 [2]	ISSCC2013 [3]	JSSC2016 [4]	JSSC2013 [5]	VLSI2016 [6]
Beamformer integration	Analog RX / All-digital TX	TX	Analog + Digital RX	TX	-	-	RX
Number of channels	3072 / 128	7 / 7	64 / 8	256 / 256	256 / 256	4 / 4	1024 / 96
Die area	416.64 mm^2	2.00 mm^2	19.40 mm^2	60.00 mm^2	33.00 mm^2	-	37.21 mm^2
Area / channel	0.09 mm^2	0.08 mm^2	0.17 mm^2	0.14 mm^2	0.07 mm^2	0.33 mm^2	0.022 mm^2
Power consumption / channel	0.7 mW*	18.6 mW	1.0 mW	1.0 mW	8.5 mW	66.7 mW	0.27 mW (RX only)
Delay time resolution	25 ns	5ns	6.25 ns	-	-	-	30.3 ns
Max delay time	750 ns	-	8000 ns	-	-	-	210 ns
TX max amplitude	138 Vpp	32 Vpp	-	25 Vpp	30 Vpp	30 Vpp	30 Vpp
Transducer type	Bulk Piezoelectric Material Transducer	PMUT	CMUT	CMUT	CMUT	CMUT	PZT
Process	0.18 μm HV SOI CMOS	TSMC 0.18 μm 32V	0.13 μm CMOS	1.5 μm high voltage	TSMC 0.18 μm HV CMOS	-	0.18μm LV CMOS

*Under B mode imaging condition
TX: Center freq. 2 MHz, Pulse-repetition freq. 4.3 kHz, RX: Input sensitivity 56 μVpp, Dynamic range 85 dB, -3dB Bandwidth 4.6 MHz

Figure 27.6.6: Comparison table of ultrasound array IC.

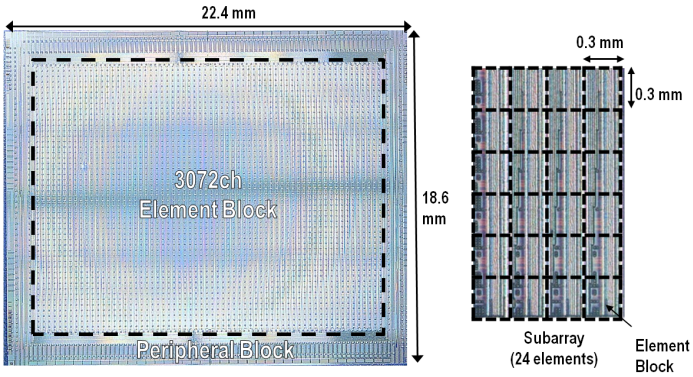

Figure 27.6.7: Die photograph.

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