

Verification of Digital Circuits – lab 1

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Repository URL: <https://github.com/Aleksandra564/VDIC/tree/lab1>

Test specification:

1. Test of parity error flag (`arg_parity_error = 1`) when input parity (`arg_a_parity` or `arg_b_parity`) is incorrect.
2. Test of multiplication for corner values at input (minimum, maximum and zero).
3. Test of parity calculation (`result_parity`) for input corner values and correct/incorrect parity bit.