Verification of Digital Circuits – lab 1

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Repository URL: https://github.com/Aleksandra564/VDIC/tree/lab1

Test specification:

1. Check if parity error flag works (displays „Parity error flag test PASSED/FAILED”).
2. Check if multiplication result is correct (displays „MUL test PASSED/FAILED”) for positive and negative numbers.
3. Check if parity is calculated correctly ("Parity test PASSED/FAILED").
4. Check if reset signal works.
5. Check if req flag makes that data is being processed.