Verification of Digital Circuits

Aleksandra Fudali, 401564

Repository URL: https://github.com/Aleksandra564/VDIC/tree/lab1

Test specification:

- 1. Test for corner values at 16-bit inputs separaterly:
 - All zeros
 - Minimum value
 - Maximum value
 - Negative values except minimum
 - Positive values except maximum
- 2. Test of parity error flag when input parity is correct/incorrect.
- 3. Test of parity calculation for both inputs separaterly, for input corner values and parity bit 0 or 1.
- 4. Change reset state during runtime.