ECSE 310 Thermodynamics of Computer, Winter 2019
Homework 1

Assigned: January 30th 2019
Due: February 8th 2019, 11:59 pm
Submission instructions: Please submit your assignment online via MyCourses assignment tool prior to the deadline. If your submission is handwritten please provide a high quality image (preferably scanned using uPrint or similar). Poor quality digital photos may be rejected. Include any workings and calculations that you performed in completing the assignment.
Late policy: 1% deduction per hour
Academic integrity reminder: In submitting this assignment on MyCourses you are attesting that it is the result of your own work.

(Each question has the same weight)

1. Briefly define the following:
   a) kWh
   b) CO2e
   c) GHG
   d) Activity factor (for microprocessor)
   e) Dynamic switching energy
   f) N-type and p-type semiconductor
   g) NMOS and PMOS (draw symbols, mark current direction, source, drain)
   h) CMOS
   i) Local interconnect
   j) Global interconnect
   k) Sheet resistance

2. Answer the following questions:
   a) Describe why capacitor and inductor can give delay.
   b) Use a formula to explain why IBM airgap process is better (in terms of switching speed and switching energy).
   c) Why is it more convenient to use sheet resistance to model interconnects?

3. The current leader of the Top500 supercomputer table (https://www.top500.org/lists/2017/11/) is the Sunway TaihuLight (National Supercomputing Center, Wuxi, China), which has a peak performance of $125*10^{15}$ Flop/s ("Flop/s" means floating point operations per second, which characterizes computing device performance) and a power consumption of 15,000 kW.
   a) Calculate the number of computations per kWh
   b) Given that an average Canadian home consumes 11,000 kWh per year of electricity, how many homes could be run on the power consumed by this supercomputer?

4. a) Using the model for interconnect power given in class (in the notes, lecture 2.2: Interconnect (III)), extend the model to obtain equations for i) interconnect **delay** and ii) **energy** for a buffered line, where we divide the total line length *L* into *N* segments.
   b) Obtain an expression for the value of *N* which minimizes the delay

c) Plot delay and energy as a function of *N* for the following parameters: C_{in} = 0.89 fF, R_L = 0.04 Ω/square, C_A = 50 aF/μm^2, C_0=5 x C_{in}, R_{in} = 14 kΩ, V = 1 V, w = 0.1 μm, L = 50 mm and validate the expression you obtained in (b) above.

5. The Intel 8086 microprocessor was introduced in 1978. It had an initial clock frequency of 5 MHz, and had 29,000 transistors, made with 3 μm technology operating at 5 V. The die size was 33 mm^2. Assume a switching energy per transistor of 1 pJ. The design power was 1.9 W.
   a) Estimate the capacitance of the transistors from the data above
   b) Assuming an activity factor of 0.1. estimate the power dissipation due to transistor switching
   c) For the given thermal design power of 1.9 W, what was the power dissipation per unit area?
   d) Assume the same technology is now scaled down to 22 nm transistors, but that the die size remains the same (i.e. the number of transistors per chip is increased commensurately—although that's not a real life scenario). Assume the activity factor remains the same. Estimate the:
      - Number of transistors
      - Clock frequency
      - Switching energy per transistor
      - Total power dissipation due to transistor switching
      - Voltage

      Which of these values have not been achieved in practice? Why?
   e) Assuming an operating voltage of 1 V (but keeping number of transistors and clock frequency as estimated above), estimate the switching energy per transistor and the associated power dissipation for the chip.