**eZ80F915050MODG**

# eZ80F91 Module

**Product Specification**

PS019312-0907

Zilog products are designed and manufactured under an ISO registered 9001:2000 Quality Management System. For more details, please visit www.zilog.com/quality.

**ISO 9001:2000**
**FS 507510**

# Revision History

Each instance in the Revision History reflects a change to this document from its previous revision. For more details, refer to the corresponding pages or appropriate links given in the table below.

| Date | Revision Level | Description | Page No |
|------|-------|-------------|---------|
| September 2007 | 12 | Changed eZ80F915050MOD to eZ80F915050MODG | i |
| July 2006 | 11 | Removed PRELIMINARY | All |
| July 2004 | 10 | Formatted to current publication standards | All |
| | | Part number change to AMD MII in Ethernet PHY and RJ45 Connector section | 12 |
| | | Part number change to internal crystal at jumper location Y3 in Table 6 | 21 |
| March 2004 | 09 | Updated  Schematics | 24 |
| Dec 2003 | 08 | Updated  eZ80F91 Module Bill of Materials | 21 |

# Table of Contents

# eZ80F91 Module

Zilog's eZ80F91 Module is a compact, high-performance Ethernet module specially designed for the rapid development and deployment of embedded systems requiring control and internet/intranet connectivity.

This expandable module is powered by Zilog's latest power-efficient, high-speed, optimized pipeline architecture eZ80F91 microcontroller, a member of Zilog's family of eZ80Acclaim! Flash microcontrollers.

The eZ80F91 is a high-speed single-cycle instruction-fetch microcontroller, which operates with a clock speed of 50 MHz. It can also operate in Z80$^{®}$-compatible addressing mode (64 KB) or full 24-bit addressing mode (16 MB).

The rich-peripheral set of the eZ80F91 Module makes it suitable for a variety of applications including industrial control, IrDA connectivity, communication, security, automation, point-of-sale terminals, and embedded networking applications.

## eZ80F91 Module Features

Features of eZ89F91 Module include:

- Factory-default operating clock frequency at 50 MHz

- 10/100 Base-T Ethernet PHY with RJ45 connector

- 512 KB fast SRAM

- 256 KB on-chip Flash memory

- 1 MB OFF-chip NOR Flash memory

- Battery-backed Real-time clock

- Input/Output connector which provides 32 general-purpose 5 V-tolerant I/O pinouts

- Zilog's industry-leading IrDA transceiver—Zilog ZHX1810

- Onboard connector provides I/O bus for external peripheral connections (IRQ, $\overline{CS}$, 24 address, and 8 data)

- Low-cost connection to carrier board via two 2 x 30 pin headers

- Small footprint 63.5 mm x 78.7 mm

- 3.3 V power supply

- Standard operating temperature range: 0 ºC to +70 ºC

# eZ80F91 Controller Features

Features of eZ80F91 Controller include:

- The eZ80F91 device contains 256 KB of Flash memory and 8 KB of SRAM

- Single-cycle instruction fetch, high-performance, pipelined eZ80 CPU core

- 10/100 Mbps Ethernet MAC with 8 KB frame buffer

- Low power features including SLEEP mode, HALT mode, and selective peripheral power-down control

- Two UARTs with independent baud rate generators and support for 9-bit operation

- SPI with independent clock generator

- $I^2C$ with independent clock generator

- Infrared data association (IrDA)-compliant infrared encoder/decoder

- New DMA-like eZ80 instructions for efficient block data transfer

- External interface with 4 chip selects, individual wait state generators, and an external WAIT input pin—supports Intel- and Motorola-style buses

- Flexible-priority vectored interrupts (both internal and external) and interrupt controller

- Real-time clock with on-chip 32 kHz oscillator, selectable 50/60 Hz input, and separate $V_{DD}$ pin for battery backup

- Four 16-bit Counter/Timers with prescalers and direct input/output drive

- Watchdog Timer (WDT)

- 32 bits of general-purpose input/output (GPIO)

- JTAG and ZDI debug interfaces

- 144-pin LQFP package

- 3.0–3.6 V supply voltage with 5 V tolerant inputs

- Standard operating temperature range: 0 ºC to +70 ºC

# Block Diagram

Figure 1 illustrates the block diagram of eZ80F91 Module.
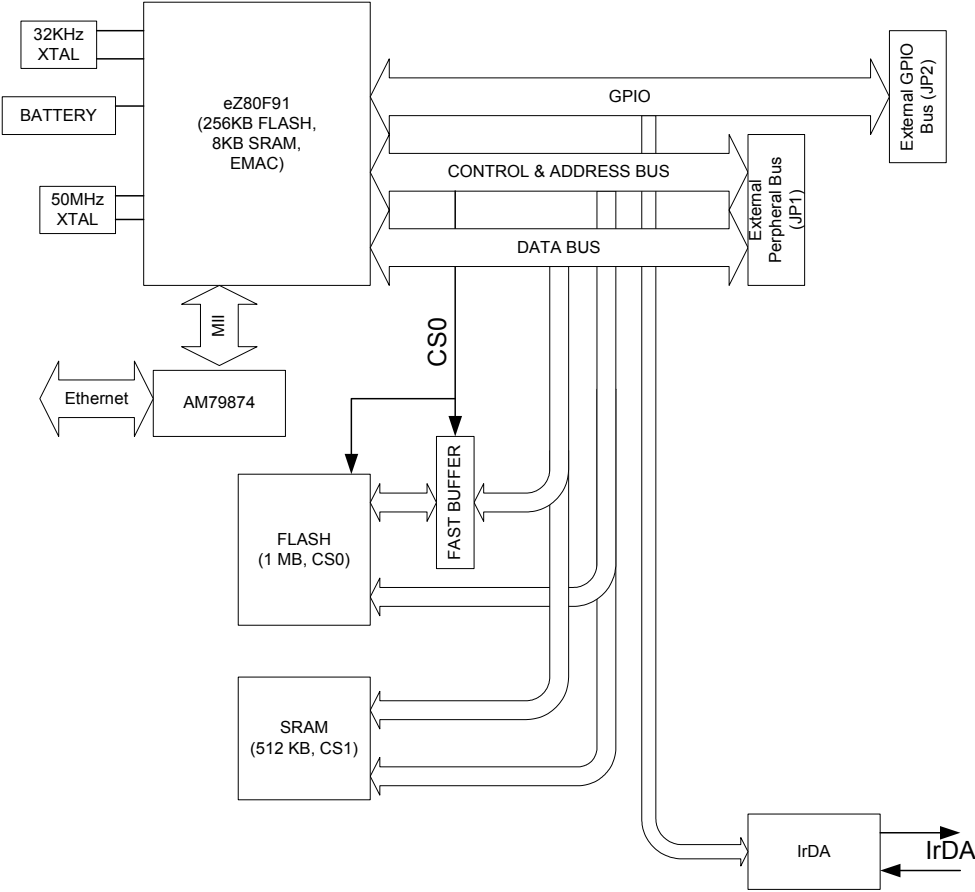


**Figure 1.  eZ80F91 Module Functional Block Diagram**

# Pin Description

## Peripheral Bus Connector

Figure 2 illustrates the pin layout of the 60-pin Peripheral Bus Connector (JP1) of the eZ80F91 Module. The eZ80 development platform, however, features a 50-pin connector. The eZ80F91 Module is designed to interface pin 60 of its JP1 connector to pin 50 of the eZ80 development platform's JP1 connector so that pins 1–10 of the eZ80F91 Module overlap the edge of the eZ80 development platform. Table 1 on page 5 describes the pins and their functions.
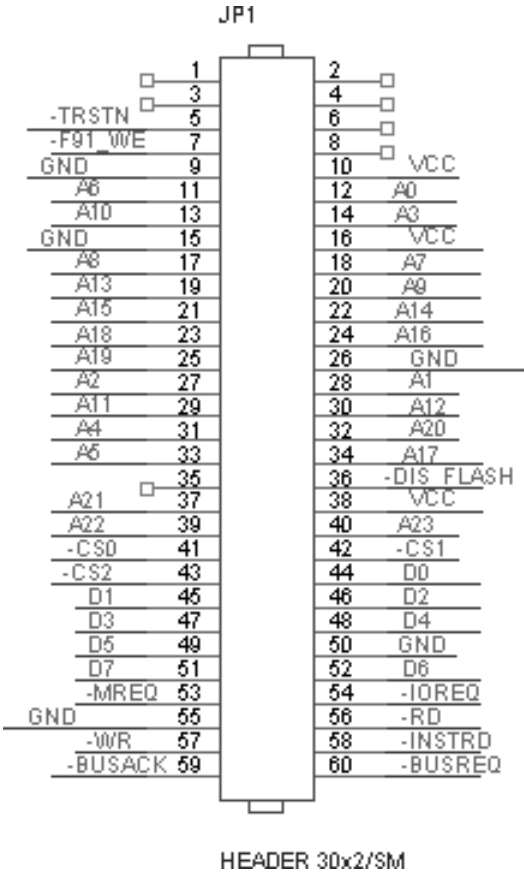


**Figure 2. eZ80F91 Module Peripheral Bus Connector Pin Configuration—JP1**

> **Note:** *All signals with an $\overline{overline}$ are active Low. For example, B/$\overline{W}$, for which WORD is active Low, and $\overline{B}$/W, for which BYTE is active Low.*

**Table 1. eZ80F91 Module Peripheral Bus Connector Pin Identification\***

| Pin No | Symbol | Pull Up/Down* | Signal Direction | Comments |
|---|---|---|---|---|
| 1 | Reserved | | | |
| 2 | Reserved | | | |
| 3 | Reserved | | | |
| 4 | Reserved | | | |
| 5 | $\overline{TRSTN}$ | | Input | Reset for on-chip instrumentation (OCI). |
| 6 | Reserved | | | |
| 7 | $\overline{F91\_WE}$ | PU 10 kΩ | Input | A Low enables a Write to on-chip Flash memory. If this pin is unconnected, on-chip Flash memory is write-protected. |
| 8 | Reserved | | | |
| 9 | GND | | | $V_{SS}$/Ground (0 V). |
| 10 | $V_{CC}$ | | | 3.3 V supply input pin. |
| 11 | A6 | | Bidirectional | |
| 12 | A0 | | Bidirectional | |
| 13 | A10 | | Bidirectional | |
| 14 | A3 | | Bidirectional | |
| 15 | GND | | | $V_{SS}$/Ground (0 V). |
| 16 | $V_{CC}$ | | | 3.3 V supply input pin. |
| 17 | A8 | | Bidirectional | |
| 18 | A7 | | Bidirectional | |
| 19 | A13 | | Bidirectional | |
| 20 | A9 | | Bidirectional | |
| 21 | A15 | | Bidirectional | |
| 22 | A14 | | Bidirectional | |
| 23 | A18 | | Bidirectional | |
| 24 | A16 | | Bidirectional | |

**Table 1. eZ80F91 Module Peripheral Bus Connector Pin Identification\* (Continued)**

| Pin No | Symbol | Pull Up/Down* | Signal Direction | Comments |
|--------|--------|---------------|------------------|----------|
| 25 | A19 | | Bidirectional | |
| 26 | GND | | | $V_{SS}$/Ground (0 V). |
| 27 | A2 | | Bidirectional | |
| 28 | A1 | | Bidirectional | |
| 29 | A11 | | Bidirectional | |
| 30 | A12 | | Bidirectional | |
| 31 | A4 | | Bidirectional | |
| 32 | A20 | | Bidirectional | |
| 33 | A5 | | Bidirectional | |
| 34 | A17 | | Bidirectional | |
| 35 | Reserved | | | |
| 36 | $\overline{\text{DIS\_Flash}}$ | PU 10 kΩ | Input | A Low disables onboard Flash memory. Flash is enabled if $\overline{\text{DIS\_Flash}}$ is not connected; CMOS Input 3.3 V (5 V tolerant). |
| 37 | A21 | | Bidirectional | |
| 38 | $V_{CC}$ | | | 3.3 V supply input pin. |
| 39 | A22 | | Bidirectional | |
| 40 | A23 | | Bidirectional | |
| 41 | $\overline{\text{CS0}}$ | | Output | |
| 42 | $\overline{\text{CS1}}$ | | Output | |
| 43 | $\overline{\text{CS2}}$ | | Output | |
| 44 | D0 | PU 4 kΩ | Bidirectional | |
| 45 | D1 | PU 4 kΩ | Bidirectional | |
| 46 | D2 | PU 4 kΩ | Bidirectional | |
| 47 | D3 | PU 4 kΩ | Bidirectional | |
| 48 | D4 | PU 4 kΩ | Bidirectional | |
| 49 | D5 | PU 4 kΩ | Bidirectional | |
| 50 | GND | | | $V_{SS}$/Ground (0 V). |
| 51 | D7 | PU 4 kΩ | Bidirectional | |

**Table 1. eZ80F91 Module Peripheral Bus Connector Pin Identification\* (Continued)**

| Pin No | Symbol | Pull Up/Down* | Signal Direction | Comments |
|---|---|---|---|---|
| 52 | D6 | | Bidirectional | |
| 53 | $\overline{\text{MREQ}}$ | | Bidirectional | |
| 54 | $\overline{\text{IORQ}}$ | | Bidirectional | |
| 55 | GND | | | $V_{SS}$/Ground (0 V). |
| 56 | $\overline{\text{RD}}$ | | Bidirectional | |
| 57 | $\overline{\text{WR}}$ | | Bidirectional | |
| 58 | $\overline{\text{INSTRD}}$ | | Output | |
| 59 | $\overline{\text{BUSACK}}$ | | Output | |
| 60 | $\overline{\text{BUSREQ}}$ | PU 2 kΩ | Input | |

\*Notes

1. External capacitive loads on $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{IORQ}}$, $\overline{\text{MREQ}}$, D0–D7, and A0–A23 must be below 10 pF to satisfy timing requirements for the CPU.
2. All unused inputs must be pulled to either $V_{DD}$ or GND, depending on their inactive levels, to reduce power consumption and to reduce noise sensitivity.
3. All inputs are CMOS level 3.3 V (5 V tolerant), except where otherwise noted.

# Input/Output Connector

Figure 3 on page 8 illustrates the pin layout of the 60-pin I/O Connector (JP2) of the eZ80F91 Module. However, the eZ80 development platform features a 50-pin connector. The eZ80F91 Module is designed to interface pin 60 of its JP2 connector to pin 50 of the eZ80 development platform's JP2 connector so that pins 1–10 of the eZ80F91 Module overlap the edge of the eZ80 development platform. Table 2 on page 8 describes the pins and their functions.
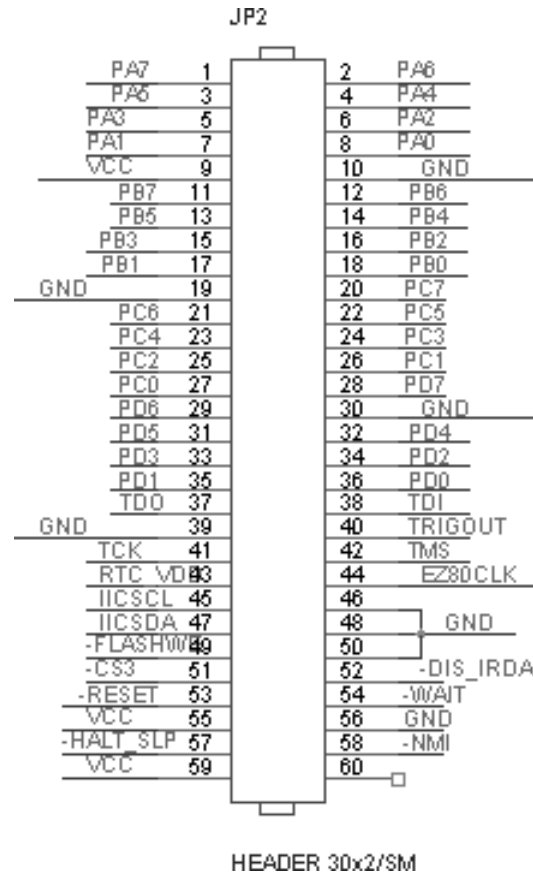
**Figure 3. eZ80F91 Module Input/Output Connector Pin Configuration—JP2**

**Table 2. eZ80F91 Module Input/Output Connector Pin Identification\***

| Pin No | Symbol | Pull Up/Down | Signal Direction | Comments |
|--------|--------|--------------|------------------|----------|
| 1 | PA7 | | Bidirectional | |
| 2 | PA6 | | Bidirectional | |
| 3 | PA5 | | Bidirectional | |
| 4 | PA4 | | Bidirectional | |
| 5 | PA3 | | Bidirectional | |
| 6 | PA2 | | Bidirectional | |
| 7 | PA1 | | Bidirectional | |
| 8 | PA0 | | Bidirectional | |

**Table 2. eZ80F91 Module Input/Output Connector Pin Identification\* (Continued)**

| Pin No | Symbol | Pull Up/Down | Signal Direction | Comments |
|--------|--------|--------------|------------------|----------|
| 9 | $V_{CC}$ | | | 3.3 V supply input pin. |
| 10 | GND | | | $V_{SS}$/Ground (0 V). |
| 11 | PB7 | | Bidirectional | |
| 12 | PB6 | | Bidirectional | |
| 13 | PB5 | | Bidirectional | |
| 14 | PB4 | | Bidirectional | |
| 15 | PB3 | | Bidirectional | |
| 16 | PB2 | | Bidirectional | |
| 17 | PB1 | | Bidirectional | |
| 18 | PB0 | | Bidirectional | |
| 19 | GND | | | $V_{SS}$/Ground (0 V). |
| 20 | PC7 | | Bidirectional | |
| 21 | PC6 | | Bidirectional | |
| 22 | PC5 | | Bidirectional | |
| 23 | PC4 | | Bidirectional | |
| 24 | PC3 | | Bidirectional | |
| 25 | PC2 | | Bidirectional | |
| 26 | PC1 | | Bidirectional | |
| 27 | PC0 | | Bidirectional | |
| 28 | PD7 | | Bidirectional | |
| 29 | PD6 | | Bidirectional | |
| 30 | GND | | | $V_{SS}$/Ground (0 V). |
| 31 | PD5 | | Bidirectional | |
| 32 | PD4 | PD 4 k$\Omega$ | Bidirectional | |
| 33 | PD3 | | Bidirectional | |
| 34 | PD2 | | Bidirectional | |
| 35 | PD1 | | Bidirectional | |
| 36 | PD0 | | Bidirectional | |
| 37 | TDO | | Output | JTAG Data Output pin. |

**Table 2. eZ80F91 Module Input/Output Connector Pin Identification\* (Continued)**

| Pin No | Symbol | Pull Up/Down | Signal Direction | Comments |
|---|---|---|---|---|
| 38 | TDI/ZDA | | Input | JTAG Data Input pin. |
| 39 | GND | | | $V_{SS}$/Ground (0 V). |
| 40 | TRIGOUT | | Output | Active High trigger event indicator. |
| 41 | TCK/ZCL | PU 10 kΩ | Input | JTAG Input. High on reset enables ZDI mode; Low on reset enables OCI debug. |
| 42 | TMS | PU 10 kΩ | Input | JTAG Test Mode Select Input. |
| 43 | RTC_$V_{DD}$ | | | RTC supply. For proper operation of the eZ80F91 Module, this pin must be connected to the same power source that powers the module (as is done on the Zilog development platform). |
| 44 | EZ80CLK | | Output | Synchronous CPU clock output. |
| 45 | I²CSCL | PU 4 kΩ | Bidirectional | I²C Bus Clock. |
| 46 | GND | | | $V_{SS}$/Ground (0 V). |
| 47 | I²CSDA | PU 4 kΩ | Bidirectional | I²C Data Clock. |
| 48 | GND | | Power | $V_{SS}$/Ground (0 V). |
| 49 | $\overline{FlashWE}$ | PU 10 kΩ | Input | A Low enables a Write to external Flash memory boot block area. If this pin is unconnected, the Flash memory boot block area is write-protected. |
| 50 | GND | | | $V_{SS}$/Ground (0 V). |
| 51 | $\overline{CS3}$ | | Output | Used on the eZ80190, eZ80L92, eZ80F92, eZ80F93 devices and connected to the CS8900 EMAC. |
| 52 | $\overline{DIS\_IRDA}$ | PU 10 kΩ | Input | A Low disables the onboard IRDA transceiver to use PC0/PC1 UART pins externally. |
| 53 | $\overline{RESET}$ | PU 2 kΩ | Bidirectional | Reset Output from module or push-button reset. |
| 54 | $\overline{WAIT}$ | PU 2 kΩ | Input | Driving the $\overline{WAIT}$ pin Low forces the CPU to provide additional clock cycles for an external peripheral or external memory to complete its Read or Write operation. |
| 55 | $V_{CC}$ | | | 3.3 V supply input pin. |
| 56 | GND | | | $V_{SS}$/Ground (0 V). |

**Table 2. eZ80F91 Module Input/Output Connector Pin Identification\* (Continued)**

| Pin No | Symbol | Pull Up/Down | Signal Direction | Comments |
|---|---|---|---|---|
| 57 | $\overline{\text{HALT\_SLP}}$ | | Output, Active Low | A Low on this pin indicates that the CPU enters either HALT or SLEEP mode because of execution of either a HALT or SLP instruction. |
| 58 | $\overline{\text{NMI}}$ | PU 10 kΩ | Schmitt Trigger Input, Active Low | The $\overline{\text{NMI}}$ input is a higher priority input than the maskable interrupts. It is always recognized at the end of an instruction, regardless of the state of the interrupt enable control bits. This input includes a Schmitt trigger to allow RC rise times. This external $\overline{\text{NMI}}$ signal is combined with an internal $\overline{\text{NMI}}$ signal generated from the WDT block before being connected to the $\overline{\text{NMI}}$ input of the CPU. |
| 59 | $V_{CC}$ | | | 3.3 V supply input pin. |
| 60 | Reserved | | NC | Reserved—No Connection. |

\*Notes
1. External capacitive loads on $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{IORQ}}$, $\overline{\text{MREQ}}$, D0–D7, and A0–A23 must be below 10 pF to satisfy timing requirements for the CPU.
2. All unused inputs must be pulled to either $V_{DD}$ or GND, depending on their inactive levels, to reduce power consumption and to reduce noise sensitivity.
3. All inputs are CMOS level 3.3 V (5 V tolerant), except where otherwise noted.

# Onboard Component Description

## Logic-Level Input/Outputs

The I/O connector features 32 general-purpose 3.3 V CMOS I/O pins that can be used as outputs or inputs interfacing to external logic. All I/Os are 5 V tolerant. Some of the general-purpose I/O pins support dual mode functions (SPI, Timer I/O, UARTs, and bit I/O with edge- or level-triggered interrupt functions on each pin). For more information on eZ80F91 dual modes, refer to *eZ80F91 Product Specification (PS0192)*.

## Onboard Battery Backup

An onboard Panasonic VL-1220-1VC 3 V Lithium battery powers the 32 kHz real-time clock when external power is removed. The battery is charged through diode CR1 and resistor R28 when external power is applied to the board.

## Ethernet PHY and RJ45 Connector

The eZ80F92 Ethernet Module contains Advanced Micro Devices' Am79C874 Media-Independent Interface (MII) and a HALO RJ45 with integrated magnetics (transformer and common-mode chokes) and two LED indicators.

The MII enables different modes of Ethernet communication, configurable by resistors R19, R21, R23, and R24. The eZ80F92 Ethernet Module is shipped with all four resistors installed. Table 3 lists the available resistor settings and is excerpted from the Am79C874 data sheet published by AMD.

**Table 3. eZ80F92 Ethernet Module MII Resistor Configuration**

| R24 ANEG | R19 (Tech[2]) | R23 (Tech[1]) | R21 (Tech[0]) | Speed | Full-Duplex | ANEG-EN | Capabilities | ANEG |
|:---:|:---:|:---:|:---:|:---:|:---:|:---:|:---:|:---:|
| IN | IN | IN | IN | Yes[1] | Yes[1] | No | All | Disabled |
| IN | IN | IN | OUT | No | No | No | 10HD | Disabled |
| IN | IN | OUT | IN | No | No | No | 100HD | Disabled |
| IN | IN | OUT | OUT | No | No | No | 100HD | Disabled |
| IN | OUT | IN | IN | Yes[1] | Yes[1] | No | All | Disabled |
| IN | OUT | IN | OUT | No | No | No | 10FD | Disabled |
| IN | OUT | OUT | IN | No | No | No | 100FD | Disabled |

**Table 3. eZ80F92 Ethernet Module MII Resistor Configuration (Continued)**

| R24 ANEG | R19 (Tech[2]) | R23 (Tech[1]) | R21 (Tech[0]) | Speed | Full-Duplex | ANEG-EN | Capabilities | ANEG |
|---|---|---|---|---|---|---|---|---|
| IN | OUT | OUT | OUT | No | No | No | 100FD | Disabled |
| OUT | IN | IN | IN | Yes$^2$ | Yes$^2$ | Yes$^3$ | None | Enabled |
| OUT | IN | IN | OUT | Yes$^2$ | Yes$^2$ | Yes$^3$ | 10HD | Enabled |
| OUT | IN | OUT | IN | Yes$^2$ | Yes$^2$ | Yes$^3$ | 100HD | Enabled |
| OUT | IN | OUT | OUT | Yes$^2$ | Yes$^2$ | Yes$^3$ | 100HD, 10HD | Enabled |
| OUT | OUT | IN | IN | Yes$^2$ | Yes$^2$ | Yes$^3$ | None | Enabled |
| OUT | OUT | IN | OUT | Yes$^2$ | Yes$^2$ | Yes$^3$ | 10FD/HD | Enabled |
| OUT | OUT | OUT | IN | Yes$^2$ | Yes$^2$ | Yes$^3$ | 100FD/HD | Enabled |
| OUT | OUT | OUT | OUT | Yes$^3$ | Yes$^2$ | Yes$^3$ | All | Enabled |

*Notes
1. MII Register 0 (Speed and Duplex Bits) must be set by a MAC to achieve a link.
2. When autonegotiation is enabled, these bits are written but will be ignored by PHY.
3. The advertised abilities of MII Register 4 cannot exceed the abilities of MII Register 1. Autonegotiation must always be enabled.

## Ethernet LEDs

The Ethernet connection is provided by the HALO RJ45 connector. It consists of two green LEDs that are located next to each other on the eZ80F91 Module. When PHY is receiving data, the left LED is ON. When the PHY is transmitting data, the right LED is ON.

# Fast Buffer (U10)

The eZ80F91 Module's fast buffer (see Figure 1 on page 3) exists to prevent bus contention that occurs because of slow turn-off time of the module's external Flash and the fast bus turn-around time of the eZ80F91 (generic feature of the eZ80 family when it is used in NATIVE mode).

The problem related to bus contention when using eZ80 family of the microprocessors in NATIVE eZ80 mode is explained below, see Figure 4 on page 14. For more details, refer to *eZ80F91 Product Specification (PS0192)*.

Bus contention occurs when two or more devices drive a common bus. The eZ80F91's CS0 drives the Flash CE. After the access to Flash, CS0 is driven High a maximum of 8.8 ns after the next rising edge of the Clock (T6 in Figure 4). The Flash turn-off time ($T_{OD}$) is 25 ns, which is the time from OE or CE going High to the Flash output drivers going into

High-Z mode. That is, after the end of the eZ80F91 Read access to Flash, it takes 8.8 ns+25 ns = 33.8 ns before Flash stops driving the data bus. At this point, the eZ80F91 device is already well into the next bus cycle.

Consider the next cycle is Memory Write. During the Memory Write cycle, data (output) from the eZ80F91 device is valid not later than T3 = 7.5 ns, and the Write pulse is asserted not later than 4.5 ns after the falling edge of the Clock (14.5 ns from the Rising edge if Clock is 50 MHz). It means that during $T_{CON}$ = (33.8 ns – 7.5 ns) = 26.3 ns; two devices drive the common Data Bus—the eZ80F91 device and Flash. In turn, data that is being written during the Write operation might be corrupted. The part used to isolate a slow Flash data bus from a fast eZ80F91 bus has 5.5 ns turn-off time, which reduces 25 ns part of the $T_{CON}$ to 5.5 ns. As a result, bus contention still occurs, but its duration is not 26.3 ns, as the following equation explains:

$$\text{Time of contention} = (8.8 \text{ ns} - 7.5 \text{ ns} + 5.5 \text{ ns}) = 6.8 \text{ ns}$$

Data being written is not corrupted because the Write pulse is not yet asserted.
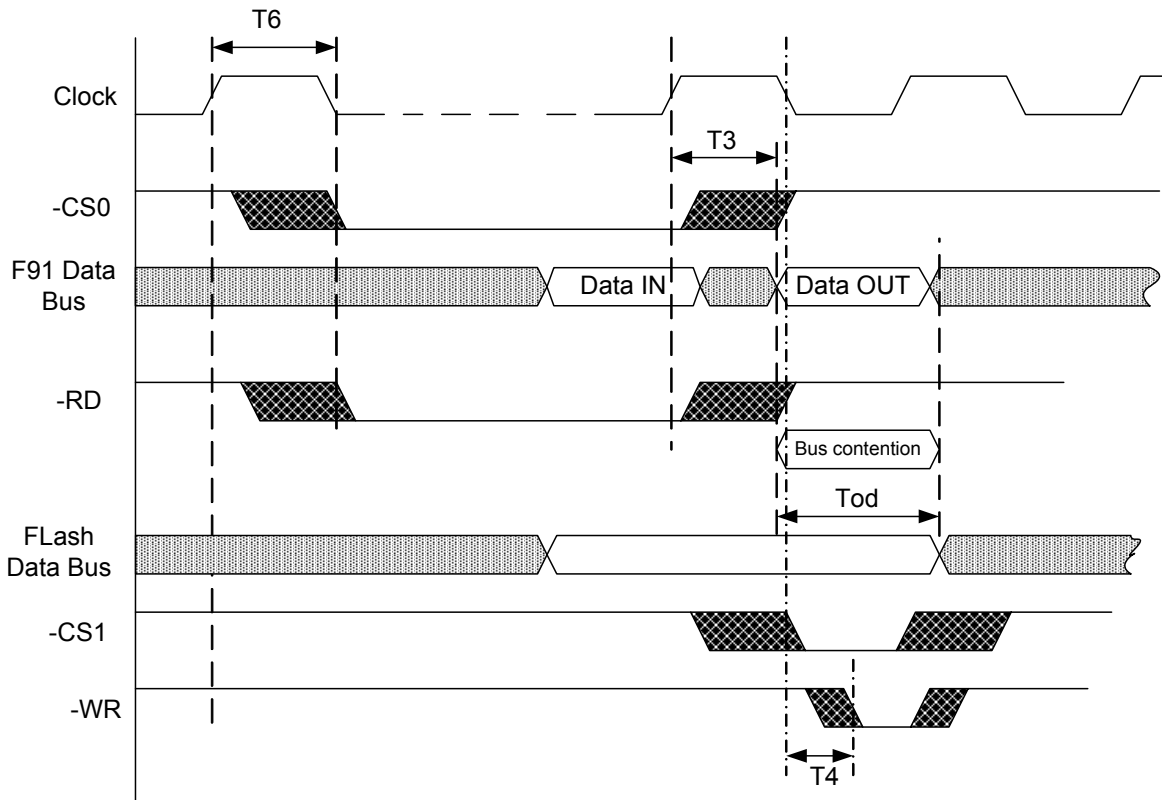


**Figure 4. Bus Contention without the eZ80F91 Module Fast Buffer Feature**

# Memory

The eZ80F91 Module contains external Flash memory and the eZ80F91 MCU contains internal Flash memory. To allow Read/Write access to Flash memory on the eZ80F91 Module, there are two signals provided on connectors JP1 and JP2. A jumper JP3 on the module enables programming of on-chip Flash.

There is also a signal that duplicates the function of this jumper. Table 4 describes the states of the signals and the status of the jumper for different modes.

**Table 4. Flash Memory Programming Signals and Jumpers**

| Signal/Jumper | Function | State/Status |
|---|---|---|
| DIS_FLASH | Controls Read/Write access to eZ80F91 Module external Flash memory | When Low, access is enabled |
| FlashWE | Controls Write operations to the boot block of eZ80F91 Module external Flash memory | When Low, Write is enabled |
| JP3 | Controls Write access to eZ80F91 MCU on-chip Flash memory | When IN, Write is enabled |
| F91_WE | Controls Write access to eZ80F91 MCU on-chip Flash memory | When Low, Write is enabled |

The external Flash memory of eZ80F91 Module has an access time of 100 ns. At least five wait states must be added to the cycle when accessing external Flash at 50 MHz clock speed. eZ80F91 MCU on-chip Flash is faster; its minimum access time is 60 ns, which requires only three wait states at 50 MHz.

There is 512 KB of fast SRAM on the eZ80F91 Module. Access time is 12 ns, which requires one wait-state access. The eZ80F91's on-chip SRAM is used with zero wait states.

# IrDA Transceiver

An onboard IrDA transceiver (Zilog ZHX1810) is connected to PD0 (TX), PD1 (RX), and PD2 (Shutdown, R_SD). The IrDA transceiver is of the LED type 870 nm Class 1.

The receiver supply current is 90 μA to 150 μA and the transmitter supply current is 260 mA when the LED is active. The IrDA transceiver is accessible via the IrDA controller attached to UART0 on the eZ80F91 device. The UART0 console and the IrDA transceiver cannot be used simultaneously.

To use the UART0 for console or to save power, the transceiver is disabled by the software or by an off-board signal when using the proper jumper selection. The transceiver is disabled by setting PD2 (IR_SD) High or by pulling the $\overline{\text{DIS\_IRDA}}$ pin on the I/O connector Low. The shutdown is used for power savings. To enable the IrDA transceiver, $\overline{\text{DIS\_IRDA}}$ is left floating and PD2 is set to Low.

# Reset Generator

The onboard Reset Generator Chip performs reliable Power-on reset. The chip generates a reset pulse with a duration of 200 ms if the power supply drops below 2.93 V. This reset pulse ensures that the board always starts in a defined condition. The RESET pin on the I/O connector reflects the status of the RESET line. It is a bidirectional pin for resetting external peripheral components or for resetting the eZ80F91 Module with a low-impedance output (for example, a 100 Ω pushbutton).

# Serial Interface Ports

The CPU contains two UARTs with programmable baud rate generators. UART0 is connected to GPIO PD[0:7] on the I/O connector. UART1 is connected to GPIO PC[0:7] on the I/O connector.

▶ **Note:** *Do not connect an RS232 interface without level shifters. There are no RS232-level shifters on the eZ80F91 Module.*

# Physical Dimensions

The footprint of the eZ80F91 Module PCB is 63.5 mm x 78.7 cm. With an RJ-45 Ethernet connector, the overall height is 25 mm, see
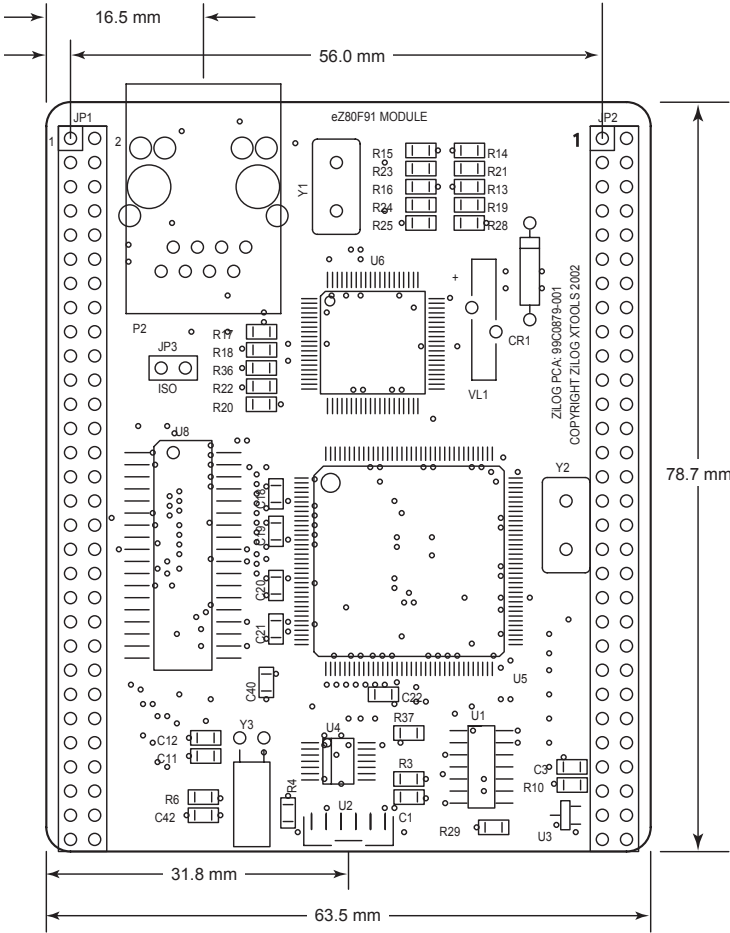
**Figure 5.  Physical Dimensions of the eZ80F91 Module**

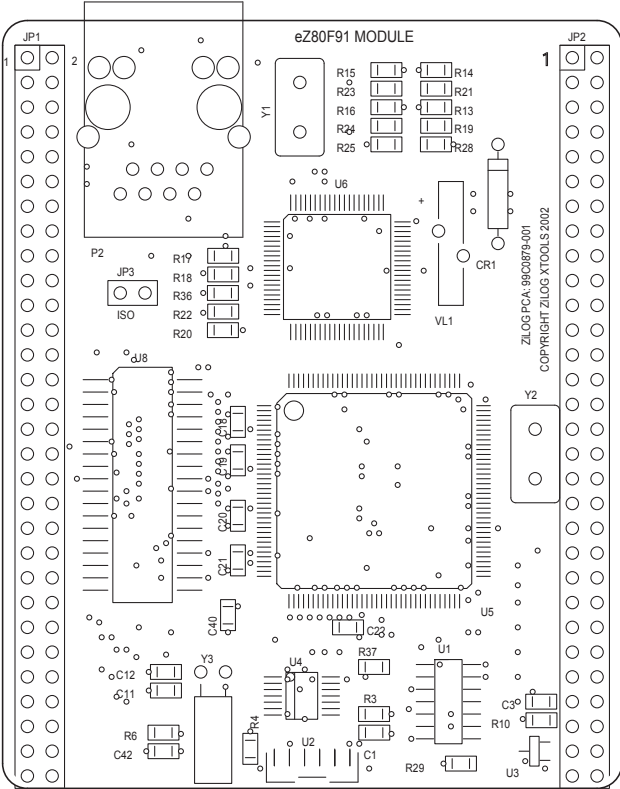Figure 6 illustrates the top layer silk-screen of the eZ80F91 Module.

**Figure 6.  eZ80F91 Module—Top Layer**

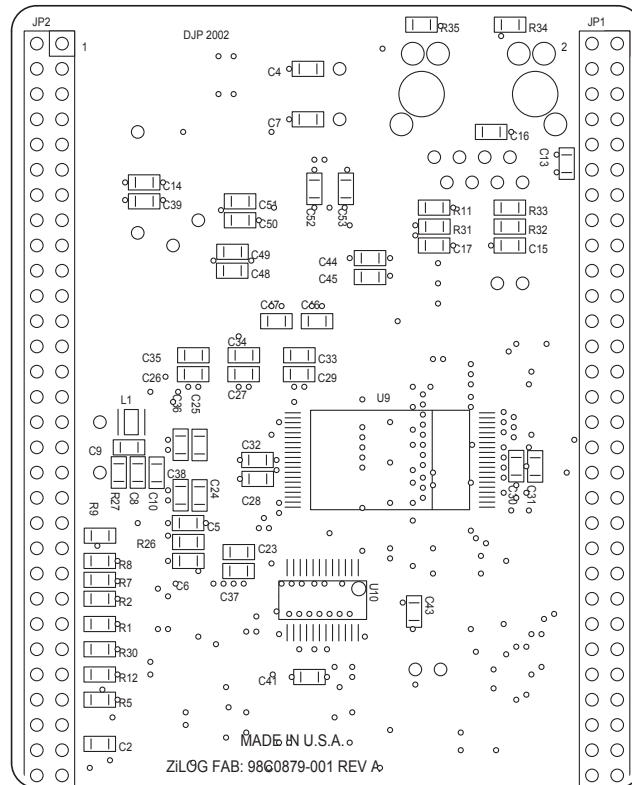Figure 7 illustrates the bottom layer silk-screen of the eZ80F91 Module.



**Figure 7.  eZ80F91 Module—Bottom Layer**

## Absolute Maximum Ratings

Stresses greater than those listed in Table 5 on page 20 causes permanent damage to the device. These ratings are stress ratings only. Operation of the device at any condition outside those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. For improved reliability, unused inputs must be tied to one of the supply voltages ($V_{DD}$ or $V_{SS}$).

**Table 5. Absolute Maximum Ratings**

| Parameter | Minimum | Maximum | Units |
|---|---|---|---|
| Standard operating temperature | 0 | +70 | °C |
| Storage temperature | –45 | +85 | °C |
| Operating Humidity (RH @ 50 °C) | 25% | 90% | |
| Operating Voltage | — | 3.6 | V |

## eZ80F91 Module Bill of Materials

Table 6 lists the installed components of the eZ80F91 Module.

**Table 6. Bill of Materials for the eZ80F91 Module**

| Part Number | Part Name | Quantity | Jumper Location | Manufacturer |
|---|---|---|---|---|
| 98C0879-001 | Fab, eZ80F91 Module, Rev. B | 1 | — | Prime Technologies |
| 35-0180-12 | IC, SRAM, 512Kx8, 12 ns, 3 V, 36-SOJ | 1 | U8 | Alliance Semi. AS7C34096-12JC |
| 35-0016-05 | IC, 74LVC04, 3.3 V, GATE, 14-SOIC | 1 | U1 | Texas Instruments SN74LVC04AD |
| 35-0720-10 | IC, Flash, 1Mx8, 100 ns, 3 V, 40-TSSOP | 1 | U9 | Micron Technologies MT28F008B3VG-10B |
| 35-0719-00 | IC, MAX6328, RESET, SOT-23 | 1 | U3 | Maxim Inc. MAX6328UR29-T |
| ZHX1810 | IC, IR Transceiver, Low Profile | 1 | U2 | Zilog Inc. ZHX1810MV115THTR |
| 35-0062-01 | IC, 74LCX32, LV, QUAD OR, 14-TSSOP | 1 | U4 | Fairchild Semi. 74LCX32MTC |
| 35-0022-01 | IC, AM7C874, PHY XCVR, 80QFP | 1 | U6 | AMD AM79C874VC |
| eZ80F91 | IC, eZ80F91, 50 MHZ, 144VQFP | 1 | U5 | Zilog Inc. eZ80F91 |
| 35-0731-00 | IC, 74CBTLV3861PWR, 24-TSSOP | 1 | U10 | Texas Instruments SN74CBTLV3861PWR |
| 48-1013-01 | Diode, TVS Array, XCVR Prot, 8-SOIC | 1 | U9 | Semtec LCDA15C-6 |
| 17-2005-70 | CAP, 1000 pF, 50 V, Ceramic Chip, 0603 | 15 | C13, C14, C31-43 | Panasonic ECJ-1VC1H561J |
| 17-2005-66 | CAP, 0.1 µF, 16 V, Ceramic Chip, 0603 | 28 | C2,10, C15-30, C44-53 | Kemet Inc. C0603C104K5RAC |
| 17-2005-54 | CAP, 0.01 µF, 50 V, Ceramic Chip, 0603 | 1 | C3 | Panasonic ECJ-1VB1C103K |
| 17-2005-83 | CAP, 0.33 µF, 16 V, Ceramic Chip, 0603 | 1 | C1 | Panasonic ECJ-1VF1C334Z |
| 17-2005-63 | CAP, 560 pF, 50 V, Ceramic Chip, 0603 | 1 | C6 | Panasonic ECJ-1VC1H563K |

**Table 6. Bill of Materials for the eZ80F91 Module (Continued)**

| Part Number | Part Name | Quantity | Jumper Location | Manufacturer |
|---|---|---|---|---|
| 17-2001-03 | CAP, 12 pF, 50 V, Ceramic Chip, 0603 | 4 | C9, C11, C12 | Panasonic ECJ-1VC1H120J |
| 17-2001-05 | CAP, 22 pF, 50 V, CER CHIP, 0603 | 2 | C4, C7 | PANASONIC ECJ-1VC1H220J |
| 17-2001-20 | CAP, 270 pF, 50 V, CER CHIP, 0603 | 1 | C5 | PANASONIC ECJ-1VC1H271J |
| 17-2001-01 | CAP, 5 pF, 50 V, CER CHIP, 0603 | 1 | C8 | PANASONIC ECJ-1VC1H050C |
| 48-0051-00 | DIODE, 1N5817, RCTFR | 1 | CR1 | MOTOROLA 1N5817 |
| 16-9005-33 | INDUCTOR, 3.3 µH, 20%, 1210 SMD | 1 | L1 | PANASONIC ELJ-PA3R3MF |
| 46-3001-03 | Resistor, 10 K¾, 1%, 1/16 W, 0603 SMT | 15 | R3, 8, 10, R12-18, R20, 25, 29, 30, 37 | Sprague 420CK472X2PD |
| 46-3000-00 | Resistor, 0¾, 1%, 1/16 W, 0603 SMT | 4 | R19, 21, 23, 24 | " |
| 46-3000-71 | Resistor, 2.21 K¾, 1%, 1/16 W, 0603 SMT | 2 | R5, R6 | " |
| 46-3000-35 | Resistor, 68¾, 1%, 1/16 W, 0603 SMT | 1 | R3 | " |
| 46-3000-02 | RES, 2.2¾, 1%, 1/16 W, 0603 SMT | 1 | R4 | " |
| 46-3000-32 | RES, 49.9¾, 1%, 1/16 W, 0603 SMT | 4 | R11, 31, 32, 33 | " |
| 46-3000-63 | RES, 1 K¾, 1%, 1/16 W, 0603 SMT | 1 | R22 | " |
| 46-3000-56 | RES, 499 ¾,1%, 1/16 W, 0603 SMT | 1 | R26 | " |
| 46-3001-34 | RES, 200 K¾, 1%, 1/16 W, 0603 SMT | 1 | R27 | " |
| 46-3000-47 | RES, 221 ¾, 1%, 1/16 W, 0603 SMT | 1 | R28 | " |
| 46-3000-51 | RES, 332¾, 1%, 1/16 W, 0603 SMT | 2 | R34, R35 | " |
| 46-3001-75 | RES, 10 M¾, 1%, 1/16 W, 0603 SMT | 1 | R38 | " |
| 23-0000-25 | XTAL, 25.0000 MHz, SER/RESN, HC49S | 1 | Y1 | CITIZEN HC49US25.000MABJ |
| 23-0000-50 | XTAL, 50.0000 MHz, SER/RESN, HC49S | 1 | Y2 | CITIZEN HC49US50.000MABJ |

**Table 6. Bill of Materials for the eZ80F91 Module (Continued)**

| Part Number | Part Name | Quantity | Jumper Location | Manufacturer |
|---|---|---|---|---|
| 23-0006-00 | Internal crystal, 32.768 kHz, SER/RESN, TF case | 1 | Y3 | Fox NC-38 |
| 21-0907-01 | Connector, RJ45, Fast jack,10/100 Base-T | 1 | P2 | Halo Electronics HFJ11-2450E-L11 |
| 21-0055-02 | Connector, HDR/PIN, .025SQ, double row | 2 | JP1, JP2 (backside) | Harwin M-20-976-3622 |

# Schematics

Figure 8 through Figure 10 describes the layout of the eZ80F91 Module. Ethernet circuiting devices are not loaded on the eZ80F91 Module. However, these devices appear in the following schematics for reference.
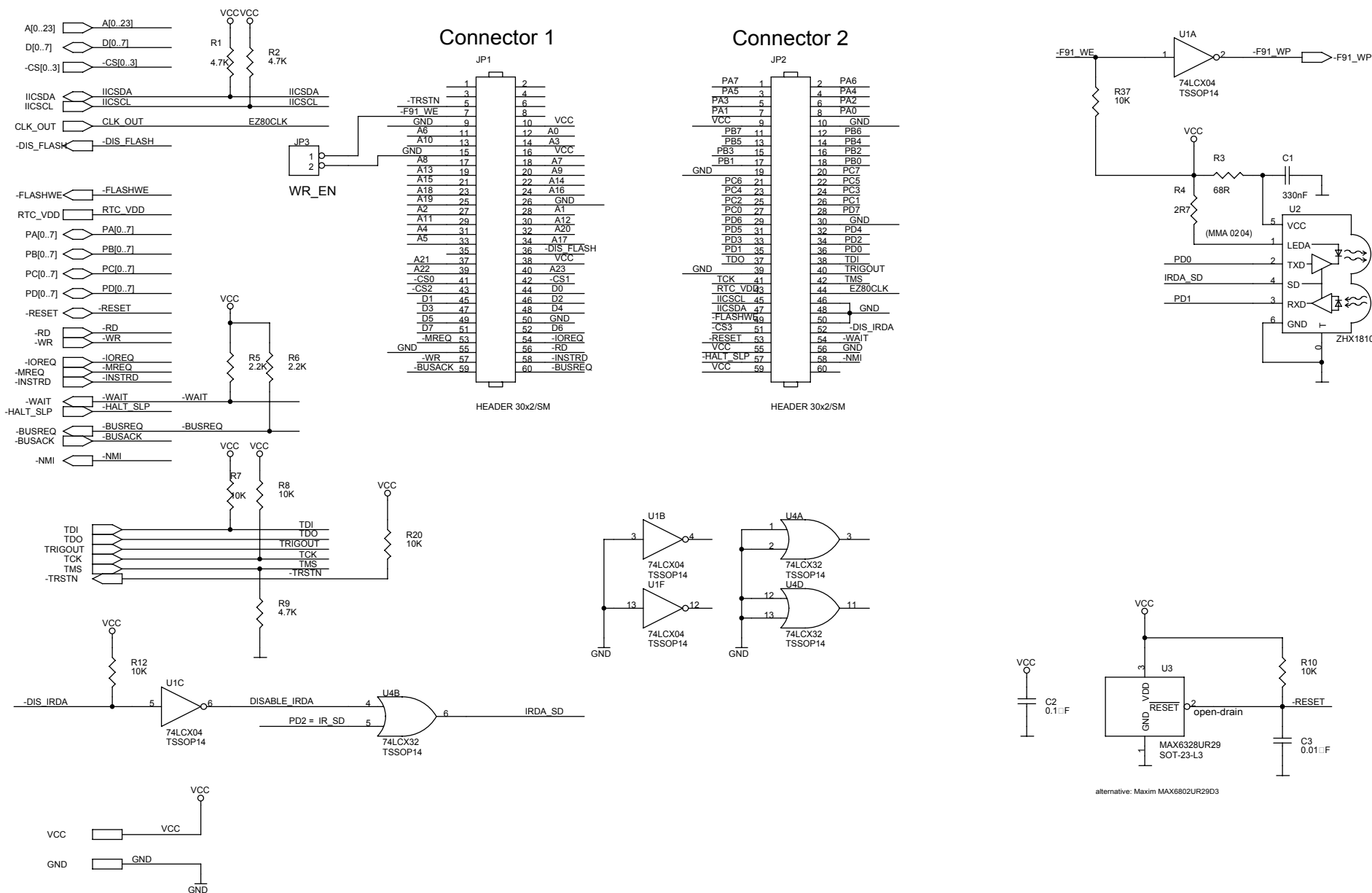


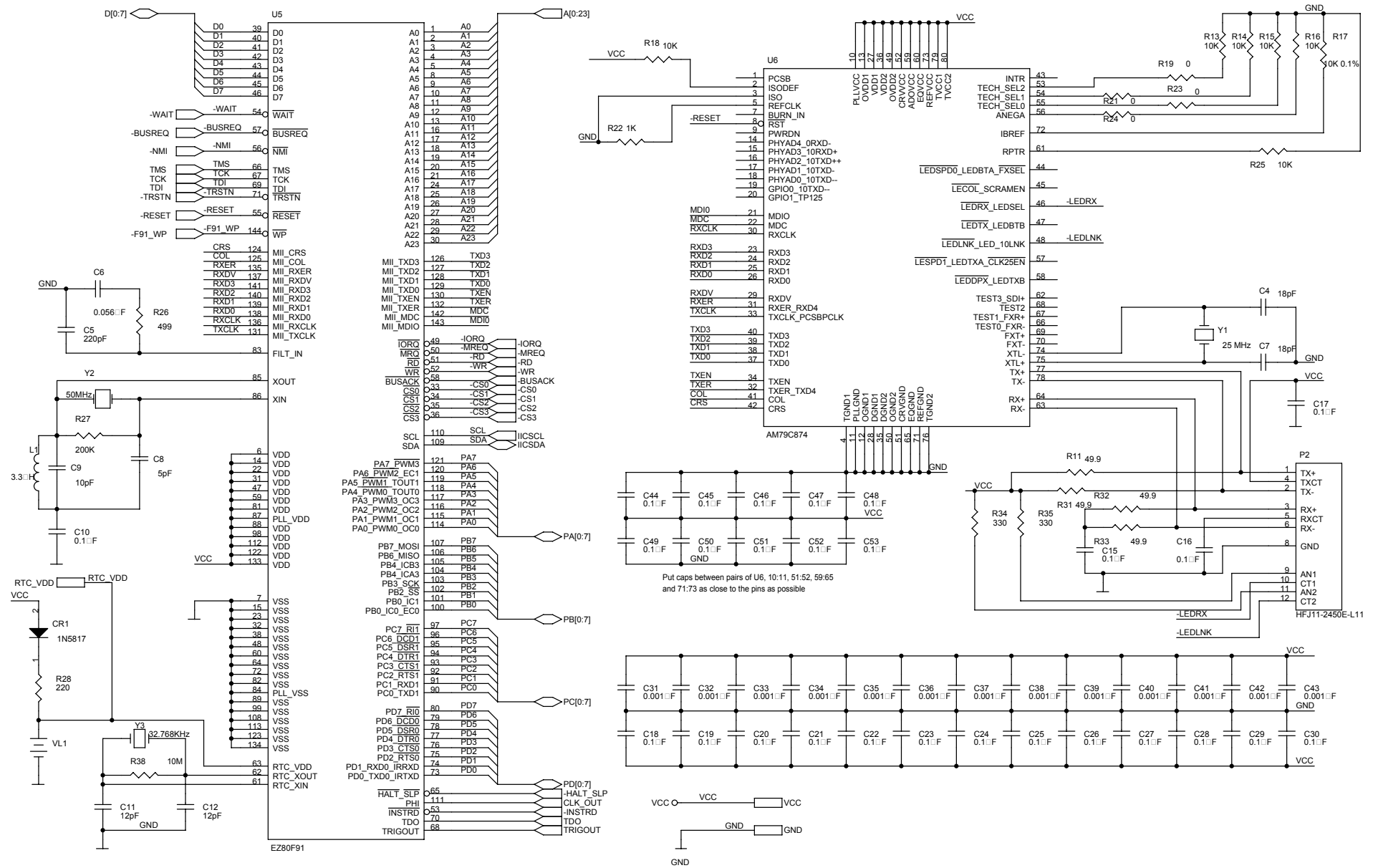**Figure 8. eZ80F91 Module Schematic Diagram—Connectors and Miscellaneous**

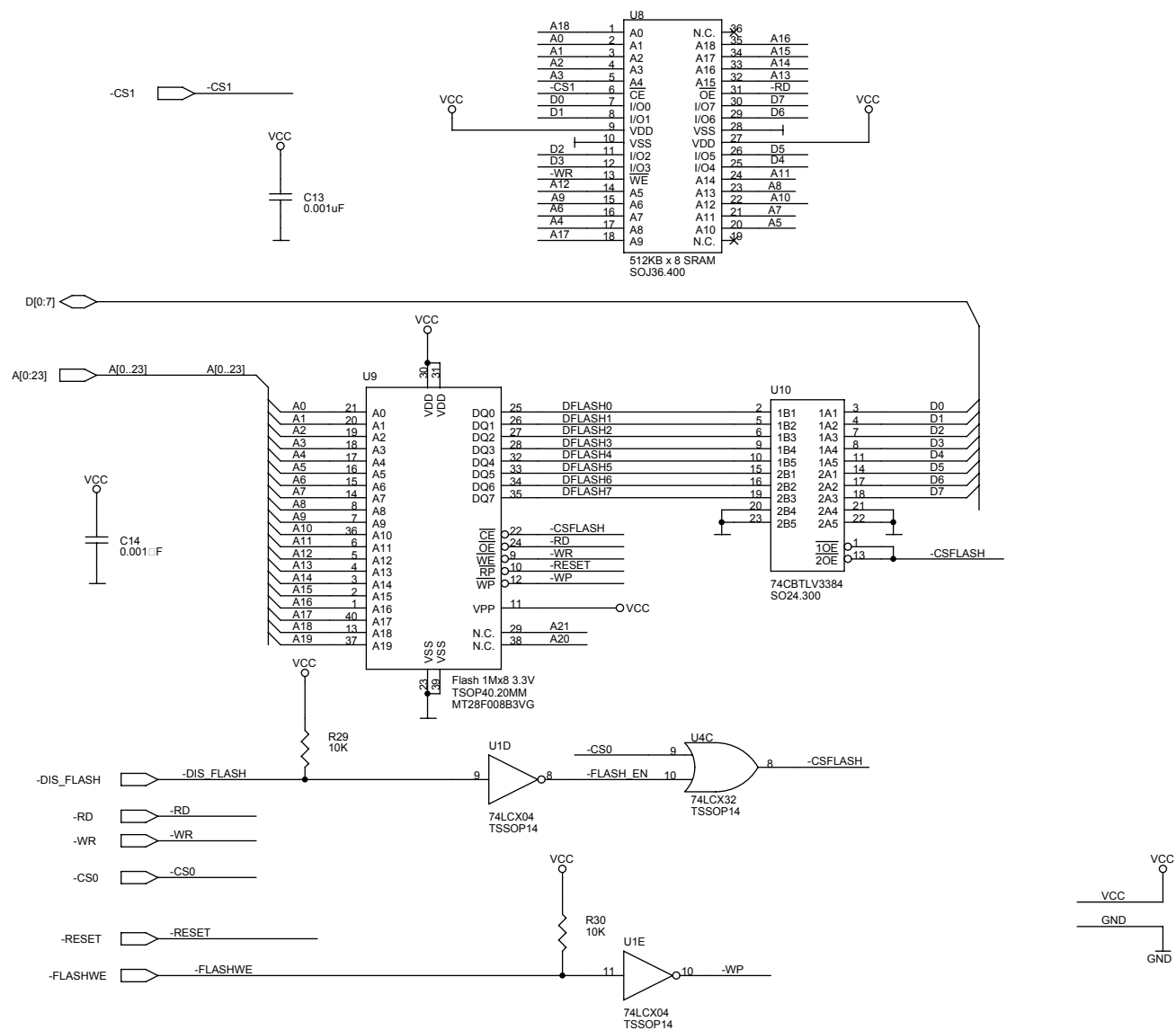Figure 9.  eZ80F91 Module Schematic Diagram—CPU and PHY

**Figure 10. eZ80F91 Module Schematic Diagram—Module Memory**

# Customer Support

For answers to technical questions about the product, documentation, or any other issues with Zilog's offerings, please visit Zilog's Knowledge Base at http://www.zilog.com/kb.

For any comments, detail technical questions, or reporting problems, please visit Zilog's Technical Support at http://support.zilog.com.