phys. stat. sol. (a) **95**, 283 (1986)

Subject classification: 71.55; 73.40; S5.11

Institute of Semiconductors, Academy of Sciences of the Ukrainian SSSR, Kiev[1])

Isothermal DLTS Method Using Sampling Time Scanning

By

V. I. TURCHANIKOV, V. S. LYSENKO, and V. A. GUSEV

An isothermal DLTS (I-DLTS) method is proposed where the transient capacitance signal from the structure under study (MIS, p–n or Schottky diodes) is measured at two times, with the interval between them successively changing from cycle-to-cycle of the periodically repeated processes. Parameters of deep levels are determined from the time positions and amplitudes of the I-DLTS peaks recorded at several fixed temperatures. The I-DLTS method provides more accurate correlation between deep level parameters with measured temperature and is less time consuming.

Предложен метод изотермической DLTS (I-DLTS), в котором сигнал релаксации емкости исследуемой структуры (МДП, p–n и Шоттки диоды) измеряется для двух моментов времени при последовательном изменении интервала между ними от цикла к циклу периодически повторяющихся процессов релаксации. По временным положениям и амплитудам пиков сигнала I-DLTS, записанного при нескольких фиксированных температурах, определяют параметры глубоких уровней. Метод I-DLTS позволяет точно соотнести измеряемые параметры глубоких уровней с температурой и отличается экспрессностью измерений.

1. Introduction

The DLTS method has been widely applied in determining parameters of deep levels of semiconductor structures [1] due to its high sensitivity and the simplicity of the interpretation of measurement results.

However, conventional DLTS involves repeated and slow heating and cooling of the structure in a wide temperature range (from 77 to 400 K) which requires a long measurement time. Moreover, heating to high temperature may cause irreversible changes in the structure, e.g. an annealing of deep levels.

To date, the DLTS method has several modifications differing in experimental arrangement [2], processing of the transient signal [3], types of the measured parameters (charge or current) [4, 5]. These modifications widen the range of the DLTS potentialities.

The common feature of all the DLTS modifications consists in measuring a certain parameter of the structure (capacitance, charge, or current) at two fixed times t_1 and t_2 (two sampling times) during periodically repeated relaxation processes. From these measurements, a difference-averaged DLTS signal is formed. When the relation $(t_2 - t_1 = \tau \ln (t_2/t_1))$ between the rate window $(t_2 - t_1)$ and relaxation time constant τ is fulfilled the DLTS signal reaches its peak. The temperature position of the peak bears information on deep level parameters.

In isothermal DLTS [6, 7], the I-DLTS peak is achieved by automatic successive change of the time intervals $t_2 - t_1$ during the transient capacitance measurements at a fixed temperature.

[1]) Prospekt Nauki 115, 252650 Kiev-28, USSR.

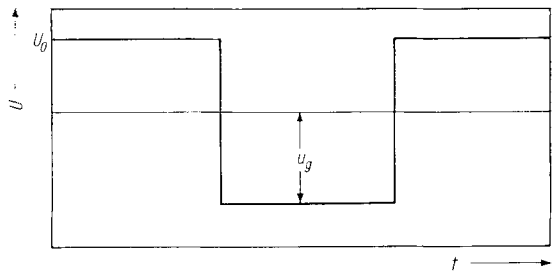

Fig. 1. The voltage in the MIS structure

2. The Main Principles of Measurements

We consider the principles of the isothermal DLTS method on an example of the determination of the parameters of an acceptor-type electron trap in the subsurface region of an n-type semiconductor of a MIS structure. The consideration presented below may be extended to other semiconductor structures with a surface barrier and to other types of deep levels.

The structure under study exists at a fixed temperature T. An accumulating constant bias U_0 is applied to the structure to fill the deep levels with energy position E_t and concentration N_t. The constant bias is superimposed by a periodic depleting pulse voltage to trigger the emission of the carriers captured on deep levels in the region $0 < z < w$ of the depletion layer, where w is the distance between the semiconductor surface and the intersection plane between the energy position of the deep level and that of the Fermi level (Fig. 1 and 2). In this region, the charge variation $\left(\Delta Q_t = \right.$ $\left. = qN_t w \exp\left(-t/\tau\right)\right)$ in the course of the carrier emission from the deep level brings about a transient capacitance of the depletion layer and, correspondingly, a transient of capacitance in the entire MIS structure, the relaxation time constant being $\tau =$ $= (\sigma\langle v\rangle N_c)^{-1} \exp(E_t/kT)$ (where σ is the capture cross-section of the deep level,

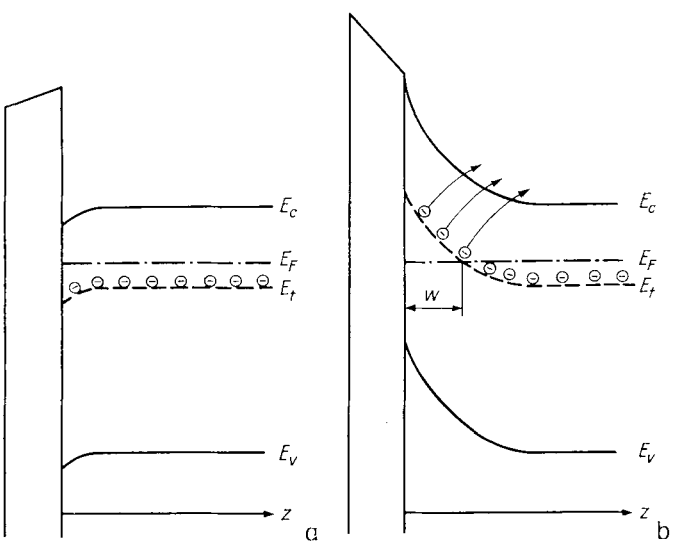

Fig. 2. Band diagram for the MIS structure: a) the deep level being filled with carriers; b) the captured carrier emission from the deep level

$\langle v \rangle$ the thermal velocity of the carriers, N_c the effective state density in the conduction band).

By choosing appropriate magnitudes of the constant bias and the amplitude of the pulse voltage one may achieve a selective filling and emission of carriers from the given deep level.

By presenting the MIS structure capacitance C as the equivalent capacitance of the series-connected capacitances of the dielectric and the depletion layer of the semiconductor one may find the following relation between the change in the charge on the metal electrode (ΔQ_g) and the change in the MIS structure capacitance and transient charge:

$$\Delta Q_g = U_g \, \Delta C = q N_t w \exp\left(-\frac{t}{\tau}\right). \tag{1}$$

From (1), it follows that the MIS structure capacitance variation measured from the instance of the depleting voltage pulse application is

$$C(0) - C(t) = \frac{q N_t w}{V_g}\left[1 - \exp\left(-\frac{t}{\tau}\right)\right]. \tag{2}$$

The transient capacitance signal $C(t)$ repeated with a period equal to that of the applied pulse voltage is measured during the time span t_s ($t_s \ll \tau$) at t_1 and t_2 counted off from the onset of the capacitance transient. From repeatedly measured values of the transient capacitances $C(t_1) = \int_{t_1}^{t_1+t_s} C(t)\,\mathrm{d}t$ and $C(t_2) = \int_{t_2}^{t_2+t_s} C(t)\,\mathrm{d}t$ a difference signal is formed as

$$\Delta S(\tau) = C(t_1) - C(t_2) = q N_t \frac{w}{V_g} \tau (1 - \mathrm{e}^{-t_s/\tau})\,(\mathrm{e}^{-t_1/\tau} - \mathrm{e}^{-t_2/\tau}) \tag{3}$$

which is averaged over the cycle of the repeated relaxation processes to improve the signal-to-noise ratio.

In isothermal DLTS, the times of the transient capacitance t_1 and t_2 are changed automatically from cycle-to-cycle of the repeated relaxation processes in such a manner that the time interval between them (rate window) increases while their ratio remains constant ($t_2/t_1 = \text{const} = b$) (Fig. 3). The relations determing the time positions t_1 and t_2 about zero time $t = 0$ of the relaxation process in the m-th cycle ($m = 1, 2, \ldots, 250$) have the form

$$t_2^{(m)} - t_1^{(m)} = m t_i; \qquad \frac{t_2^{(m)}}{t_1^{(m)}} = b$$

or (4)

$$t_1^{(m)} = \frac{m}{b-1} t_i\,; \qquad t_2^{(m)} = \frac{mb}{b-1} t_i\,,$$

where t_i is the interval which serves as a factor by which the time positions $t_1^{(m)}$ and $t_2^{(m)}$ and the rate window are multiplied from cycle-to-cycle. Taking (4) into account, we may write the difference transient capacitance averaged over the m-th cycle at $t_s \ll \tau$ as

$$\Delta S^{(m)}(\tau) = q N_t \frac{w}{V_g} t_s \, \mathrm{e}^{-m t_i/(b-1)\tau} (1 - \mathrm{e}^{-m t_i/\tau})\,. \tag{5}$$

From the maximum condition for the function $\Delta S^{(m)}(\tau)$ it may be concluded that at a certain cycle a peak signal will be observed whose position in time t_m is related to

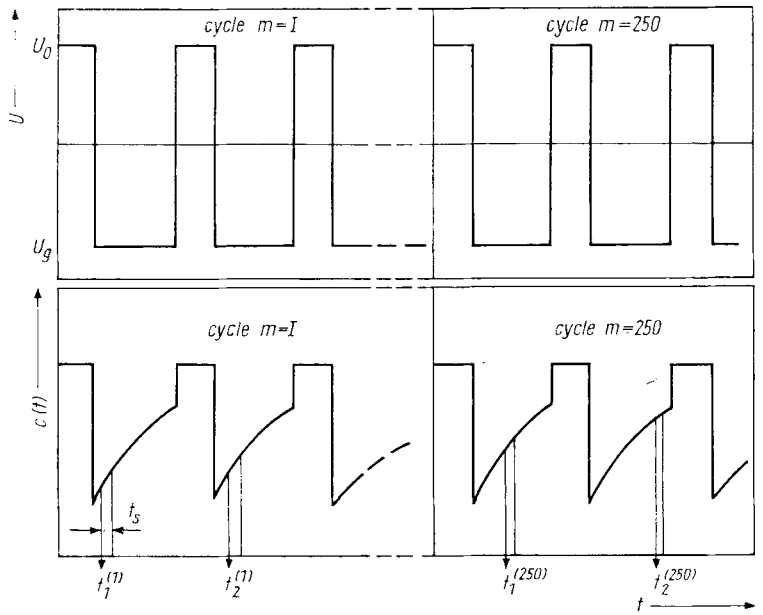

Fig. 3. Voltage applied to the structure studied and the transient capacitance measurement cycles for time instants t_1 and t_2 scanning from cycle to cycle: (1) cycle $m = 1$; (2) cycle $m = 250$

the relaxation constant τ characterizing the carrier emission from the deep level E_t,

$$t_{\tilde{m}} = \tilde{m}t_1 = \tau \ln b = (\sigma\langle v\rangle N_c)^{-1} e^{E_t/kT} \ln b . \quad (6)$$

If in the region of the space charge of the semiconductor there are deep levels with different energy positions, the I-DLTS signal $\Delta S^{(m)}(\tau)$ will consist of separate peaks each of which is related to a certain deep level. The time position of the $\Delta S^{\tilde{m}}(\tau)$ peak depends on the energy position of the level and the fixed temperature of measurements, while the peak magnitude depends on the deep-level concentration and depth of the region w,

$$\Delta S^{(\tilde{m})}(\tau) = qN_t \frac{w}{V_g} t_s \frac{b-1}{b} e^{-\ln b/b-1} . \quad (7)$$

From (7) and (5), one may obtain the peak width which, at the half-maximum value, with $b = 2$, equals

$$\Delta t_{1/2} = 1.76\tau . \quad (8)$$

From (8), it is obvious that a deeper level will be represented by a wider peak whose position is shifted towards greater times.

An increase in measurement temperature would lead to a narrowing of the peak and its displacement towards smaller time.

3. I-DLTS Parameters of a Deep Level

a) The type of the deep level and that of the carriers captured on this level define the sign and form of the transient capacitance of MIS structure which, in turn, governs the polarity of the I-DLTS signal. From the latter, the type of deep levels may be identified (electron or hole trap).

b) The relaxation constant time τ for emission from the given deep level is determined from the time position of the relevant I-DLTS peak according to (6).

c) The energy position of the deep level can be determined from several runs (two at minimum) of measurements at various fixed temperatures T_i. The energy position of a given level is determined from the slope of the dependence of $\ln t_{\tilde{m}} T_i^2$ on reciprocal temperature. The factor $\sigma\langle v\rangle N_c$ is supposed to have a square-law dependence on temperature.

Consistent with (5), for two runs of isothermal measurements of transient capacitance at temperatures T_1 and T_2 one may derive the following analytical expression for determining the energy position of the deep level:

$$E_t = \frac{kT_1T_2}{T_2 - T_1} \ln \frac{t_{\tilde{m}1} T_1^2}{t_{\tilde{m}2} T_2^2} . \tag{9}$$

d) The deep-level concentration is determined from the value of the corresponding I-DLTS peak $\left(\Delta S^{(\tilde{m})}(\tau)\right)$ as follows from (6), under the assumption $t_i \ll \tau$ (which is always realizable in experiment),

$$N_t = \frac{b}{b-1} \frac{U_g'}{qwt_s} \Delta S^{(\tilde{m})}(\tau)\, e^{\ln b/b - 1} . \tag{10}$$

4. Experimental Device

Fig. 4 shows the block diagram of the device in which the proposed IDLTS method can be realized.

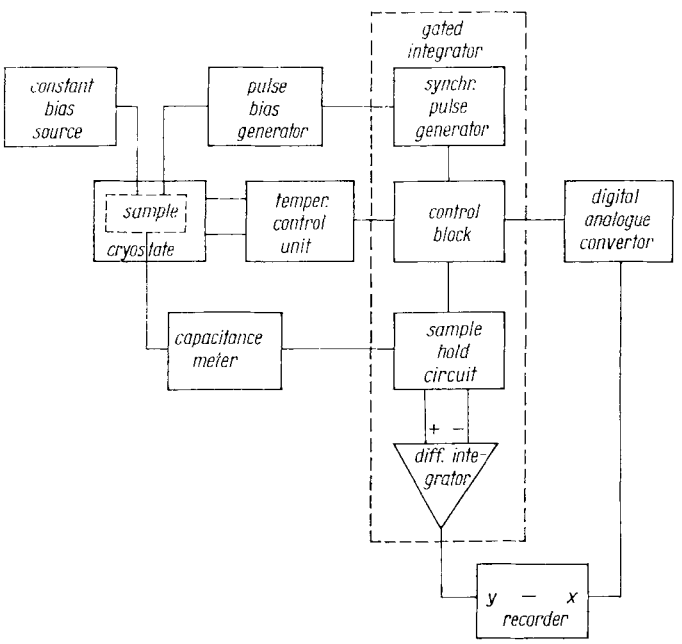

Fig. 4. Block diagram of the device: 1 cryostat; 2 temperature control unit; 3 control block; 4 constant bias source; 5 pulse bias generator; 6 synchronous pulse generator; 7 capacitancemeter; 8 gated integrator; 9 differential integrator, 10 inputs of the two-coordinate recorder; 11 digital-to-analogue converter

The structure to be studied is placed into the cryostat. The temperature regime of transient capacitance measurements is maintained by the temperature control block that is connected with the control block of the gate generator.

The device works as follows. From the constant bias source, the accumulating voltage is fed to the structure to fill deep levels with carriers. At the arrival of the synchronizing pulse from the generator at $t = 0$, the pulse generator feeds a depleting pulse to the structure, and the process of the capacitance relaxation towards equilibrium sets in due to the emission of the previously captured carriers from deep levels. The capacitancemeter provides continuous measurements of transient capacitance, and the corresponding transient capacitance signal is fed to the input of the sample and circuit of the gated integrator. The sample and hold circuit record the transient capacitance signal at the times t_1 and t_2 counted off always from the beginning of the relaxation process. The time instants t_1 and t_2 for the transient capacitance sampling, as well as the sampling duration $t_s = 10$ μs, are given by the gate pulses formed in the control block of the gated generator. Transient capacitance records at t_1 and t_2 are obtained for two relaxation processes following each other, respectively, i.e. in the periods when two adjacent pulses of the depleting voltage operate (Fig. 3). From the output of the sample and hold circuit, the recorded capacitances $C(t_1)$ and $C(t_2)$ are fed to the uninverted and inverted inputs of differential integrator where the capacitance measurements $C(t_1)$ and $C(t_2)$ are integrated and averaged over 50 periods of the applied pulse voltage making a cycle of repeated transient capacitance measurements to form an averaged difference signal.

During the first operation cycle of the device, the sampling times t_1 and t_2 differ from the initial instant of the relaxation processes by the time interval $t_i = 10$ μs. This is the duration of a gate pulse as well as a sampling. In every following cycle, the sampling instant t_1 is displaced by the time interval t_i, while t_2 is displaced by $2t_i(t_2/t_1 = b = 2)$. Within the cycle of the repeated capacitance transient processes which lasts 1 s the sampling times $t_1^{(m)}$ and $t_2^{(m)}$ are fixed with a high accuracy. The total number of cycles realized in a measurement succession at a given fixed temperature is 250, the interval between the sampling times $t_2^{(m)} - t_1^{(m)}$ (the rate window) scanning automatically from 10 μs in the first cycle to 2500 μs in the last (250th) one.

The averaged difference signal formed at each cycle is fed from the differential integrator output to the input "y" of a two-coordinate recorder, while the input "x" of the latter is fed by a voltage proportional to the interval $t_2^{(m)} - t_1^{(m)}$ from the digital-to-analogue converter. With this, the recorder gives a time-averaged difference signal at one fixed measurement temperature of the gated integrator to the temperature control block, then the system is automatically switched to the next fixed temperature, and the whole process is repeated as described above.

The device provides the possibility to conduct the measurement using the conventional method [1]. For this purpose, we fix the sampling instants t_1 and t_2, and the structure is heated uniformly.

5. Experimental Results

Using I-DLTS and conventional DLTS, we have investigated the effect of rf annealing on MNOS structures formed on p-type silicon wafers ($\varrho = 7.5$ Ω cm) with two layers — the thermally grown oxide SiO_2 ($d_1 = 520$ nm) and low-temperature silicon nitride ($d_2 = 400$ nm). The samples in the form of varactors with an Al gate were subject to rf annealing in an atmosphere of residual gases at $p = 2 \times 10^{-2}$ Torr for 15 min.

Fig. 5 a shows a record of the output conventional DLTS signal against temperature for different fixed sampling times. Fig. 5 b shows the ouput I-DLTS signal against time

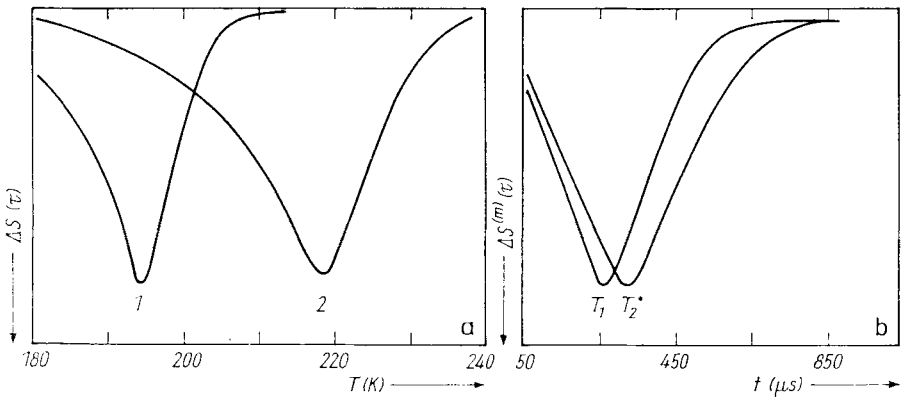

Fig. 5. a) Output DLTS signal corresponding to the deep level of energy $E_v = 0.22$ eV recorded at different sampling times t_1 and t_2: (1) $t_1 = 1000$ μs, $t_2 = 2000$ μs; (2) $t_1 = 250$ μs, $t_2 = 500$ μs. b) Output I-DLTS signal corresponding to the deep level $E_v + 0.22$ eV recorded at different fixed temperatures: $T_1 = 218$ K, $T_2 = 213$ K

for several fixed temperatures. The peaks of these signals correspond to the transien capacitance due to carrier emission from the deep level $E_v + 0.22$ eV. Apart from this level, the rf annealing leads to the formation of the energy level $E_v + 0.06$ eV.

6. Conclusions

From (9), it follows that the accuracy of the determination of the deep-level position depends on the accuracy of the determination of the time positions of the I-DLTS peaks $\Delta S^{\tilde{m}}(\tau)$ and on the accuracy with which the fixed temperature is maintained in the course of isothermal relaxations of the structure capacitance. In the method proposed, the measurement of the peak position in time has an error not more than $t_i/t^{(\tilde{m})}$ ($t_i \ll t^{(\tilde{m})}$). Under the conditions of a steady thermal regime, temperature stabilization is achieved with the help of the temperature control device within an error of 0.1 K. This provides a high accuracy in determining the energy position of a deep level.

Acknowledgement

The authors express their thanks to I. B. Puzin for useful comments.

References

[1] D. Lang, J. appl. Phys. **45**, 3023 (1974).
[2] D. May, M. Tsai, B. Steetman, and D. Lang, J. appl. Phys. **50**, 5093 (1979).
[3] A. le Bloa, P. N. Favennec, and Y. Colin, phys. stat. sol. (a) **64**, 85 (1981).
[4] K. I. Kirov and K. B. Radev, phys. stat. sol. (a) **63**, 711 (1981).
[5] J. A. Borsuk and R. M. Swanson, IEEE Trans. Electron Devices **27**, 2217 (1980).
[6] V. I. Turchaninov, V. S. Lysenko, and V. A. Gusev, Inventors Certificate N1101088 "Otkrytia i izobretenya" Bulletin (USSR), No. 8, 1985 (p. 199).
[7] C. H. Henry, J. appl. Phys. **57**, 628 (1985).

(Received November 26, 1985)