# Alenkruth Krishnan Murali

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## EDUCATION

**Ph.D. in Computer Engineering** GPA: 4.0/4.0 | August 2022 - Present
University of Virginia, Charlottesville, VA
Advisor: Dr. Ashish Venkat
Milestones: Completed Qualifying Exam in Spring 2023

**B.Eng. in Electrical and Electronics Engineering** June 2017 - May 2021
Anna University, Chennai, India GPA: 9.02/10
Capstone Project: Optimized Execution Unit for RISC-V Packed SIMD Extension

## RESEARCH INTERESTS

Computer Architecture, Hardware Security, Hardware Accelerators, and RTL Design.

## PUBLICATIONS

Ceviche: Capability-Enhanced Secure Virtualization of Caches link | pdf
A. Kalita, Y. Yang, **A. Krishnan Murali**, and A. Venkat,
in 2025 IEEE Symposium on Security and Privacy (S&P).

## EXPERIENCE

*Graduate Research Assistant* University of Virginia | August 2022 - Present
Advisor: Dr. Ashish Venkat

- Building a reconfigurable RISC-V processor to deploy and test novel security verification techniques.
- Exploring fuzzing based approaches for hardware security, microarchitectural optimizations, and software optimizations.

*Graduate Research Intern* Intel Corporation, India | May 2024 - December 2024
Manager(s): Anant Nori and Sreenivas Subramoney

- Worked on a profile-guided branch correction/prediction technique targeting data-dependent hard-to-predict (h2p) branches.

*CPU Verification Engineer* Incore Semiconductors, India | June 2021 - May 2022
Manager: Dr. Neel Gala

- Built a framework to automatically generate assembly tests to functionally verify in-house RISC-V core generators.

*RTL Design Intern* Incore Semiconductors, India | January 2021 - May 2021
Manager: Dr. Neel Gala

- Designed an optimized Packed SIMD unit to be integrated as a functional unit or as a co-processor to in-house RISC-V cores.

*Research Intern* IIT Palakkad, India | May 2020 - August 2020
Manager: Dr. Satyajit Das (Now at IIT Guwahati)

- Worked on extending RISC-V ISA with cryptography specific instructions, and built and integrated a power and area optimized AES-256 unit in the pipeline of the CV32E40P core.

## TECHNICAL SKILLS

*Programming Languages:* C++, Python, C, RISC-V Assembly.
*Hardware Description Languages & Tools:* Verilog, Chisel, System Verilog, Bluespec System Verilog, Xilinx Vitis/Vivado, Openlane, Synopsys DC, QuestaSim.

**TALKS AND PRESENTATIONS**

*CoreFuzzing* SRC Techcon 2023, Austin, TX | September 2023
Presented an initial version of CoreFuzzing at Semiconductor Research Corporation's Annual Technical Conference.

*Functional Verification of Chromite using UATG and RiVer Core* | Fall 2021
Incore Semiconductors & PES University | An introductory talk on using our framework to find functional bugs in RISC-V cores.

*Embedded System Design Using TI-MSP432 Boards* | February 2020
PSGiTech, India | Presented an introductory talk about the features and capabilities of the board and discussed the trade-offs involved in embedded systems design.

**RESEARCH PROJECTS**

*CoreFuzzing*

- Building a reconfigurable superscalar, out-of-order RISC-V core based on the BOOM core to deploy and test security verification techniques.
- Implementing Dynamic Information Flow Tracking in the reconfigurable core.
- Using Fuzzing to test target software on a intelligently selected microarchitectural configurations.

*Profile guided branch prediction/correction* | Research done at Intel

- Built a dataflow-based profiler to identify data sources, their values, and sinks (data dependent h2p branches).
- Implemented branch correction on a cycle-accurate simulator that uses the profiles generated by the profiler.

**TEACHING**

*Computer System Organization I* | Spring 2024 & 2025
Taught by Dr. Daniel Graham

- Built a simple compiler using lex, yacc to compile a C like high-level language to x86 assembly. Currently used as an assignment in the course.
- Manage a TA team of approximately 40 undergraduate students.
- Maintain course website, grade exams, set up autograders, and address student concerns on Piazza/ticketing system.

*Graduate Computer Architecture* | Fall 2023
Taught by Dr. Adwait Jog

- Create and grade quizzes, assignments, and final exams.

*Functional Verification of Chromite using UATG and RiVer Core* | Fall 2021
Taught at PES University with Incore Semiconductors - Lab Course

- Teach senior undergraduates the microarchitecture of a 5-stage RISC-V core and a 2-stage RISC-V core.
- Help students identify functional bugs in the design.
- Grade assignments and final presentations.

**SERVICE**

*Steering Committee Member* | November 2022 - Present
Computer Architecture Student Association (CASA)

- Organized a Mental Health Workshop in September 2024.

*Artifact Evaluation Committees* | ISCA '25, '24; HPCA '24; CCS '24; Eurosys '25
*Chairman - EEE Association* PSGiTech | September 2020 - August 2021

**MENTORING**

Alexander Schaefer on CoreFuzzing | Now Ph.D at Penn | Spring 2024 - Spring 2025.

**HONORS AND AWARDS**

Ranked 15 out of 9542 students in the state | 2022
Best Outgoing Student - Awarded for all-round excellence | 2022

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**References available upon request**