PLC Stamp 1200 micro Datasheet

I2SE GmbH

January 15, 2018

Contents

Revisions

Revision	Release Date	Changes
5	January 15, 2018	added footprint measures, updated address
4	June 28, 2017	added section GPIO test feature
3	March 22, 2017	corrected size in section ”Abstract”
2	March 09, 2017	corrected GPIO pinout (incorrectly mentioned GPIO5, which is not existent)
1	February 15, 2017	initial release

1 Abstract

The PLC (PowerLine Communication) module gives your application access to Gigabit powerline communication based on the HomePlug® AV2 compliant MAC/PHY Transceiver QCA7500. You can realize point-to-point and multi-point connections depending on your application. The data will be transmitted as Ethernet packets over the power line. This gives you the opportunity to use TCP/IP or whatever network protocols you wish to use.
The galvanic isolation from the power line as well as the power supply is left to you so that you can design it right for you application.
The QCA7500 from Qualcomm Atheros guarantees the compatibility with many other commercial powerline devices.

Parameter	Value
External Power supply	3.3 V @ 1000 mA (peak) / 760 mA (average)
Power consumption	idle: 1750 mW / rx active: 2200 mW / tx active: 2500 mW
Data rate powerline	max. 1200 MBit/s
Data rate R(G)MII	max. 1000 MBit/s
Reach	max. 300 m over the Powerline
Temperature range	Consumer (see technical data)
Outline dimension	43.7 mm x 36.2 mm x 3.8 mm
Weight	7.5 g
RoHS	PLC Stamp 1200 micro is manufactured RoHS compliant

2 Applications

- interconnection of household appliances to the Smart Grid
- connecting smart meters to Smart Meter Gateways and/or LAN/WAN/Wifi
- connecting sensors
- connecting photovoltaics
- connecting heating and air conditioning
- coupling of machines and measurement devices
- forwarding of digital Signals (remote I/O)
- coupling of RF-cells for home automation
- interconnection of media streaming appliances

3 Interfaces

Powerline: MIMO 230 V AC, 110 V AC, DC, dead-wire 2-wire-connections, dead wire 3-wire-connections
Ethernet: RGMII, RGMII MDIO

4 Handling

This electronic component is sensitive to electrostatic discharge (ESD).
The module contains components with **moisture sensitivity level (MSL) 3**. Please handle them accordingly.

5 Module overview

The block diagram in Figure 1 shows the components on the module in the grey box as well as the connections and external components that you need additionally.

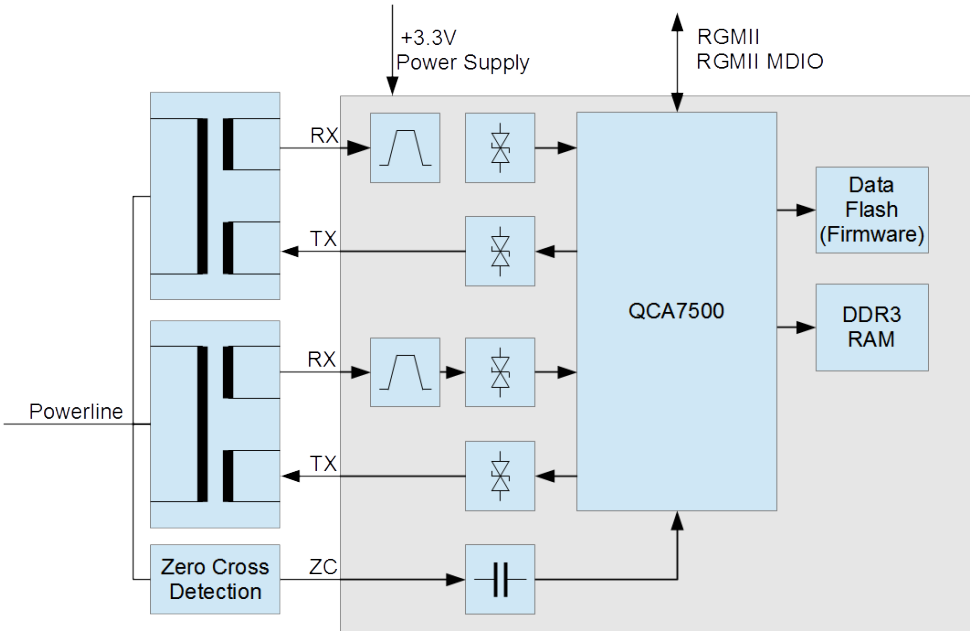


Figure 1: Block diagram of PLC Stamp 1200 micro

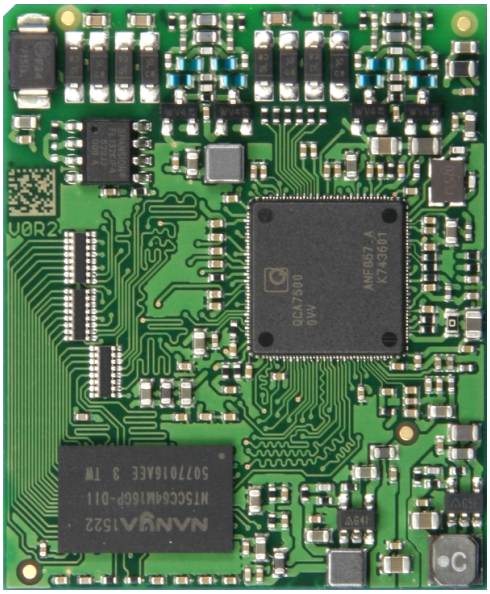


Figure 2: Top View of PLC Stamp 1200 micro

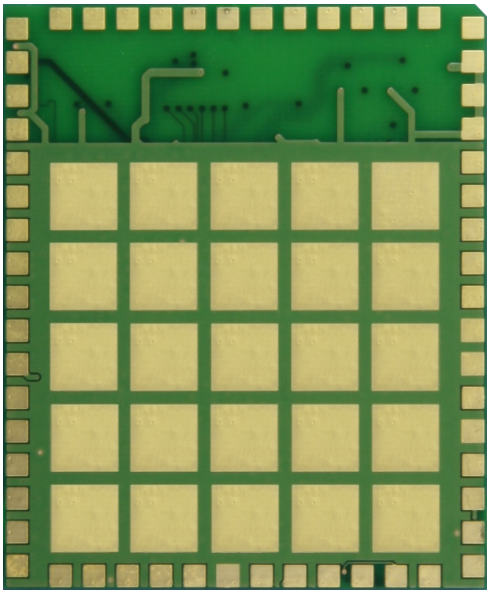


Figure 3: Bottom View of PLC Stamp 1200 micro

6 Technical Data

6.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	Min.	Max.	UNIT
VDD	Digtal supply voltage	-0.3	3.46	V
VDIO	Digtal input voltage	-0.3	3.6	V
VDDA	Analog input voltage	-0.3	3.6	V
TSTORE	Storage temperature	-40	150	°C

6.2 Operating conditions

SYMBOL	PARAMETER	Min.	Typ.	Max.	UNIT
VDD	Digtal supply voltage	3.13	3.3	3.46	V
TCASE	Top of QCA7500 case temperature	*	-	110	°C
I_GPIO	GPIO current	-	-	12	mA

* No specification for the minimum operating temperature of the QCA7500 is available, all other components are selected for down to -40 °C.

7 Firmware and MAC Addresses

These modules are pre-programmed with firmware and parameter information block (PIB). The PIB contains the MAC addresses of the module as well as the prescaler values which are defining the transmission power on the power line frequencies. The MAC address uses a prefix (organizationally unique identifier) that is assigned to I2SE. The prescaler values that are set in the production process were defined by I2SE for the intended application.

8 Pin Description

Direction Nomenclature	
NC	not connected pin
I	input
I-	negative input of differential signal
I+	positive input of differential signal
IO	input / output
O	output
O-	negative output of differential signal
O+	positive out put of differential signal
PI	power input
PO	power output

PIN#	Name	Direction	Description
1	-	NC	do not connect anything
2	GND		Ground connection
3	GND		Ground connection
4	GND		Ground connection
5	-		do not connect anything
6	-		do not connect anything
7	-		do not connect anything
8	-		do not connect anything
9	-		do not connect anything

10	GND		Ground connection
11	GND		Ground connection
12	-		do not connect anything
13	GND		Ground connection
14	GPIO_10	IO	General Purpose I/O 10
15	GPIO_9	IO	General Purpose I/O 9
16	GPIO_8	IO	General Purpose I/O 8
17	GPIO_7	IO	General Purpose I/O 7
18	GPIO_6	IO	General Purpose I/O 6
19	GPIO_4	IO	General Purpose I/O 4
20	GPIO_3	IO	General Purpose I/O 3
21	GPIO_2	IO	General Purpose I/O 2
22	GPIO_1	IO	General Purpose I/O 1
23	GPIO_0	IO	General Purpose I/O 0
24	GND		Ground connection
25	+3V3	PI	connect to 3.3V Supply
26	PHY_MDC	IO	MII Management Data Clock
27	PHY_MDIO	IO	MII Management Data
28	PHY_CLK	O	25 MHz Clock Out
29	PHY_RST_N	IO	Connect to PHY Chip reset pin (low active)
30	MRX_CTRL	I	Ethernet Receive Control
31	MRX_CLK	I	Ethernet Receive Clock
32	MRX_D0	I	Ethernet Receive Data
33	MRX_D1	I	Ethernet Receive Data
34	MRX_D2	I	Ethernet Receive Data
35	MRX_D3	I	Ethernet Receive Data
36	2P5V_LDO	PO	connect to DVDD25_33 if desired RGMII voltage domain is 2.5 V
37	DVDD33	PO	connect to DVDD25_33 if desired RGMII voltage domain is 3.3 V
38	RESET_N	I	QCA7500 reset (low active)
39	MTX_CTRL	O	Ethernet Transmit Control
40	MTX_CLK	O	Ethernet Transmit Clock
41	MTX_D0	O	Ethernet Transmit Data
42	MTX_D1	O	Ethernet Transmit Data
43	MTX_D2	O	Ethernet Transmit Data
44	MTX_D3	O	Ethernet Transmit Data
45	DVDD25_33	PI	connect either to 2P5V_LDO or DVDD33, use heavy traces and capacitors
46	-	NC	do not connect anything
47	ZC_INP	I	Zero Cross Detection
48	-	NC	do not connect anything
49	RX0-	I-	MIMO Differential input for MIMO Channel #0
50	RX0+	I+	MIMO Differential input for MIMO Channel #0
51	TX0-	O-	MIMO Differential output for MIMO Channel #0
52	TX0+	O+	MIMO Differential output for MIMO Channel #0
53	-	NC	do not connect anything
54	RX1-	I-	MIMO Differential input for MIMO Channel #1
55	RX1+	I+	MIMO Differential input for MIMO Channel #1
56	TX1-	O-	MIMO Differential output for MIMO Channel #1
57	TX1+	O+	MIMO Differential output for MIMO Channel #1
58	-	NC	do not connect anything
TH1...25	GND		Ground connection

8.1 Configuration Straps

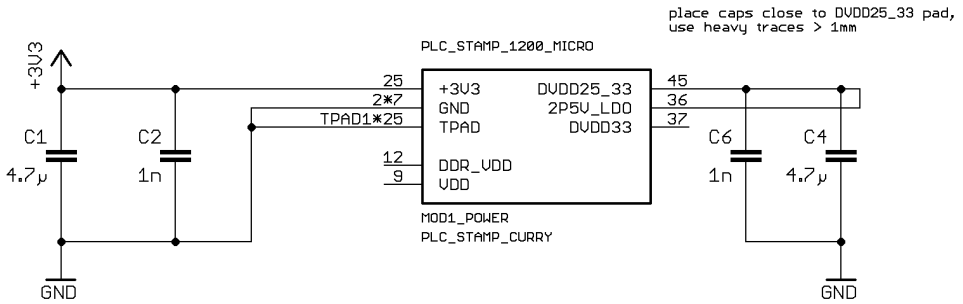
The QCA7500 has 15 pins with mapped strap options. The Table 8 shows how to configure the QCA7500 on boot time. If the opposite direction of the weak preselection is desired use a 10k Ohm pull up/down resistor.

Strap	Mapped Pin	Voltage Domain	Encoding	Weak Preselection	Note
BOOT_FROM_FLASH	GPIO0	3.3 V	1: Flash 0: Ethernet	1	
ETH_MAC_MODE	GPIO1	3.3 V	1: MAC mode 0: PHY mode	-	
ETH_RGMII	GPIO2	3.3 V	1: RGMII 0: RMII	1	
ETH_SPEED_SEL[1]	GPIO3	3.3 V	00: 10 Mbps 01: 100 Mbps 10: 1000 Mbps 11: Reserved	1	GPIO3 special purpose GPIO, is in conjunction with low power mode
ETH_SPEED_SEL[0]	GPIO4	3.3 V		0	
ETH_DUPLEX	PHY_RST_N	3.3 V	1: Full 0: Half	1	PHY mode only, when MAC mode provide pull down resistor and connect to PHY chip
ETH_SCAN_CFG	MTX_CTL	RGMII: 2.5/3.3V	1: Scan Configuration Enabled 0: Scan Configuration Disabled	1	MAC mode only
ETH_AUTO_NEG	MTX_CTL	RGMII: 2.5/3.3V	1: Auto Negotiation Enabled 0: Auto Negotiation Disabled	1	PHY mode only
ETH_ISOLATE	GPIO10	3.3 V	1: Isolate 0: Normal	0	
ETH_PHY_ADDR[4]	TXD3	RGMII: 2.5/3.3V	00: Addr = 00 01: Addr = 08 10: Addr = 16 11: Addr = 24	0	
ETH_PHY_ADDR[3]	TXD2	RGMII: 2.5/3.3V		1	
ETH_RMII_REF_CLK_IS_OUTPUT	TXD0	RGMII: 2.5/3.3V	1: Output 0: Input	0	RMII only
ETH_RGMII_DELAY_RX	TXD0	RGMII: 2.5/3.3V	1: 2 ns Delay 0: No Delay	0	RGMII only
ETH_RGMII_DELAY_TX	TXD1	RGMII: 2.5/3.3V	1: 2 ns Delay 0: No Delay	0	RGMII only
CFG_STRAP0	GPIO6	3.3 V	DDR3 = 0	0	
CFG_STRAP1	GPIO7	3.3 V	Reserved	0	
CFG_STRAP2	SPI_DI	3.3 V	Reserved	0	
CFG_STRAP3	PHY_CLK	3.3 V	Reserved	0	

Table 8: boot strap options

8.2 Power Management

The module is to be powered by an external 3.3 V supply. Bypass the voltage input with 1 nF and 4.7 μF.
Pins 2P5V_LDO and DVDD33 output 2.5 and 3.3 V. This voltage is only to be used for the module - you need to feed one of those voltages back into the module for selection of the voltage domain for the R(G)MII signals. Never use those to power any external circuitry. Feed one of the two voltages back into DVDD25_33 and add two bypass capacitors near DVDD25_33: 1 nF and 4.7μF.



8.3 GPIO

8.3.1 General Purpose I/O Functions

The QCA7500 uses the GPIO pins for boot time configuration. See Table 8 for more information.
The GPIOs of the QCA7500 have different functions after booting. They can either be used as input or output to display various states or trigger some actions. It is not possible to use these pins from your own application - only the QCA75000 firmware can control these GPIOs. The GPIOs are set up as noted in Table 10.

GPIO#	Direction	Function	Behavior
0	output	Power	1 / 0
1	input	Pairing, Randomisation, Factory Default	1 (1 s, 8 s, 13 s) / 0
2	output	Pairing	Pulse 500ms/500ms
4	input	GPIO test feature	1 / 0
6	output	PLC Link Status	1 / 0
7	output	PLC Activity	Pulse 60 ms / 60 ms
8	output	Ethernet Activity	Pulse 60 ms / 60 ms
9	output	Fast PLC Throughput	High 1, Mid 1, Low 0
10	output	Slow PLC Throughput	High 0, Mid 1, Low 1

Table 10:

Since the GPIO are also used as bootstrap pins special attention should be paid to the LED (Figure 4) and switch (Figure 5) connection according to the strap direction. Behaviour in Table 10 states a ’1’ for a pressed button or a lit LED, the electrical state (high/low) depends on the direction of the bootstrap resistor.

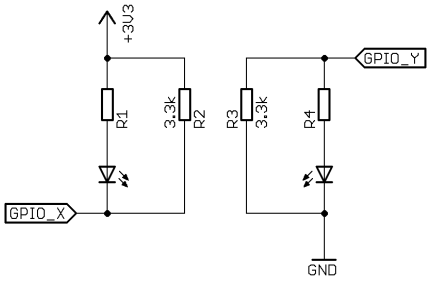


Figure 4: LED Connection

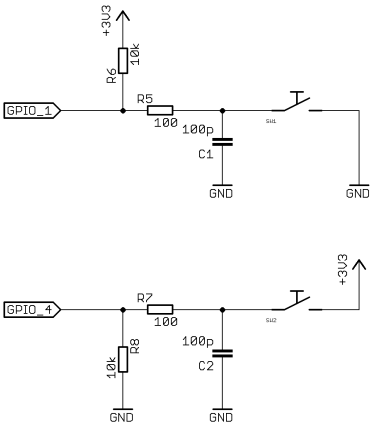


Figure 5: Switch Connection

8.3.2 GPIO test feature

This GPIO test feature is available on PLC Stamp 1200 micro with MAC higher than 00:01:87:0B:00:9C.
Once activated via input GPIO4 all outputs configured as output will pulse once with 500 ms ON and 500 ms OFF time at the same time.

8.4 RGMII / RGMII MDIO

If needed it is possible to add 2 ns clock delay to the RGMII clock signals according to the RGMII standard version 2.0 . See strap pins for instruction. The RGMII signals should be routed with a single ended trace impedance of 50 Ohm, as short as possible and with matched length within the specific groups.

8.5 MIMO Powerline

This module provides Multiple Input Multiple Output coupling to the power line with two channel.

- MIMO Channel 0 - Line-Neutral coupling
- MIMO Channel 1 - Line-Ground coupling

Surge protection for the TX path and a RX bandpass for the Homeplug AV2 specific frequencys are implemented onto this module. Please refer to the I2SE reference design for the external needs of the coupling circuit.

8.6 MAC / PHY mode

The gigabit powerline chip QCA7500 supports two different modes. The MAC and the PHY mode.
In PHY mode the QCA7500 acts like a PHY and has to be controlled by an external MAC controller e.g. processor with RMII interface.
In MAC mode the QCA7500 acts like a MAC controller and should be connected to an ethernet PHY.
The mode is selected via strap option.
Both modes can work in RGMII and in RMII mode which differs in the duplex modes (Table 12) and the R(G)MII-voltage domain - RGMII = 2.5V, RMII = 3.3V .

Mode	10HD	10FD	100HD	100FD	1000HD	1000FD
MAC RMII	+	+	+	+	-	-
PHY RMII	+	+	+	+	-	-
MAC RGMII	+	+	+	+	-	+
PHY RGMII	-	+	-	+	-	+

Table 12: MAC/PHY mode available duplex

9 Getting started

An easy way to put PLC Stamp 1200 micro into operation is to use it with the evaluation kit that is offered by I2SE. Please contact your distributor about it.
For your own design please have a look at the reference design documentation. I2SE provides you with all non standard parts that you will need to put that design into your own application. See section ,,Available Accessories" for further references to these parts.

10 Processing

- Process the modules according to IPC/JEDEC J–STD-020 and J-STD-033 guidelines.
- Limit repeated reflow processes to maximum 2.

10.1 Recommended Land Pattern

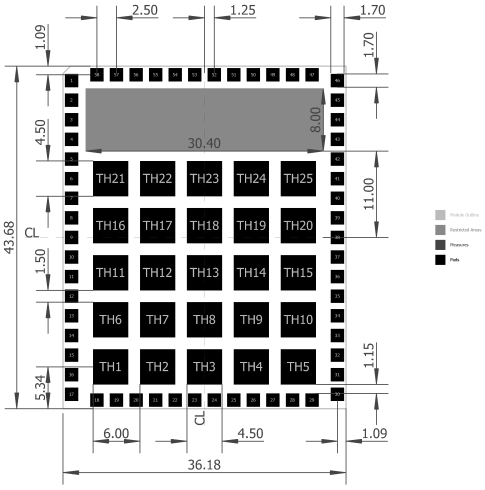


Figure 6: Recommended Land Pattern, all measures in mm

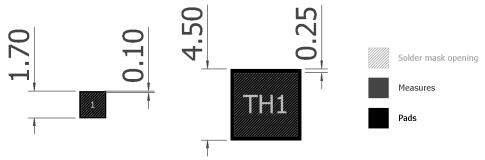


Figure 7: Recommended Solder mask opening, all measures in mm

11 Order Information

The following table gives you an overview about the available variants of PLC Stamp 1200 micro. The column identification gives you a guideline to identify each variant.

Order code	Temperature Range / °C	Parameter Optimization	availability
I2PLCCMC-CXL-001	Consumer	EN50561 ready	standard

Table 14: Order Codes

Product Family Code	Chip		Temperature Range		Parameter Optimization	Version
I2PLC	C: QCA7500	MC-	C: Consumer	X	L: EN50561 ready	-001

Table 16: Order Code construction

11.1 Available accessories

I2SE provides you with tested powerline transformers. These are part of the reference designs. Please see further documentation for a full specification of these transformers.

Description	I2SE Order Code
1:4:3 for mains power line coupling (UMEC UT11361)	I2PLCTR-4

12 How to reach us

Home Page: http://www.i2se.com

I2SE GmbH
Friedrich-List-Platz 2
04103 Leipzig
Germany