Integrated Systems Architectures

Design of a RISC-V-lite processor Assignment

1 Assignment

The output of this lab is the following:

1. Design in VHDL the RISC-V-lite processor. **Note:** do not include the memories in the design, put them in the test-bench instead;
2. Verify the correct behaviour of the processor by running the assembly program, which is available on "Portale della didattica" (minv-rv.s).
3. Synthesize the VHDL and verify that the netlist still behaves as your RTL description.
   When launching the `elaborate` command, log the output on a file and check **all** the messages.
   In particular, check that all the memory elements are flip-flops.
   If you have one or more latches, modify your RTL.
4. Modify the processor by adding a new instruction and a *special function unit* to compute the absolute value. Modify the asm to accomodate the new instruction.
5. Verify the correct behaviour of the new processor by running the modified assembly program.
6. Synthesize the VHDL and verify that the netlist still behaves as your RTL description.
7. Place and route both designs and verify that the two netlists still behave as the RTL descriptions.