# 1. Description

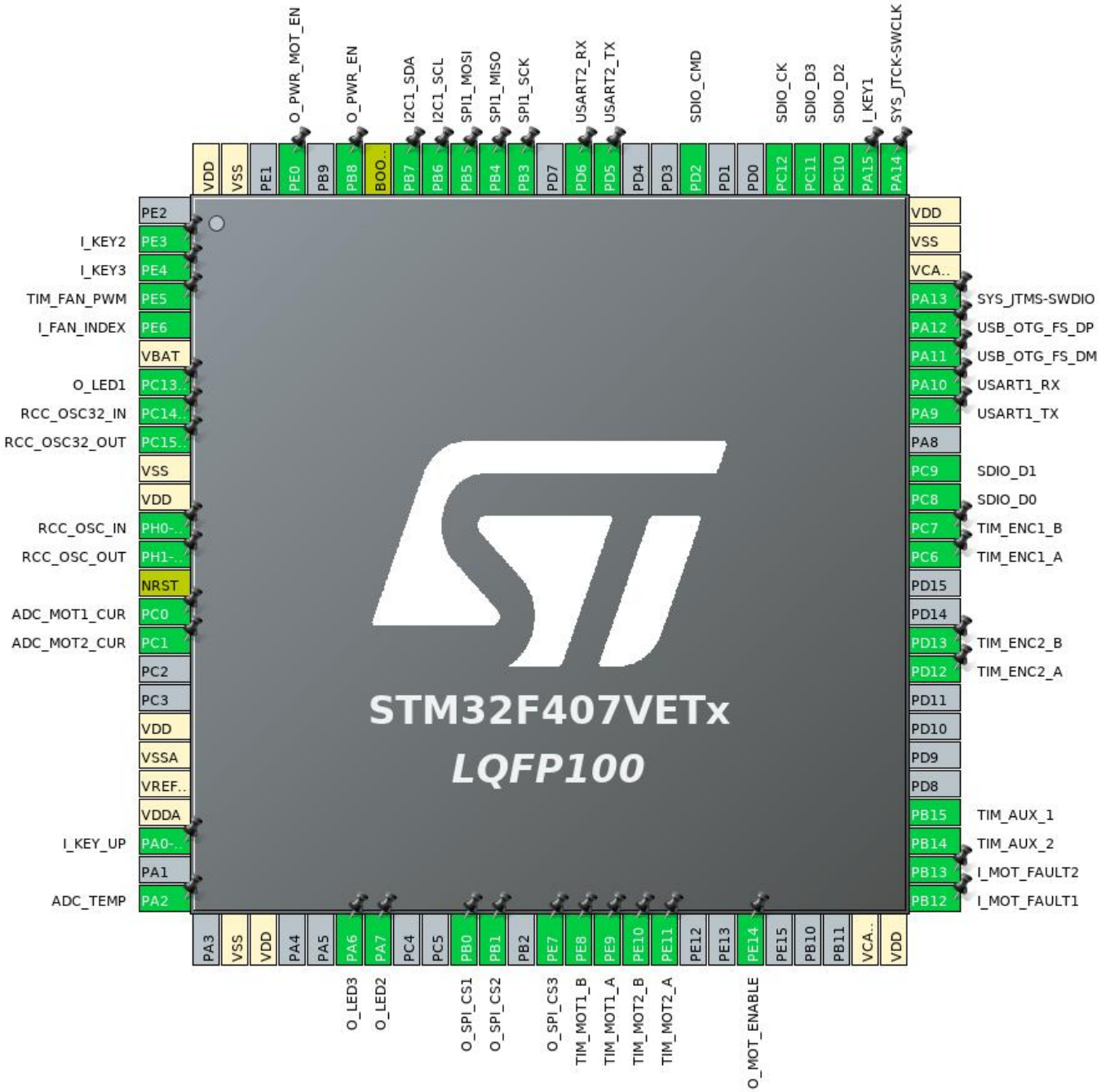
## 1.1. Project

| | |
|---|---|
| Project Name | UNAVng_fw |
| Board Name | custom |
| Generated with: | STM32CubeMX 5.4.0 |
| Date | 12/21/2019 |

## 1.2. MCU

| | |
|---|---|
| MCU Series | STM32F4 |
| MCU Line | STM32F407/417 |
| MCU name | STM32F407VETx |
| MCU Package | LQFP100 |
| MCU Pin number | 100 |

## 2. Pinout Configuration



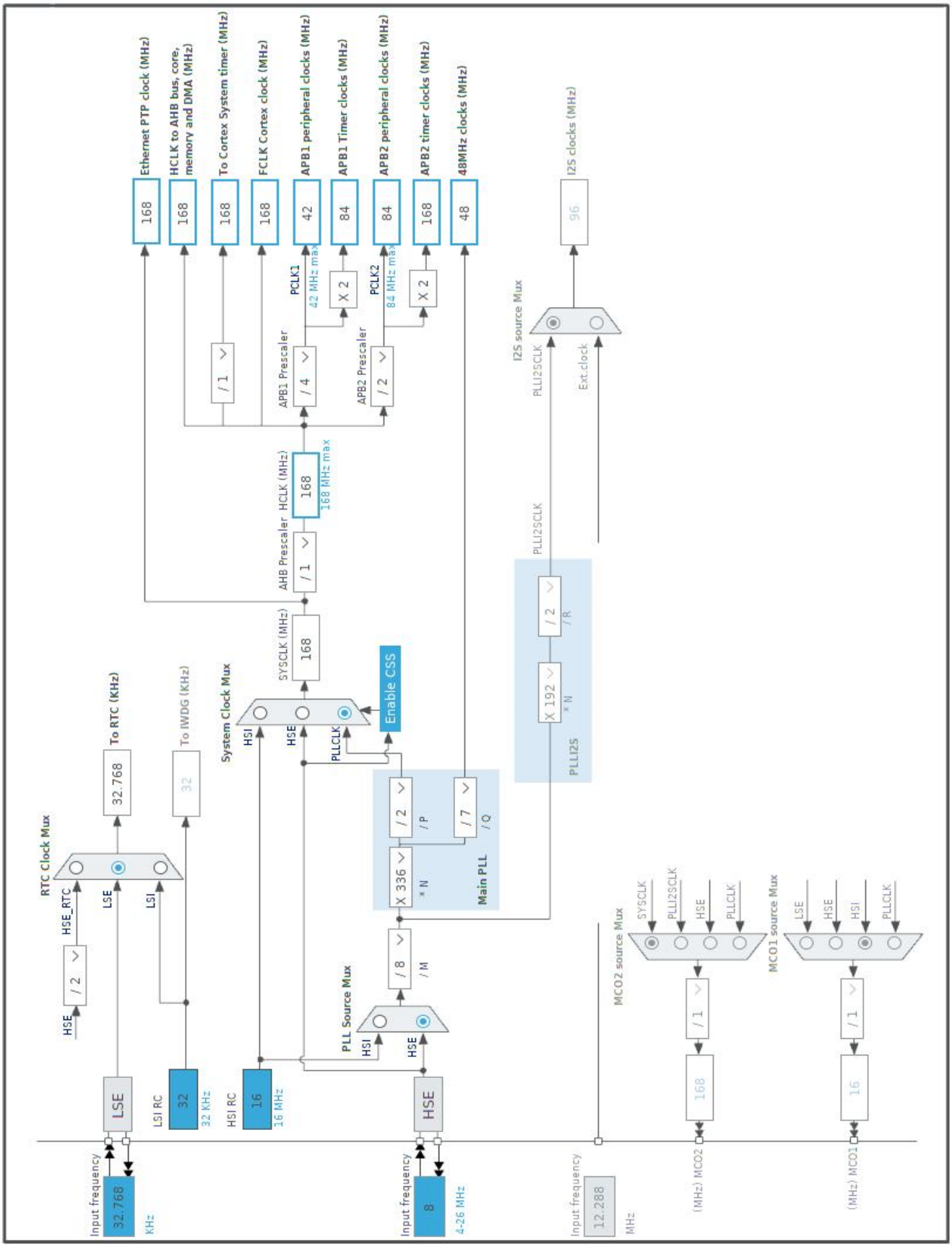
# 3. Pins Configuration

| Pin Number LQFP100 | Pin Name (function after reset) | Pin Type | Alternate Function(s) | Label |
|---|---|---|---|---|
| 2 | PE3 * | I/O | GPIO_Input | I_KEY2 |
| 3 | PE4 * | I/O | GPIO_Input | I_KEY3 |
| 4 | PE5 | I/O | TIM9_CH1 | TIM_FAN_PWM |
| 5 | PE6 | I/O | TIM9_CH2 | I_FAN_INDEX |
| 6 | VBAT | Power | | |
| 7 | PC13-ANTI_TAMP * | I/O | GPIO_Output | O_LED1 |
| 8 | PC14-OSC32_IN | I/O | RCC_OSC32_IN | |
| 9 | PC15-OSC32_OUT | I/O | RCC_OSC32_OUT | |
| 10 | VSS | Power | | |
| 11 | VDD | Power | | |
| 12 | PH0-OSC_IN | I/O | RCC_OSC_IN | |
| 13 | PH1-OSC_OUT | I/O | RCC_OSC_OUT | |
| 14 | NRST | Reset | | |
| 15 | PC0 | I/O | ADC2_IN10 | ADC_MOT1_CUR |
| 16 | PC1 | I/O | ADC2_IN11 | ADC_MOT2_CUR |
| 19 | VDD | Power | | |
| 20 | VSSA | Power | | |
| 21 | VREF+ | Power | | |
| 22 | VDDA | Power | | |
| 23 | PA0-WKUP | I/O | GPIO_EXTI0 | I_KEY_UP |
| 25 | PA2 | I/O | ADC1_IN2 | ADC_TEMP |
| 27 | VSS | Power | | |
| 28 | VDD | Power | | |
| 31 | PA6 * | I/O | GPIO_Output | O_LED3 |
| 32 | PA7 * | I/O | GPIO_Output | O_LED2 |
| 35 | PB0 * | I/O | GPIO_Output | O_SPI_CS1 |
| 36 | PB1 * | I/O | GPIO_Output | O_SPI_CS2 |
| 38 | PE7 * | I/O | GPIO_Output | O_SPI_CS3 |
| 39 | PE8 | I/O | TIM1_CH1N | TIM_MOT1_B |
| 40 | PE9 | I/O | TIM1_CH1 | TIM_MOT1_A |
| 41 | PE10 | I/O | TIM1_CH2N | TIM_MOT2_B |
| 42 | PE11 | I/O | TIM1_CH2 | TIM_MOT2_A |
| 45 | PE14 * | I/O | GPIO_Output | O_MOT_ENABLE |
| 49 | VCAP_1 | Power | | |
| 50 | VDD | Power | | |
| 51 | PB12 | I/O | GPIO_EXTI12 | I_MOT_FAULT1 |

| Pin Number LQFP100 | Pin Name (function after reset) | Pin Type | Alternate Function(s) | Label |
|---|---|---|---|---|
| 52 | PB13 | I/O | GPIO_EXTI13 | I_MOT_FAULT2 |
| 53 | PB14 | I/O | TIM12_CH1 | TIM_AUX_2 |
| 54 | PB15 | I/O | TIM12_CH2 | TIM_AUX_1 |
| 59 | PD12 | I/O | TIM4_CH1 | TIM_ENC2_A |
| 60 | PD13 | I/O | TIM4_CH2 | TIM_ENC2_B |
| 63 | PC6 | I/O | TIM3_CH1 | TIM_ENC1_A |
| 64 | PC7 | I/O | TIM3_CH2 | TIM_ENC1_B |
| 65 | PC8 | I/O | SDIO_D0 | |
| 66 | PC9 | I/O | SDIO_D1 | |
| 68 | PA9 | I/O | USART1_TX | |
| 69 | PA10 | I/O | USART1_RX | |
| 70 | PA11 | I/O | USB_OTG_FS_DM | |
| 71 | PA12 | I/O | USB_OTG_FS_DP | |
| 72 | PA13 | I/O | SYS_JTMS-SWDIO | |
| 73 | VCAP_2 | Power | | |
| 74 | VSS | Power | | |
| 75 | VDD | Power | | |
| 76 | PA14 | I/O | SYS_JTCK-SWCLK | |
| 77 | PA15 | I/O | GPIO_EXTI15 | I_KEY1 |
| 78 | PC10 | I/O | SDIO_D2 | |
| 79 | PC11 | I/O | SDIO_D3 | |
| 80 | PC12 | I/O | SDIO_CK | |
| 83 | PD2 | I/O | SDIO_CMD | |
| 86 | PD5 | I/O | USART2_TX | |
| 87 | PD6 | I/O | USART2_RX | |
| 89 | PB3 | I/O | SPI1_SCK | |
| 90 | PB4 | I/O | SPI1_MISO | |
| 91 | PB5 | I/O | SPI1_MOSI | |
| 92 | PB6 | I/O | I2C1_SCL | |
| 93 | PB7 | I/O | I2C1_SDA | |
| 94 | BOOT0 | Boot | | |
| 95 | PB8 * | I/O | GPIO_Output | O_PWR_EN |
| 97 | PE0 * | I/O | GPIO_Output | O_PWR_MOT_EN |
| 99 | VSS | Power | | |
| 100 | VDD | Power | | |

* The pin is affected with an I/O function

# 4. Clock Tree Configuration



# 5. Software Project

## 5.1. Project Settings

| Name | Value |
|---|---|
| Project Name | UNAVng_fw |
| Project Folder | /home/alessio/code/unav2/hardware/UNAVng_fw |
| Toolchain / IDE | Makefile |
| Firmware Package Name and Version | STM32Cube FW_F4 V1.24.2 |

## 5.2. Code Generation Settings

| Name | Value |
|---|---|
| STM32Cube MCU packages and embedded software | Copy all used libraries into the project folder |
| Generate peripheral initialization as a pair of '.c/.h' files | Yes |
| Backup previously generated files when re-generating | No |
| Delete previously generated files when not re-generated | No |
| Set all free pins as analog (to optimize the power consumption) | No |

# 6. Power Consumption Calculator report

6.1. Microcontroller Selection

| | |
|---|---|
| Series | STM32F4 |
| Line | STM32F407/417 |
| MCU | STM32F407VETx |
| Datasheet | 022152_Rev8 |

6.2. Parameter Selection

| | |
|---|---|
| Temperature | 25 |
| Vdd | 3.3 |

# 7. IPs and Middleware Configuration

## 7.1. ADC1

**mode: IN2**

**mode: Temperature Sensor Channel**

**mode: Vrefint Channel**

**mode: Vbat Channel**

### 7.1.1. Parameter Settings:

**ADCs_Common_Settings:**

| | |
|---|---|
| Mode | Independent mode |

**ADC_Settings:**

| | |
|---|---|
| Clock Prescaler | **PCLK2 divided by 6 *** |
| Resolution | 12 bits (15 ADC Clock cycles) |
| Data Alignment | Right alignment |
| Scan Conversion Mode | Disabled |
| Continuous Conversion Mode | Disabled |
| Discontinuous Conversion Mode | Disabled |
| DMA Continuous Requests | Disabled |
| End Of Conversion Selection | EOC flag at the end of single channel conversion |

**ADC_Regular_ConversionMode:**

| | |
|---|---|
| Number Of Conversion | 1 |
| External Trigger Conversion Source | Regular Conversion launched by software |
| External Trigger Conversion Edge | None |
| Rank | 1 |
| Channel | **Channel Vbat *** |
| Sampling Time | 3 Cycles |

**ADC_Injected_ConversionMode:**

| | |
|---|---|
| Number Of Conversions | 0 |

**WatchDog:**

| | |
|---|---|
| Enable Analog WatchDog Mode | false |

## 7.2. ADC2

**mode: IN10**

**mode: IN11**

### 7.2.1. Parameter Settings:

**ADCs_Common_Settings:**

| | |
|---|---|
| Mode | Independent mode |

**ADC_Settings:**

| | |
|---|---|
| Clock Prescaler | **PCLK2 divided by 6 *** |
| Resolution | 12 bits (15 ADC Clock cycles) |
| Data Alignment | Right alignment |
| Scan Conversion Mode | Enabled |
| Continuous Conversion Mode | Disabled |
| Discontinuous Conversion Mode | **Enabled *** |
| Number Of Discontinuous Conversions | 1 |
| DMA Continuous Requests | **Enabled *** |
| End Of Conversion Selection | **EOC flag at the end of all conversions *** |

**ADC_Regular_ConversionMode:**

| | |
|---|---|
| Number Of Conversion | **4 *** |
| External Trigger Conversion Source | **Timer 8 Trigger Out event *** |
| External Trigger Conversion Edge | Trigger detection on the rising edge |
| Rank | 1 |
| Channel | Channel 10 |
| Sampling Time | **28 Cycles *** |
| Rank | **2 *** |
| Channel | **Channel 11 *** |
| Sampling Time | **28 Cycles *** |
| Rank | **3 *** |
| Channel | Channel 10 |
| Sampling Time | **28 Cycles *** |
| Rank | **4 *** |
| Channel | **Channel 11 *** |
| Sampling Time | **28 Cycles *** |

**ADC_Injected_ConversionMode:**

| | |
|---|---|
| Number Of Conversions | 0 |

**WatchDog:**

| | |
|---|---|
| Enable Analog WatchDog Mode | false |

## *7.3. GPIO*

## 7.4. I2C1

### I2C: I2C

### 7.4.1. Parameter Settings:

**Master Features:**

| | |
|---|---|
| I2C Speed Mode | Standard Mode |
| I2C Clock Speed (Hz) | 100000 |

**Slave Features:**

| | |
|---|---|
| Clock No Stretch Mode | Disabled |
| Primary Address Length selection | 7-bit |
| Dual Address Acknowledged | Disabled |
| Primary slave address | 0 |
| General Call address detection | Disabled |

## 7.5. RCC

### High Speed Clock (HSE): Crystal/Ceramic Resonator

### Low Speed Clock (LSE) : Crystal/Ceramic Resonator

### 7.5.1. Parameter Settings:

**System Parameters:**

| | |
|---|---|
| VDD voltage (V) | 3.3 |
| Instruction Cache | Enabled |
| Prefetch Buffer | Enabled |
| Data Cache | Enabled |
| Flash Latency(WS) | 5 WS (6 CPU cycle) |

**RCC Parameters:**

| | |
|---|---|
| HSI Calibration Value | 16 |
| HSE Startup Timout Value (ms) | 100 |
| LSE Startup Timout Value (ms) | 5000 |

**Power Parameters:**

| | |
|---|---|
| Power Regulator Voltage Scale | Power Regulator Voltage Scale 1 |

## 7.6. RTC

### mode: Activate Clock Source

### mode: Activate Calendar

### 7.6.1. Parameter Settings:

**General:**

| | |
|---|---|
| Hour Format | Hourformat 24 |
| Asynchronous Predivider value | 127 |
| Synchronous Predivider value | 255 |

**Calendar Time:**

| | |
|---|---|
| Data Format | BCD data format |
| Hours | 0 |
| Minutes | 0 |
| Seconds | 0 |
| Day Light Saving: value of hour adjustment | Daylightsaving None |
| Store Operation | Storeoperation Reset |

**Calendar Date:**

| | |
|---|---|
| Week Day | **Thursday *** |
| Month | **July *** |
| Date | **7 *** |
| Year | **18 *** |

## *7.7. SDIO*

### Mode: SD 4 bits Wide bus

### 7.7.1. Parameter Settings:

**SDIO parameters:**

| | |
|---|---|
| Clock transition on which the bit capture is made | Rising transition |
| SDIO Clock divider bypass | Disable |
| SDIO Clock output enable when the bus is idle | Disable the power save for the clock |
| SDIO hardware flow control | **The hardware control flow is enabled *** |
| SDIOCLK clock divide factor | **1 *** |

## *7.8. SPI1*

### Mode: Full-Duplex Master

### 7.8.1. Parameter Settings:

**Basic Parameters:**

| | |
|---|---|
| Frame Format | Motorola |
| Data Size | 8 Bits |
| First Bit | MSB First |

**Clock Parameters:**

| | |
|---|---|
| Prescaler (for Baud Rate) | 2 |
| Baud Rate | **42.0 MBits/s *** |
| Clock Polarity (CPOL) | Low |
| Clock Phase (CPHA) | 1 Edge |

**Advanced Parameters:**

| | |
|---|---|
| CRC Calculation | Disabled |
| NSS Signal Type | Software |

## *7.9. SYS*

**Debug: Serial Wire**

**Timebase Source: TIM10**

## *7.10. TIM1*

**Clock Source : Internal Clock**

**Channel1: PWM Generation CH1 CH1N**

**Channel2: PWM Generation CH2 CH2N**

### 7.10.1. Parameter Settings:

**Counter Settings:**

| | |
|---|---|
| Prescaler (PSC - 16 bits value) | **7 *** |
| Counter Mode | Up |
| Counter Period (AutoReload Register - 16 bits value ) | **1024 *** |
| Internal Clock Division (CKD) | No Division |
| Repetition Counter (RCR - 8 bits value) | 0 |
| auto-reload preload | **Enable *** |

**Trigger Output (TRGO) Parameters:**

| | |
|---|---|
| Master/Slave Mode (MSM bit) | Disable (Trigger input effect not delayed) |
| Trigger Event Selection | Reset (UG bit from TIMx_EGR) |

**Break And Dead Time management - BRK Configuration:**

| | |
|---|---|
| BRK State | Disable |
| BRK Polarity | High |

**Break And Dead Time management - Output Configuration:**

| | |
|---|---|
| Automatic Output State | Disable |
| Off State Selection for Run Mode (OSSR) | Disable |
| Off State Selection for Idle Mode (OSSI) | Disable |
| Lock Configuration | Off |
| Dead Time | **2 *** |

**PWM Generation Channel 1 and 1N:**

| | |
|---|---|
| Mode | PWM mode 1 |
| Pulse (16 bits value) | **512 *** |
| Output compare preload | Enable |
| Fast Mode | Disable |
| CH Polarity | High |
| CHN Polarity | High |
| CH Idle State | Reset |
| CHN Idle State | Reset |

**PWM Generation Channel 2 and 2N:**

| | |
|---|---|
| Mode | PWM mode 1 |
| Pulse (16 bits value) | **512 *** |
| Output compare preload | Enable |
| Fast Mode | Disable |
| CH Polarity | High |
| CHN Polarity | High |
| CH Idle State | Reset |
| CHN Idle State | Reset |

## *7.11. TIM3*

## Combined Channels: Encoder Mode

### 7.11.1. Parameter Settings:

**Counter Settings:**

| | |
|---|---|
| Prescaler (PSC - 16 bits value) | 0 |
| Counter Mode | Up |
| Counter Period (AutoReload Register - 16 bits value ) | **65535 *** |
| Internal Clock Division (CKD) | No Division |
| auto-reload preload | Disable |

**Trigger Output (TRGO) Parameters:**

| | |
|---|---|
| Master/Slave Mode (MSM bit) | Disable (Trigger input effect not delayed) |
| Trigger Event Selection | Reset (UG bit from TIMx_EGR) |

**Encoder:**

| | |
|---|---|
| Encoder Mode | **Encoder Mode TI1 and TI2 *** |
| ____ Parameters for Channel 1 ____ | |
| Polarity | Rising Edge |
| IC Selection | Direct |
| Prescaler Division Ratio | No division |
| Input Filter | 0 |
| ____ Parameters for Channel 2 ____ | |
| Polarity | Rising Edge |
| IC Selection | Direct |
| Prescaler Division Ratio | No division |
| Input Filter | 0 |

## *7.12. TIM4*

### Combined Channels: Encoder Mode

### 7.12.1. Parameter Settings:

**Counter Settings:**

| | |
|---|---|
| Prescaler (PSC - 16 bits value) | **1 *** |
| Counter Mode | Up |
| Counter Period (AutoReload Register - 16 bits value ) | **65535 *** |
| Internal Clock Division (CKD) | No Division |
| auto-reload preload | Disable |

**Trigger Output (TRGO) Parameters:**

| | |
|---|---|
| Master/Slave Mode (MSM bit) | Disable (Trigger input effect not delayed) |
| Trigger Event Selection | Reset (UG bit from TIMx_EGR) |

**Encoder:**

| | |
|---|---|
| Encoder Mode | **Encoder Mode TI1 and TI2 *** |
| ____ Parameters for Channel 1 ____ | |
| Polarity | Rising Edge |
| IC Selection | Direct |
| Prescaler Division Ratio | No division |
| Input Filter | 0 |
| ____ Parameters for Channel 2 ____ | |
| Polarity | Rising Edge |
| IC Selection | Direct |
| Prescaler Division Ratio | No division |
| Input Filter | 0 |

## 7.13. TIM8

**Clock Source : Internal Clock**

**Channel1: Output Compare No Output**

### 7.13.1. Parameter Settings:

**Counter Settings:**

| | |
|---|---|
| Prescaler (PSC - 16 bits value) | **168 *** |
| Counter Mode | Up |
| Counter Period (AutoReload Register - 16 bits value ) | **1000 *** |
| Internal Clock Division (CKD) | No Division |
| Repetition Counter (RCR - 8 bits value) | 0 |
| auto-reload preload | **Enable *** |

**Trigger Output (TRGO) Parameters:**

| | |
|---|---|
| Master/Slave Mode (MSM bit) | Disable (Trigger input effect not delayed) |
| Trigger Event Selection | **Update Event *** |

**Break And Dead Time management - BRK Configuration:**

| | |
|---|---|
| BRK State | Disable |
| BRK Polarity | High |

**Break And Dead Time management - Output Configuration:**

| | |
|---|---|
| Automatic Output State | Disable |
| Off State Selection for Run Mode (OSSR) | Disable |
| Off State Selection for Idle Mode (OSSI) | Disable |
| Lock Configuration | Off |

**Output Compare No Output Channel 1:**

| | |
|---|---|
| Mode | **Active Level on match *** |
| Pulse (16 bits value) | 0 |
| Output compare preload | Disable |
| CH Polarity | High |
| CH Idle State | Reset |

## 7.14. TIM9

**mode: Clock Source**

**Channel1: PWM Generation CH1**

**Channel2: Input Capture direct mode**

### 7.14.1. Parameter Settings:

**Counter Settings:**

| | |
|---|---|
| Prescaler (PSC - 16 bits value) | **15 *** |
| Counter Mode | Up |
| Counter Period (AutoReload Register - 16 bits value ) | **4096 *** |
| Internal Clock Division (CKD) | No Division |
| auto-reload preload | **Enable *** |

**PWM Generation Channel 1:**

| | |
|---|---|
| Mode | PWM mode 1 |
| Pulse (16 bits value) | 0 |
| Output compare preload | Enable |
| Fast Mode | Disable |
| CH Polarity | High |

**Input Capture Channel 2:**

| | |
|---|---|
| Polarity Selection | Rising Edge |
| IC Selection | Direct |
| Prescaler Division Ratio | No division |
| Input Filter (4 bits value) | 0 |

## *7.15. TIM11*

**mode: Activated**

### 7.15.1. Parameter Settings:

**Counter Settings:**

| | |
|---|---|
| Prescaler (PSC - 16 bits value) | 0 |
| Counter Mode | Up |
| Counter Period (AutoReload Register - 16 bits value ) | 0 |
| Internal Clock Division (CKD) | No Division |
| auto-reload preload | Disable |

## *7.16. TIM12*

**Channel1: PWM Generation CH1**

**Channel2: PWM Generation CH2**

### 7.16.1. Parameter Settings:

**Counter Settings:**

| | |
|---|---|
| Prescaler (PSC - 16 bits value) | 0 |
| Counter Mode | Up |
| Counter Period (AutoReload Register - 16 bits value ) | 0 |
| Internal Clock Division (CKD) | No Division |
| auto-reload preload | Disable |

**PWM Generation Channel 1:**

| | |
|---|---|
| Mode | PWM mode 1 |
| Pulse (16 bits value) | 0 |
| Output compare preload | Enable |
| Fast Mode | Disable |
| CH Polarity | High |

**PWM Generation Channel 2:**

| | |
|---|---|
| Mode | PWM mode 1 |
| Pulse (16 bits value) | 0 |
| Output compare preload | Enable |
| Fast Mode | Disable |
| CH Polarity | High |

## *7.17. TIM13*

**mode: Activated**

### 7.17.1. Parameter Settings:

**Counter Settings:**

| | |
|---|---|
| Prescaler (PSC - 16 bits value) | **15 *** |
| Counter Mode | Up |
| Counter Period (AutoReload Register - 16 bits value ) | **1024 *** |
| Internal Clock Division (CKD) | No Division |
| auto-reload preload | **Enable *** |

## *7.18. TIM14*

**mode: Activated**

### 7.18.1. Parameter Settings:

**Counter Settings:**

| | |
|---|---|
| Prescaler (PSC - 16 bits value) | **15 *** |
| Counter Mode | Up |
| Counter Period (AutoReload Register - 16 bits value ) | |

| | |
|---|---|
| | **1024 *** |
| Internal Clock Division (CKD) | No Division |
| auto-reload preload | **Enable *** |

## *7.19. USART1*

### Mode: Asynchronous

### 7.19.1. Parameter Settings:

**Basic Parameters:**

| | |
|---|---|
| Baud Rate | 115200 |
| Word Length | 8 Bits (including Parity) |
| Parity | None |
| Stop Bits | 1 |

**Advanced Parameters:**

| | |
|---|---|
| Data Direction | Receive and Transmit |
| Over Sampling | 16 Samples |

## *7.20. USART2*

### Mode: Asynchronous

### 7.20.1. Parameter Settings:

**Basic Parameters:**

| | |
|---|---|
| Baud Rate | 115200 |
| Word Length | 8 Bits (including Parity) |
| Parity | None |
| Stop Bits | 1 |

**Advanced Parameters:**

| | |
|---|---|
| Data Direction | Receive and Transmit |
| Over Sampling | 16 Samples |

## *7.21. USB_OTG_FS*

### Mode: Device_Only

### 7.21.1. Parameter Settings:

| | |
|---|---|
| Speed | Device Full Speed 12MBit/s |
| Low power | Disabled |
| Link Power Management | Disabled |
| VBUS sensing | Disabled |
| Signal start of frame | Disabled |

## 7.22. FREERTOS

### Interface: CMSIS_V1

### 7.22.1. Config parameters:

#### API:

| | |
|---|---|
| FreeRTOS API | CMSIS v1 |

#### Versions:

| | |
|---|---|
| FreeRTOS version | 10.0.1 |
| CMSIS-RTOS version | 1.02 |

#### Kernel settings:

| | |
|---|---|
| USE_PREEMPTION | Enabled |
| CPU_CLOCK_HZ | SystemCoreClock |
| TICK_RATE_HZ | 1000 |
| MAX_PRIORITIES | 7 |
| MINIMAL_STACK_SIZE | 128 |
| MAX_TASK_NAME_LEN | 16 |
| USE_16_BIT_TICKS | Disabled |
| IDLE_SHOULD_YIELD | Enabled |
| USE_MUTEXES | Enabled |
| USE_RECURSIVE_MUTEXES | **Enabled *** |
| USE_COUNTING_SEMAPHORES | Disabled |
| QUEUE_REGISTRY_SIZE | 8 |
| USE_APPLICATION_TASK_TAG | Disabled |
| ENABLE_BACKWARD_COMPATIBILITY | Enabled |
| USE_PORT_OPTIMISED_TASK_SELECTION | Enabled |
| USE_TICKLESS_IDLE | Disabled |
| USE_TASK_NOTIFICATIONS | Enabled |
| RECORD_STACK_HIGH_ADDRESS | Disabled |

#### Memory management settings:

| | |
|---|---|
| Memory Allocation | Dynamic / Static |
| TOTAL_HEAP_SIZE | **65535 *** |
| Memory Management scheme | heap_4 |

**Hook function related definitions:**

| | |
|---|---|
| USE_IDLE_HOOK | Disabled |
| USE_TICK_HOOK | Disabled |
| USE_MALLOC_FAILED_HOOK | Disabled |
| USE_DAEMON_TASK_STARTUP_HOOK | Disabled |
| CHECK_FOR_STACK_OVERFLOW | Disabled |

**Run time and task stats gathering related definitions:**

| | |
|---|---|
| GENERATE_RUN_TIME_STATS | **Enabled *** |
| USE_TRACE_FACILITY | Disabled |
| USE_STATS_FORMATTING_FUNCTIONS | Disabled |

**Co-routine related definitions:**

| | |
|---|---|
| USE_CO_ROUTINES | Disabled |
| MAX_CO_ROUTINE_PRIORITIES | 2 |

**Software timer definitions:**

| | |
|---|---|
| USE_TIMERS | Disabled |

**Interrupt nesting behaviour configuration:**

| | |
|---|---|
| LIBRARY_LOWEST_INTERRUPT_PRIORITY | 15 |
| LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY | 5 |

## 7.22.2. Include parameters:

**Include definitions:**

| | |
|---|---|
| vTaskPrioritySet | Enabled |
| uxTaskPriorityGet | Enabled |
| vTaskDelete | Enabled |
| vTaskCleanUpResources | Disabled |
| vTaskSuspend | Enabled |
| vTaskDelayUntil | **Enabled *** |
| vTaskDelay | Enabled |
| xTaskGetSchedulerState | Enabled |
| xTaskResumeFromISR | Enabled |
| xQueueGetMutexHolder | Disabled |
| xSemaphoreGetMutexHolder | Disabled |
| pcTaskGetTaskName | Disabled |
| uxTaskGetStackHighWaterMark | **Enabled *** |
| xTaskGetCurrentTaskHandle | Disabled |
| eTaskGetState | Disabled |
| xEventGroupSetBitFromISR | Disabled |
| xTimerPendFunctionCall | Disabled |
| xTaskAbortDelay | Disabled |
| xTaskGetHandle | Disabled |

## *7.23. USB_DEVICE*

### Class For FS IP: Communication Device Class (Virtual Port Com)

### 7.23.1. Parameter Settings:

**Basic Parameters:**

| | |
|---|---|
| USBD_MAX_NUM_INTERFACES (Maximum number of supported interfaces) | **8 *** |
| USBD_MAX_NUM_CONFIGURATION (Maximum number of supported configuration) | 1 |
| USBD_MAX_STR_DESC_SIZ (Maximum size for the string descriptors) | 0x200 |
| USBD_SELF_POWERED (Enabled self power) | Enabled |
| USBD_DEBUG_LEVEL (USBD Debug Level) | 0: No debug message |

**Class Parameters:**

| | |
|---|---|
| USB CDC Rx Buffer Size | 2048 |
| USB CDC Tx Buffer Size | 2048 |

### 7.23.2. Device Descriptor:

**Device Descriptor:**

| | |
|---|---|
| VID (Vendor IDentifier) | 1155 |
| LANGID_STRING (Language Identifier) | English(United States) |
| MANUFACTURER_STRING (Manufacturer Identifier) | STMicroelectronics |

**Device Descriptor FS:**

| | |
|---|---|
| PID (Product IDentifier) | 22336 |
| PRODUCT_STRING (Product Identifier) | **UNAVng *** |
| CONFIGURATION_STRING (Configuration Identifier) | CDC Config |
| INTERFACE_STRING (Interface Identifier) | CDC Interface |

*** User modified value**

# 8. System Configuration

## 8.1. GPIO configuration

| IP | Pin | Signal | GPIO mode | GPIO pull/up pull down | Max Speed | User Label |
|---|---|---|---|---|---|---|
| ADC1 | PA2 | ADC1_IN2 | Analog mode | No pull-up and no pull-down | n/a | ADC_TEMP |
| ADC2 | PC0 | ADC2_IN10 | Analog mode | No pull-up and no pull-down | n/a | ADC_MOT1_CUR |
| | PC1 | ADC2_IN11 | Analog mode | No pull-up and no pull-down | n/a | ADC_MOT2_CUR |
| I2C1 | PB6 | I2C1_SCL | Alternate Function Open Drain | Pull-up | **Very High *** | |
| | PB7 | I2C1_SDA | Alternate Function Open Drain | Pull-up | **Very High *** | |
| RCC | PC14-OSC32_IN | RCC_OSC32_IN | n/a | n/a | n/a | |
| | PC15-OSC32_OUT | RCC_OSC32_OUT | n/a | n/a | n/a | |
| | PH0-OSC_IN | RCC_OSC_IN | n/a | n/a | n/a | |
| | PH1-OSC_OUT | RCC_OSC_OUT | n/a | n/a | n/a | |
| SDIO | PC8 | SDIO_D0 | Alternate Function Push Pull | No pull-up and no pull-down | Very High | |
| | PC9 | SDIO_D1 | Alternate Function Push Pull | No pull-up and no pull-down | Very High | |
| | PC10 | SDIO_D2 | Alternate Function Push Pull | No pull-up and no pull-down | Very High | |
| | PC11 | SDIO_D3 | Alternate Function Push Pull | No pull-up and no pull-down | Very High | |
| | PC12 | SDIO_CK | Alternate Function Push Pull | No pull-up and no pull-down | Very High | |
| | PD2 | SDIO_CMD | Alternate Function Push Pull | No pull-up and no pull-down | Very High | |
| SPI1 | PB3 | SPI1_SCK | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | |
| | PB4 | SPI1_MISO | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | |
| | PB5 | SPI1_MOSI | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | |
| SYS | PA13 | SYS_JTMS-SWDIO | n/a | n/a | n/a | |
| | PA14 | SYS_JTCK-SWCLK | n/a | n/a | n/a | |
| TIM1 | PE8 | TIM1_CH1N | Alternate Function Push Pull | No pull-up and no pull-down | Low | TIM_MOT1_B |
| | PE9 | TIM1_CH1 | Alternate Function Push Pull | No pull-up and no pull-down | Low | TIM_MOT1_A |
| | PE10 | TIM1_CH2N | Alternate Function Push Pull | No pull-up and no pull-down | Low | TIM_MOT2_B |
| | PE11 | TIM1_CH2 | Alternate Function Push Pull | No pull-up and no pull-down | Low | TIM_MOT2_A |

| IP | Pin | Signal | GPIO mode | GPIO pull/up pull down | Max Speed | User Label |
|---|---|---|---|---|---|---|
| TIM3 | PC6 | TIM3_CH1 | Alternate Function Push Pull | No pull-up and no pull-down | Low | TIM_ENC1_A |
| | PC7 | TIM3_CH2 | Alternate Function Push Pull | No pull-up and no pull-down | Low | TIM_ENC1_B |
| TIM4 | PD12 | TIM4_CH1 | Alternate Function Push Pull | No pull-up and no pull-down | Low | TIM_ENC2_A |
| | PD13 | TIM4_CH2 | Alternate Function Push Pull | No pull-up and no pull-down | Low | TIM_ENC2_B |
| TIM9 | PE5 | TIM9_CH1 | Alternate Function Push Pull | No pull-up and no pull-down | Low | TIM_FAN_PWM |
| | PE6 | TIM9_CH2 | Alternate Function Push Pull | No pull-up and no pull-down | Low | I_FAN_INDEX |
| TIM12 | PB14 | TIM12_CH1 | Alternate Function Push Pull | No pull-up and no pull-down | Low | TIM_AUX_2 |
| | PB15 | TIM12_CH2 | Alternate Function Push Pull | No pull-up and no pull-down | Low | TIM_AUX_1 |
| USART1 | PA9 | USART1_TX | Alternate Function Push Pull | Pull-up | **Very High *** | |
| | PA10 | USART1_RX | Alternate Function Push Pull | Pull-up | **Very High *** | |
| USART2 | PD5 | USART2_TX | Alternate Function Push Pull | Pull-up | **Very High *** | |
| | PD6 | USART2_RX | Alternate Function Push Pull | Pull-up | **Very High *** | |
| USB_OTG_FS | PA11 | USB_OTG_FS_DM | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | |
| | PA12 | USB_OTG_FS_DP | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | |
| GPIO | PE3 | GPIO_Input | Input mode | No pull-up and no pull-down | n/a | I_KEY2 |
| | PE4 | GPIO_Input | Input mode | No pull-up and no pull-down | n/a | I_KEY3 |
| | PC13-ANTI_TAMP | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | O_LED1 |
| | PA0-WKUP | GPIO_EXTI0 | External Interrupt Mode with Rising edge trigger detection | No pull-up and no pull-down | n/a | I_KEY_UP |
| | PA6 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | O_LED3 |
| | PA7 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | O_LED2 |
| | PB0 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | O_SPI_CS1 |
| | PB1 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | O_SPI_CS2 |
| | PE7 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | O_SPI_CS3 |
| | PE14 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | O_MOT_ENABLE |
| | PB12 | GPIO_EXTI12 | External Interrupt Mode with Rising edge trigger detection | No pull-up and no pull-down | n/a | I_MOT_FAULT1 |
| | PB13 | GPIO_EXTI13 | External Interrupt Mode with Rising edge trigger detection | No pull-up and no pull-down | n/a | I_MOT_FAULT2 |
| | PA15 | GPIO_EXTI15 | External Interrupt Mode with Rising edge trigger detection | No pull-up and no pull-down | n/a | I_KEY1 |
| | PB8 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | O_PWR_EN |
| | PE0 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | O_PWR_MOT_EN |

## 8.2. DMA configuration

| DMA request | Stream | Direction | Priority |
|---|---|---|---|
| SDIO_RX | DMA2_Stream6 | Peripheral To Memory | Low |
| SDIO_TX | DMA2_Stream3 | Memory To Peripheral | Low |
| USART1_RX | DMA2_Stream5 | Peripheral To Memory | **Medium *** |
| USART1_TX | DMA2_Stream7 | Memory To Peripheral | **Medium *** |
| USART2_RX | DMA1_Stream5 | Peripheral To Memory | **Medium *** |
| USART2_TX | DMA1_Stream6 | Memory To Peripheral | **Medium *** |
| ADC2 | DMA2_Stream2 | Peripheral To Memory | **High *** |

### *SDIO_RX: DMA2_Stream6 DMA request Settings:*

| | |
|---|---|
| Mode: | **Peripheral Flow Control *** |
| Use fifo: | **Enable *** |
| FIFO Threshold: | Full |
| Peripheral Increment: | Disable |
| Memory Increment: | **Enable *** |
| Peripheral Data Width: | **Word *** |
| Memory Data Width: | Word |
| Peripheral Burst Size: | **4 Increment *** |
| Memory Burst Size: | 4 Increment |

### *SDIO_TX: DMA2_Stream3 DMA request Settings:*

| | |
|---|---|
| Mode: | **Peripheral Flow Control *** |
| Use fifo: | **Enable *** |
| FIFO Threshold: | Full |
| Peripheral Increment: | Disable |
| Memory Increment: | **Enable *** |
| Peripheral Data Width: | **Word *** |
| Memory Data Width: | Word |
| Peripheral Burst Size: | **4 Increment *** |
| Memory Burst Size: | 4 Increment |

### *USART1_RX: DMA2_Stream5 DMA request Settings:*

| | |
|---|---|
| Mode: | Normal |
| Use fifo: | Disable |
| Peripheral Increment: | Disable |
| Memory Increment: | **Enable *** |
| Peripheral Data Width: | Byte |
| Memory Data Width: | Byte |

### *USART1_TX: DMA2_Stream7 DMA request Settings:*

| | |
|---|---|
| Mode: | Normal |
| Use fifo: | Disable |
| Peripheral Increment: | Disable |
| Memory Increment: | **Enable *** |
| Peripheral Data Width: | Byte |
| Memory Data Width: | Byte |

### *USART2_RX: DMA1_Stream5 DMA request Settings:*

| | |
|---|---|
| Mode: | Normal |
| Use fifo: | Disable |
| Peripheral Increment: | Disable |
| Memory Increment: | **Enable *** |
| Peripheral Data Width: | Byte |
| Memory Data Width: | Byte |

### *USART2_TX: DMA1_Stream6 DMA request Settings:*

| | |
|---|---|
| Mode: | Normal |
| Use fifo: | Disable |
| Peripheral Increment: | Disable |
| Memory Increment: | **Enable *** |
| Peripheral Data Width: | Byte |
| Memory Data Width: | Byte |

### *ADC2: DMA2_Stream2 DMA request Settings:*

| | |
|---|---|
| Mode: | **Circular *** |
| Use fifo: | Disable |

| | |
|---|---|
| Peripheral Increment: | Disable |
| Memory Increment: | **Enable *** |
| Peripheral Data Width: | Half Word |
| Memory Data Width: | Half Word |

## 8.3. NVIC configuration

| Interrupt Table | Enable | Preenmption Priority | SubPriority |
|---|---|---|---|
| Non maskable interrupt | true | 0 | 0 |
| Hard fault interrupt | true | 0 | 0 |
| Memory management fault | true | 0 | 0 |
| Pre-fetch fault, memory access fault | true | 0 | 0 |
| Undefined instruction or illegal state | true | 0 | 0 |
| System service call via SWI instruction | true | 0 | 0 |
| Debug monitor | true | 0 | 0 |
| Pendable request for system service | true | 15 | 0 |
| System tick timer | true | 15 | 0 |
| DMA1 stream5 global interrupt | true | 5 | 0 |
| DMA1 stream6 global interrupt | true | 5 | 0 |
| TIM1 update interrupt and TIM10 global interrupt | true | 0 | 0 |
| DMA2 stream2 global interrupt | true | 5 | 0 |
| DMA2 stream3 global interrupt | true | 5 | 0 |
| USB On The Go FS global interrupt | true | 5 | 0 |
| DMA2 stream5 global interrupt | true | 5 | 0 |
| DMA2 stream6 global interrupt | true | 5 | 0 |
| DMA2 stream7 global interrupt | true | 5 | 0 |
| PVD interrupt through EXTI line 16 | unused | | |
| Flash global interrupt | unused | | |
| RCC global interrupt | unused | | |
| EXTI line0 interrupt | unused | | |
| ADC1, ADC2 and ADC3 global interrupts | unused | | |
| TIM1 break interrupt and TIM9 global interrupt | unused | | |
| TIM1 trigger and commutation interrupts and TIM11 global interrupt | unused | | |
| TIM1 capture compare interrupt | unused | | |
| TIM3 global interrupt | unused | | |
| TIM4 global interrupt | unused | | |
| I2C1 event interrupt | unused | | |
| I2C1 error interrupt | unused | | |
| SPI1 global interrupt | unused | | |
| USART1 global interrupt | unused | | |
| USART2 global interrupt | unused | | |
| EXTI line[15:10] interrupts | unused | | |
| TIM8 break interrupt and TIM12 global interrupt | unused | | |
| TIM8 update interrupt and TIM13 global interrupt | unused | | |
| | | | |

| Interrupt Table | Enable | Preenmption Priority | SubPriority |
|---|---|---|---|
| TIM8 trigger and commutation interrupts and TIM14 global interrupt | unused | | |
| TIM8 capture compare interrupt | unused | | |
| SDIO global interrupt | unused | | |
| FPU global interrupt | unused | | |

*** User modified value**

# 9. Software Pack Report