ECE385

Fall 2020

Experiment #1

Introductory Experiment

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D225
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Introduction

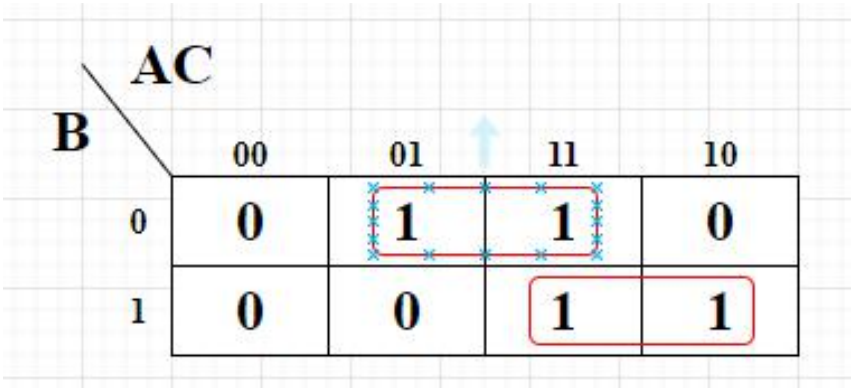
Lab1 mainly tell us how to use the new software - Quartus and how to handle the static hazard well.
In processing the software, we can understand why the static hazard will occur which confused me in ECE120, and we can cover all adjacent min-terms in the K-map to solve the hazard.
The chip we choose in this lab is 7400. The software we use for simulation is Quartus v18.1.

Write Description of the operation of circuits

The function of the circuit is a 2-to-1 MUX. We have two inputs(A,C), one select signal(B) and one output(Z).

For PartA:

The detail expression is $Z = BA + B'C$.
The K-maps are shown below:



For PartB:

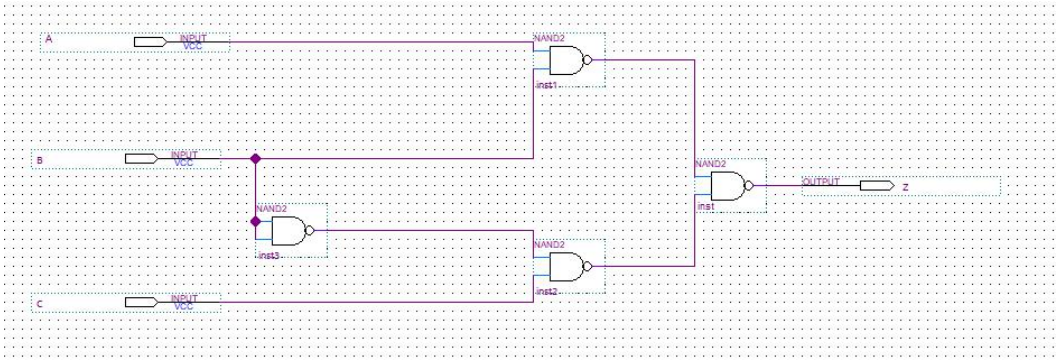
We do not see the static hazard even we use the timing simulation because the delay time caused by the inverter (one nand gate in this lab) is too short and the glitch will not happen. When we add more inverter to the circuit, the glitch will not happen as well because the quartus will automaticly optimize the circuit to the simpliest.

For PartC:

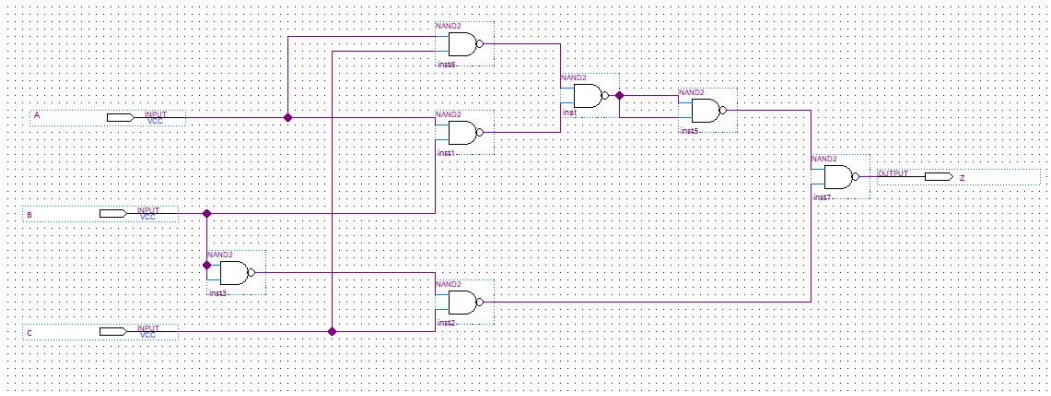
We modify the circuit by adding one more term to overcome the static hazard. The new expression is $Z = AB + B'C + AC$.
The Truth-table is same as the above one.
When A and C set 1 and B change from 1 to 0, the term AC will keep Z 1 to remove the effect caused by hazard.
Because we are only allowed to use 7400 chip(i.e. 2nand). So we need to change the expression to fit the chip. By DeMorgan's Law, we replace AB to x, B'C to y, AC to z, x'+y'+z' = (xyc)' = (xy)'+z', in this case, we can build the circuit.

Circuit Diagram

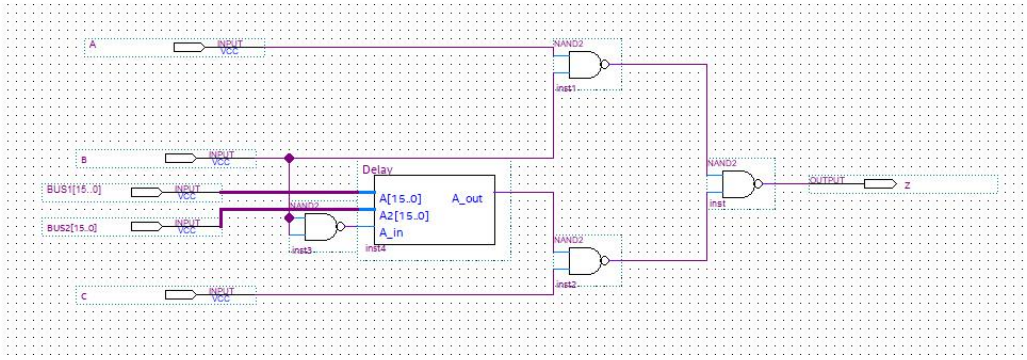
Prelab part A:



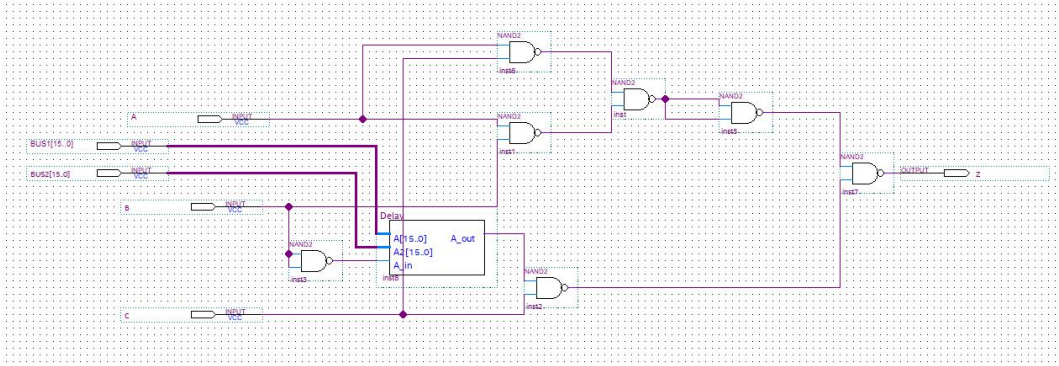
Prelab Part C:



Lab Part 1:



Lab Part 2:

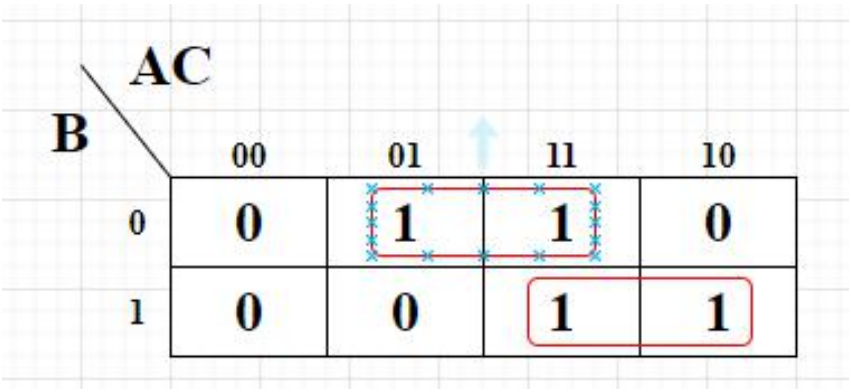


Documentation of Lab

Truth Table for Prelab PartA:

A	B	C	Z
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

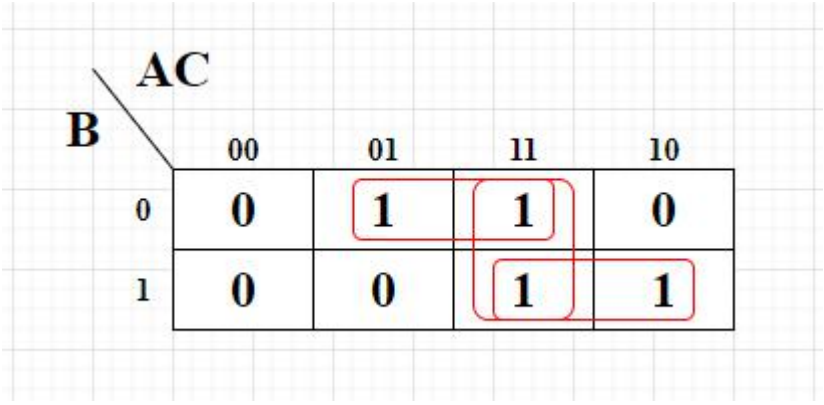
K-maps for Prelab PartA:



Truth Table for Prelab PartB:

A	B	C	Z
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

L-maps for Prelab PartB:

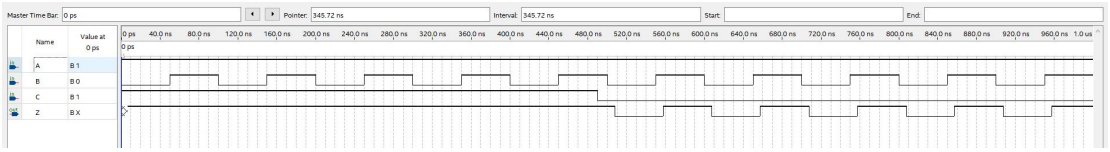


Prelab-Question:

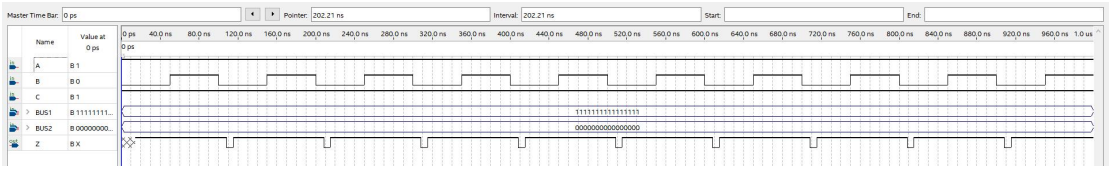
1. We do not observe the static hazard because the delay time caused by the inverter (one nand gate in this lab) is too short and the glitch will not happen.
2. When we add an odd numbers of inverters together inplace of the single inverter, we still no not observe the static hazard because the quartus will automaticly optimize the circuit to the simpliest, so the couples of inverters will be deleted when processing.

Simulation Result:

Prelab part A:

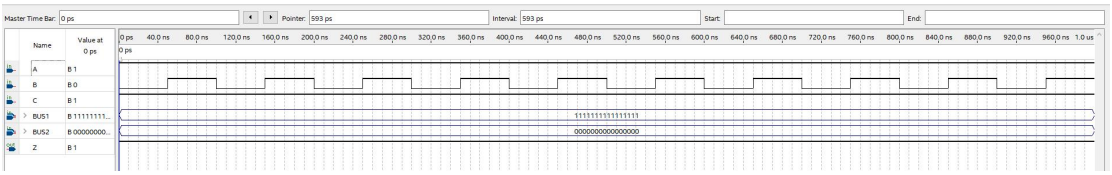


Lab Part 1:



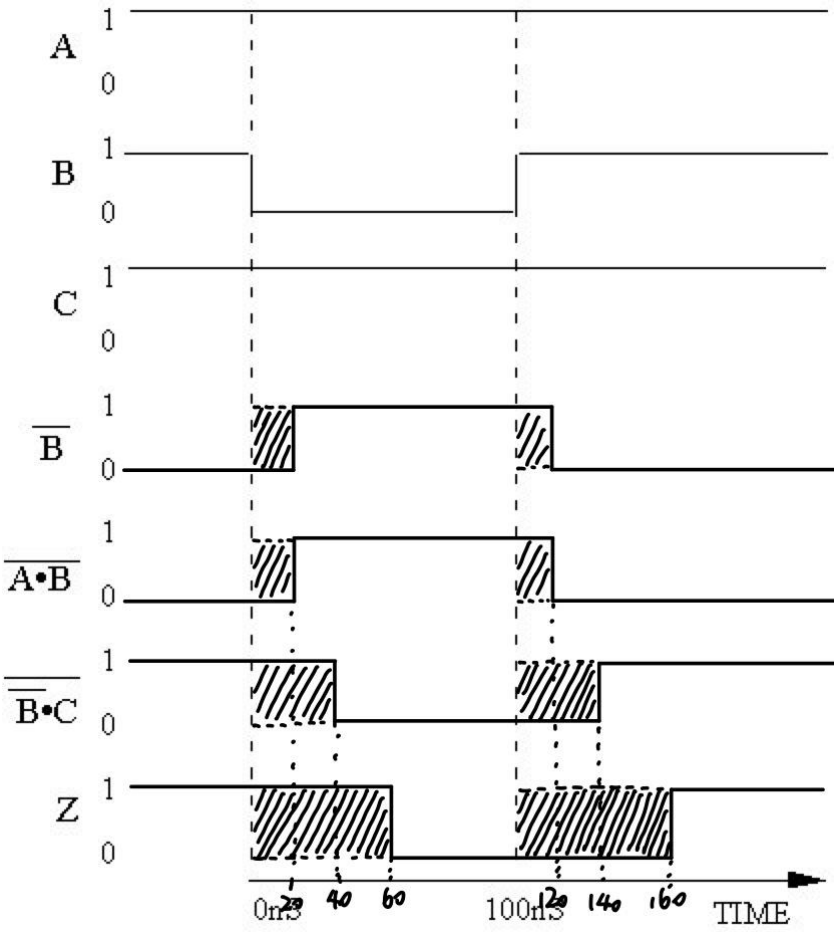
We can see the static hazard problem happens

Lab Part 2:



The hazard problem is solved by adding one more term.

Post-lab questions:



How long does it take the output Z to stabilize on the falling edge of B (in ns)? How long does it take on the rising edge (in ns)? Are there any potential glitches in the output, Z? If so, explain what makes these glitches occur.

It takes 60ns for Z to stabilize on the falling edge of B.

It takes 40ns for Z to stabilize on the rising edge of B.

There will be glitches in the output. Because when B changes from 1 to 0, (B'C)' will change from 1 to 0 20ns later than (AB)'. so in this 20ns, (B'C)' and (AB)' are both 1, so Z will be 0, which caused the glitches.

General Guide Questions:

GG.6

What is the advantage of a larger noise immunity?

The larger noise immunity can reduce the effect to circuit caused by the noise, which can greatly improve the success rate.

Why is the last inverter observed rather than simply the first?

For an inverter that touched the input, it needs to compress and integrate the voltage to get the expression of logic 0 and logic 1. If we only use one inverter to get the nominal 1 and 0, the result is not accurate enough.Because we know the high and low voltage level is a relative concept. In the reality, for an inverter that just touches the

input, it has less chance to access the nominal input. If the input is not nominal, the output is also not nominal. So we need to use the last inverter to ensure the correctness.

Given a graph of output voltage (VOUT) vs. input voltage (VIN) for an inverter, how would you calculate the noise immunity for the inverter?

We find that there are two value for the noise immunity. The first value is 0-input noise immunity t, it is (1.15-.35=0.8). The second one is 1-input, it is (3.5-1.35=2.15). Since 0.8<2.15, we need to choose the smaller one for the noise immunity, so we choose 0.8.

GG.29

If we have two or more LEDs to monitor several signals, why is it bad practice to share resistors?

The connection between LEDs and resistors is to reduce the current through the LEDs. If two or more LEDs share one resistor, the current through LEDs will reduce, the LED light will be dim, which may cause ambiguity. Moreover, the different LEDs have different internal resistances, the life of the diode will be affected because different LEDs have different current tolerance.

Conclusion:

In this lab, I learn deeply about the static hazard which is unclear in ECE120. We know why the static hazard will occur and its harm that may caused to circuit. Then I learn how to eliminate the static hazard by adding the prime term to the expression. I also learn how to use the new software Quartus and get the simulation result step by step. In building the analog circuit, we encountered no obvious obstacles.