FXDPHYRX420HH0L
UMC 40 nm Logic LP/RVT Low-K Process

MIPI D-PHY RECEIVER

Data Sheet
Rev.: 0.2
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REVISION HISTORY

FXDPHYRX420HH0L Data Sheet

Date	Rev.	From	To
Jul. 2014	0.1	-	Original
Nov. 2014	0.2	-	Updated the IP version to (0.2.1)

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Chapter 1

Introduction

This chapter contains the following sections:

1.1 Version of the IP

IP release version: 0.2.1

1.2 Features

- Compliant to MIPI Alliance Standard for D-PHY Specification, Ver. 1.0
- Compliant with MIPI alliance specification: CSI-2 version 1.01
- Supports unidirectional clock lane (As a slave)
- Supports HS-RX and LP-RX for clock lane
- Supports HS-RX and LP-RX for data lanes 0 ~ 3
- Supports High-Speed receiving mode with bit rate range from 80 Mb/s to 1000 Mb/s for both data lane and clock lane
- Supports Low-Power receiving mode with 10-Mb/s bit rate for data lanes 0 ~ 3
- Supports low-power receiving mode with 10-Mb/s bit rate for clock lane
- Supports ULPS for clock lane
- Supports Escape mode for all data lanes
- Supports one data lane and one clock lane or multiple data lanes and one clock lane
- Supports error detection mechanism
- Generates one divided down clock for parallel data reception
- Supports reception terminator to activate or inactivate high speed or low power
- Supports "FullPowerDown" feature to turn off entire PHY
- Supports I^2C and APB programmability for performance optimization and debugging
- Provides HS-mode and LP-mode BIST functions for MP test

1.3 Block Diagram

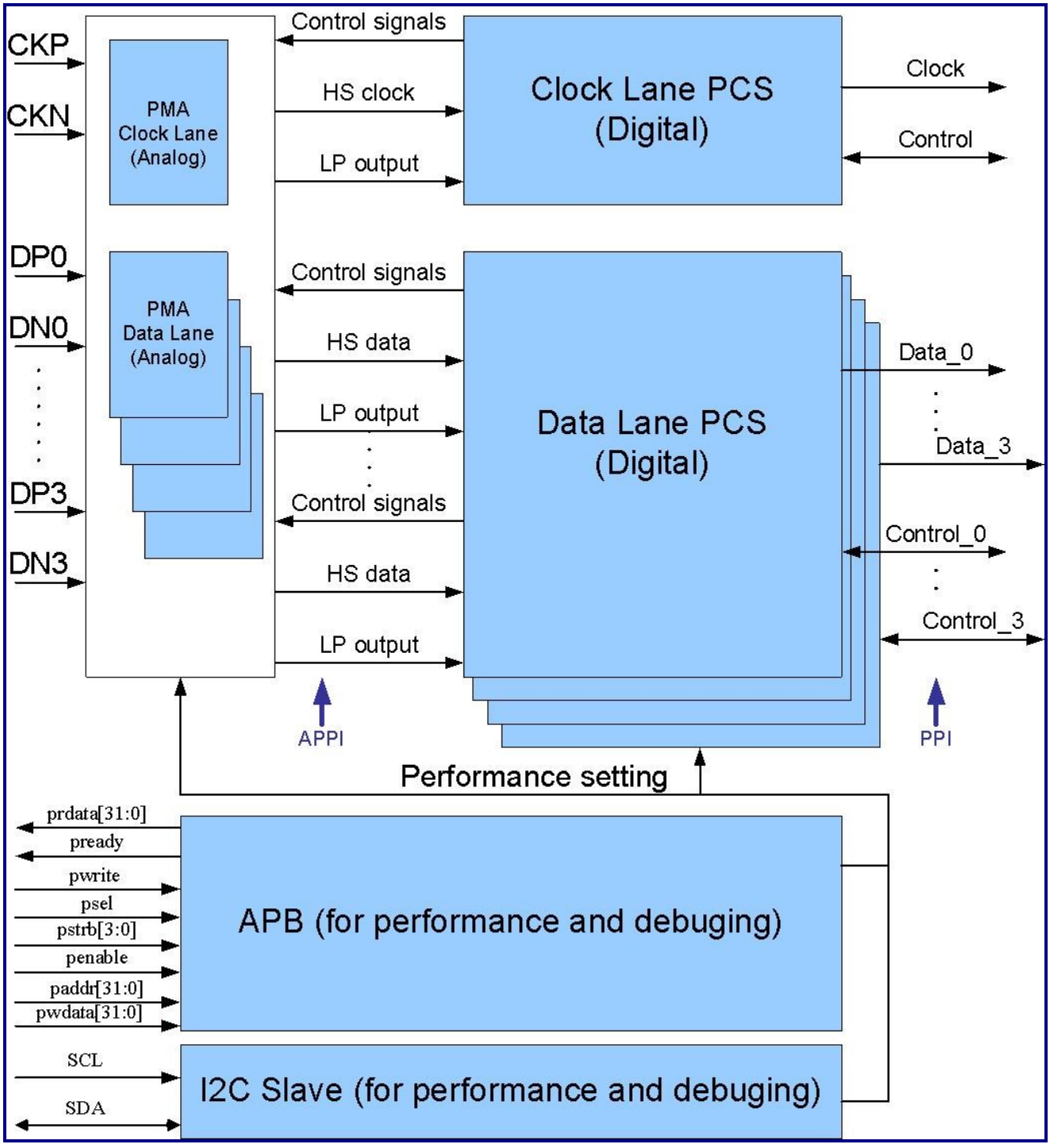

Figure 1-1. Block Diagram

1.4 Overview

This PHY provides a low-cost and high-speed serial interface solution for communication and interconnection between the components inside a mobile device. To achieve this function, this PHY integrates one High-Speed MIPI receiver, which supports up to 1.0 Gbps data reception and the Low-Power MIPI receiver. This PHY is integrated and has the PPI interface to interact with the controller. The designed architecture can support up to four data lanes.

Chapter 2

Signal Description

Table 2-1. Pin Descriptions for PPI Pins of Data Lane

Pin Name	I/O Type	Function	Note
DataLnEn0 DataLnEn1 DataLnEn2 DataLnEn3	Input	Enable data lane module Active high	-
DataForceRxmode0 DataForceRxmode1 DataForceRxmode2 DataForceRxmode3	Input	Force data lane module to enter the receive mode and wait for the stop state Active high	This signal is used during the initialization or to resolve a contention situation. When this signal is high, the lane module immediately transitions into the receive mode and waits for a stop state on the lane interconnect.
DataForceTxStopmode0	Input	Force data lane 0 module to enter the transmit mode and generate the stop state Active high	This signal allows the protocol to force a lane module to the transmit mode and stop state during initialization or following an error situation. If the transmitter mode is useless, DataForceTxStopmode0 should be tied to ‘b0.
DataTurnDisable0	Input	Disable turn-around for data lane 0 Active high	If the transmitter mode is useless, DataTurnDisable0 should be tied to ‘b1.
DataTurnRequest0	Input	Turn-around request for data lane 0 Active high	This signal is valid at the rising edge of TxClkEsc. DataTurnRequest0 is only meaningful for a lane module that is currently assigned as a transmitter. If the transmitter mode is useless, DataTurnRequest0 should be tied to ‘b0.

Pin Name	I/O Type	Function	Note
DataTxDataEsc0[7:0]	Input	Transmit data for data lane 0 in the Escape mode	This is the 8-bit Escape-mode data to be transmitted in the Low-Power data transmission mode. This signal, connected to DataTxDataEsc*[0], is transmitted first. Data are captured at the rising edge of TxClkEsc. If the transmitter mode is useless, DataTxDataEsc0 should be tied to ‘b0.
DataTxLpdtEsc0	Input	Transmit the low-power data for data lane 0 the in Escape mode Active high	This active-high signal asserts DataTxRequestEsc to force the lane module to enter the Low-Power data transmission mode. The lane module will remain in this mode until DataTxRequestEsc0 is de-asserted. If the transmitter mode is useless, DataTxLpdtEsc0 should be tied to ‘b0.
DataTxRequestEsc0	Input	Transmit request for data lane 0 in the Escape mode Active high	This active-high signal is used to request the entry of the Escape mode. Once in the Escape mode, the lane will stay in the Escape mode until DataTxRequestEsc is de-asserted. If the transmitter mode is useless, DataTxRequestEsc should be tied to ‘b0.
DataTxTriggerEsc0[3:0]	Input	Transmit triggers 0 ~ 3 for data lane 0 in the Escape mode Active high	This active-high signal asserts DataTxRequestEsc to send the associated trigger across the lane interconnect. This signal will assert only one bit of DataTxTriggerEsc at any given time when DataTxLpdtEsc, DataTxUndefEsc, and DataTxUlpsEsc are low. If the transmitter mode is useless, DataTxTriggerEsc0 should be tied to ‘b0.
DataTxUlpsEsc0	Input	Transmit the ULP state for data lane 0 in the Escape mode Active high	This active-high signal asserts DataTxRequestEsc to force the lane module to enter the ULP state. The lane module will remain in this mode until DataTxRequestEsc is de-asserted. If the transmitter mode is useless, DataTxUlpsEsc should be tied to ‘b0.
DataTxUlpsExit0	Input	Transmit the ULP exit sequence for data lane 0 Active high	This active-high signal is asserted when the ULP state is active and protocol is ready to exit from the ULP state. If the transmitter mode is useless, DataTxUlpsExit should be tied to ‘b0.
DataTxUndefEsc0[1:0]	Input	Transmit the undefined states 1 ~ 0 for data lane 0 in the Escape mode Active high	This active-high signal asserts DataTxRequestEsc to send the associated undefined across the lane interconnect. This signal asserts only one bit of DataTxUndefEsc* at any given time when DataTxLpdtEsc, DataTxTriggerEsc, and DataTxUlpsEsc are low. If the transmitter mode is useless, DataTxUndefEsc0 should be tied to ‘b0.
DataTxValidEsc0	Input	Transmit data valid for data lane 0 in Escape mode Active high	This active-high signal uses protocol to transmit the driving valid data on DataTxDataEsc*. The lane module accepts data when DataTxRequestEsc, DataTxVaildEsc, and DataTxReadyEsc are active at the same rising edge of the TxClkEsc clock. If the transmitter mode is useless, DataTxValidEsc should be tied to ‘b0.

Pin Name	I/O Type	Function	Note
DataLaneReady0 DataLaneReady1 DataLaneReady2 DataLaneReady3	Output	Data lane module is ready after the initialization. Active high	This is a non-PPI signal and only for reference.
RxByteClkHS	Output	The high-speed receive byte clock is used to synchronize signals in the high-speed receive clock domain.	This clock is generated by dividing the received HS DDR clock.
DataRxDataHs0[7:0] DataRxDataHs1[7:0] DataRxDataHs2[7:0] DataRxDataHs3[7:0]	Output	8-bit high-speed receive data	The signal, DataRxDataHs*[0], is received first. Data are transferred at the rising edges of RxByteClkHS.
DataRxValidHs0 DataRxValidHs1 DataRxValidHs2 DataRxValidHs3	Output	High-speed receive data valid Active high	This active-high uses the lane module to drive data to the protocol layer on the DataRxDataHs* output. This signal is transferred at the rising edge of RxByteClkHS. This signal will be asserted once the HS data are valid. It will be de-asserted after the last valid HS data if the master side does not perform the EOT process.
DataRxActiveHS0 DataRxActiveHS1 DataRxActiveHS2 DataRxActiveHS3	Output	Active high-speed reception Active high	This active-high signal indicates that the lane module is actively receiving a high-speed transmission from the lane interconnect. This signal is transferred at the rising edge of RxByteClkHS.
DataRxSyncHS0 DataRxSyncHS1 DataRxSyncHS2 DataRxSyncHS3	Output	Receiver synchronization observed Active high	This active-high signal indicates that the lane module has detected an appropriate synchronization event. In a high-speed transmission, this signal will be high for one RxByteClkHS cycle at the beginning of a high-speed transmission when DataRxActiveHS* is first asserted. This signal is transferred at the rising edge of RxByteClkHS.
DataRxClkEsc0 DataRxClkEsc1 DataRxClkEsc2 DataRxClkEsc3	Output	Receive clock in the Escape mode	This signal is used to transfer the received data to the protocol layer in the Escape mode. This clock may not be periodic.
DataRxLpdtEsc0 DataRxLpdtEsc1 DataRxLpdtEsc2 DataRxLpdtEsc3	Output	Escape low-power data receive mode Active high	This active-high signal is asserted to indicate that the lane module is in the low-power data receive mode.

Pin Name	I/O Type	Function	Note
DataRxUlpsEsc0 DataRxUlpsEsc1 DataRxUlpsEsc2 DataRxUlpsEsc3	Output	Escape ultra-low-power mode Active high	This active-high signal is asserted to indicate that he lane module has entered the ultra-low-power state. The lane module remains in this mode when DataRxUlpsEsc* is asserted until a STOP state is detected on the lane interconnect. This signal is asynchronous to any clock on the PPI interface.
DataRxTriggerEsc0[3:0] DataRxTriggerEsc1[3:0] DataRxTriggerEsc2[3:0] DataRxTriggerEsc3[3:0]	Output	Receive triggers 0 ~ 3 in the Escape mode Active high	An active-high signal indicates that a trigger event has been received.
DataRxUndefEsc0[1:0] DataRxUndefEsc1[1:0] DataRxUndefEsc2[1:0] DataRxUndefEsc3[1:0]	Output	Receive undefined event in the Escape mode Active high	The active-high signal indicates that an undefined event has been received.
DataRxUlpsActiveNot0 DataRxUlpsActiveNot1 DataRxUlpsActiveNot2 DataRxUlpsActiveNot3	Output	ULP state Active low 1'b1: Not at the ULP state 1'b0: At the ULP state	This active-low signal is asserted to indicate that the data lane is at the ULP state. This signal becomes inactive to indicate that the Mark-1 state has been observed.
DataRxDataEsc0[7:0] DataRxDataEsc1[7:0] DataRxDataEsc2[7:0] DataRxDataEsc3[7:0]	Output	Receive data in the Escape mode	This is the 8-bit Low-Power data received by the lane module in the Escape mode. The signal, connected to DataRxDataEsc*[0], will be received first. Data are synchronous to the rising edges of DataRxClkEsc*.
DataRxValidEsc0 DataRxValidEsc1 DataRxValidEsc2 DataRxValidEsc3	Output	Receive data valid in the Escape mode Active high	This active-high signal indicates that the lane module is driving valid data to the protocol layer on the DataRxDataEsc* output.
DataTxReadyEsc0	Output	Transmit ready in the Escape mode Active high	This active-high signal indicates that DataTxDataEsc* is accepted by the lane module to be serially transmitted. DataTxReadyEsc* is valid at the rising edges of TxClkEsc. If the transmitter mode is useless, DataTxReadyEsc0 could be floating.
DataTxUlpsActiveNot0	Output	Data lane TX at the ULP state Active low	This active-low signal is asserted to indicate that the lane is at the ULP state. This signal will be asserted after DataTxUlpsEsc and DataTxRequestEsc are asserted. To exit from the ULP state, the transmitter needs to drive DataTxUlpsExit high then wait for DataTxUlpsActiveNot high. At this point, the transmitting PHY is active and starts transmitting Mark-1 on the lane. The protocol waits for a wake-up time, T_{weakup}, and inactivates DataTxRequestEsc to return the lane to the Stop state. If the transmitter mode is useless, DataTxUlpsActiveNot0 could be floating.

Pin Name	I/O Type	Function	Note
DataStopState0 DataStopState1 DataStopState2 DataStopState3	Output	Data lane at the STOP state Active high	This active-high signal indicates that the lane module is currently at the STOP state. This signal is asynchronous to any clock on the PPI interface.
DirectionD0 DirectionD1 DirectionD2 DirectionD3	Output	Data lane transmit/receive direction 1'b1: Input direction 1'b0: Output direction	This signal indicates the direction of data lane interconnect. When DirectionD* = '0', the lane is in the transmit mode. When DirectionD* = '1', the lane is in the receive mode.
DataErrSotHS0 DataErrSotHS1 DataErrSotHS2 DataErrSotHS3	Output	Start-of-Transmission (SOT) error Active high	If the High-Speed SOT leader sequence is corrupted and proper synchronization can still be achieved, this active-high signal will be asserted for one RxByteClkHS cycle. This is considered to be a "soft error" in the leader sequence and the payload data will be reduced. This signal is transferred at the rising edge of RxByteClkHS.
DataErrSotSyncHS0 DataErrSotSyncHS1 DataErrSotSyncHS2 DataErrSotSyncHS3	Output	Start-of-Transmission synchronization error Active High	If the High-Speed SOT leader sequence is corrupted and proper synchronization cannot be expected, this active-high signal will be asserted for one RxByteClkHS cycle. This signal is transferred at the rising edge of RxByteClkHS.
DataErrEsc0 DataErrEsc1 DataErrEsc2 DataErrEsc3	Output	Escape entry error Active high	If an unrecognized escape entry command is received, this active-high signal will be asserted and will remain asserted until changing to the next line state. This signal is asynchronous to any clock on the PPI interface.
DataErrSyncEsc0 DataErrSyncEsc1 DataErrSyncEsc2 DataErrSyncEsc3	Output	Low-power data transmission synchronization error Active high	If the bits received during a Low-Power data transmission are not multiples of 8 when the transmission ends, this active-high signal will be asserted and will remain asserted until changing to the line state.
DataErrControl0 DataErrControl1 DataErrControl2 DataErrControl3	Output	Control error Active high	This active-high signal will be asserted when an incorrect line state sequence is detected. For example, if an Escape-mode request is immediately followed by a STOP state instead of the required Bridge state, this signal will be asserted and will remain asserted until changing to the line state. This signal is asynchronous to any clock on the PPI interface.
DataErrContenLP00 DataErrContenLP10 DataErrContenLP20 DataErrContenLP30	Output	LP0 contention error Active high	This active-high signal will be asserted when the data lane module detects a contention situation on a line when trying to drive the line low.

Pin Name	I/O Type	Function	Note
DataErrContenLP01 DataErrContenLP11 DataErrContenLP21 DataErrContenLP31	Output	LP1 contention error Active high	This active-high signal will be asserted when the data lane module detects a contention situation on a line when trying to drive the line high.

Table 2-2. Pin Descriptions for PPI Pins of Clock Lane

Pin Name	Direction	Function	Note
ClkLnEn	Input	Enable clk lane module Active high	-
TxEscClk	Input	Fixed 20-MHz input clock	This clock is used to directly generate the TX Escape sequence and handle other functions. This clock must be alive even D-PHY is in the receiving direction. Otherwise, the entire D-PHY will be at the ULP state or “FULLPOWERDOWN” state.
ClkForceRxmode	Input	Force clock lane module to enter the receive mode and wait for the stop state Active high	This signal is used during the initialization or to resolve a contention situation. When this signal is high, the lane module immediately transitions into the receive mode and waits for a stop state on the lane interconnect.
ClkLaneReady	Output	The clk lane module is ready after the initialization. Active high	This is a non-PPI signal and can only be as reference.
RxClkActiveHS	Output	High-speed receiver clock Active high	This active-high signal indicates that a clock lane is receiving a DDR high-speed clock signal. This signal is asynchronous to any clock on the PPI interface.
RxUlpsClkNot	Output	Receive ultra-low-power state on clock lane Active low	This active-low signal is asserted to indicate that the clock lane has entered the ultra-low-power state. The clock lane remains at ULPS with asserted RxUlpsClkNot until a STOP state is detected on the lane interconnect. This signal is asynchronous to any clock on the PPI interface.
ClkRxUlpsActiveNot	Output	ULP state Active low 1’b1: Not at the ULP state 1’b0: At the ULP state	This active-low signal is asserted to indicate that the clk lane is at the ULP state. This signal becomes inactive to indicate that the Mark-1 state has been observed.

Pin Name	Direction	Function	Note
DirectionCk	Output	Current direction of clk lane module 1'b1: Input mode (RX) 1'b0: Output mode (TX)	-
ClkStopState	Output	Clk lane module at STOP state Active high	This active-high signal indicates that the clk lane module is currently at the STOP state. This signal is asynchronous to any clock in the PPI interface.

Table 2-3. PPI Pin List of the General Purpose

Pin Name	Direction	Function	Note
ResetN	Input	Reset PHY Active low	This signal resets PHY, except for the I^2C module.
PORn	Input	Reset the I^2C module Active low	This signal resets the entire PHY, including the I^2C module.
Master	Input	IP plays as a master. Active high	Please set to 1'b0 for this IP (As a slave mode).
Enable	Input	Enable IP Active high	1'b1: Enable IP 1'b0: For IDDQ or a state which needs the lowest power consumption (Full power-down mode)
ModeSel[4:0]	Input	Select the operation mode of D-PHY	5'b00000: Normal mode 5'b00001: HiSpi mode 5'b00010: CD Pass Through mode 5'b00011: FpgaSyncEsc 5'b00100: FpgaSyncHs 5'b00101: LvdsMode 5'b00110: SubLvdsMode 5'b00111: PMA mux-out for normal mode (Only available if PMA mux-out module is added.) 5'b01000: PMA mux-out for HiSpi mode (Only available if PMA mux-out module is added.) 5'b01001: PMA mux-out for LVDS mode (Only available if PMA mux-out module is added.) 5'b01010: PMA mux-out for Sub LVDS mode (Only available if PMA mux-out module is added.) 5'b10000: Force at TX + LP-TX 11 + NonStop 5'b10001: Force at TX + LP-TX 00 + NonStop

Pin Name	Direction	Function	Note
			5'b10010: HS-TX 1 + NonStop 5'b10011: HS-TX 0 + NonStop 5'b11001: HSDT with bypassing lane initilization 5'b10100: LPDT BIST test It needs TXDPHY and RXDPHY for performing this test. TXDPHY will generate and transmit the PRBS pattern to RXDPHY in the LPDT mode. RXDPHY will compare the received pattern until the end. Both TXDPHY and RXDPHY have to be set in this mode. 5'b10101: HSDT BIST test It needs TXDPHY and RXDPHY for performing this test. TXDPHY will generate and transmit the PRBS pattern to RXDPHY in the HSDT mode. RXDPHY will compare the received pattern until the end. Both TXDPHY and RXDPHY have to be set in this mode. 5'b10110: TA+LPDT+TA This mode is used to test DPHY turnaround and LPDT functions. It needs Faraday TXDPHY and RXDPHY. Both PHYs have to be set to this mode. 5'b10111: LPDT BIST test (Non-stop) It needs TXDPHY and RXDPHY for performing this test. TXDPHY will generate and transmit the PRBS pattern to RXDPHY in the LPDT mode. RXDPHY will compare the received pattern. Both TXDPHY and RXDPHY have to be set in this mode 5'b11000: HSDT BIST test (Non-stop) It needs TXDPHY and RXDPHY for performing this test. TXDPHY will generate and transmit the PRBS pattern to RXDPHY in the HSDT mode. RXDPHY will compare the received pattern. Both TXDPHY and RXDPHY have to be set in this mode.
SlvScl	Input	I^2C SCL clock input	This signal is used to perform the optimization and debugging. SlvScl is the I^2C serial-data clock.
SlvSda_in	Input	I^2C SDA data input	This signal is used to perform the optimization and debugging. SlvSda_in is the I^2C serial-data.
SlvI2CslaveAdd0 SlvI2CslaveAdd1 SlvI2CslaveAdd2 SlvI2CslaveAdd3 SlvI2CslaveAdd4 SlvI2CslaveAdd5 SlvI2CslaveAdd6	Input	I^2C slave address	This signal is used to perform the optimization and debugging. SlvI2CslaveAdd is the I^2C device address of the IP.
SlvSda_oe	Output	I^2C SDA output control	This signal is used to perform the optimization and debugging. SlvSda_oe is the I^2C direction control.

Pin Name	Direction	Function	Note
I2c_Apb	Input	Select the vendor-controlled input source 1'b0: Internal source (From APB register) is selected. 1'b1: Internal source (From I^2C register) is selected.	This IP provides two vendor-controlled options. One option comes from APB. The other option comes from the internal I^2C. I2c_Apb is used to select the option.
I2cApbClk	Input	Main clock for I^2C and APB	This clock is used to be the main clock for I^2C and APB.
pwrite	Input	APB direction signal	This signal indicates an APB write access when HIGH and an APB read access when LOW.
psel	Input	APB select signal	The APB bridge unit generates this signal to each peripheral bus slave. It indicates that the slave device is selected and a data transfer is required.
pstrb[3:0]	Input	APB write strobes	This signal is used to update the byte lanes during a write transfer. There is one write strobe for each eight bits of the write data bus. Therefore, pstrb **[n]** corresponds to pwdata **[(8n + 7):(8n)]**. Write strobes must not be active during a read transfer.
penable	Input	APB enable signal	This signal indicates the second and subsequent cycles of an APB transfer.
paddr[31:0]	Input	APB address	This is the APB address bus. It can be up to 32 bits wide and is driven by the peripheral bus bridge unit.
pwdata[31:0]	Input	APB write data	This bus is driven by the peripheral bus bridge unit during write cycles when pwrite is HIGH. This bus can be up to 32 bits wide.
prdata[31:0]	Output	APB read Data	The selected slave drives this bus during read cycles when pwrite is LOW. This bus can be up to 32-bits wide.
pready	Output	APB ready signal	The slave uses this signal to extend an APB transfer.
DebugOutPort[7:0]	Output	For debugging purpose	Please mux out this bus for the future debugging purpose.

Table 2-4. Analog Pad List

Pin Name	I/O Type	Function	Note
CKP	Input	Differential clock lane +	-
CKN	Input	Differential clock lane -	-
DP0	Input	Differential data lane 0 +	-
DN0	Input	Differential data lane 0 -	-
DP1	Input	Differential data lane 1 +	-
DN1	Input	Differential data lane 1 -	-

Pin Name	I/O Type	Function	Note
DP2	Input	Differential data lane 2 +	-
DN2	Input	Differential data lane 2 -	-
DP3	Input	Differential data lane 3 +	-
DN3	Input	Differential data lane 3 -	-
RBIAS	Bidirectional	For BIAS	-

Table 2-5. Power and Ground Pad/Pin List

Pin Name	I/O Type	Function	Note
VCC11A	Input	1.1-V analog power	This is a pad.
GND11A	Input	Analog ground	This is a pad.
VCC11K	Input	1.1-V digital core power	This is a pin.
GND11K	Input	Digital core ground	This is a pin.
VCC25A	Input	2.5-V or 3.3-V analog power	This is a pad.

Table 2-6. BIST Test

Pin Name	Direction	Function	Note
ModeSel[4:0]	Input	5'b10100 → LPDT 5'b10101 → HSDT	Please mux out this signal.
TS_TestDone0 TS_TestDone1 TS_TestDone2 TS_TestDone3	Output	For data-lane TX/RX BIST test For TX (HS or LPDT), this signal will be asserted if D-PHY completes transmitting the desired pattern length to the other side. For RX (HS or LPDT), this signal will be asserted if D-PHY completes receiving the desired pattern length from the other side.	Please mux out this signal.
TS_TestPass0 TS_TestPass1 TS_TestPass2 TS_TestPass3	Output	For data-lane RX BIST test only This signal will be asserted when the RX BIST test starts. However, if it is de-asserted during the test, the received data cannot match the expected data.	Please mux out this signal.
TS_TestDone_Ck	Output	For clock lane timing check between PHY and the controller	Please mux out this signal for the future mass production test.

Pin Name	Direction	Function	Note
TS_TestPass_Ck	Output	For clock lane timing check between PHY and the controller	Please mux out this signal for the future mass production test.
PORn	Input	Reset the I^2C and APB modules Active low	Please mux out this signal.
ResetN	Input	Reset PHY Active low	Please mux out this signal.
TC_RESET	Input	Reset TCB Set to “Low” to enter the DFT mode Set to “High” to enter the normal mode	Please mux out this signal or set as 1’b1.
Enable	Input	Enable the IP Active high	Please mux out this signal.
TxEscClk	Input	Fixed 20-MHz input clock	Please mux out this signal.
ClkLnEn	Input	Enable the clock lane module Active high	Please mux out this signal or set as 1’b1.
DataLnEn0 DataLnEn1 DataLnEn2 DataLnEn3	Input	Enable the data lane module Active high	Please mux out this signal or set as 4’b1111.
DirectionCk	Output	Current direction of the clock lane module 1’b1: Input mode (RX) 1’b0: Output mode (TX)	Please mux out this signal.
ClkStopState	Output	Clock lane is at the Stop state. Active high	Please mux out this signal.
DirectionD0 DirectionD1 DirectionD2 DirectionD3	Output	Transmit/Receive direction of data lane 1’b1: Input direction 1’b0: Output direction	Please mux out this signal.
DataStopState0 DataStopState1 DataStopState2 DataStopState3	Output	Data lane is at the Stop state. Active high	Please mux out this signal.

Pin Name	Direction	Function	Note
ClkLaneReady	Output	The clock lane module is ready after initialization. Active high	Please mux out this signal.
DataLaneReady0 DataLaneReady1 DataLaneReady2 DataLaneReady3	Output	Data lane module is ready after initialization. Active high	Please mux out this signal.
Master	Input	IP acts as a master. Active high	Please mux out this signal.

Table 2-7. ATPG Test

Pin Name	Direction	Function	Note
VC_SI[3:0]	Input	Scan inputs for the scan chains inside this IP Set to '0' to enter the normal mode	-
TCLK	Input	Test clock for TCB Set to '0' to enter the normal mode	-
TC_RESET	Input	Reset TCB Set to "Low" to enter the DFT mode Set to "High" to enter the normal mode	-
TC_SHIFT	Input	Shift enable for the shift registers inside TCB Set to '0' to enter the normal mode	-
TC_SI	Input	Scan input of TCB Set to '0' to enter the normal mode	-
TC_UPDATE	Input	Update enable for the shift registers inside TCB Set to '0' to enter the normal mode	-
TEST_CLK	Input	Test clock for the scan chains Set to '0' to enter the normal mode	-
TEST_RST	Input	Test reset for the scan chains Set to '0' to enter the normal mode	-
VC_SHIFT	Input	Shift enable for the shift registers of the scan chains inside this IP and the wrapper registers Set to '0' to enter the normal mode	-
WP_CLK	Input	Test clock for the wrapper register Set to '0' to enter the normal mode	-
WP_SI	Input	Scan input for the wrapper register Set to '0' to enter the normal mode	

Pin Name	Direction	Function	Note
VC_SO[3:0]	Output	Scan output for the scan chains inside this IP	
TC_SO	Output	Scan output of TCB	
WP_SO	Output	Scan output for the wrapper register	

Chapter 3

Electrical Specification

Table 3-1. DC Electrical Characteristics of HS Receiver

Parameter	Description	Min.	Typ.	Max.	Unit	Note
$V_{CMRX(DC)}$	Common-mode voltage in the HS receive mode	70	-	330	mV	1, 2
V_{IDTH}	Differential input high threshold	-	-	70	mV	-
V_{IDTL}	Differential input low threshold	-70	-	-	mV	-
V_{IHHS}	Single-ended input high voltage	-	-	460	mV	1
V_{ILHS}	Single-ended input low voltage	-40	-	-	-	1
$V_{TERM-EN}$	Single-ended threshold for the HS termination enable	-	-	450	mV	-
Z_{ID}	Differential input impedance	80	100	125	Ω	-

Notes:

1. The values listed exclude the possible additional RF interference of 100-mV peak sine wave beyond 450 MHz.
2. The values listed include a ground difference of 50-mV between the transmitter and the receiver, the static common-mode level tolerance and variations below 450 MHz.

Table 3-2. AC Electrical Characteristics of HS Receiver

Parameter	Description	Min	Nom	Max	Units	Note
$\Delta V_{CMRX(HF)}$	Common-mode interference beyond 450 MHz	-	-	100	mV	2
$\Delta V_{CMRX(LF)}$	Common-mode interference beyond 50 MHz ~ 450 MHz	-50	-	50	mV	1
C_{CM}	Common-mode termination	-	-	60	pF	3

Notes:

1. The values listed exclude the "static" ground shift of 50 mV.
2. $\Delta V_{CMRX(HF)}$ is the peak amplitude of a sine wave superimposed on the receiver inputs.
3. For higher bit rates, a 14-pF capacitor is needed to meet the common-mode return loss specification.

Table 3-3. DC Electrical Characteristics of LP Receiver

Parameter	Description	Min.	Typ.	Max.	Unit	Note
V_{IH}	Logic 1 input voltage	880	-	-	mV	-
V_{IL}	Logic 0 input voltage not at the ULP state	-	-	550	mV	-
$V_{IL-ULPS}$	Logic 0 input voltage at the ULP state	-	-	300	mV	-
V_{HYST}	Input hysteresis	25	-	-	mV	-

Table 3-4. AC Electrical Characteristics of LP Receiver

Parameter	Description	Min.	Typ.	Max.	Unit	Note
e_{SPIKE}	Input pulse rejection	-	-	300	Vps	1, 2, 3
T_{MIN-RX}	Minimum pulse width response	20	-	-	ns	4
V_{INT}	Peak interference amplitude	-	-	200	mV	-
f_{INT}	Interference frequency	450	-	-	MHz	-

Notes:

1. Time-voltage integration of a spike will be above V_{IL} when being the LP-0 state or below V_{IH} when being the LP-1 state.
2. An impulse less than this value will not change the receiver state.
3. In addition to the required glitch rejection, implementers must ensure the rejection of known RF-interferers.
4. An input pulse greater than this value must toggle the output.

Chapter 4

Function Description

This chapter contains the following sections:

4.1 Architecture

This section covers the basic structure and function operations of this PHY so that users can utilize this PHY to achieve the MIPI system communication.

4.1.1 Lane Module

This PHY contains one clock lane module and one or more data lane modules. Each lane module can communicate with the link partner via two lines (P and N).

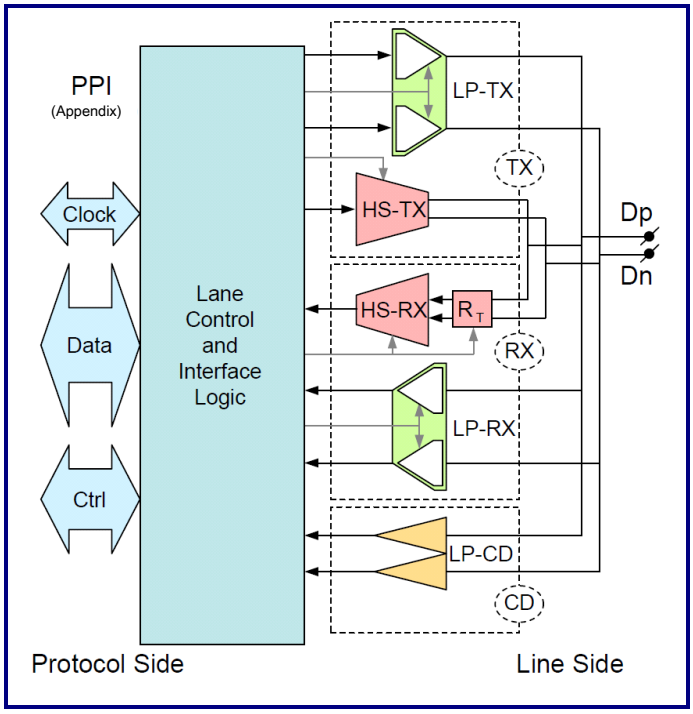

Figure 4-1. General Concept of Functional Block Diagram of Lane Module

Basically, each lane module consists of one or more differential High-Speed functions utilizing the P and N differential lines, one or more single-ended Low-Power functions, and control interface. The High-Speed functions are used for the High-Speed data transmission and the Low-Power functions are mainly used for control or other optional cases. The I/O functions are controlled by a lane control interface logic block. This block interfaces with the protocol and decides the option of the lane module. Please note that the functional block diagram shown in Figure 4-1 is a general concept. However, this IP does not support HS-TX and LP-TX due to the market consideration.

4.1.2 Master and Slave

Each link has the master and slave sides. The master side provides the High-Speed DDR clock to slave side through the clock lane as well as the High-Speed data through the data lanes. Thus, the slave side can utilize the received DDR clock to sample the received High-Speed data for the data transmission between the master and slave sides.

4.1.3 Clock Lane, Data Lanes, and PHY Protocol Interface

The logic PHY Protocol Interface (PPI) for each lane includes a set of signals to cover the functionality of that lane so that the protocol layer can control or access PHY through the PPI interface.

4.2 Global Operation

4.2.1 Lane States and Line Levels

During the normal operation, a HS-TX or a LP-TX is used to drive a lane. A HS-TX always differentially drives the lane. Two LP-TXs independently drive two lines of a lane and the single-ended results are at two possible high-speed lane states and four possible low-power lane states. The high-speed lane states are Differential-0 and Differential-1. The interpretation of the low-power lane states depends on the operation mode. The LP receivers must always interpret both high-speed differential states as LP-00. Transmitter functions determine the lane state by driving certain line levels.

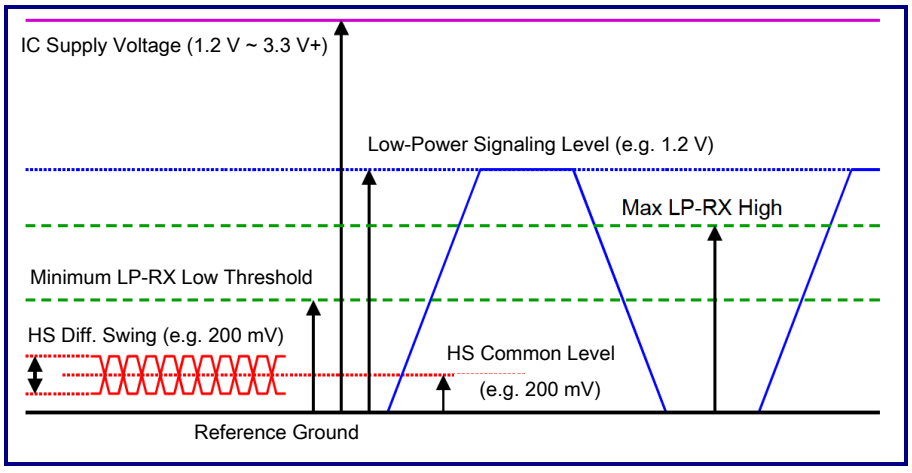

Figure 4-2. Land States and Line Levels

Table 4-1. Line State Settings

State Code	Line Voltage Level		High-speed	Low-power	
	Dp-LIne	Dn-Line	Burst Mode	Control Mode	Escape Mode
HS-0	HS Low	HS High	Differential-0	N/A, Note1	N/A, Note1
HS-1	HS High	HS Low	Differential-1	N/A, Note1	N/A, Note1
LP-00	LP Low	LP Low	N/A	Bridge	Space
LP-01	LP Low	LP High	N/A	HS-Rqst	Mark-0
LP-10	LP High	LP Low	N/A	LP-Rqst	Mark-1
LP-11	LP High	LP High	N/A	Stop	N/A, Note2

Table 4-1 lists all states that appear on a lane during the normal operation. A clock signal in the Low-Power mode can be reconstructed by exclusive-ORing the DP and DN lines.

4.2.2 Operation Modes of Control, High-Speed, and Escape

During the normal operation, a data lane will be in the Control or High-Speed mode. The sigh-speed data transmission happens in bursts and will start from/end to at the Stop state (LP-11), which is by definition in the Control mode. The lane can only be in the High-Speed mode during data bursts. The Escape mode can only be entered via a request within the Control mode. If not in the High-Speed or Escape mode, the data lane must stay in the Control mode. The possible events starting from the Stop state are the high-speed data transmission request, Escape mode request, or Turnaround request.

4.2.2.1 Global Operation Flow Diagram

Figure 4-3 shows the operational flow diagram for a data lane module. In both TX and RX, four main processes can be distinguished: High-Speed Transmission, Escape mode, Turnaround, and Initialization.

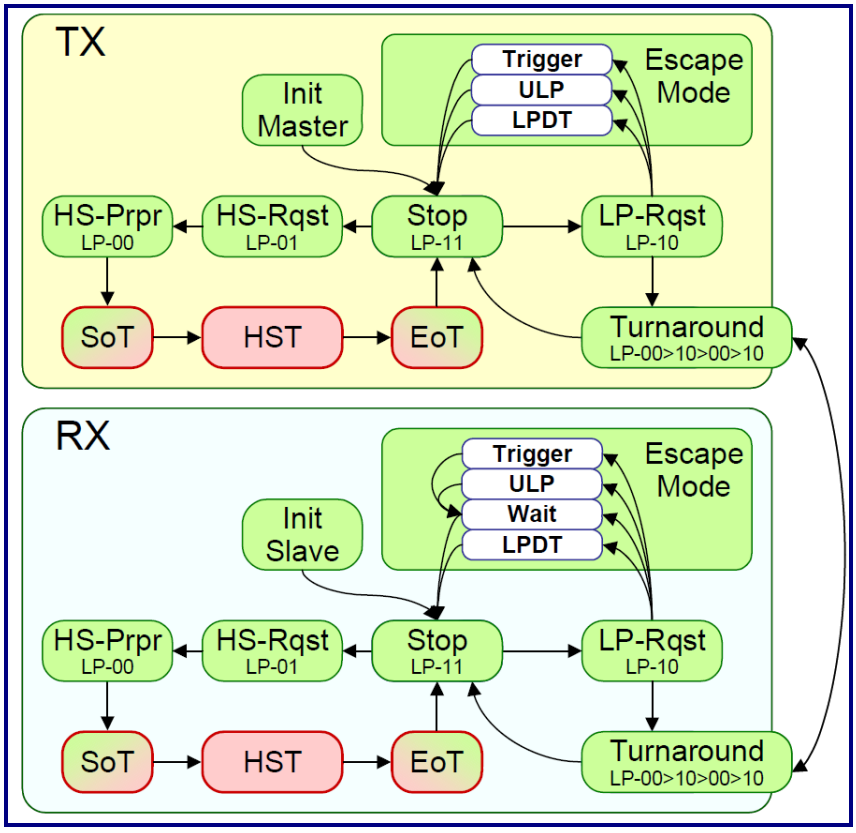

Figure 4-3. Operational Flow Diagram of Data Lane Module

Figure 4-4 shows the state diagram for a clock lane module. The clock lane module has four major operational states: Initialization, Low-Power Stop state, Ultra-Low Power state, and High-Speed clock transmission.

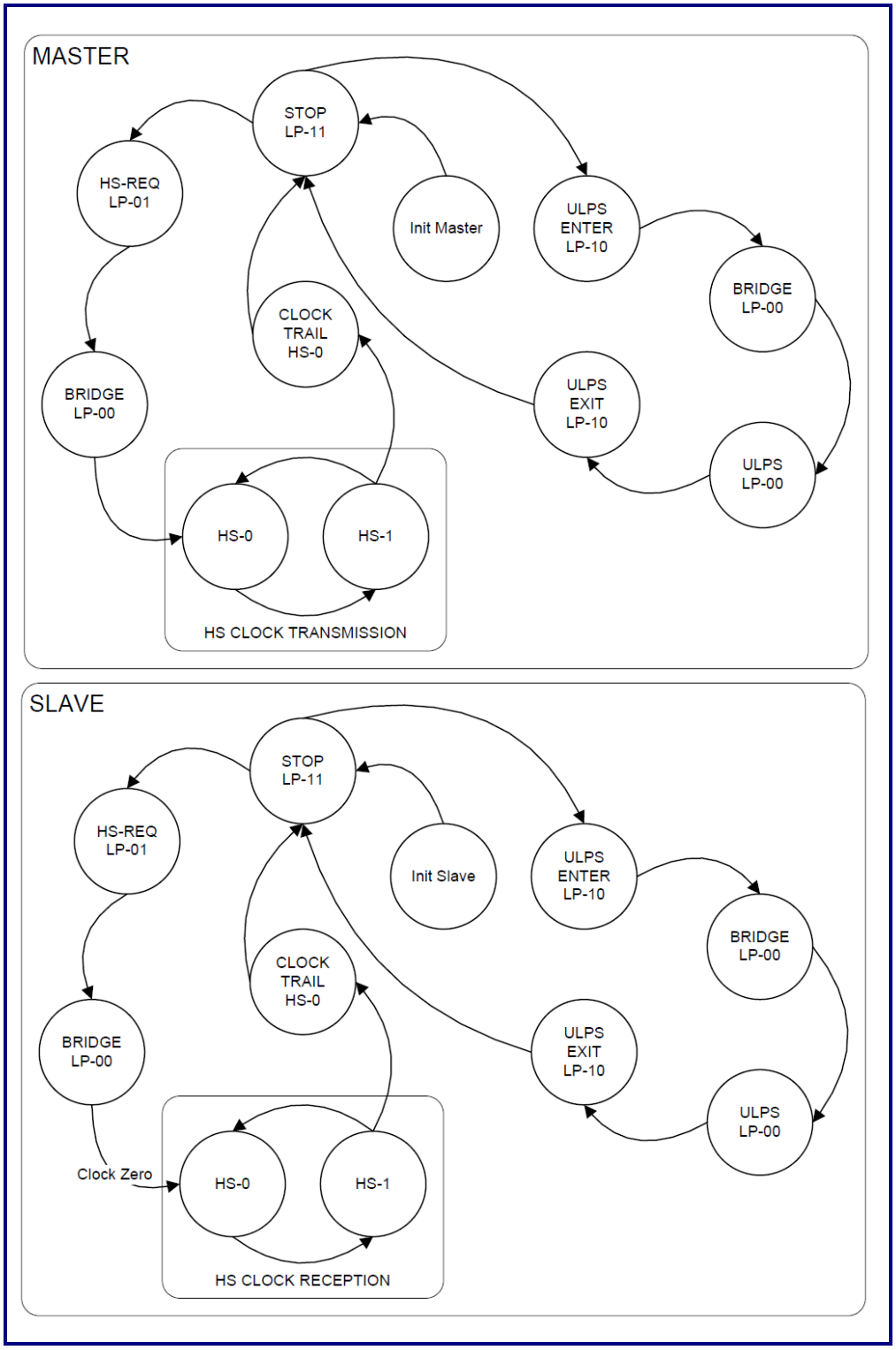

Figure 4-4. State Diagram of Clock Lane Module

4.2.2.2 HS Clock and Data Transmission

A clock lane is similar to a unidirectional data lane. However, there are some timing differences and a clock lane transmits a high-speed DDR clock signal instead of the data bits. Furthermore, the low-power mode functionality is defined differently for a clock lane than a data lane. A clock lane has to be unidirectional and must not include the regular Escape-mode functionality. Only ULPS has to be supported via a special entry sequence using the LP-Rqst state. The high-speed clock transmission must start from and exit to a Stop state. The clock lane module is controlled by the protocol via the clock lane PPI.

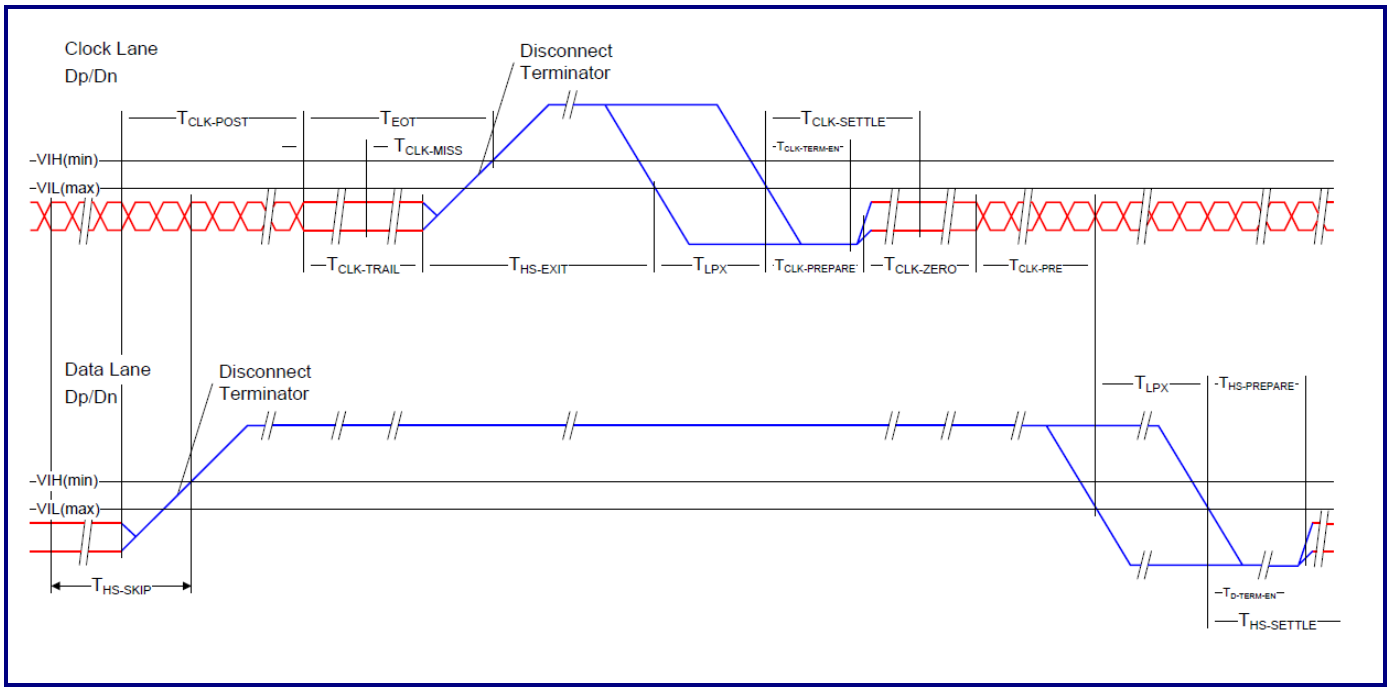

Figure 4-5. Switching Clock Lane between Clock Transmission and Low-Power Mode

Figure 4-6 shows the sequence of events during the transmission of a data burst. Transmission can be independently started and ended for any lane by the protocol. However, for most applications, the lanes will start synchronously but may end at different times due to an unequal amount of transmitted bytes per lane.

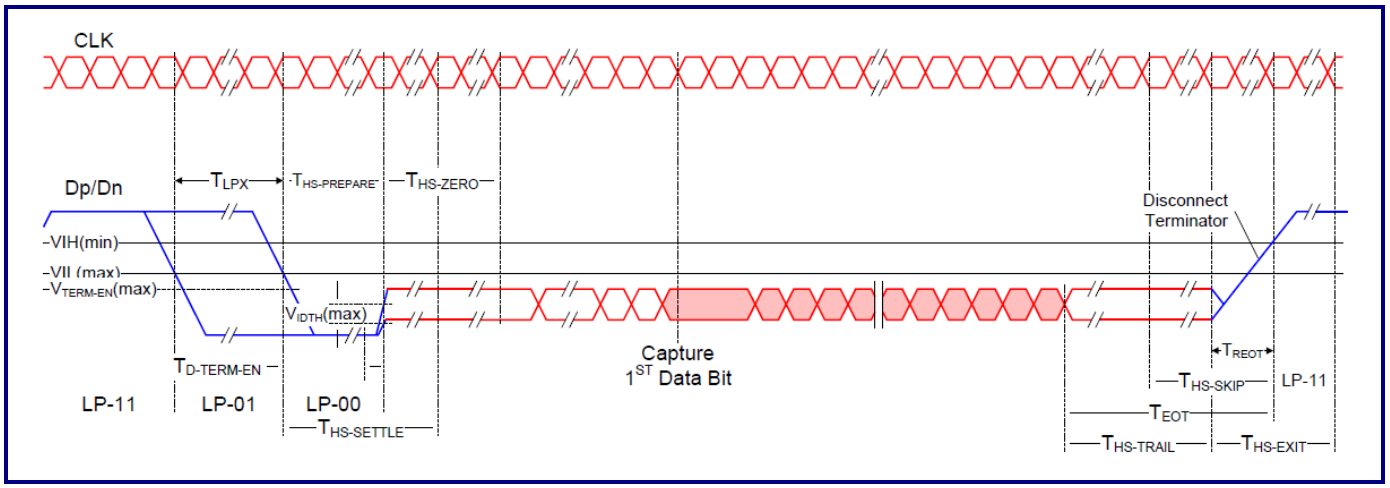

Figure 4-6. High-Speed Data Transmission in Bursts

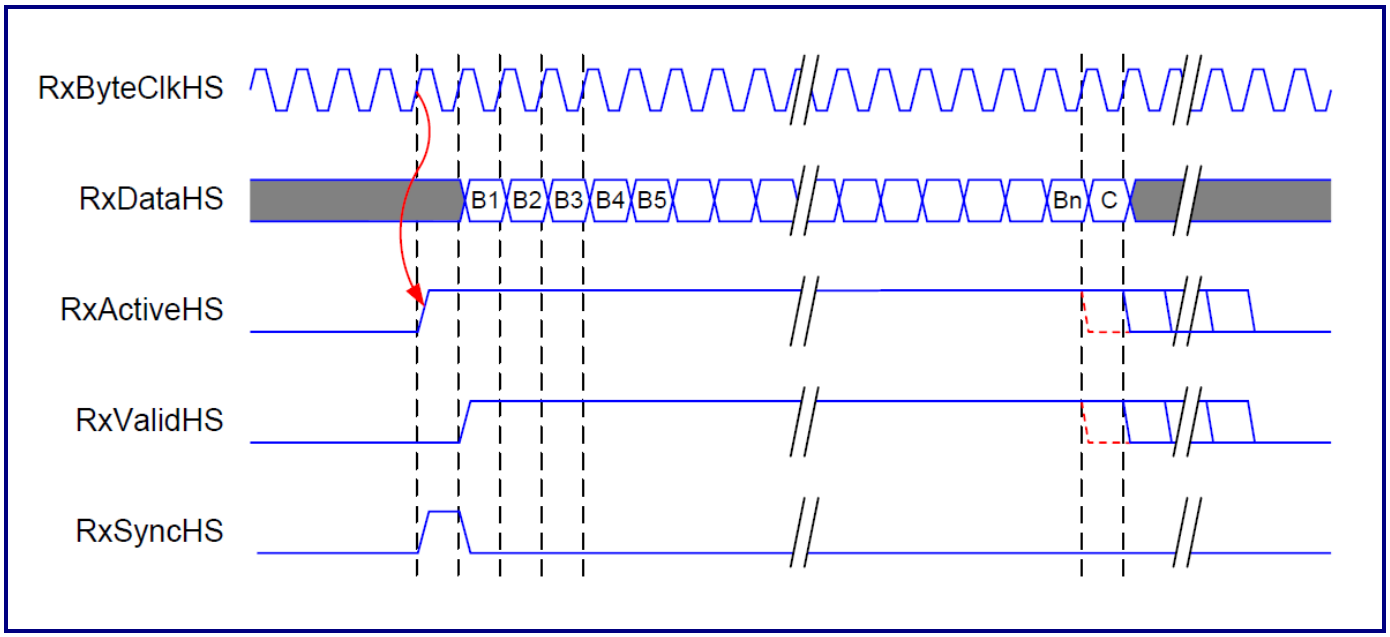

Figure 4-7. High-Speed Receive at PPI of Slave Side

4.2.2.3 Escape Mode

Escape mode is a special operation mode for data lanes using the low-power states. In this mode, some additional functionality (As shown in Table 4-2) will be available. The Escape-mode operation will be supported in the forward direction and is optional in the reverse direction.

Table 4-2. Available Escape Mode Commands and Actions

Escape Mode Action	Command Type	Entry Command Pattern (First Bit Transmitted to Last Bit Transmitted)
Low-Power data transmission	Mode	11100001
Ultra Low-Power state	Mode	00011110
Undefined-1	Mode	10011111
Undefined-2	Mode	01100010
Reset-trigger (Remote application)	Trigger	01100010
Unknown-3	Trigger	01011101
Unknown-4	Trigger	00100001
Unknown-5	Trigger	10100000

A data lane enters the Escape mode via an Escape-mode entry procedure (LP-11, LP-10, LP-00, LP-01, and LP-00). As soon as the final bridge state (LP-00) is observed on the line, the lane will enter the Escape mode at the Space state (LP-00). After entering the Escape mode, the transmitter will send an 8-bit entry command to indicate the requested action. Table 4-2 lists all currently available Escape mode commands and actions. All unassigned commands are reserved for future usage.

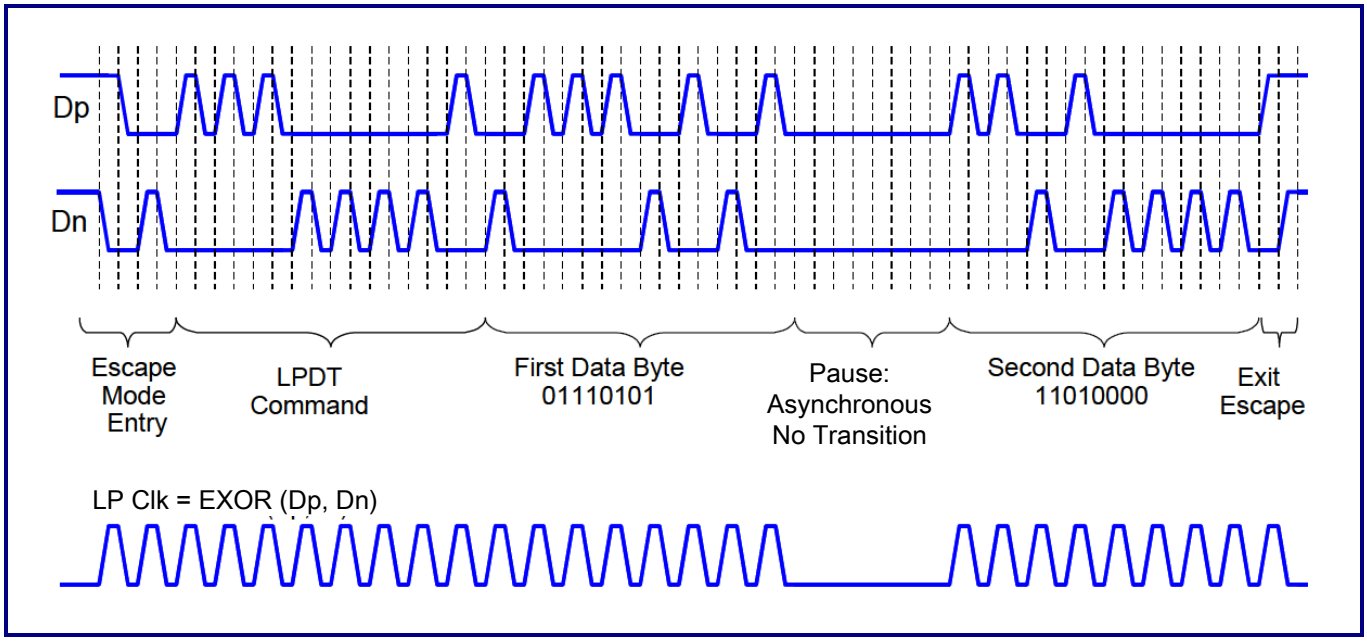

Figure 4-8. Low-Power Data Transmission in Escape Mode

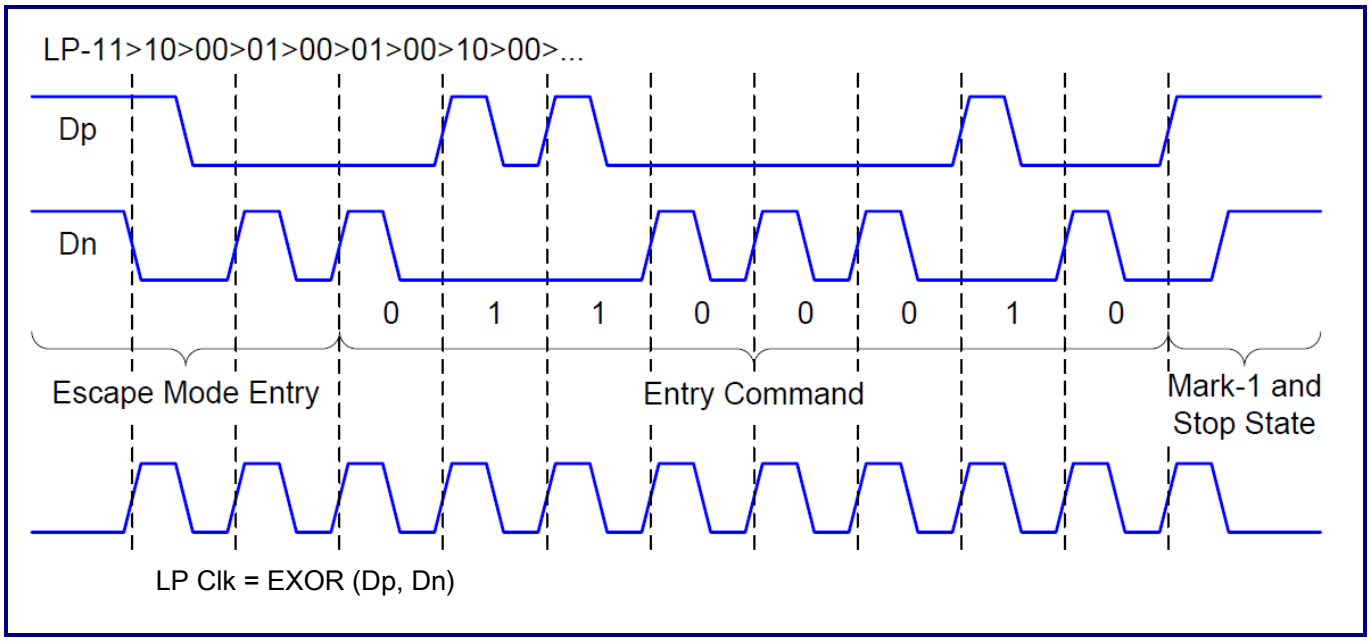

Figure 4-9. Triggering Reset Command in Escape Mode

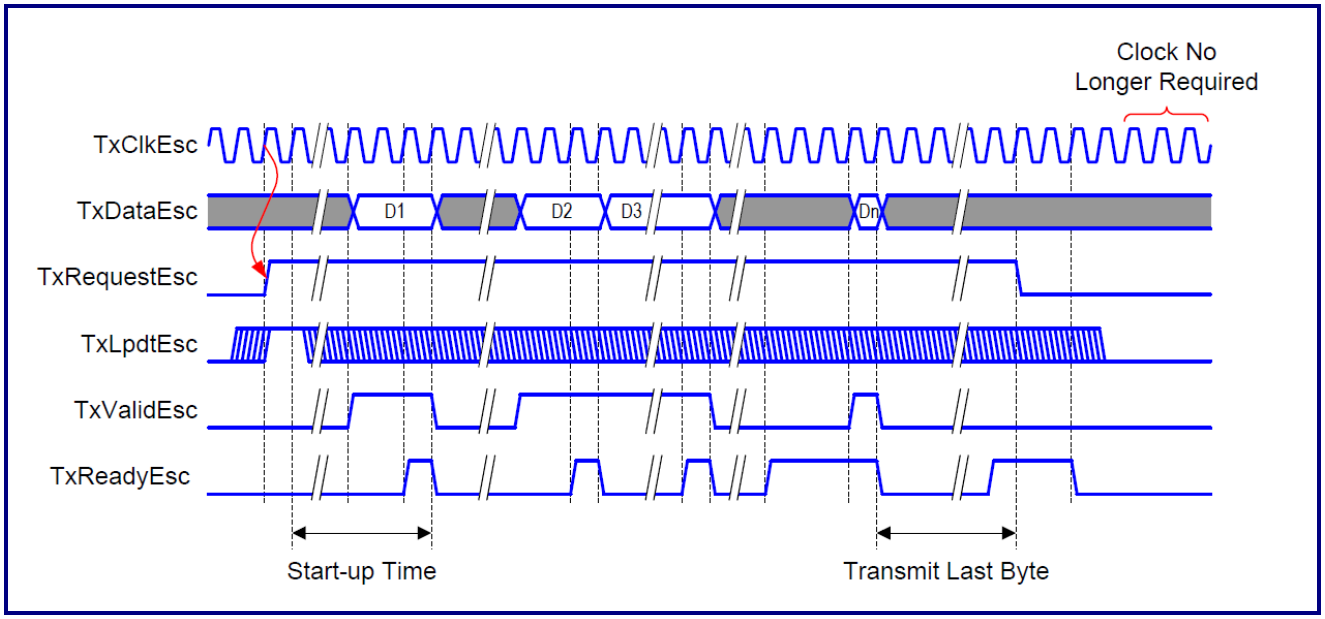

Figure 4-10. Low-Power Data Transmission

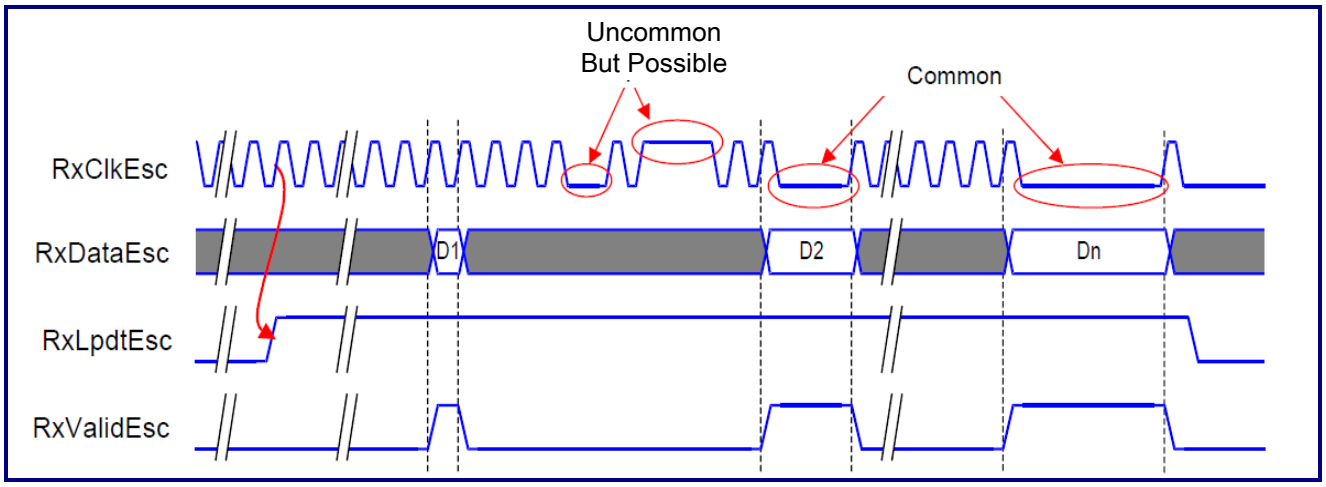

Figure 4-11. Low-Power Data Reception

The transmission direction of a bidirectional data lane (Only data lane 0 is available.) is swapped by the link turnaround procedure. This procedure transfers information in the opposite direction of the current direction. This procedure is the same as the change in the forward-to-reverse direction or in the reverse-to-forward direction. Users must not change the Master and Slave sides by turnaround. Link turnaround must be completely handled in the Control mode. However, this IP does not support bidirectional data lane due to the market consideration.

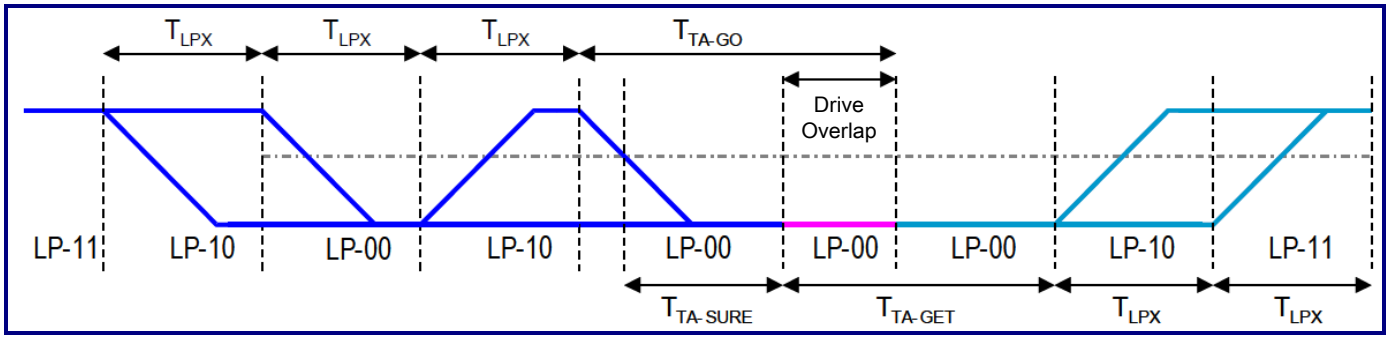

Figure 4-12. Turnaround Procedure