112-1 Soc Design Laboratory

Lab2

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1. Introduction

此次實驗為使用 FIR 程式透過兩種不同 interface 來傳遞，第一種為 AXI-Master，第二種為 AXI-Stream，實驗步驟主要與上次大致相同，都會先使用 HLS，不同的部分在於會使用插入兩種 interface，引入 IP 後，Stream 會使用到 in 跟 out 的 DMA，最後驗證的部分 MAXI 我使用的是 PYNQ 的板子，Stream 則是使用 kv260 做驗證。

2. Observed & Learned

在兩種 interface 中，我了解到其中 AXI-Master 的特色為有更高的效能，而 Stream 則是會透過 DMA，通常會使用在 function 間傳遞資料，從合成完的報告中也可看出 interface 使用的情形，並了解 Memory 跟 Address 是如何去分配的，以及 ap_start、ap_done 等訊號所代表的意義。

3. Screen dump

FIRN11MAXI

(1) Performance

```
================================================================
== Synthesis Summary Report of 'fir_n11_maxi'
================================================================
+ General Information:
    * Date:           Wed Sep 27 12:24:15 2023
    * Version:        2022.1 (Build 3526262 on Mon Apr 18 15:47:01 MDT 2022)
    * Project:        hls_FIRN11MAXI
    * Solution:       solution1 (Vivado IP Flow Target)
    * Product family: zynq
    * Target device:  xc7z020-clg400-1


+ Performance & Resource Estimates:

    PS: '+' for module; 'o' for loop; '*' for dataflow
    +-----------------------------------+------+-------+---------+---------+----------+---------+------+----------+------+----------+----------+----------+-----+
    |              Modules              | Issue|       | Latency | Latency | Iteration|         | Trip |          |      |          |          |          |     |
    |              & Loops              | Type | Slack | (cycles)|   (ns)  |  Latency | Interval| Count| Pipelined| BRAM |    DSP   |    FF    |    LUT   | URAM|
    +-----------------------------------+------+-------+---------+---------+----------+---------+------+----------+------+----------+----------+----------+-----+
    |+ fir_n11_maxi                     |     -|  0.00|        -|        -|         -|        -|     -|        no|     -|  33 (15%)|  4456 (4%)|  3053 (5%)|    -|
    | + fir_n11_maxi_Pipeline_XFER_LOOP |     -|  0.00|        -|        -|         -|        -|     -|        no|     -|  33 (15%)|  2794 (2%)|  1084 (2%)|    -|
    |  o XFER_LOOP                      |     -|  7.30|        -|        -|         8|        1|     -|       yes|     -|         -|         -|         -|    -|
    +-----------------------------------+------+-------+---------+---------+----------+---------+------+----------+------+----------+----------+----------+-----+
```

(2) Utilization

```
================================================================
== Utilization Estimates
================================================================
* Summary:
+-----------------+---------+-----+--------+-------+-----+
|       Name      | BRAM_18K| DSP |   FF   |  LUT  | URAM|
+-----------------+---------+-----+--------+-------+-----+
|DSP              |        -|    -|       -|      -|    -|
|Expression       |        -|    -|       0|     40|    -|
|FIFO             |        -|    -|       -|      -|    -|
|Instance         |        0|   33|    3806|   2838|    -|
|Memory           |        -|    -|       -|      -|    -|
|Multiplexer      |        -|    -|       -|    175|    -|
|Register         |        -|    -|     650|      -|    -|
+-----------------+---------+-----+--------+-------+-----+
|Total            |        0|   33|    4456|   3053|    0|
+-----------------+---------+-----+--------+-------+-----+
|Available        |      280|  220|  106400|  53200|    0|
+-----------------+---------+-----+--------+-------+-----+
|Utilization (%)  |        0|   15|       4|      5|    0|
+-----------------+---------+-----+--------+-------+-----+

+ Detail:
    * Instance:
    +-----------------------------------------------+-----------------------------------+---------+---+------+------+-----+
    |                    Instance                   |               Module              | BRAM_18K| DSP|  FF  |  LUT | URAM|
    +-----------------------------------------------+-----------------------------------+---------+---+------+------+-----+
    |control_s_axi_U                                |control_s_axi                      |        0|  0|   294|   436|    0|
    |grp_fir_n11_maxi_Pipeline_XFER_LOOP_fu_242     |fir_n11_maxi_Pipeline_XFER_LOOP    |        0|  33|  2794|  1084|    0|
    |gmem_m_axi_U                                   |gmem_m_axi                         |        0|  0|   718|  1318|    0|
    +-----------------------------------------------+-----------------------------------+---------+---+------+------+-----+
    |Total                                          |                                   |        0|  33|  3806|  2838|    0|
    +-----------------------------------------------+-----------------------------------+---------+---+------+------+-----+
```

* DSP:
N/A

* Memory:
N/A

* FIFO:
N/A

* Expression:

Variable Name	Operation	DSP	FF	LUT	Bitwidth P0	Bitwidth P1
add_ln16_fu_289_p2	+	0	0	40	33	2
Total		0	0	40	33	2

* Multiplexer:

Name	LUT	Input Size	Bits	Total Bits
an32Coef_address0	65	12	4	48
ap_NS_fsm	65	15	1	15
gmem_ARVALID	9	2	1	2
gmem_AWVALID	9	2	1	2
gmem_BREADY	9	2	1	2
gmem_RREADY	9	2	1	2
gmem_WVALID	9	2	1	2
Total	175	37	10	73

* Register:

Name	FF	LUT	Bits	Const Bits
an32Coef_load_10_reg_446	32	0	32	0
an32Coef_load_1_reg_340	32	0	32	0
an32Coef_load_2_reg_350	32	0	32	0
an32Coef_load_3_reg_360	32	0	32	0
an32Coef_load_4_reg_370	32	0	32	0
an32Coef_load_5_reg_380	32	0	32	0
an32Coef_load_6_reg_390	32	0	32	0
an32Coef_load_7_reg_400	32	0	32	0
an32Coef_load_8_reg_410	32	0	32	0
an32Coef_load_9_reg_420	32	0	32	0
an32Coef_load_reg_330	32	0	32	0
ap_CS_fsm	14	0	14	0
grp_fir_n11_maxi_Pipeline_XFER_LOOP_fu_242_ap_start_reg	1	0	1	0
lshr_ln16_cast_reg_440	31	0	31	0
pn32HPInput_read_reg_435	64	0	64	0
pn32HPOutput_read_reg_430	64	0	64	0
trunc_ln18_1_reg_451	62	0	62	0
trunc_ln30_1_reg_456	62	0	62	0
Total	650	0	650	0

(3) Interface

```
================================================================
== HW Interfaces
================================================================
* M_AXI
+------------+-------------+---------------+---------+--------+----------+-----------+--------------+--------------+-------------+-------------+
| Interface  | Data Width  | Address Width | Latency | Offset | Register | Max Widen | Max Read     | Max Write    | Num Read    | Num Write   |
|            | (SW->HW)    |               |         |        |          | Bitwidth  | Burst Length | Burst Length | Outstanding | Outstanding |
+------------+-------------+---------------+---------+--------+----------+-----------+--------------+--------------+-------------+-------------+
| m_axi_gmem | 32 -> 32    | 64            | 0       | slave  | 0        | 0         | 16           | 16           | 16          | 16          |
+------------+-------------+---------------+---------+--------+----------+-----------+--------------+--------------+-------------+-------------+

* S_AXILITE Interfaces
+---------------+------------+---------------+--------+----------+
| Interface     | Data Width | Address Width | Offset | Register |
+---------------+------------+---------------+--------+----------+
| s_axi_control | 32         | 7             | 16     | 0        |
+---------------+------------+---------------+--------+----------+

* S_AXILITE Registers
+---------------+-----------------+--------+-------+--------+----------------------------------+----------------------------------------------------------------------+
| Interface     | Register        | Offset | Width | Access | Description                      | Bit Fields                                                           |
+---------------+-----------------+--------+-------+--------+----------------------------------+----------------------------------------------------------------------+
| s_axi_control | CTRL            | 0x00   | 32    | RW     | Control signals                  | 0=AP_START 1=AP_DONE 2=AP_IDLE 3=AP_READY 7=AUTO_RESTART 9=INTERRUPT |
| s_axi_control | GIER            | 0x04   | 32    | RW     | Global Interrupt Enable Register | 0=Enable                                                             |
| s_axi_control | IP_IER          | 0x08   | 32    | RW     | IP Interrupt Enable Register     | 0=CHAN0_INT_EN 1=CHAN1_INT_EN                                        |
| s_axi_control | IP_ISR          | 0x0c   | 32    | RW     | IP Interrupt Status Register     | 0=CHAN0_INT_ST 1=CHAN1_INT_ST                                        |
| s_axi_control | pn32HPInput_1   | 0x10   | 32    | W      | Data signal of pn32HPInput       |                                                                      |
| s_axi_control | pn32HPInput_2   | 0x14   | 32    | W      | Data signal of pn32HPInput       |                                                                      |
| s_axi_control | pn32HPOutput_1  | 0x1c   | 32    | W      | Data signal of pn32HPOutput      |                                                                      |
| s_axi_control | pn32HPOutput_2  | 0x20   | 32    | W      | Data signal of pn32HPOutput      |                                                                      |
| s_axi_control | regXferLeng     | 0x28   | 32    | W      | Data signal of regXferLeng       |                                                                      |
+---------------+-----------------+--------+-------+--------+----------------------------------+----------------------------------------------------------------------+

* TOP LEVEL CONTROL
+-----------+------------+-----------+
| Interface | Type       | Ports     |
+-----------+------------+-----------+
| ap_clk    | clock      | ap_clk    |
| ap_rst_n  | reset      | ap_rst_n  |
| interrupt | interrupt  | interrupt |
| ap_ctrl   | ap_ctrl_hs |           |
+-----------+------------+-----------+
```

(4) Co-simulation transcript/waveform

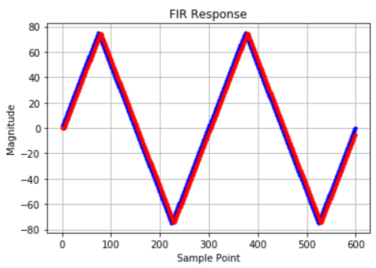
```
INFO: [SIM 2] *************** CSIM start ***************
INFO: [SIM 4] CSIM will launch GCC as the compiler.
make: 'csim.exe' is up to date.
>> Start test!
>> Comparing against output data...
>> Test passed!
------------------------
INFO: [SIM 1] CSim done with 0 errors.
INFO: [SIM 3] *************** CSIM finish ***************
```

(5) Jupyter Notebook execution results

```
xSeq = range(len(inBuffer0))
if n32DCGain == 0:
    plt.plot(xSeq, inBuffer0, 'b.', xSeq, outBuffer0, 'r.')
else:
    plt.plot(xSeq, inBuffer0, 'b.', xSeq, outBuffer0 / n32DCGain, 'r.')
plt.grid(True)
plt.show() # In Jupyter, press Tab + Shift keys to show plot then redo run

print("============================")
print("Exit process")
```

```
Entry: /usr/local/share/pynq-venv/lib/python3.8/site-packages/ipykernel_launcher.py
System argument(s): 3
Start of "/usr/local/share/pynq-venv/lib/python3.8/site-packages/ipykernel_launcher.py"
Kernel execution time: 0.0006163120269775391 s
```




```
============================
Exit process
```

```
In [ ]:
```

FIRN11Stream

(1)Performance

```
================================================================
== Synthesis Summary Report of 'fir_n11_strm'
================================================================
+ General Information:
    * Date:           Thu Sep 21 10:17:06 2023
    * Version:        2022.1 (Build 3526262 on Mon Apr 18 15:47:01 MDT 2022)
    * Project:        hls_FIRN11Stream
    * Solution:       solution1 (Vivado IP Flow Target)
    * Product family: zynquplus
    * Target device:  xck26-sfvc784-2LV-c


+ Performance & Resource Estimates:

    PS: '+' for module; 'o' for loop; '*' for dataflow
    +-----------------------------------+------+------+---------+---------+----------+---------+------+----------+------+---------+---------+------------+-----+
    |              Modules              | Issue|      | Latency | Latency| Iteration|         | Trip |          |      |         |         |            |     |
    |              & Loops              | Type | Slack| (cycles)|  (ns)  |  Latency | Interval| Count| Pipelined| BRAM |   DSP   |    FF   |     LUT    | URAM|
    +-----------------------------------+------+------+---------+---------+----------+---------+------+----------+------+---------+---------+------------+-----+
    |+ fir_n11_strm                     |     -|  1.01|        -|        -|         -|        -|     -|        no|     -|  33 (2%)|  952 (~0%)|  1082 (~0%)|    -|
    | + fir_n11_strm_Pipeline_XFER_LOOP |     -|  1.01|        -|        -|         -|        -|     -|        no|     -|  33 (2%)|  762 (~0%)|   825 (~0%)|    -|
    |  o XFER_LOOP                      |    II|  7.30|        -|        -|        12|       11|     -|       yes|     -|        -|         -|           -|    -|
    +-----------------------------------+------+------+---------+---------+----------+---------+------+----------+------+---------+---------+------------+-----+
```

(2)Utilization

```
================================================================
== Utilization Estimates
================================================================
* Summary:
+-----------------+---------+------+--------+--------+-----+
|       Name      | BRAM_18K|  DSP |   FF   |   LUT  | URAM|
+-----------------+---------+------+--------+--------+-----+
|DSP              |        -|     -|       -|       -|    -|
|Expression       |        -|     -|       0|      42|    -|
|FIFO             |        -|     -|       -|       -|    -|
|Instance         |        0|    33|     916|    1005|    0|
|Memory           |        -|     -|       -|       -|    -|
|Multiplexer      |        -|     -|       -|      35|    -|
|Register         |        -|     -|      36|       -|    -|
+-----------------+---------+------+--------+--------+-----+
|Total            |        0|    33|     952|    1082|    0|
+-----------------+---------+------+--------+--------+-----+
|Available        |      288|  1248|  234240|  117120|   64|
+-----------------+---------+------+--------+--------+-----+
|Utilization (%)  |        0|     2|      ~0|      ~0|    0|
+-----------------+---------+------+--------+--------+-----+

+ Detail:
    * Instance:
    +-----------------------------------------------+---------------------------------+---------+----+-----+-----+-----+
    |                    Instance                   |              Module             | BRAM_18K| DSP|  FF | LUT | URAM|
    +-----------------------------------------------+---------------------------------+---------+----+-----+-----+-----+
    |control_s_axi_U                                |control_s_axi                    |        0|   0|  154|  180|    0|
    |grp_fir_n11_strm_Pipeline_XFER_LOOP_fu_112     |fir_n11_strm_Pipeline_XFER_LOOP  |        0|  33|  762|  825|    0|
    +-----------------------------------------------+---------------------------------+---------+----+-----+-----+-----+
    |Total                                          |                                 |        0|  33|  916| 1005|    0|
    +-----------------------------------------------+---------------------------------+---------+----+-----+-----+-----+

    * DSP:
    N/A

    * Memory:
    N/A

    * FIFO:
    N/A

    * Expression:
    +-----------------------------------------------------------------+----------+---+---+----+------------+------------+
    |                         Variable Name                           | Operation| DSP| FF| LUT| Bitwidth P0| Bitwidth P1|
    +-----------------------------------------------------------------+----------+---+---+----+------------+------------+
    |ret_V_fu_171_p2                                                  |         +|   0|  0|  40|          33|           2|
    |grp_fir_n11_strm_Pipeline_XFER_LOOP_fu_112_pstrmOutput_TREADY    |       and|   0|  0|   2|           1|           1|
    +-----------------------------------------------------------------+----------+---+---+----+------------+------------+
    |Total                                                            |          |   0|  0|  42|          34|           3|
    +-----------------------------------------------------------------+----------+---+---+----+------------+------------+

    * Multiplexer:
    +--------------------------------+----+------------+----+------------+
    |              Name              | LUT| Input Size|Bits| Total Bits|
    +--------------------------------+----+------------+----+------------+
    |ap_NS_fsm                       |  26|           5|   1|           5|
    |pstrmInput_TREADY_int_regslice  |   9|           2|   1|           2|
    +--------------------------------+----+------------+----+------------+
    |Total                           |  35|           7|   2|           7|
    +--------------------------------+----+------------+----+------------+

    * Register:
    +-----------------------------------------------------------+----+----+-----+-----------+
    |                            Name                           | FF | LUT| Bits| Const Bits|
    +-----------------------------------------------------------+----+----+-----+-----------+
    |ap_CS_fsm                                                  |   4|   0|    4|          0|
    |grp_fir_n11_strm_Pipeline_XFER_LOOP_fu_112_ap_start_reg    |   1|   0|    1|          0|
    |tmp_reg_187                                                |  31|   0|   31|          0|
    +-----------------------------------------------------------+----+----+-----+-----------+
    |Total                                                      |  36|   0|   36|          0|
    +-----------------------------------------------------------+----+----+-----+-----------+
```

(3)Interface

```
=================================================================
== HW Interfaces
=================================================================
* S_AXILITE Interfaces
+---------------+------------+---------------+--------+----------+
| Interface     | Data Width | Address Width | Offset | Register |
+---------------+------------+---------------+--------+----------+
| s_axi_control | 32         | 7             | 64     | 0        |
+---------------+------------+---------------+--------+----------+

* S_AXILITE Registers
+---------------+-------------+--------+-------+--------+----------------------------------+---------------------------------------------------------------------+
| Interface     | Register    | Offset | Width | Access | Description                      | Bit Fields                                                          |
+---------------+-------------+--------+-------+--------+----------------------------------+---------------------------------------------------------------------+
| s_axi_control | CTRL        | 0x00   | 32    | RW     | Control signals                  | 0=AP_START 1=AP_DONE 2=AP_IDLE 3=AP_READY 7=AUTO_RESTART 9=INTERRUPT |
| s_axi_control | GIER        | 0x04   | 32    | RW     | Global Interrupt Enable Register | 0=Enable                                                            |
| s_axi_control | IP_IER      | 0x08   | 32    | RW     | IP Interrupt Enable Register     | 0=CHAN0_INT_EN 1=CHAN1_INT_EN                                       |
| s_axi_control | IP_ISR      | 0x0c   | 32    | RW     | IP Interrupt Status Register     | 0=CHAN0_INT_ST 1=CHAN1_INT_ST                                       |
| s_axi_control | regXferLeng | 0x10   | 32    | W      | Data signal of regXferLeng       |                                                                     |
+---------------+-------------+--------+-------+--------+----------------------------------+---------------------------------------------------------------------+

* AXIS
+-------------+---------------+-------+-------+-----+-------+-------+--------+-------+-------+--------+
| Interface   | Register Mode | TDATA | TDEST | TID | TKEEP | TLAST | TREADY | TSTRB | TUSER | TVALID |
+-------------+---------------+-------+-------+-----+-------+-------+--------+-------+-------+--------+
| pstrmInput  | both          | 32    | 1     | 1   | 4     | 1     | 1      | 4     | 1     | 1      |
| pstrmOutput | both          | 32    | 1     | 1   | 4     | 1     | 1      | 4     | 1     | 1      |
+-------------+---------------+-------+-------+-----+-------+-------+--------+-------+-------+--------+

* TOP LEVEL CONTROL
+-----------+------------+-----------+
| Interface | Type       | Ports     |
+-----------+------------+-----------+
| ap_clk    | clock      | ap_clk    |
| ap_rst_n  | reset      | ap_rst_n  |
| interrupt | interrupt  | interrupt |
| ap_ctrl   | ap_ctrl_hs |           |
+-----------+------------+-----------+
```

(4)Co-simulation transcript/waveform

```
INFO: [SIM 2] *************** CSIM start ***************
INFO: [SIM 4] CSIM will launch GCC as the compiler.
   Compiling ../../../FIRTester.cpp in debug mode
   Compiling ../../../FIR.cpp in debug mode
   Generating csim.exe
>> Start test!
>> Comparing against output data...
>> Test passed!
------------------------
INFO: [SIM 1] CSim done with 0 errors.
INFO: [SIM 3] *************** CSIM finish ***************
```

(5)Jupyter Notebook execution results

jupyter FIRN11Stream Last Checkpoint: 幾秒前 (unsaved changes)

Logout

File Edit View Insert Cell Kernel Widgets Help

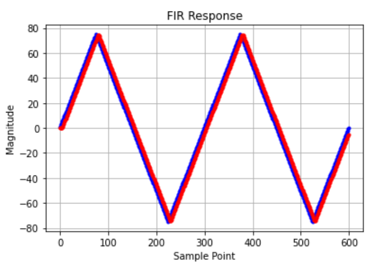
Not Trusted | Python 3

Run | Code | Voilà

```
    xSeq = range(len(inBuffer0))
    if n32DCGain == 0:
        plt.plot(xSeq, inBuffer0, 'b.', xSeq, outBuffer0, 'r.')
    else:
        plt.plot(xSeq, inBuffer0, 'b.', xSeq, outBuffer0 / n32DCGain, 'r.')
    plt.grid(True)
    plt.show() # In Jupyter, press Tab + Shift keys to show plot then redo run

    print("============================")
    print("Exit process")
```

```
Entry: /usr/local/share/pynq-venv/lib/python3.8/site-packages/ipykernel_launcher.py
System argument(s): 3
Start of "/usr/local/share/pynq-venv/lib/python3.8/site-packages/ipykernel_launcher.py"
Kernel execution time: 0.0010042190551757812 s
```




```
============================
Exit process
```

In [ ]: 1