112-1 Soc Design Laboratory

Lab1 submission guide

學號:112061619

姓名:王證皓

1. Introduction

此實驗目的為完成 tool 的虛擬機環境安裝，以及使用乘法器程式實現 High-Level Synthesis，將 C code 轉成 RTL，並使用 vivado 進行整合 ip 與合成，最後輸出 bitstream 到 PYNQ-Z2 板上做驗證。

2. Observed & Learned

從實驗中，我學習到了如何使用 Virtualbox 建立 Ubuntu 環境以安裝 Xilinx 的相關工具，安裝的過程中雖有出現一些錯誤，但是這些錯誤卻能使我主動去找尋產生的原因，以及了解講義上指令背後的意義，安裝後實際操作 vitis hls，能從 report 中觀察到電路的面積是由 LUT、FF、BRAM、DSP 所組成，效能上可以透過分析 Slack、Latency、Interval 等來了解時序，接著了解到如何用 vivado 建立 block design 來輸出 bitstream，最後由線上 FPGA 來驗證模擬結果與 C/RTL 相符。

3. Screen dump

(1)Performance

```
================================================================
== Synthesis Summary Report of 'multip_2num'
================================================================
+ General Information:
    * Date:           Wed Sep 13 10:25:17 2023
    * Version:        2022.1 (Build 3526262 on Mon Apr 18 15:47:01 MDT 2022)
    * Project:        hls_ip
    * Solution:       solution1 (Vivado IP Flow Target)
    * Product family: zynq
    * Target device:  xc7z020-clg400-1


+ Performance & Resource Estimates:

    PS: '+' for module; 'o' for loop; '*' for dataflow
    +---------------+------+------+---------+--------+----------+---------+------+----------+------+--------+-----------+-----------+------+
    |    Modules    | Issue|      | Latency | Latency| Iteration|         | Trip |          |      |        |           |           |      |
    |    & Loops    | Type | Slack| (cycles)|  (ns)  |  Latency | Interval| Count| Pipelined| BRAM |   DSP  |     FF    |    LUT    | URAM|
    +---------------+------+------+---------+--------+----------+---------+------+----------+------+--------+-----------+-----------+------+
    |+ multip_2num  |     -|  0.39|        3|  30.000|         -|        4|     -|        no|     -|  3 (1%)|  409 (~0%)|  307 (~0%)|    -|
    +---------------+------+------+---------+--------+----------+---------+------+----------+------+--------+-----------+-----------+------+


================================================================
== Performance Estimates
================================================================
+ Timing:
    * Summary:
    +--------+----------+----------+------------+
    |  Clock |  Target  | Estimated| Uncertainty|
    +--------+----------+----------+------------+
    |ap_clk  |  10.00 ns|  6.912 ns|     2.70 ns|
    +--------+----------+----------+------------+

+ Latency:
    * Summary:
    +---------+---------+-----------+-----------+-----+-----+---------+
    |  Latency (cycles) |   Latency (absolute)  |  Interval | Pipeline|
    |   min   |   max   |    min    |    max    | min | max |   Type  |
    +---------+---------+-----------+-----------+-----+-----+---------+
    |        3|        3|  30.000 ns|  30.000 ns|    4|    4|       no|
    +---------+---------+-----------+-----------+-----+-----+---------+

    + Detail:
        * Instance:
        N/A

        * Loop:
        N/A
```

(2)Utilization

```
================================================================
== Utilization Estimates
================================================================
* Summary:
+-----------------+---------+-----+--------+-------+-----+
|       Name      | BRAM_18K| DSP |   FF   |  LUT  | URAM|
+-----------------+---------+-----+--------+-------+-----+
|DSP              |        -|    -|       -|      -|    -|
|Expression       |        -|    -|       -|      -|    -|
|FIFO             |        -|    -|       -|      -|    -|
|Instance         |        0|    3|     309|    282|    -|
|Memory           |        -|    -|       -|      -|    -|
|Multiplexer      |        -|    -|       -|     25|    -|
|Register         |        -|    -|     100|      -|    -|
+-----------------+---------+-----+--------+-------+-----+
|Total            |        0|    3|     409|    307|    0|
+-----------------+---------+-----+--------+-------+-----+
|Available        |      280|  220|  106400|  53200|    0|
+-----------------+---------+-----+--------+-------+-----+
|Utilization (%)  |        0|    1|      ~0|     ~0|    0|
+-----------------+---------+-----+--------+-------+-----+

+ Detail:
    * Instance:
    +-----------------------+---------------------+---------+----+-----+-----+-----+
    |        Instance       |        Module       | BRAM_18K| DSP|  FF | LUT | URAM|
    +-----------------------+---------------------+---------+----+-----+-----+-----+
    |control_s_axi_U        |control_s_axi        |        0|   0|  144|  232|    0|
    |mul_32s_32s_32_2_1_U1  |mul_32s_32s_32_2_1   |        0|   3|  165|   50|    0|
    +-----------------------+---------------------+---------+----+-----+-----+-----+
    |Total                  |                     |        0|   3|  309|  282|    0|
    +-----------------------+---------------------+---------+----+-----+-----+-----+

    * DSP:
    N/A

    * Memory:
    N/A

    * FIFO:
    N/A

    * Expression:
    N/A

    * Multiplexer:
    +-----------+----+-----------+-----+-----------+
    |    Name   | LUT| Input Size| Bits| Total Bits|
    +-----------+----+-----------+-----+-----------+
    |ap_NS_fsm  |  25|          5|    1|          5|
    +-----------+----+-----------+-----+-----------+
    |Total      |  25|          5|    1|          5|
    +-----------+----+-----------+-----+-----------+

    * Register:
    +--------------------+----+----+-----+-----------+
    |        Name        | FF | LUT| Bits| Const Bits|
    +--------------------+----+----+-----+-----------+
    |ap_CS_fsm           |   4|   0|    4|          0|
    |mul_ln11_reg_71     |  32|   0|   32|          0|
    |n32In1_read_reg_66  |  32|   0|   32|          0|
    |n32In2_read_reg_61  |  32|   0|   32|          0|
    +--------------------+----+----+-----+-----------+
    |Total               | 100|   0|  100|          0|
    +--------------------+----+----+-----+-----------+
```

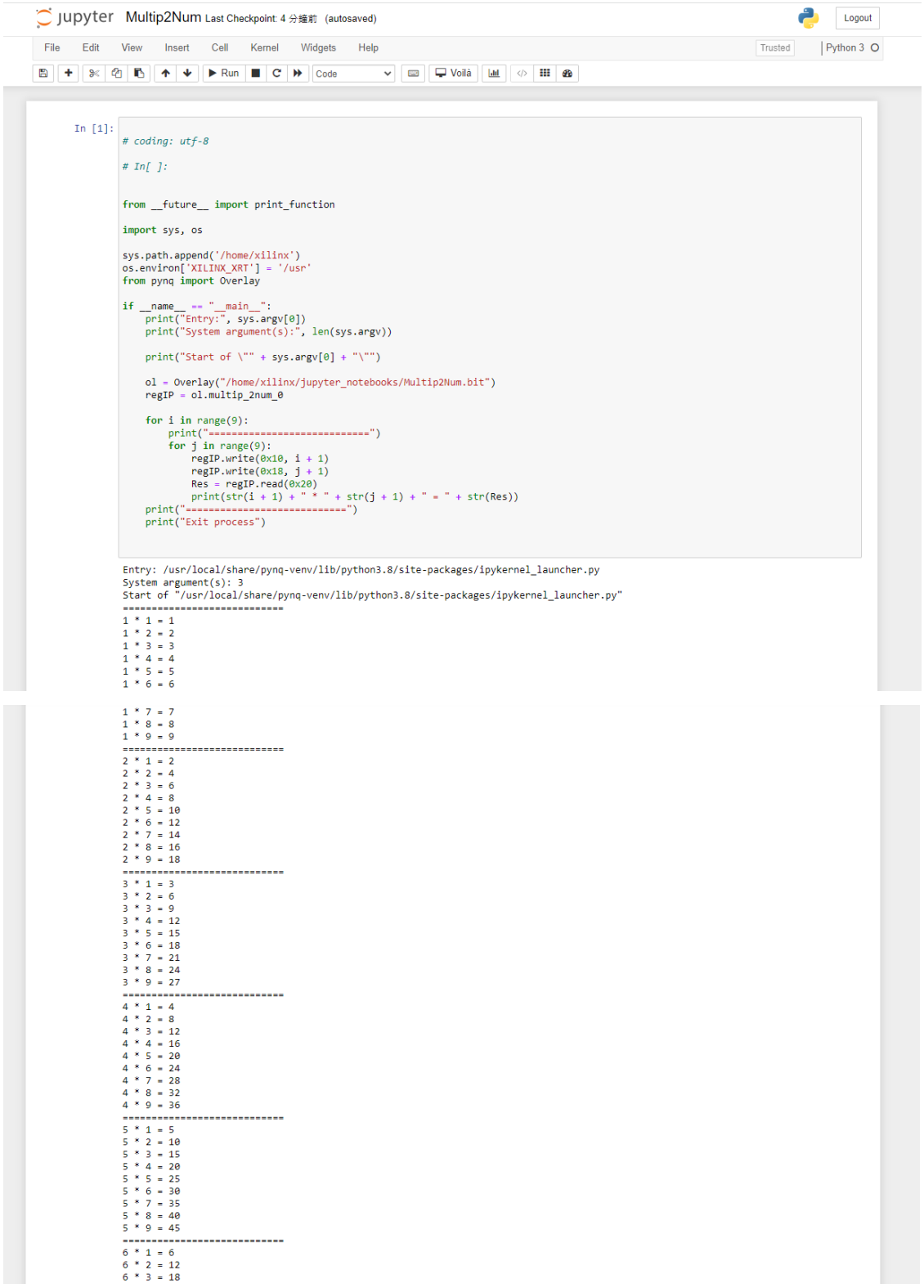
(3)Interface

```
================================================================
== Interface
================================================================
* Summary:
+------------------------+-----+-----+-------------+-------------+-------------+
|       RTL Ports        | Dir | Bits|   Protocol  | Source Object|    C Type   |
+------------------------+-----+-----+-------------+-------------+-------------+
|s_axi_control_AWVALID   |   in|    1|        s_axi|      control|      pointer|
|s_axi_control_AWREADY   |  out|    1|        s_axi|      control|      pointer|
|s_axi_control_AWADDR    |   in|    6|        s_axi|      control|      pointer|
|s_axi_control_WVALID    |   in|    1|        s_axi|      control|      pointer|
|s_axi_control_WREADY    |  out|    1|        s_axi|      control|      pointer|
|s_axi_control_WDATA     |   in|   32|        s_axi|      control|      pointer|
|s_axi_control_WSTRB     |   in|    4|        s_axi|      control|      pointer|
|s_axi_control_ARVALID   |   in|    1|        s_axi|      control|      pointer|
|s_axi_control_ARREADY   |  out|    1|        s_axi|      control|      pointer|
|s_axi_control_ARADDR    |   in|    6|        s_axi|      control|      pointer|
|s_axi_control_RVALID    |  out|    1|        s_axi|      control|      pointer|
|s_axi_control_RREADY    |   in|    1|        s_axi|      control|      pointer|
|s_axi_control_RDATA     |  out|   32|        s_axi|      control|      pointer|
|s_axi_control_RRESP     |  out|    2|        s_axi|      control|      pointer|
|s_axi_control_BVALID    |  out|    1|        s_axi|      control|      pointer|
|s_axi_control_BREADY    |   in|    1|        s_axi|      control|      pointer|
|s_axi_control_BRESP     |  out|    2|        s_axi|      control|      pointer|
|ap_clk                  |   in|    1| ap_ctrl_none|  multip_2num| return value|
|ap_rst_n                |   in|    1| ap_ctrl_none|  multip_2num| return value|
+------------------------+-----+-----+-------------+-------------+-------------+
```

(4)Co-simulation transcript/waveform

```
INFO: [Sim 2] *************** CSim start ***************
INFO: [Sim 4] CSim will launch GCC as the compiler.
   Compiling ../../../../hls_multiplication/multiptester.cpp in debug mode
   Compiling ../../../../hls_multiplication/multiplication.cpp in debug mode
   Generating csim.exe
>> Start test!
------------------------
1 * 1 = 1
1 * 2 = 2
1 * 3 = 3
1 * 4 = 4
1 * 5 = 5
1 * 6 = 6
1 * 7 = 7
1 * 8 = 8
1 * 9 = 9
------------------------
2 * 1 = 2
2 * 2 = 4
2 * 3 = 6
2 * 4 = 8
2 * 5 = 10
2 * 6 = 12
2 * 7 = 14
2 * 8 = 16
2 * 9 = 18
------------------------
3 * 1 = 3
3 * 2 = 6
3 * 3 = 9
3 * 4 = 12
3 * 5 = 15
3 * 6 = 18
3 * 7 = 21
3 * 8 = 24
3 * 9 = 27
------------------------
4 * 1 = 4
4 * 2 = 8
4 * 3 = 12
4 * 4 = 16
4 * 5 = 20
4 * 6 = 24
4 * 7 = 28
4 * 8 = 32
4 * 9 = 36
------------------------
5 * 1 = 5
5 * 2 = 10
5 * 3 = 15
5 * 4 = 20
5 * 5 = 25
5 * 6 = 30
5 * 7 = 35
5 * 8 = 40
5 * 9 = 45
------------------------
6 * 1 = 6
6 * 2 = 12
6 * 3 = 18
6 * 4 = 24
6 * 5 = 30
6 * 6 = 36
6 * 7 = 42
6 * 8 = 48
6 * 9 = 54
------------------------
7 * 1 = 7
7 * 2 = 14
7 * 3 = 21
7 * 4 = 28
7 * 5 = 35
7 * 6 = 42
7 * 7 = 49
7 * 8 = 56
7 * 9 = 63
------------------------
8 * 1 = 8
8 * 2 = 16
8 * 3 = 24
8 * 4 = 32
8 * 5 = 40
8 * 6 = 48
8 * 7 = 56
8 * 8 = 64
8 * 9 = 72
------------------------
9 * 1 = 9
9 * 2 = 18
9 * 3 = 27
9 * 4 = 36
9 * 5 = 45
9 * 6 = 54
9 * 7 = 63
9 * 8 = 72
9 * 9 = 81
------------------------
>> Test passed!
------------------------
INFO: [Sim 1] CSim done with 0 errors.
INFO: [Sim 3] *************** CSim finish ***************
```

(5)Jupyter Notebook execution results



```
6 * 4 = 24
6 * 5 = 30
6 * 6 = 36
6 * 7 = 42
6 * 8 = 48
6 * 9 = 54
============================
7 * 1 = 7
7 * 2 = 14
7 * 3 = 21
7 * 4 = 28
7 * 5 = 35
7 * 6 = 42
7 * 7 = 49
7 * 8 = 56
7 * 9 = 63
============================
8 * 1 = 8
8 * 2 = 16
8 * 3 = 24
8 * 4 = 32
8 * 5 = 40
8 * 6 = 48
8 * 7 = 56
8 * 8 = 64
8 * 9 = 72
============================
9 * 1 = 9
9 * 2 = 18
9 * 3 = 27
9 * 4 = 36
9 * 5 = 45
9 * 6 = 54
9 * 7 = 63
9 * 8 = 72
9 * 9 = 81
============================
Exit process
```

In [ ]: