112-1 時序電路設計及應用

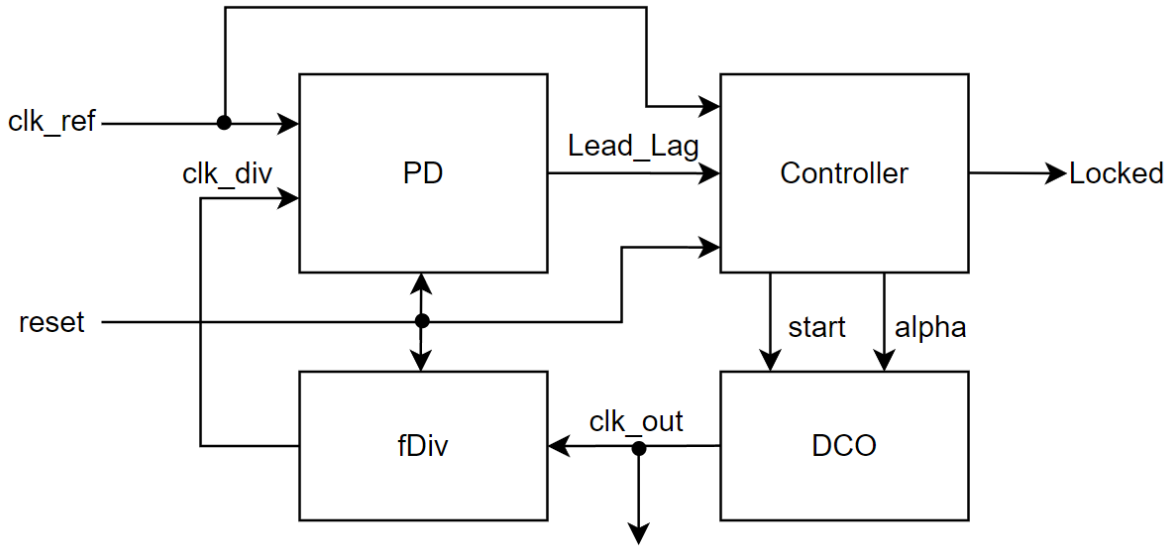
HW3

學號:112061619

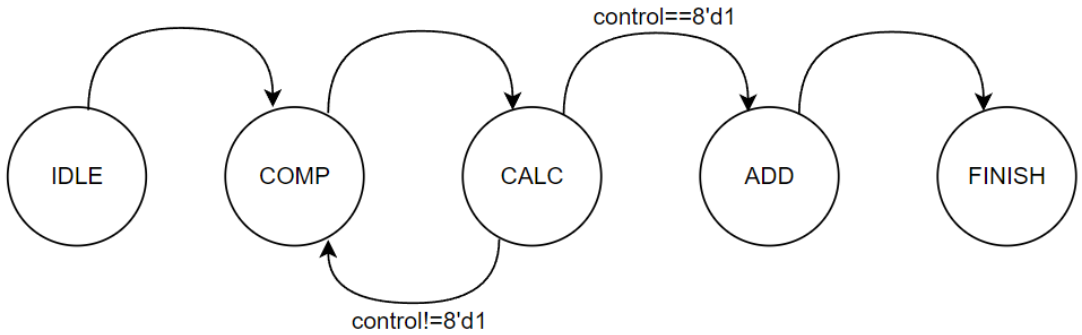
姓名:王證皓

(a) PLL

1. Architecture



Finite State Machine



IDLE:reset 完後進入初始狀態

COMP:比較 clk_ref 與 clk_div 的相位並設置控制碼

CALC:將控制碼做運算得到 alpha code

ADD:最後做 alpha code 的修正

FINISH:達成鎖定

2. Verilog Code

PLL

```
module PLL
(
    input clk_ref,
    input reset,
    output clk_out,
    output Locked
);
    wire clk_div,Lead_Lag,start;
    wire [2:0]alpha;
    PD U0(.en(reset),.clk_ref(clk_ref),.clk_div(clk_div),.Lead_Lag(Lead_Lag));
    Controller U1(.Lead_Lag(Lead_Lag),.clk(clk_ref),.reset(reset),.Locked(Locked),.alpha(alpha),.start(start));
    DCO U2(.E(start),.alpha(alpha),.clk_out(clk_out));
    fDiv U3(.clk_DCO(clk_out),.reset(reset),.DIVN(8'd92),.clk_div(clk_div));
endmodule
```

Phase Detector

```
module PD
(
    input en,
    input clk_ref,
    input clk_div,
    output Lead_Lag
);
    wire reset,Rst,up,down,S,R,d;
    DFF U0(.D(1'b1),.reset(reset),.clk(clk_div),.Q(up));
    DFF U1(.D(1'b1),.reset(reset),.clk(clk_ref),.Q(down));
    nand u5(Rst,up,down);
    and u7(reset,Rst,en);
    nand n1(S,up,R);
    nand n2(R,down,S);
    nand n3(Lead_Lag,S,d);
    nand n4(d,Lead_Lag,R);
endmodule

module DFF
(
    input D,
    input reset,
    input clk,
    output reg Q
);
    always@(posedge clk or negedge reset)begin
        if(~reset)begin
            Q<=1'b0;
        end
        else begin
            Q<=D;
        end
    end
endmodule
```

Controller

```
module Controller(
    input Lead_Lag,
    input clk,
    input reset,
    output reg Locked,
    output reg[2:0]alpha,
    output reg start
);
    reg [2:0]control;
    reg [2:0]state,next_state;
    reg [2:0]count_p,count_n;
    reg register;

    parameter [2:0] IDLE =0;
    parameter [2:0] COMP = 1;
    parameter [2:0] CALC = 2;
    parameter [2:0] ADD = 3;
    parameter [2:0] FINISH =4;

    always@(posedge clk)begin
        if(~reset)begin
            state<=IDLE;
            alpha<=3'b100;
            control<=3'b010;
            Locked<=1'b0;
            count_p<=3'd0;
            count_n<=3'd0;
            start<=1'b0;
        end
        else begin
            state<=next_state;
            start<=1'b1;
            case(state)
                IDLE:begin
                    alpha<=3'b100;
                    control<=3'b010;
                    Locked<=1'b0;
                end
                COMP:begin
                    if(Lead_Lag)begin
                        alpha<=alpha+control;
                    end
                    else begin
                        alpha<=alpha-control;
                    end
                    Locked<=1'b0;
                    control<=control;
                end
```

```
                CALC:begin
                    if(control==3'd1)begin
                        control<=8'd1;
                    end
                    else begin
                        control<=control>>1;
                    end
                    Locked<=1'b0;
                    alpha<=alpha;
                end
                ADD:begin
                    Locked<=1'b1;
                    if(Lead_Lag)begin
                        alpha<=alpha+8'd1;
                    end
                    else begin
                        alpha<=alpha-8'd1;
                    end
                    Locked<=1'b0;
                    control<=control;
                end
                FINISH:begin
                    Locked<=1'b1;
                    alpha<=alpha;
                end
                default:begin
                    alpha<=alpha;
                    Locked<=Locked;
                    control<=control;
                end
            endcase
        end
    end

    always@(*)begin
            case(state)
                IDLE:next_state=COMP;
                COMP:next_state=CALC;
                CALC:next_state=(control==8'd1)?ADD:COMP;
                ADD:next_state=FINISH;
                FINISH:next_state=FINISH;
                default:next_state=IDLE;
            endcase
    end
endmodule
```

DCO

```
module DCO#(
    parameter alpha_num = 3,
    parameter delay_num = 36
)
(
    input E,
    input [alpha_num-1:0]alpha,
    output clk_out

);
    wire [7:0]u;
    wire [delay_num-1:0]g;
    wire y;

    NAND2X2 NAND0(.A(E),.B(clk_out),.Y(g[0]));

    genvar j;
    generate
        for(j=0;j<delay_num-1;j=j+1)begin:delay
            TBUFX1 TBUF0(.A(g[j]),.OE(1'b1),.Y(g[j+1]));
        end
    endgenerate
    BUFX18 buf7(.A(g[delay_num-1]),.Y(y));
    BUFX16 buf8(.A(y),.Y(u[0]));

    BUFX16 buf0(.A(u[0]),.Y(u[1]));
    BUFX18 buf1(.A(u[1]),.Y(u[2]));
    BUFX18 buf2(.A(u[2]),.Y(u[3]));
    BUFX18 buf3(.A(u[3]),.Y(u[4]));
    BUFX18 buf4(.A(u[4]),.Y(u[5]));
    BUFX18 buf5(.A(u[5]),.Y(u[6]));
    BUFX18 buf6(.A(u[6]),.Y(u[7]));

    MUX8to1 U0(.A(u),.sel(alpha),.Dout(clk_out));

endmodule
```

Frequency Divider

```
module fDiv
(
    input clk_DCO,
    input reset,
    input [7:0]DIVN,
    output clk_div
);
    wire [7:0]half;
    reg [7:0]count;

    always@(posedge clk_DCO or negedge reset)begin
        if(~reset)begin
            count<=8'd0;
        end
        else if(count==DIVN-8'd1)begin
            count<=8'd0;
        end
        else begin
            count<=count+8'd1;
        end
    end

    assign half=DIVN>>1;
    assign clk_div=(count>half)?1'b0:1'b1;
endmodule
```

3. Synthesis report

(1) Area

```
****************************************
Report : area
Design : PLL
Version: R-2020.09-SP5
Date   : Fri Dec 15 00:36:35 2023
****************************************

Information: Updating design information... (UID-85)
Information: Timing loop detected. (OPT-150)
        U2/U2/A U2/U2/Y U2/delay_0__TBUF0/A U2/delay_0__TBUF0/Y U2/delay_1__TBUF0/A U2/d
UF0/A U2/delay_4__TBUF0/Y U2/delay_5__TBUF0/A U2/delay_5__TBUF0/Y U2/delay_6__TBUF0/A U2
TBUF0/A U2/delay_9__TBUF0/Y U2/delay_10__TBUF0/A U2/delay_10__TBUF0/Y U2/delay_11__TBUF0
/delay_14__TBUF0/A U2/delay_14__TBUF0/Y U2/delay_15__TBUF0/A U2/delay_15__TBUF0/Y U2/del
__TBUF0/Y U2/delay_19__TBUF0/A U2/delay_19__TBUF0/Y U2/delay_20__TBUF0/A U2/delay_20__TB
 U2/delay_23__TBUF0/Y U2/delay_24__TBUF0/A U2/delay_24__TBUF0/Y U2/delay_25__TBUF0/A U2/
_28__TBUF0/A U2/delay_28__TBUF0/Y U2/delay_29__TBUF0/A U2/delay_29__TBUF0/Y U2/delay_30_
0/Y U2/delay_33__TBUF0/A U2/delay_33__TBUF0/Y U2/delay_34__TBUF0/A U2/delay_34__TBUF0/Y
2/A0 U2/U0/U2/Y U2/U0/U1/A0 U2/U0/U1/Y
Information: Timing loop detected. (OPT-150)
        U0/U3/A1N U0/U3/Y
Warning: Disabling timing arc between pins 'A' and 'Y' on cell 'U2/U2'
         to break a timing loop. (OPT-314)
Warning: Disabling timing arc between pins 'A1N' and 'Y' on cell 'U0/U3'
         to break a timing loop. (OPT-314)
Warning: Disabling timing arc between pins 'A0N' and 'Y' on cell 'U0/U4'
         to break a timing loop. (OPT-314)
Library(s) Used:

    slow (File: /usr/cadtool/ee5216/CBDK_TSMC90GUTM_Arm_f1.0/CIC/SynopsysDC/db/slow.db)

Number of ports:                           68
Number of nets:                           268
Number of cells:                          198
Number of combinational cells:            129
Number of sequential cells:                55
Number of macros/black boxes:               0
Number of buf/inv:                         24
Number of references:                       4

Combinational area:               640.684814
Buf/Inv area:                     138.297603
Noncombinational area:            535.550402
Macro/Black Box area:               0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                 1176.235215
Total area:                 undefined
1

****************************************
```

Total cell area:1176.235215

Gate count:1176.235215/2.8224=416.75

(2) Timing

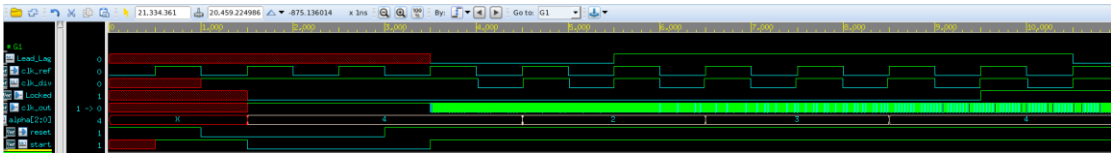
```
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : PLL
Version: R-2020.09-SP5
Date   : Fri Dec 15 00:36:35 2023
****************************************

Operating Conditions: slow   Library: slow
Wire Load Model Mode: top

  Startpoint: U1/alpha_reg_1_
              (rising edge-triggered flip-flop clocked by clk_ref)
  Endpoint: U1/alpha_reg_2_
            (rising edge-triggered flip-flop clocked by clk_ref)
  Path Group: clk_ref
  Path Type: max

  Point                                   Incr       Path
  -----------------------------------------------------------
  clock clk_ref (rise edge)               0.00       0.00
  clock network delay (ideal)             0.00       0.00
  U1/alpha_reg_1_/CK (DFFTRXL)            0.00       0.00 r
  U1/alpha_reg_1_/Q (DFFTRXL)             0.35       0.35 f
  U1/U6/Y (OAI2BB1X1)                     0.18       0.54 f
  U1/U5/Y (OAI21X1)                       0.04       0.58 r
  U1/U25/Y (XOR2X1)                       0.08       0.66 r
  U1/U23/Y (OAI22X1)                      0.07       0.73 f
  U1/U21/Y (AOI22XL)                      0.08       0.81 r
  U1/U19/Y (OAI211XL)                     0.11       0.92 f
  U1/alpha_reg_2_/D0 (MDFFHQX1)           0.00       0.92 f
  data arrival time                                  0.92

  clock clk_ref (rise edge)              10.87      10.87
  clock network delay (ideal)             0.00      10.87
  U1/alpha_reg_2_/CK (MDFFHQX1)           0.00      10.87 r
  library setup time                     -0.19      10.68
  data required time                                10.68
  -----------------------------------------------------------
  data required time                                10.68
  data arrival time                                 -0.92
  -----------------------------------------------------------
  slack (MET)                                        9.77


1
Loading db file '/usr/cadtool/ee5216/CBDK_TSMC90GUTM_Arm_f1.0/CIC/SynopsysDC/db/slow.db'
Information: Propagating switching activity (low effort zero delay simulation). (PWR-6)
Warning: Design has unannotated primary inputs. (PWR-414)
Warning: Design has unannotated sequential cell outputs. (PWR-415)

****************************************
```

(3) Power

```
****************************************
Report : power
        -analysis_effort low
Design : PLL
Version: R-2020.09-SP5
Date   : Fri Dec 15 00:36:36 2023
****************************************


Library(s) Used:

    slow (File: /usr/cadtool/ee5216/CBDK_TSMC90GUTM_Arm_f1.0/CIC/SynopsysDC/db/slow.db)


Operating Conditions: slow   Library: slow
Wire Load Model Mode: top


Global Operating Voltage = 0.9
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  =  40.3215 uW   (85%)
  Net Switching Power  =   7.2738 uW   (15%)
                         ---------
Total Dynamic Power    =  47.5953 uW  (100%)

Cell Leakage Power     =   4.9532 uW


                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %    )  Attrs
--------------------------------------------------------------------------------------------------
io_pad             0.0000           0.0000              0.0000           0.0000  (   0.00%)
memory             0.0000           0.0000              0.0000           0.0000  (   0.00%)
black_box          0.0000           0.0000              0.0000           0.0000  (   0.00%)
clock_network      0.0000           0.0000              0.0000           0.0000  (   0.00%)
register       1.2719e-02       4.5482e-04        5.0490e+05       1.3679e-02  (  26.03%)
sequential     4.1635e-03       2.2525e-04        3.0340e+05       4.6921e-03  (   8.93%)
combinational  2.3439e-02       6.5937e-03        4.1449e+06       3.4177e-02  (  65.04%)
--------------------------------------------------------------------------------------------------
Total          4.0322e-02 mW     7.2738e-03 mW     4.9532e+06 pW     5.2549e-02 mW
```

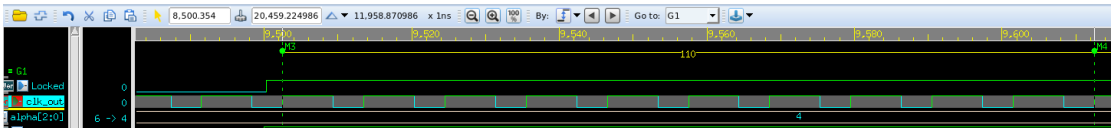
4. Gate-Level Simulation

(1) Waveform



從上圖可看到當 reset 完後，DCO 會在 clk_ref 的正緣開始產生震盪，並透過比較 clk_ref 與 clk_div 的相位差輸出 Lead_Lag 訊號進行 Binary Search，最後將 alpha code 鎖在 4 結束運算，Locked 訊號也轉變為 1，Locking Time 為 7 個 clk。

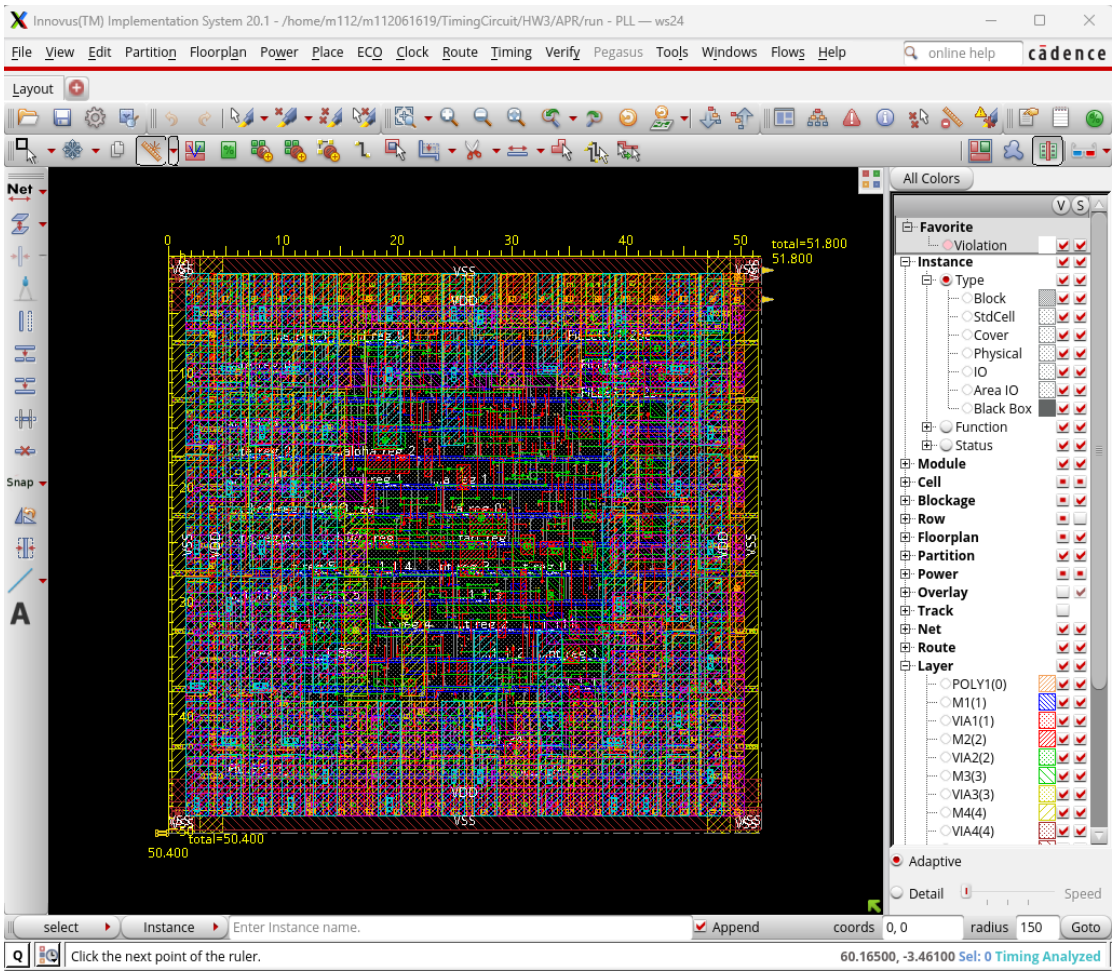
(2) Clock Cycle Time



在鎖定後測量 10 個 clk 的時間差可得到 110ns，換算 1 個 clk 的週期為 11ns，頻率約為 91MHz，其 error 為 11ns-10.87ns=130ps。

(b) APR report

1. Layout



Layout size=50.4 x 51.8 (um^2)

2. Power Analysis

```
Total Power
--------------------------------------------------------------------------------
---------
Total Internal Power:        0.03315290            76.0893%
Total Switching Power:       0.00807607            18.5354%
Total Leakage Power:         0.00234205             5.3753%
Total Power:                 0.04357103
--------------------------------------------------------------------------------
---------
Ended Static Power Report Generation: (cpu=0:00:00, real=0:00:00,
mem(process/total/peak)=1219.11MB/2695.46MB/1219.14MB)

Begin Creating Binary Database
Ended Creating Binary Database: (cpu=0:00:00, real=0:00:00,
mem(process/total/peak)=1733.40MB/3465.88MB/1733.42MB)

Output file is .//PLL.rpt
```

3. Verify

(1) Verify Geometry

```
 *** Starting Verify Geometry (MEM: 1376.0) ***

**WARN: (IMPVFG-257):   setVerifyGeometryMode/verifyGeometry command is obsolete
 and should not be used any more. It still works in this release but will be rem
oved in future release. You should change to use set_verify_drc_mode/verify_drc
which is the replacement tool for verifyGeometry.
  VERIFY GEOMETRY ..... Starting Verification
  VERIFY GEOMETRY ..... Initializing
  VERIFY GEOMETRY ..... Deleting Existing Violations
  VERIFY GEOMETRY ..... Creating Sub-Areas
                  ..... bin size: 3840
  VERIFY GEOMETRY ..... SubArea : 1 of 1
  VERIFY GEOMETRY ..... Cells          :  0 Viols.
  VERIFY GEOMETRY ..... SameNet        :  0 Viols.
  VERIFY GEOMETRY ..... Wiring         :  0 Viols.
  VERIFY GEOMETRY ..... Antenna        :  0 Viols.
VG: elapsed time: 0.00
Begin Summary ...
  Cells       : 0
  SameNet     : 0
  Wiring      : 0
  Antenna     : 0
  Short       : 0
  Overlap     : 0
End Summary

  Verification Complete : 0 Viols.  0 Wrngs.

**********End: VERIFY GEOMETRY**********
 *** verify geometry (CPU: 0:00:00.1  MEM: 75.8M)
```

(2) Verify Connectivity

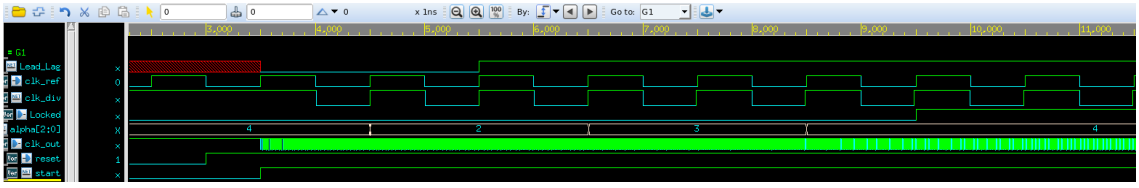
```
******** End: VERIFY CONNECTIVITY ********
  Verification Complete : 0 Viols.  0 Wrngs.
  (CPU Time: 0:00:00.0  MEM: 0.000M)
```

(3) Verify Antenna

```
******* START VERIFY ANTENNA ********
Report File: PLL.antenna.rpt
LEF Macro File: PLL.antenna.lef
Verification Complete: 0 Violations
******* DONE VERIFY ANTENNA ********
(CPU Time: 0:00:00.0  MEM: 0.000M)
```

(c) Post-Layout Simulation

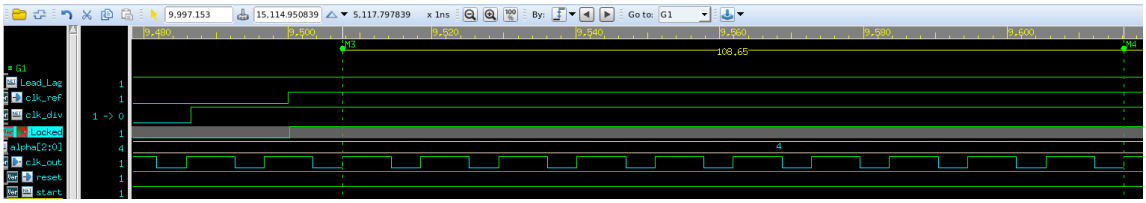
(1) Waveform



波形與 Pre-Layout Simulation 符合，alpha code

最後也鎖在 4

(2) Clock Cycle Time



Post-Layout Simulation 後測量鎖定後的 10 個 clk 的時間差為 108.65ns，換算 1 個 clk 的週期為 10.865ns，其 error 為 10.87ns-10.865ns=5ps，頻率約為 92.03MHz，Post-Layout Simulation 相較 Gate-Level Simulation 的誤差更小，更加接近 92MHz。