112-1 時序電路設計及應用

HW1

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一、 Source Code

1. C++ Code

HW1.cpp

```cpp
#include <stdio.h>
#include <iostream>
using namespace std;
int x;
int SuccessiveApproximation(int target)
{
    int x = 128;
    uint8_t control = 64;
    int y = 607;
    for (int i = 0; i < 8; i++)
    {
        if ((control == 0) & (y > target))
        {
            x = x - 1;
        }
        else if (y > target)
        {
            x = x - control;
        }
        else
        {
            x = x + control;
        }
        control = control >> 1;
        y = (x << 1) + (13 * x >> 5) + 300;
    }
    return x;
}
int main()
{
    cout << "Taget=550 , x=" << SuccessiveApproximation(550) << endl;
    cout << "Taget=800 , x=" << SuccessiveApproximation(800) << endl;
    return 0;
}
```

2. 模擬結果

```
PROBLEMS  OUTPUT  DEBUG CONSOLE  TERMINAL  PORTS

PS D:\TimingCircuit\HW1> .\HW1.exe
Taget=550 , x=104
Taget=800 , x=208
PS D:\TimingCircuit\HW1>
```

3. 演算法

演算法的步驟主要從中間值 x=128 開始搜索，方程式

y=2.4*x+300 所對應的 y 值為 607，這邊使用一組叫 control 的二進位數值 0100_0000 來做控制，只要 y 大於目標值就將 x 減去 control，小於就將 x 加上 control，之後將 control 右移一位並算出 y，其中最後一次迴圈 control 會變成 0 無法運算，故再加上判斷式去修正，從模擬結果也能看出輸出能逼近目標值。

二、 Verilog Code

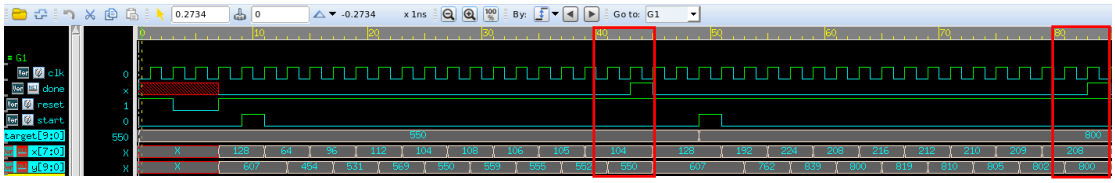
1. Verilog

```
`timescale 1ns / 100ps
module SA(
    input [9:0]target,
    input clk,
    input reset,
    input start,
    output reg done,
    output reg[7:0]x,
    output reg[9:0]y
);
    reg [7:0]control;
    reg [1:0]state,next_state;

    parameter [1:0] IDLE =0;
    parameter [1:0] COMP = 1;
    parameter [1:0] CALC = 2;
    parameter [1:0] FINISH =3;

    always@(posedge clk)begin
        if(~reset)begin
            state<=IDLE;
        end
        else begin
            state<=next_state;
            case(state)
                IDLE:begin
                    y=10'd607;
                    x=8'b1000_0000;
                    done=1'b0;
                    control=8'b0100_0000;
                end
                COMP:begin
                    if((control==8'd0)&(y>target))begin
                        x=x-1;
                    end
                    else if(y>target)begin
                        x=x-control;
                    end
                    else begin
                        x=x+control;
                    end
                end
                CALC:begin
                    control=control>>1;
                    y=(x<<1)+(13*x>>5)+300;
                end
                FINISH:done=1'b1;
            endcase
        end
    end

    always@(*)begin
            case(state)
                IDLE:next_state=(start)?COMP:IDLE;
                COMP:next_state=CALC;
                CALC:next_state=(control==8'd0)?FINISH:COMP;
                FINISH:next_state=IDLE;
                default:next_state=IDLE;
            endcase
    end
endmodule
```

2. 模擬結果

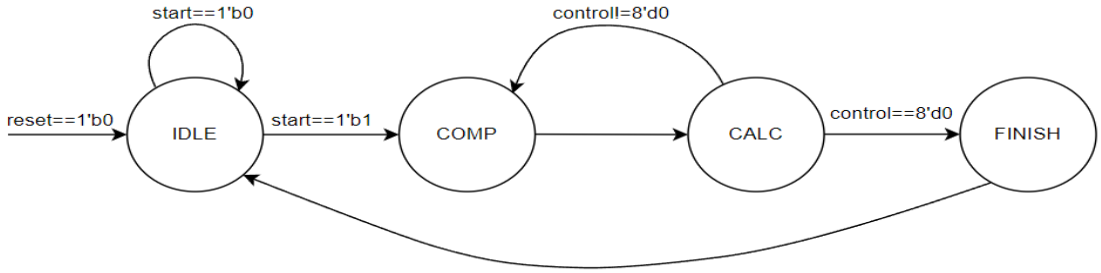
```
*Verdi* : End of traversing.
                  0 y=   x x=  x
                  7 y= 607 x=128
                 11 y= 607 x= 64
                 13 y= 454 x= 64
                 15 y= 454 x= 96
                 17 y= 531 x= 96
                 19 y= 531 x=112
                 21 y= 569 x=112
                 23 y= 569 x=104
                 25 y= 550 x=104
                 27 y= 550 x=108
                 29 y= 559 x=108
                 31 y= 559 x=106
                 33 y= 555 x=106
                 35 y= 555 x=105
                 37 y= 552 x=105
                 39 y= 552 x=104
                 41 y= 550 x=104
-------------------------------------------------
Done:         Taget= 550 y= 550 x=104
-------------------------------------------------
                 45 y= 607 x=128
                 51 y= 607 x=192
                 53 y= 762 x=192
                 55 y= 762 x=224
                 57 y= 839 x=224
                 59 y= 839 x=208
                 61 y= 800 x=208
                 63 y= 800 x=216
                 65 y= 819 x=216
                 67 y= 819 x=212
                 69 y= 810 x=212
                 71 y= 810 x=210
                 73 y= 805 x=210
                 75 y= 805 x=209
                 77 y= 802 x=209
                 79 y= 802 x=208
                 81 y= 800 x=208
-------------------------------------------------
Done:         Taget= 800 y= 800 x=208
-------------------------------------------------
                 85 y= 607 x=128
$finish called from file "tb.v", line 50.
$finish at simulation time                1170
           V C S   S i m u l a t i o n   R e p o r t
Time: 117000 ps
CPU Time:      0.380 seconds;       Data structure size:   0.0Mb
```

3. RTL Simulation



從波形中，可看到 start 電路開始運作，逐一比較是否要加或減 2 的次方，從一開始的 64、32…等，當 taget=550 且 done 訊號拉起時，表示運運完成 x=104，而 taget=800 時，x=208，與 C++模擬結果相符。

4. FSM



IDLE:reset 後進行數值初始化，當 start=1 時 state 切換到 COMP

COMP:比較 y 與 target 的大小來進行 x 的運算

CALC:將 control 右移 1 位並算出 y 值，先將 x 左移一位(乘 2)，再加上 x 乘上 13 右移 5 位(約等於 0.4)，最後加上 300。

FINISH:輸出 done 表示運算結果結束並回到初始狀態

三、 Synthesis report

1. Area(clk=1.4ns)

```
****************************************
Report : area
Design : SA
Version: R-2020.09-SP5
Date   : Thu Nov  9 19:39:52 2023
****************************************

Information: Updating design information... (UID-85)
Library(s) Used:

    slow (File: /usr/cadtool/ee5216/CBDK_TSMC90GUTM_Arm_f1.0/CIC/SynopsysDC/db/slow.db)

Number of ports:                          104
Number of nets:                           543
Number of cells:                          466
Number of combinational cells:            428
Number of sequential cells:                28
Number of macros/black boxes:               0
Number of buf/inv:                        109
Number of references:                     105

Combinational area:              1774.584040
Buf/Inv area:                     259.660808
Noncombinational area:            460.051198
Macro/Black Box area:               0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                 2234.635238
Total area:                 undefined
```

Gate count=2234.635238/2.8224=791.75

2. Timing

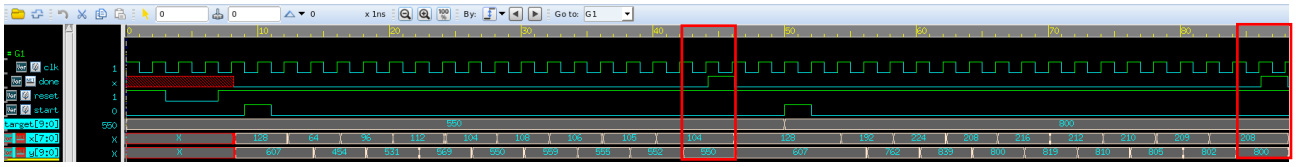
```
****************************************
Report : timing
         -path full
         -delay max
         -max_paths 1
Design : SA
Version: R-2020.09-SP5
Date   : Thu Nov  9 19:49:44 2023
****************************************

Operating Conditions: slow   Library: slow
Wire Load Model Mode: top

  Startpoint: x_reg_5_ (rising edge-triggered flip-flop clocked by clk)
  Endpoint: y_reg_7_ (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: max

  Point                                                   Incr       Path
  -----------------------------------------------------------------------
  clock clk (rise edge)                                   0.00       0.00
  clock network delay (ideal)                             0.00       0.00
  x_reg_5_/CK (DFFHQX4)                                   0.00       0.00 r
  x_reg_5_/Q (DFFHQX4)                                    0.12       0.12 f
  U92/Y (BUFX2)                                           0.11       0.22 f
  U121/Y (OAI2BB1X2)                                      0.04       0.27 r
  U129/Y (OAI2BB1X2)                                      0.06       0.32 f
  U105/Y (INVX4)                                          0.05       0.37 r
  U86/Y (NAND2X2)                                         0.05       0.42 f
  U215/Y (NAND3X4)                                        0.04       0.46 r
  U210/Y (NAND2X4)                                        0.05       0.51 f
  U123/Y (CLKINVX4)                                       0.03       0.54 r
  U234/Y (OAI32X2)                                        0.04       0.57 f
  U126/Y (NAND2BX2)                                       0.10       0.68 f
  U235/Y (INVX4)                                          0.04       0.72 r
  U91/Y (NAND2X2)                                         0.04       0.76 f
  U134/Y (AND2X4)                                         0.08       0.84 f
  U357/Y (NAND2BX8)                                       0.07       0.91 f
  U365/Y (OAI2BB1X4)                                      0.04       0.95 r
  add_0_root_add_0_root_add_45_2/B_5_ (SA_DW01_add_6)     0.00       0.95 r
  add_0_root_add_0_root_add_45_2/U93/Y (NAND2X4)          0.04       0.99 f
  add_0_root_add_0_root_add_45_2/U89/Y (OAI21X4)          0.08       1.07 r
  add_0_root_add_0_root_add_45_2/U81/Y (INVXL)            0.05       1.12 f
  add_0_root_add_0_root_add_45_2/U80/Y (OAI2BB1X2)        0.04       1.16 r
  add_0_root_add_0_root_add_45_2/U90/Y (INVX1)            0.03       1.20 f
  add_0_root_add_0_root_add_45_2/U88/Y (NAND2X2)          0.03       1.23 r
  add_0_root_add_0_root_add_45_2/U102/Y (NAND2X2)         0.03       1.26 f
  add_0_root_add_0_root_add_45_2/SUM[7] (SA_DW01_add_6)
                                                          0.00       1.26 f
  U152/Y (INVX2)                                          0.03       1.29 r
  U151/Y (OAI2BB2X2)                                      0.04       1.33 f
  y_reg_7_/D (DFFYQX2)                                    0.00       1.33 f
  data arrival time                                                  1.33

  clock clk (rise edge)                                   1.40       1.40
  clock network delay (ideal)                             0.00       1.40
  y_reg_7_/CK (DFFYQX2)                                   0.00       1.40 r
  library setup time                                     -0.07       1.33
  data required time                                                 1.33
  -----------------------------------------------------------------------
  data required time                                                 1.33
  data arrival time                                                 -1.33
  -----------------------------------------------------------------------
  slack (MET)                                                        0.00
```

Max frequency=1/1.4ns=714.28MHz

3. Power

```
****************************************
Report : power
        -analysis_effort low
Design : SA
Version: R-2020.09-SP5
Date   : Thu Nov  9 19:49:45 2023
****************************************


Library(s) Used:

    slow (File: /usr/cadtool/ee5216/CBDK_TSMC90GUTM_Arm_f1.0/CIC/SynopsysDC/db/slow.db)


Operating Conditions: slow   Library: slow
Wire Load Model Mode: top


Global Operating Voltage = 0.9
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  = 364.0699 uW   (90%)
  Net Switching Power  =  41.3387 uW   (10%)
                         ---------
Total Dynamic Power    = 405.4085 uW  (100%)

Cell Leakage Power     =  10.6682 uW


                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %    )  Attrs
--------------------------------------------------------------------------------------------------
io_pad             0.0000           0.0000              0.0000             0.0000  (   0.00%)
memory             0.0000           0.0000              0.0000             0.0000  (   0.00%)
black_box          0.0000           0.0000              0.0000             0.0000  (   0.00%)
clock_network      0.0000           0.0000              0.0000             0.0000  (   0.00%)
register           0.3175        6.1684e-03          1.8306e+06             0.3255  (  78.23%)
sequential         0.0000           0.0000              0.0000             0.0000  (   0.00%)
combinational   4.6578e-02        3.5170e-02          8.8376e+06          9.0585e-02 (  21.77%)
--------------------------------------------------------------------------------------------------
Total              0.3641 mW      4.1339e-02 mW       1.0668e+07 pW         0.4161 mW
```

4. Gate-Level Simulation

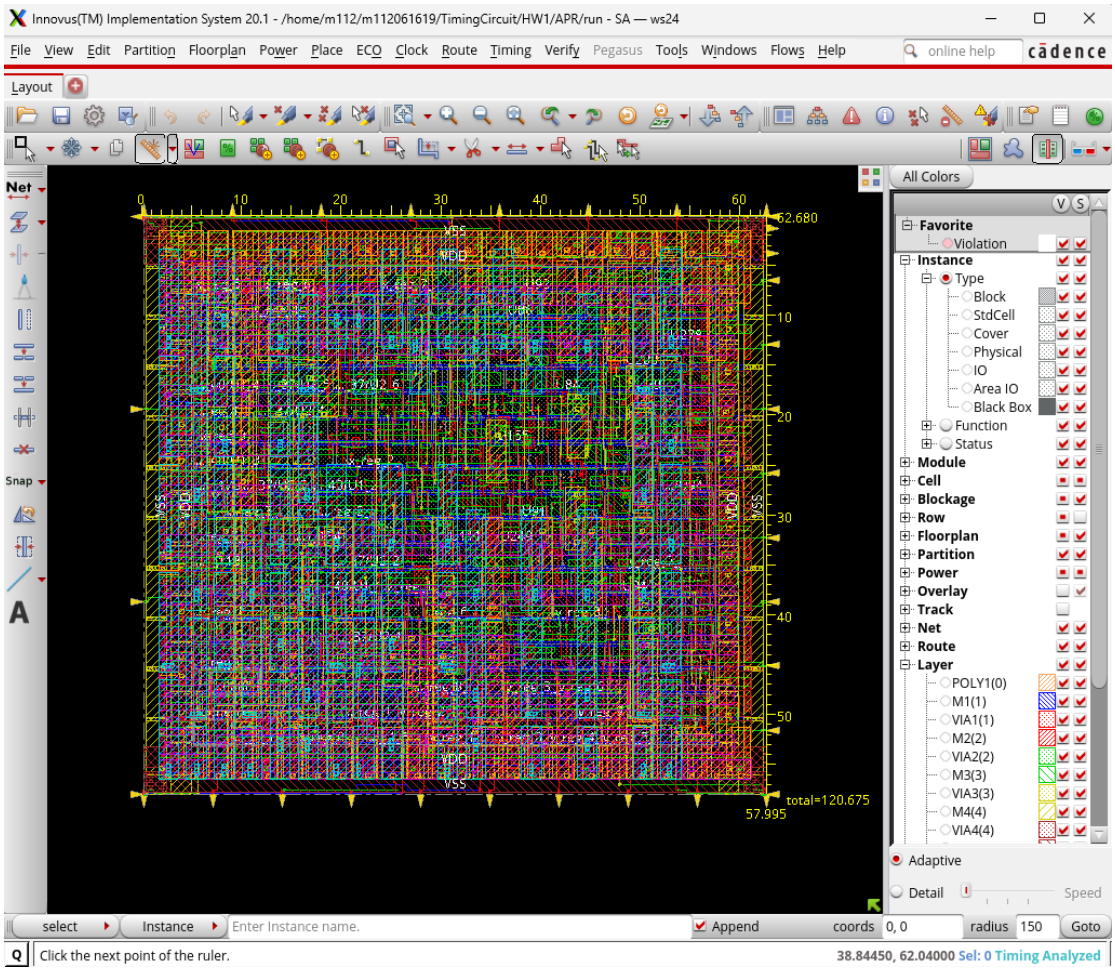


5. Insight

經過合成後，在沒有經過 wire load 的情況下，area 為 2234.635 (um^2)，Timing 的部分為透過 clk=1.4ns 去合成的，且 slack>=0，顯示已達最大頻率=714.28MHz。

四、 APR report

1. Layout



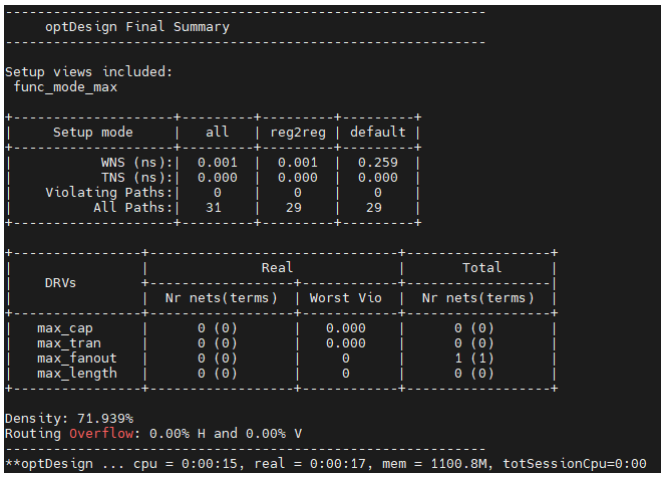
Layout size=62.68 x 57.995 (um^2)

2. Power Analysis

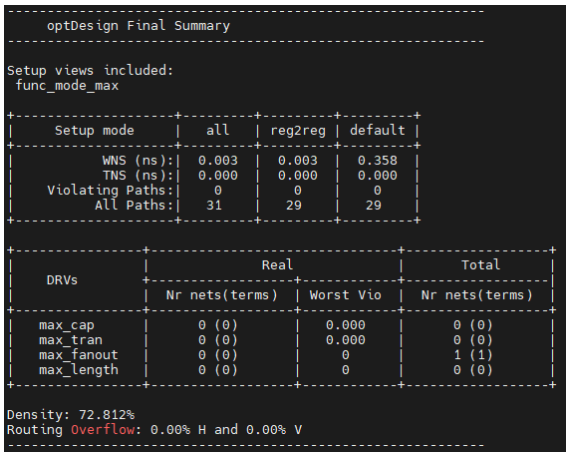
```
Total Power
--------------------------------------------------------------------------------
---------
Total Internal Power:        0.48605982            68.3842%
Total Switching Power:       0.21933970            30.8591%
Total Leakage Power:         0.00537812             0.7567%
Total Power:                 0.71077764
--------------------------------------------------------------------------------
---------
Ended Static Power Report Generation: (cpu=0:00:00, real=0:00:00,
```

3. Timing analysis

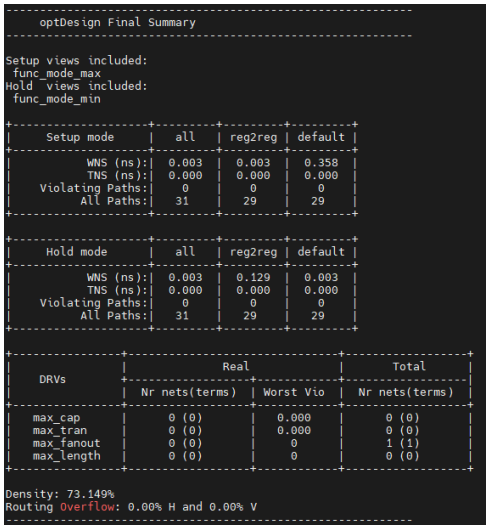
(1) pre-CTS



(2) post-CTS



(3) pre-CTS hold



確認各階段的 clock tree synthesis 中出現 WNS 皆優化至大於 0

4. Verify

(1) verifyGeometry

```
 *** Starting Verify Geometry (MEM: 1356.2) ***

**WARN: (IMPVFG-257):   setVerifyGeometryMode/verifyGeometry command is obsolete
 and should not be used any more. It still works in this release but will be rem
oved in future release. You should change to use set_verify_drc_mode/verify_drc
which is the replacement tool for verifyGeometry.
  VERIFY GEOMETRY ..... Starting Verification
  VERIFY GEOMETRY ..... Initializing
  VERIFY GEOMETRY ..... Deleting Existing Violations
  VERIFY GEOMETRY ..... Creating Sub-Areas
                  ..... bin size: 3840
  VERIFY GEOMETRY ..... SubArea : 1 of 1
  VERIFY GEOMETRY ..... Cells          :  0 Viols.
  VERIFY GEOMETRY ..... SameNet        :  0 Viols.
  VERIFY GEOMETRY ..... Wiring         :  0 Viols.
  VERIFY GEOMETRY ..... Antenna        :  0 Viols.
VG: elapsed time: 0.00
Begin Summary ...
  Cells       : 0
  SameNet     : 0
  Wiring      : 0
  Antenna     : 0
  Short       : 0
  Overlap     : 0
End Summary

  Verification Complete : 0 Viols.  0 Wrngs.

**********End: VERIFY GEOMETRY**********
 *** verify geometry (CPU: 0:00:00.2  MEM: 74.3M)
```

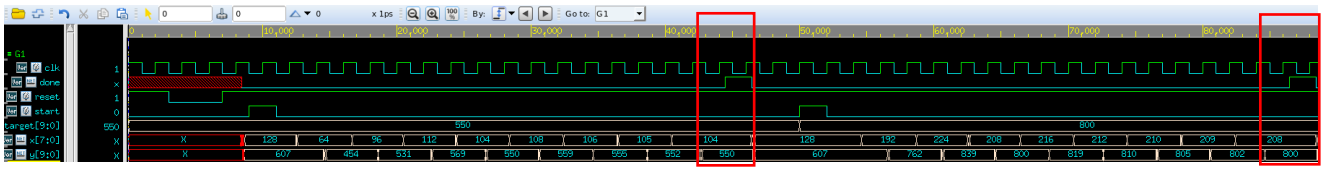
(2) verifyConnectivity

```
******** End: VERIFY CONNECTIVITY ********
  Verification Complete : 0 Viols.  0 Wrngs.
```

(3) verifyProcessAntenna

```
******* START VERIFY ANTENNA ********
Report File: SA.antenna.rpt
LEF Macro File: SA.antenna.lef
Verification Complete: 0 Violations
******* DONE VERIFY ANTENNA ********
```

5. Post-Layout Simulation



6. Pre-Layout vs Post-Layout

從觀察波形中，可看到 Pre-Layout 並無明顯的 delay 的資訊，Post-Layout 則可明確的看到資訊在傳遞過程中的 delay 及資料的轉換過程，其顯示在 APR 過程中的繞線及擺放位置都有可能影響到時序的表現，因此需要經過 Post-

Layout simulation 來做驗證電路是否能成功的運作。