112-1 時序電路設計及應用

HW2

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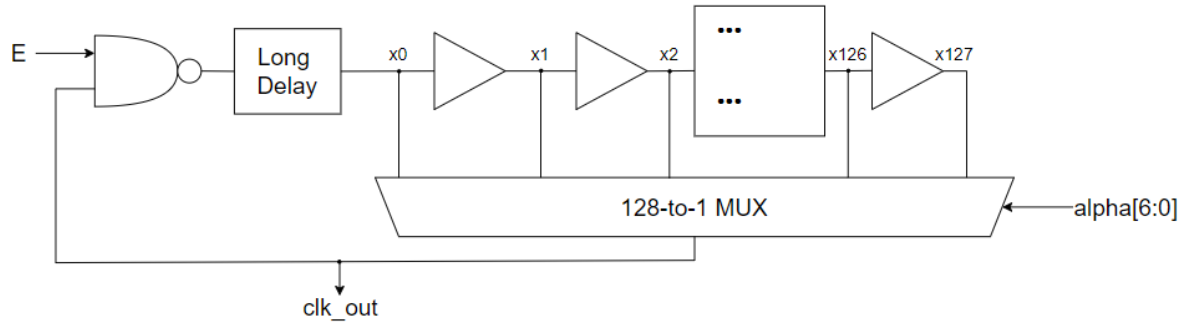
(a) Path-Selection-Based DCO

1. Architecture



此處使用 128-to-1 的多工器的架構，採用 alpha code 來選擇的適當的 path，訊號 E 則代表 enable，並與輸出 clk_out 做 nand 來產生振動頻率，Long Delay 則是使用 25 個 buffer 串聯，詳細電路如下圖 verilog code 所示。

2. Verilog

```
`timescale 1ps / 100fs
module DCO#(
    parameter alpha_num = 7,
    parameter lambda_num = 128,
    parameter delay_num = 25
)
(
    input E,
    input [alpha_num-1:0]alpha,
    output clk_out

);
    wire [lambda_num-1:0]u;
    wire [delay_num-1:0]g;

    NAND2X2 NAND0(.A(E),.B(clk_out),.Y(g[0]));

    genvar j;
    generate
        for(j=0;j<delay_num-1;j=j+1)begin:delay
            TBUFX1 TBUF0(.A(g[j]),.OE(1'b1),.Y(g[j+1]));
        end
    endgenerate

    assign u[0]=g[delay_num-1];

    genvar i;
    generate
        for(i=0;i<lambda_num-1;i=i+1)begin:RO
            TBUFX2 TBUF1(.A(u[i]),.OE(1'b1),.Y(u[i+1]));
        end
    endgenerate

    MUX128to1 m0(.A(u),.sel(alpha),.Dout(clk_out));

endmodule
```

Long Delay

Ring Oscillator

3. Synthesis report

(1) Area

```
****************************************
Report : area
Design : DCO
Version: R-2020.09-SP5
Date   : Mon Nov 20 00:50:31 2023
****************************************

Information: Updating design information... (UID-85)
Information: Timing loop detected. (OPT-150)
       U2/A U2/Y delay_0__TBUF0/A delay_0__TBUF0/Y delay_1__TBUF0/A delay_1__TBUF0/Y delay_2__TBUF0/A delay_2__TBUF0/Y delay_3__TBUF0/A delay_3__TBUF0/Y delay_4__TBUF0/A delay_4__TBUF0/Y delay_5__TBUF0/A delay_5__TBUF0/Y delay_6__TBUF0/A delay_6__TBUF0/Y delay_7__TBUF0/A delay_7__TBUF0/Y delay_8__TBUF0/A delay_8__TBUF0/Y delay_9__TBUF0/A delay_9__TBUF0/Y delay_10__TBUF0/A delay_10__TBUF0/Y delay_11__TBUF0/A delay_11__TBUF0/Y delay_12__TBUF0/A delay_12__TBUF0/Y delay_13__TBUF0/A delay_13__TBUF0/Y delay_14__TBUF0/A delay_14__TBUF0/Y delay_15__TBUF0/A delay_15__TBUF0/Y delay_16__TBUF0/A delay_16__TBUF0/Y delay_17__TBUF0/A delay_17__TBUF0/Y delay_18__TBUF0/A delay_18__TBUF0/Y delay_19__TBUF0/A delay_19__TBUF0/Y delay_20__TBUF0/A delay_20__TBUF0/Y delay_21__TBUF0/A delay_21__TBUF0/Y delay_22__TBUF0/A delay_22__TBUF0/Y delay_23__TBUF0/A delay_23__TBUF0/Y RO_0__TBUF1/A RO_0__TBUF1/Y RO_1__TBUF1/A RO_1__TBUF1/Y RO_2__TBUF1/A RO_2__TBUF1/Y RO_3__TBUF1/A RO_3__TBUF1/Y RO_4__TBUF1/A RO_4__TBUF1/Y RO_5__TBUF1/A RO_5__TBUF1/Y RO_6__TBUF1/A RO_6__TBUF1/Y m0/U13/A0 m0/U13/Y m0/U9/A m0/U9/Y m0/U3/A m0/U3/Y m0/U2/D m0/U2/Y m0/U1/B m0/U1/Y
Warning: Disabling timing arc between pins 'A' and 'Y' on cell 'U2'
        to break a timing loop. (OPT-314)
Library(s) Used:

    slow (File: /usr/cadtool/ee5216/CBDK_TSMC90GUTM_Arm_f1.0/CIC/SynopsysDC/db/slow.db)

Number of ports:                          145
Number of nets:                           415
Number of cells:                          272
Number of combinational cells:            119
Number of sequential cells:               151
Number of macros/black boxes:               0
Number of buf/inv:                          3
Number of references:                       3

Combinational area:               508.032013
Buf/Inv area:                       6.350400
Noncombinational area:            958.910396
Macro/Black Box area:               0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                 1466.942408
Total area:                 undefined
```

Total cell area:1466.942408

Gate count:1466.942408/2.8224=519.75

(2) Timing

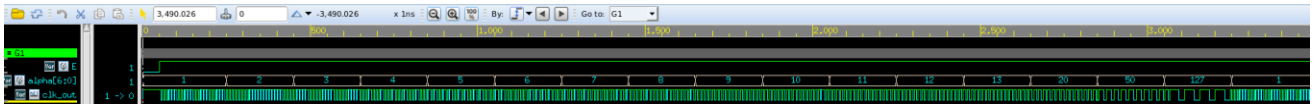
```
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : DCO
Version: R-2020.09-SP5
Date   : Mon Nov 20 00:50:31 2023
****************************************

Operating Conditions: slow   Library: slow
Wire Load Model Mode: top

  Startpoint: E (input port)
  Endpoint: clk_out (output port)
  Path Group: (none)
  Path Type: max

  Point                                    Incr       Path
  -----------------------------------------------------------
  input external delay                     0.00       0.00 r
  E (in)                                   0.01       0.01 r
  U2/Y (NAND2X8)                           0.02       0.03 f
  delay_0__TBUF0/Y (TBUFX1)                0.16       0.19 f
  delay_1__TBUF0/Y (TBUFX1)                0.17       0.36 f
  delay_2__TBUF0/Y (TBUFX1)                0.17       0.53 f
  delay_3__TBUF0/Y (TBUFX1)                0.17       0.71 f
  delay_4__TBUF0/Y (TBUFX1)                0.17       0.88 f
  delay_5__TBUF0/Y (TBUFX1)                0.17       1.05 f
  delay_6__TBUF0/Y (TBUFX1)                0.17       1.22 f
  delay_7__TBUF0/Y (TBUFX1)                0.17       1.39 f
  delay_8__TBUF0/Y (TBUFX1)                0.17       1.56 f
  delay_9__TBUF0/Y (TBUFX1)                0.17       1.74 f
  delay_10__TBUF0/Y (TBUFX1)               0.17       1.91 f
  delay_11__TBUF0/Y (TBUFX1)               0.17       2.08 f
  delay_12__TBUF0/Y (TBUFX1)               0.17       2.25 f
  delay_13__TBUF0/Y (TBUFX1)               0.17       2.42 f
  delay_14__TBUF0/Y (TBUFX1)               0.17       2.59 f
  delay_15__TBUF0/Y (TBUFX1)               0.17       2.77 f
  delay_16__TBUF0/Y (TBUFX1)               0.17       2.94 f
  delay_17__TBUF0/Y (TBUFX1)               0.17       3.11 f
  delay_18__TBUF0/Y (TBUFX1)               0.17       3.28 f
  delay_19__TBUF0/Y (TBUFX1)               0.17       3.45 f
  delay_20__TBUF0/Y (TBUFX1)               0.17       3.63 f
  delay_21__TBUF0/Y (TBUFX1)               0.17       3.80 f
  delay_22__TBUF0/Y (TBUFX1)               0.17       3.97 f
  delay_23__TBUF0/Y (TBUFX1)               0.18       4.15 f
  RO_0__TBUF1/Y (TBUFX1)                   0.19       4.34 f
  RO_1__TBUF1/Y (TBUFX1)                   0.19       4.53 f
  RO_2__TBUF1/Y (TBUFX1)                   0.19       4.72 f
  RO_3__TBUF1/Y (TBUFX1)                   0.19       4.90 f
  RO_4__TBUF1/Y (TBUFX1)                   0.19       5.09 f
  RO_5__TBUF1/Y (TBUFX1)                   0.19       5.28 f
  RO_6__TBUF1/Y (TBUFX1)                   0.19       5.47 f
  RO_86__TBUF1/Y (TBUFX1)                  0.19      20.48 f
  RO_87__TBUF1/Y (TBUFX1)                  0.19      20.67 f
  RO_88__TBUF1/Y (TBUFX1)                  0.19      20.86 f
  RO_89__TBUF1/Y (TBUFX1)                  0.19      21.05 f
  RO_90__TBUF1/Y (TBUFX1)                  0.19      21.24 f
  RO_91__TBUF1/Y (TBUFX1)                  0.19      21.42 f
  RO_92__TBUF1/Y (TBUFX1)                  0.19      21.61 f
  RO_93__TBUF1/Y (TBUFX1)                  0.19      21.80 f
  RO_94__TBUF1/Y (TBUFX1)                  0.19      21.99 f
  RO_95__TBUF1/Y (TBUFX1)                  0.19      22.18 f
  RO_96__TBUF1/Y (TBUFX1)                  0.19      22.36 f
  RO_97__TBUF1/Y (TBUFX1)                  0.19      22.55 f
  RO_98__TBUF1/Y (TBUFX1)                  0.19      22.74 f
  RO_99__TBUF1/Y (TBUFX1)                  0.19      22.93 f
  RO_100__TBUF1/Y (TBUFX1)                 0.19      23.11 f
  RO_101__TBUF1/Y (TBUFX1)                 0.19      23.30 f
  RO_102__TBUF1/Y (TBUFX1)                 0.19      23.49 f
  RO_103__TBUF1/Y (TBUFX1)                 0.19      23.68 f
  RO_104__TBUF1/Y (TBUFX1)                 0.19      23.86 f
  RO_105__TBUF1/Y (TBUFX1)                 0.19      24.05 f
  RO_106__TBUF1/Y (TBUFX1)                 0.19      24.24 f
  RO_107__TBUF1/Y (TBUFX1)                 0.19      24.43 f
  RO_108__TBUF1/Y (TBUFX1)                 0.19      24.62 f
  RO_109__TBUF1/Y (TBUFX1)                 0.19      24.80 f
  RO_110__TBUF1/Y (TBUFX1)                 0.19      24.99 f
  RO_111__TBUF1/Y (TBUFX1)                 0.19      25.18 f
  RO_112__TBUF1/Y (TBUFX1)                 0.19      25.37 f
  RO_113__TBUF1/Y (TBUFX1)                 0.19      25.55 f
  RO_114__TBUF1/Y (TBUFX1)                 0.19      25.74 f
  RO_115__TBUF1/Y (TBUFX1)                 0.19      25.93 f
  RO_116__TBUF1/Y (TBUFX1)                 0.19      26.12 f
  RO_117__TBUF1/Y (TBUFX1)                 0.19      26.30 f
  RO_118__TBUF1/Y (TBUFX1)                 0.19      26.49 f
  RO_119__TBUF1/Y (TBUFX1)                 0.19      26.68 f
  RO_120__TBUF1/Y (TBUFX1)                 0.19      26.87 f
  RO_121__TBUF1/Y (TBUFX1)                 0.19      27.06 f
  RO_122__TBUF1/Y (TBUFX1)                 0.19      27.24 f
  RO_123__TBUF1/Y (TBUFX1)                 0.19      27.43 f
  RO_124__TBUF1/Y (TBUFX1)                 0.19      27.62 f
  RO_125__TBUF1/Y (TBUFX1)                 0.19      27.81 f
  RO_126__TBUF1/Y (TBUFX1)                 0.18      27.98 f
  m0/A[127] (MUX128to1)                    0.00      27.98 f
  m0/U5/Y (AOI22XL)                        0.11      28.09 r
  m0/U4/Y (NAND4X1)                        0.13      28.22 f
  m0/U3/Y (NOR2X1)                         0.07      28.29 r
  m0/U2/Y (MX4XL)                          0.15      28.44 r
  m0/U1/Y (MXI2X1)                         0.15      28.58 f
  m0/Dout (MUX128to1)                      0.00      28.58 f
  clk_out (out)                            0.00      28.58 f
  data arrival time                                  28.58
```

(3) Power

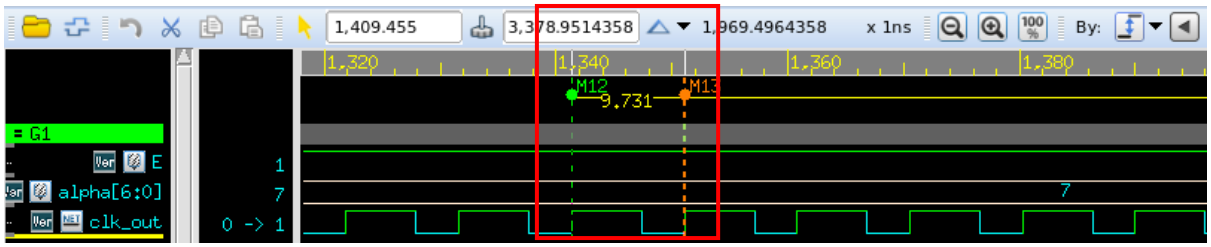
```
****************************************
Report : power
        -analysis_effort low
Design : DCO
Version: R-2020.09-SP5
Date   : Mon Nov 20 00:50:32 2023
****************************************


Library(s) Used:

    slow (File: /usr/cadtool/ee5216/CBDK_TSMC90GUTM_Arm_f1.0/CIC/SynopsysDC/db/slow.db)


Operating Conditions: slow   Library: slow
Wire Load Model Mode: top


Global Operating Voltage = 0.9
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  = 440.6039 uW   (72%)
  Net Switching Power  = 172.4359 uW   (28%)
                         ---------
Total Dynamic Power    = 613.0398 uW  (100%)

Cell Leakage Power     =   3.6042 uW

Information: report_power power group summary does not include estimated clock tree power. (PWR-789)

                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %    )  Attrs
--------------------------------------------------------------------------------------------------
io_pad           0.0000           0.0000              0.0000             0.0000  (   0.00%)
memory           0.0000           0.0000              0.0000             0.0000  (   0.00%)
black_box        0.0000           0.0000              0.0000             0.0000  (   0.00%)
clock_network    0.0000           0.0000              0.0000             0.0000  (   0.00%)
register         0.0000           0.0000              0.0000             0.0000  (   0.00%)
sequential       0.0000           0.0000              0.0000             0.0000  (   0.00%)
combinational    0.4406           0.1724          3.6042e+06             0.6166  ( 100.00%)
--------------------------------------------------------------------------------------------------
Total            0.4406 mW        0.1724 mW       3.6042e+06 pW          0.6166 mW
```

(4) Gate-Level Simulation

a. E 從 0 到 1

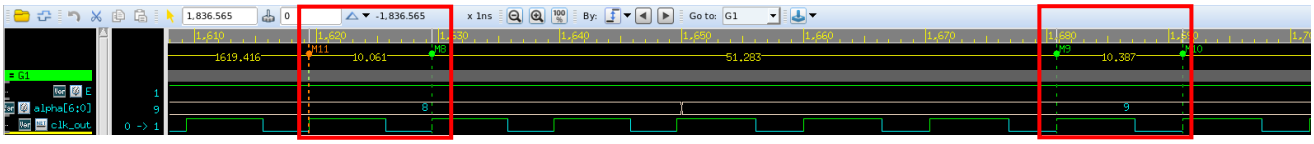


b. Alpha=7



Alpha=7 clock period=9.731ns

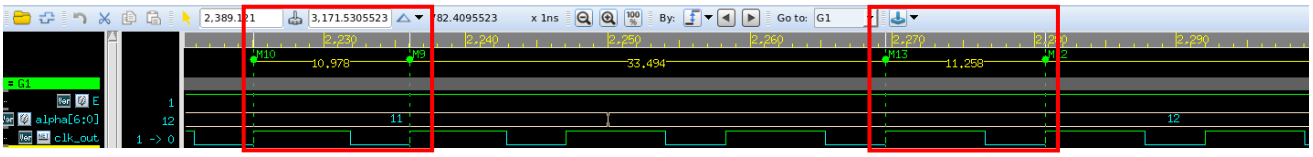
c. Alpha=8、Alpha=9



Alpha=8 clock period=10.061ns

Alpha=9 clock period=10.387ns

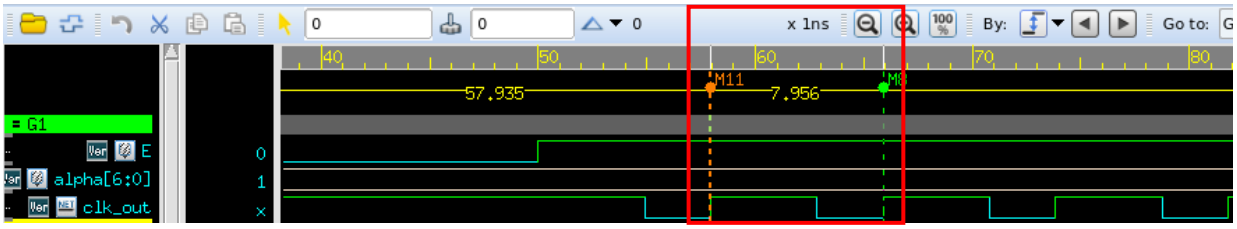
d. Alpha=11、Alpha=12



Alpha=11 clock period=10.978ns

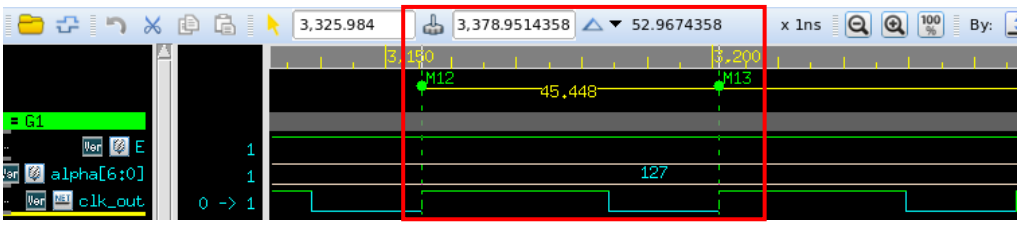
Alpha=12 clock period=11.258ns

e. Alpha=1



Alpha=1 clock period=7.956ns

f. Alpha=127



Alpha=127 clock period=45.448ns

g. Summary

Period range:7.956ns~45.448ns

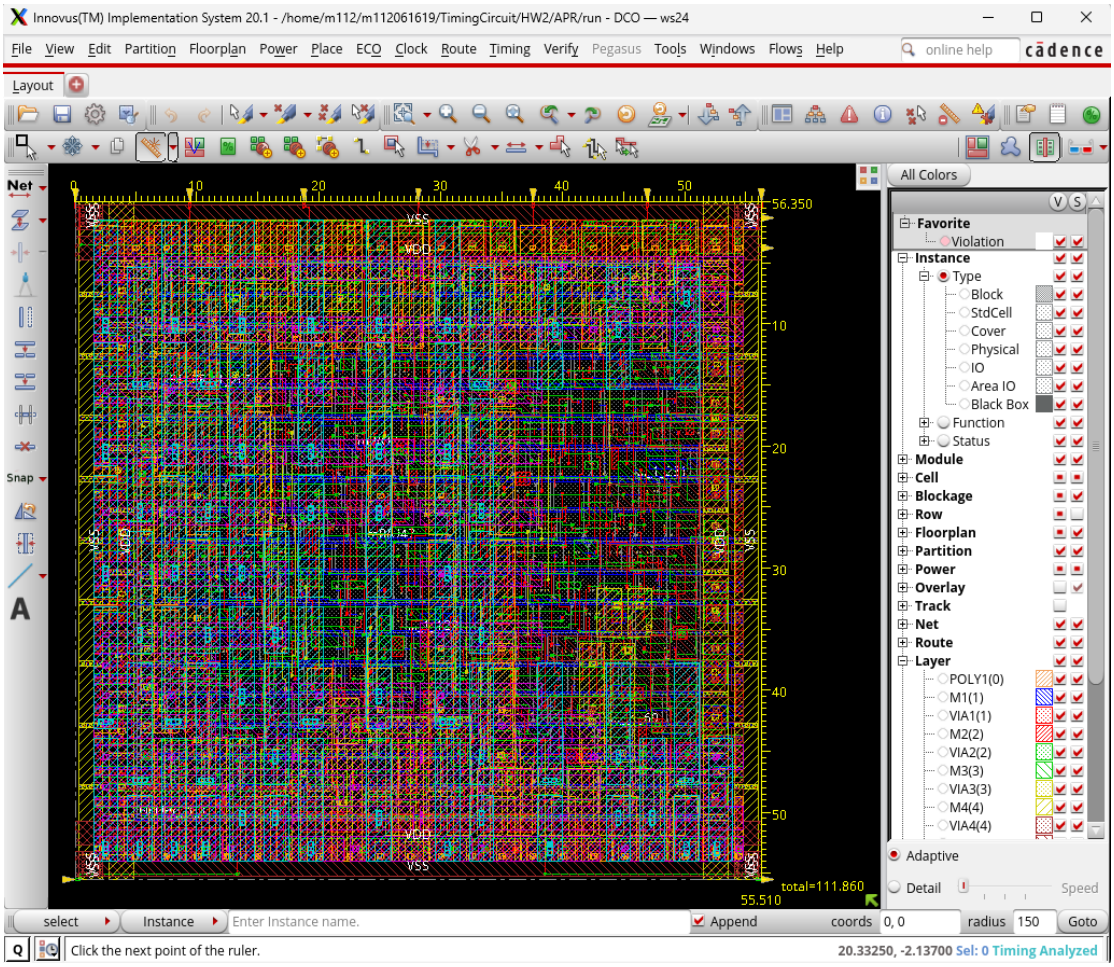
Frequency range:22.003MHz~125.691MHz

Time resolution:(45.448-7.956)/(127-1)=0.2975ns

Alpha Code 從 8~11 會 clock period 落在[10ns, 11ns]

(b) APR report

1. Layout



Layout size=55.51 x 56.35 (um^2)

2. Power Analysis

```
Total Power
-------------------------------------------------------------------------------
---------
Total Internal Power:        0.02164731            47.9825%
Total Switching Power:       0.02065817            45.7900%
Total Leakage Power:         0.00280950             6.2274%
Total Power:                 0.04511498
-------------------------------------------------------------------------------
---------
Ended Static Power Report Generation: (cpu=0:00:00, real=0:00:00,
mem(process/total/peak)=1054.40MB/2654.21MB/1112.02MB)

Begin Creating Binary Database
Ended Creating Binary Database: (cpu=0:00:00, real=0:00:00,
mem(process/total/peak)=1565.36MB/3424.63MB/1565.37MB)

Output file is .//DCO.rpt
```

3. Verify

(1) Verify Geometry

```
 *** Starting Verify Geometry (MEM: 1354.6) ***

**WARN: (IMPVFG-257):   setVerifyGeometryMode/verifyGeometry command is obsolete
 and should not be used any more. It still works in this release but will be rem
oved in future release. You should change to use set_verify_drc_mode/verify_drc
which is the replacement tool for verifyGeometry.
  VERIFY GEOMETRY ..... Starting Verification
  VERIFY GEOMETRY ..... Initializing
  VERIFY GEOMETRY ..... Deleting Existing Violations
  VERIFY GEOMETRY ..... Creating Sub-Areas
                  ..... bin size: 3840
  VERIFY GEOMETRY ..... SubArea : 1 of 1
  VERIFY GEOMETRY ..... Cells          :  0 Viols.
  VERIFY GEOMETRY ..... SameNet        :  0 Viols.
  VERIFY GEOMETRY ..... Wiring         :  0 Viols.
  VERIFY GEOMETRY ..... Antenna        :  0 Viols.
VG: elapsed time: 0.00
Begin Summary ...
  Cells       : 0
  SameNet     : 0
  Wiring      : 0
  Antenna     : 0
  Short       : 0
  Overlap     : 0
End Summary

  Verification Complete : 0 Viols.  0 Wrngs.

**********End: VERIFY GEOMETRY**********
 *** verify geometry (CPU: 0:00:00.1  MEM: 77.3M)
```

(2) Verify Connectivity

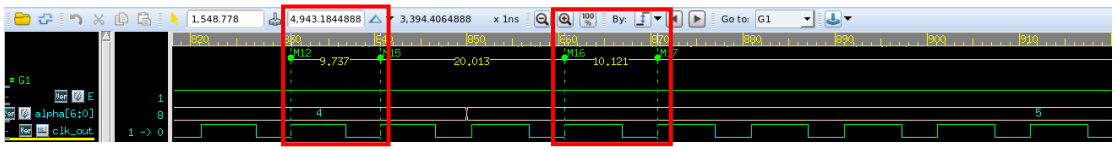
```
******** End: VERIFY CONNECTIVITY ********
  Verification Complete : 0 Viols.  0 Wrngs.
  (CPU Time: 0:00:00.0  MEM: 0.000M)
```

(3) Verify Antenna

```
******* START VERIFY ANTENNA ********
Report File: DCO.antenna.rpt
LEF Macro File: DCO.antenna.lef
Verification Complete: 0 Violations
******* DONE VERIFY ANTENNA ********
(CPU Time: 0:00:00.0  MEM: 0.000M)
```

4. Post-Layout Simulation

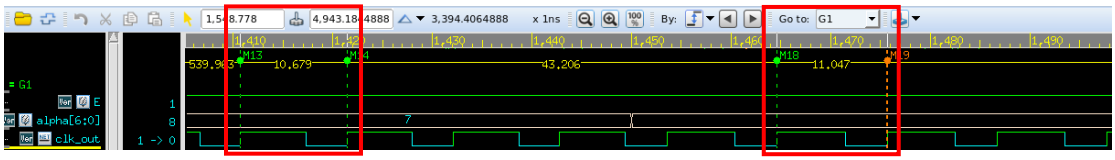
a. Alpha=4、Alpha=5



Alpha=4 clock period=9.737ns

Alpha=5 clock period=10.121ns

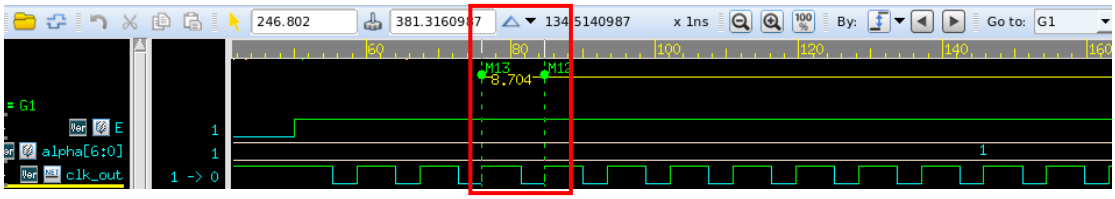
b. Alpha=7、Alpha=8



Alpha=7 clock period=10.679ns

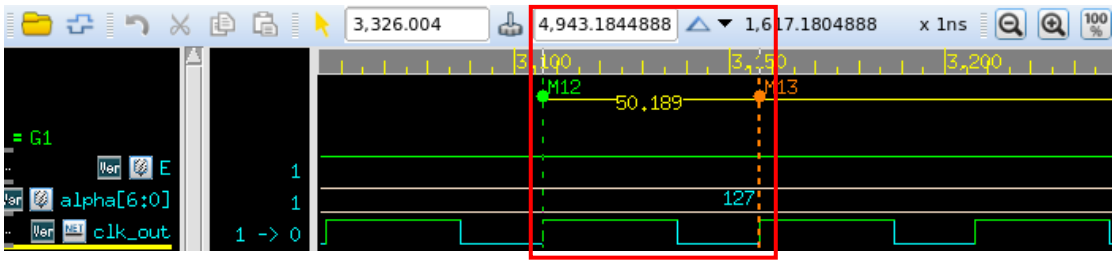
Alpha=8 clock period=11.047ns

c. Alpha=1



Alpha=1 clock period=8.704ns

d. Alpha=127



Alpha=127 clock period=50.189ns

e. Summary

Period range:8.704ns~50.189ns

Frequency range:19.924MHz~114.889MHz

Time resolution:(50.189-8.704)/(127-1)=0.329ns

Alpha Code 從 5~7 會 clock period 落在[10ns, 11ns]

(c) Pre-Layout vs Post-Layout

從 Pre-Layout simulation 中，alpha code 等於 8~11 時，frequency range 會落在[10ns, 11ns]，而到了 Post-Layout simulation 時，alpha 則須調整至 5~7 才會介於此範圍內，且操作頻率範圍的上下限也有所下降，由 Pre-Layout 的 period 範圍 7.956ns~45.448ns 上升到 Post-Layout 的範圍為 8.704ns~50.189ns，由此可看出 Post-Layout 的 delay 明顯高於 Pre-Layout，