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1 Appendix

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Table A.0.1: The Finalised timeline showing changes from previous iteration required dependencies and start and end dates

NUMBER	DELIVERABLES	DESCRIPTION	START	END	DEPENDENCIES	PROGRESS	CHANGES
1	Literature Review	Conduct literature review of relevant background research	3/4/2022	1/5/2022	-	100%	
2	Conceptual Design	Form the overall data flow and preliminary algorithm structure	10/4/2022	6/5/2022	1	100%	
3	Detailed Design	Design the detailed data flow and key elements of the algorithm	10/4/2022	13/5/2022	2	100%	
4	Algorithm	overall design of the algorithm to implement the FFT	10/4/2022	18/5/2022	3	100%	
5	Proof of Concept	MATLAB implementation to prove the algorithm can produce a correct FFT	18/5/2022	31/7/2022	4	100%	
6	Interim Report	Report detailing the progress at the mid way of the project	28/5/2022	Written 12/6/2022 Oral 19/6/2022	3	100%	

7	First Protototype	Initial prototype for basic FPGA implementation	4/6/2022	7/8/2022	3,4	100%	removed the inclusion of frame domain windowing as was not achievable under the the frame
8	Second prototype & Final design	Second prototype that has more functionality and better conforms to bitstream size and latency requirements	8/8/2022	28/9/2022	7	100%	removed the inclusion of log magnitude computing as was not achievable under the time frame
9	Experimental Implementation	Design the testing rig and associate script and peripherals to validate the FPGA implementation experimentally	21/9/2022	15/10/2022	-	90%	This was added to the timeline as to provide a way to verify the authenticity of the simulations
10	Simulation/Results	gather simulation and results for the final FPGA implementation	16/10/2022	21/10/2022	5,8,9	100%	This deliverable was added to distinguish the simulation and results as a key element of the Project
11	Final Report Draft	Draft for the Final Report	30/9/2022	22/10/2022	4,5,8,9,10	100%	

12	Final Report & Presentation	Final Report and presentation detailing design and results in full.	30/9/2022	Written 26/10/2022 Oral 11/11/2022	11	50%	
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