Project: Hardware Efficient FFTs

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| **Student Engineer:**  Alex Barnwell |  | | |
| **Student ID:**  N10264248 |  | | |
| **Supervisor:**  Mark Broadmeadow |  | | |
| **Meeting Date, Time,**  28/9/2022 3pm to 3:30pm  **& Method** |  | | |
| **Face to face Meeting** | Phone | Email | Teams/Zoom |

Report on Progress

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| Agenda & Discussion | * Discussion on SPI implementation for the simulated microphone * How to address critical warning within FPGA design methodology * Work performance assessment discussion   Decision to reduce the clock rate of the SPI (reducing the microphone clock rate) to accommodate for computation time within the microcontroller  Decision to tether the microphone input to the system and have the clock prescaler within the same process to reduce the critical errors. |
| Key project activities completed and reported on this meeting. | *This could include:*   * UART transmission out of the FPGA and its associated simulation * Further discovery on how to possibly address Twiddle factor error |
| Issues/concerns/questions remaining | Best way to debug this system, could a logic analyser be used? |
| Any risks identified (particularly HSE) | No risk identified |
| Ethical considerations | No ethical considerations |
| Sustainability considerations | No sustainability considerations |

Next actions agreed

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| Action | Who? | By when? |
| Complete the microcontroller SPI communication | Alex Barnwell | 5/10/2022 |
| Complete the receiving end to display FFT results | Alex Barnwell | 5/10/2022 |
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---- END OF MEETING NOTES ----