RF Amplifier Design Guide

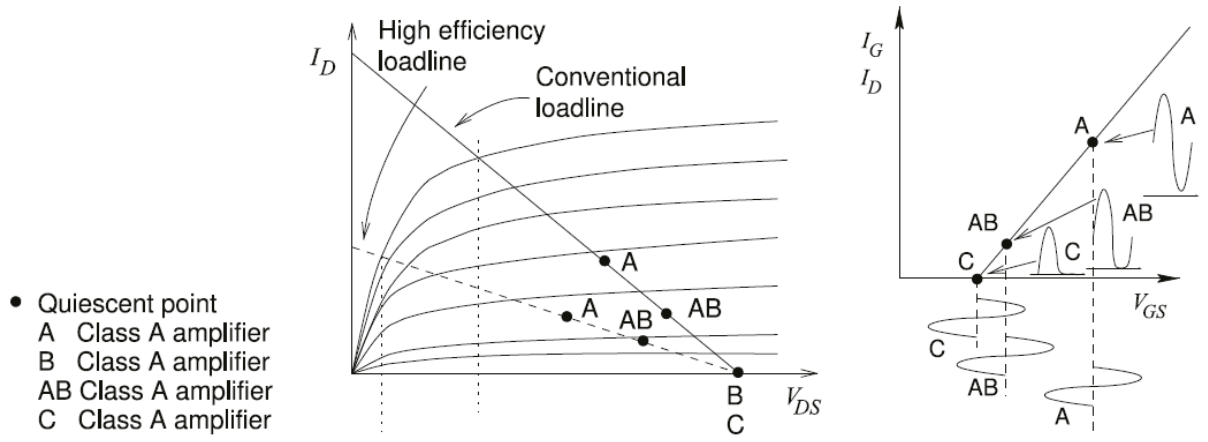
November 11th, 2024

1. Introduction

This design guide will introduce the process to design an RF amplifier, with focus and example application to Field Effect Transistor (FET) common source (CS) low noise amplifiers (LNA). In the common source amplifier configuration, the gate pin is the input port, drain pin is the output port, and source pin is grounded (common node).

1.1. Biasing and Class of Operation

DC bias selection is the first step in amplifier design. It will fix the small signal behavior (i.e., S-parameters) of the device. Supply voltage V_{DS} (Drain to Source voltage) and bias voltage V_{GS} (Gate to Source voltage) are selected from DC simulations by sweeping both values. The input and output transfer characteristics also known as current-voltage (IV) characteristics are obtained by plotting the output current I_{DS} against V_{GS} for the input characteristics and V_{DS} for the output characteristics. Depending on the selection for supply voltage V_{DS} and the bias voltage V_{GS}, the device will produce a DC current output known as quiescent current. The point on the IV characteristics that correspond to the combination of parameters is called quiescent point and it determines the class of operation.



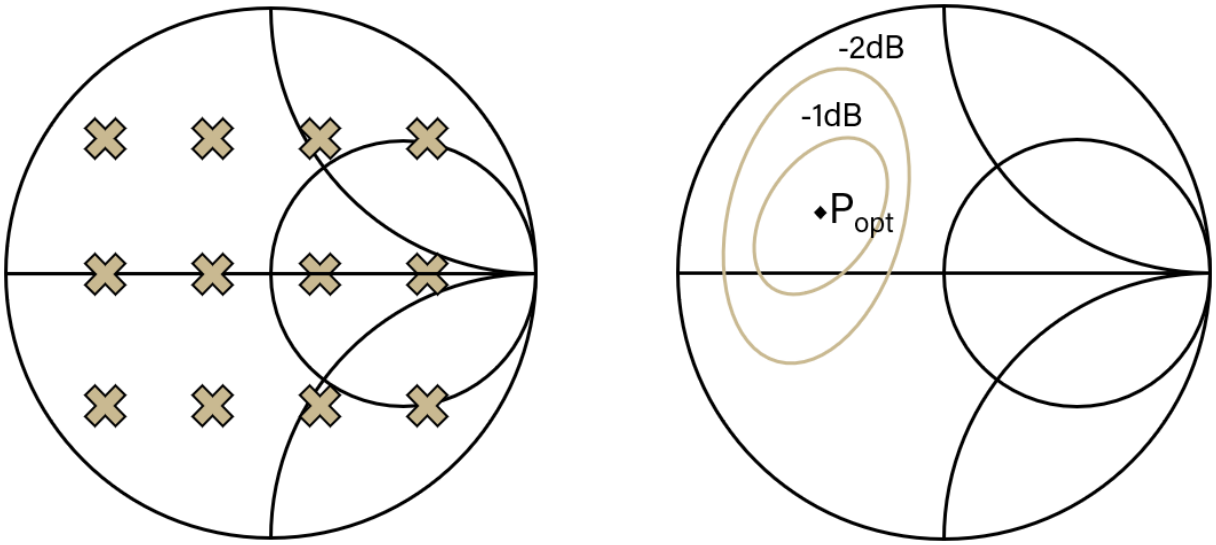
(a) Output characteristic (b) Input characteristic

If the bias is set to have a quiescent current in the midpoint of the linear input characteristics, both the negative and positive parts of the signal will receive the same linear amplification. If the bias is lowered, it will have lower power consumption, but the linearity is worse as the negative half 'clips' earlier than the positive half. Any point between the mid-point and start of the linear region is known as Class AB. The edge case, when the current is at the 'knee' or start of the linear region is known as Class B. When the bias is lower, the signal needs a big amplitude to be amplified, a sort of peaking amplifier behavior, and this bias is known as Class C. These are all the linear conduction mode classes of operation. Another category is switching mode classes of operation which have worse linearity, but better efficiency and they are used in

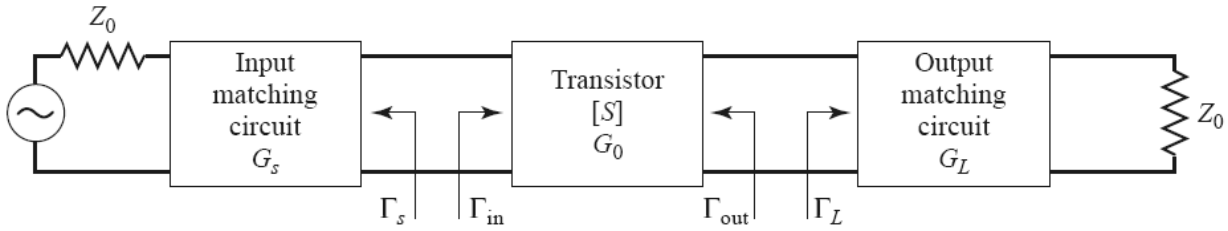
power amplifiers (PAs). Linear behavior is desired in low noise amplifiers (LNA) hence, Class A and AB are preferred.

1.2. Source/Load Pull

A source or load pull consists of a simulation or test where the termination impedance is swept at a set of points within the Smith Chart to determine the performance figures of merit (FoM) for a particular device. In LNAs, the gain and noise figure are the most important FoM. In power amplifiers (PAs), output power and efficiency are the most important FoM. Linearity and the effects of the modulation scheme can also be considered. Typically, the input is matched to an impedance that achieves the desired noise figure and the output to maximize stable gain.



Since the reverse gain (S_{12}) of the device is non-zero we must consider any changes in the output impedance will change the desired input reflection coefficient and vice versa. There is no closed form solution to this set of equations, but an iterative approach is useful.



Method 1: If the output impedance is selected first with a given reflection coefficient Γ_L, the input reflection coefficient Γ_{IN} will be calculated with the S parameters corresponding to the transistor with $Z_0 = 50\Omega$ terminations by

$$\Gamma_{IN} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L}$$

Method 2: Alternatively, if the input impedance is selected first with a given reflection coefficient Γ_S, the output reflection coefficient Γ_{OUT} will be calculated with the S parameters corresponding to the transistor with $Z_0 = 50\Omega$ terminations by

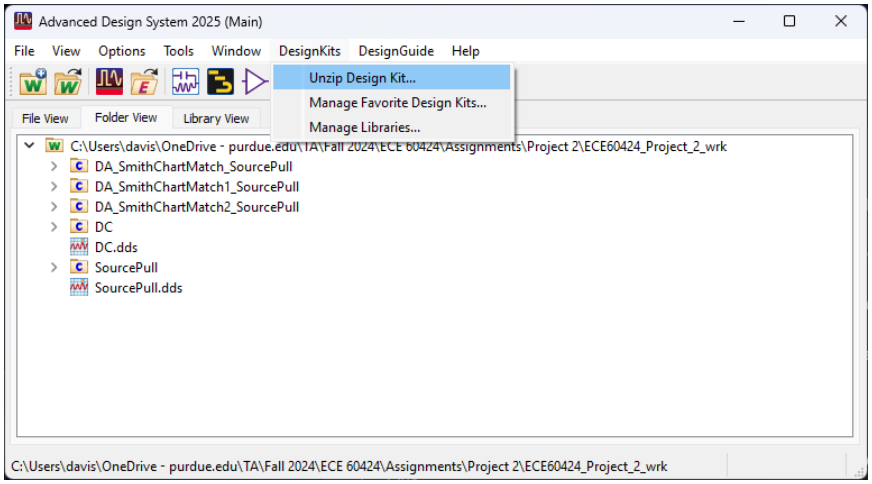
$$\Gamma_{OUT} = S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S}$$

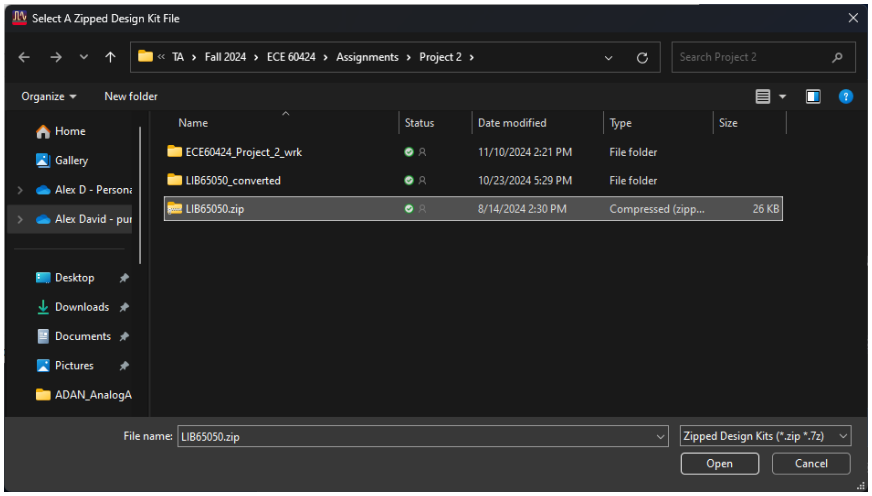
The target reflection coefficients Γ_S or Γ_L depend on the amplifier type and design goals. It is important to understand there is not a single impedance to match the amplifier but rather a continuous domain with performance tradeoffs. The design engineer needs to choose a point in the Smith Chart for the input and output that will satisfy the design goals while maintaining good return loss, typically better than 10 dB.

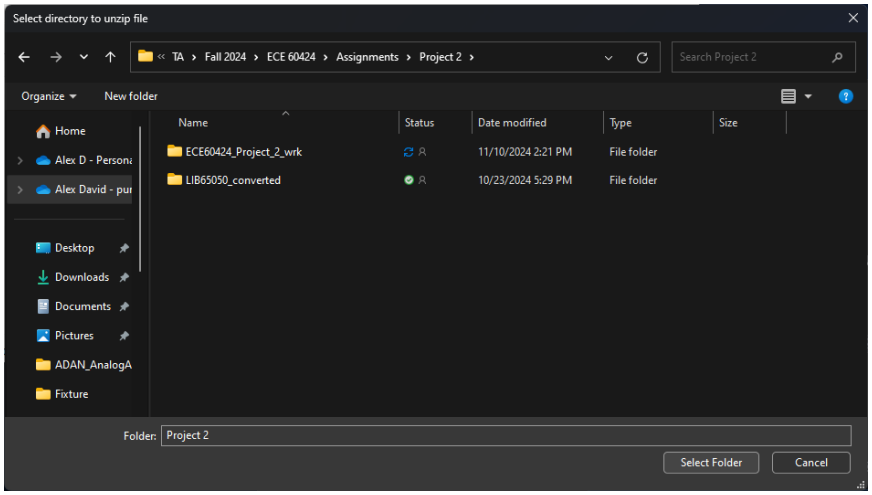
2. Simulations

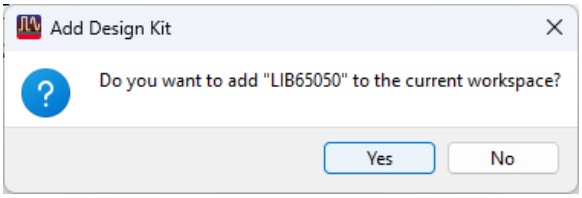
2.1. Load ADS Design Kit (Library)

The Design Kit contains the model, Download the SKY65050 ADS Design Kit from the manufacturer (also available on Brigthspace). On the main ADS window, open the workspace, click on “DesignKits>Unizp Design Kit…”. Then, select the design kit file which you downloaded (LIB65050.zip). Select a path to save the uncompressed file, the local ADS path or workspace folder are recommended. When prompted, add the library to the workspace.

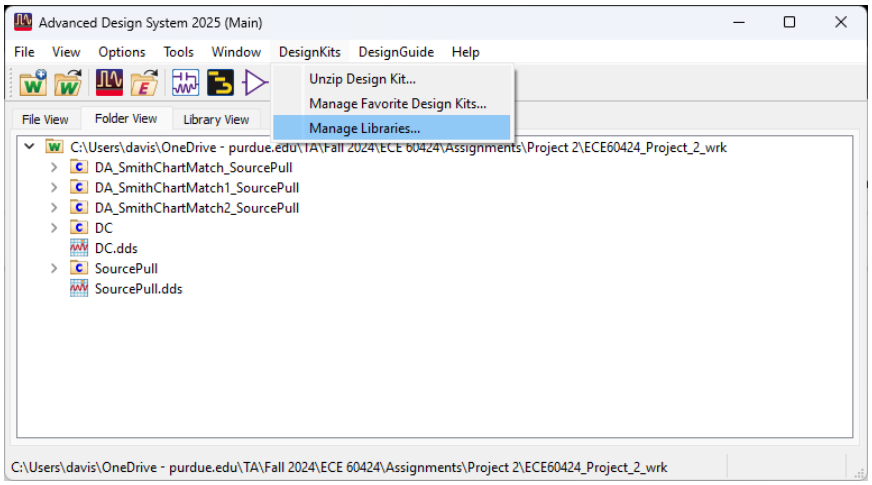


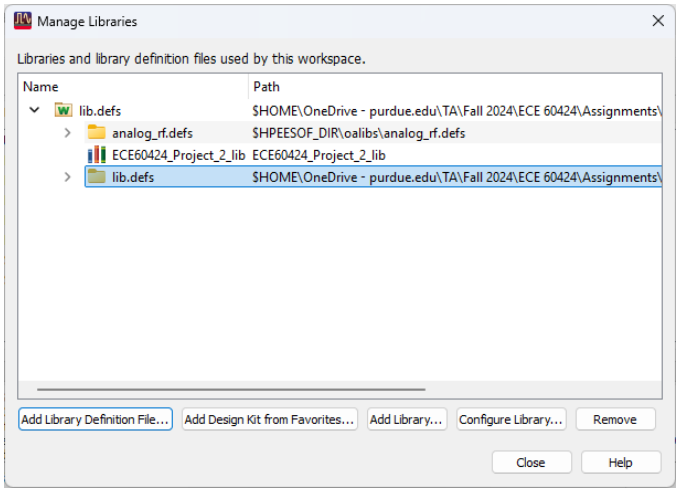




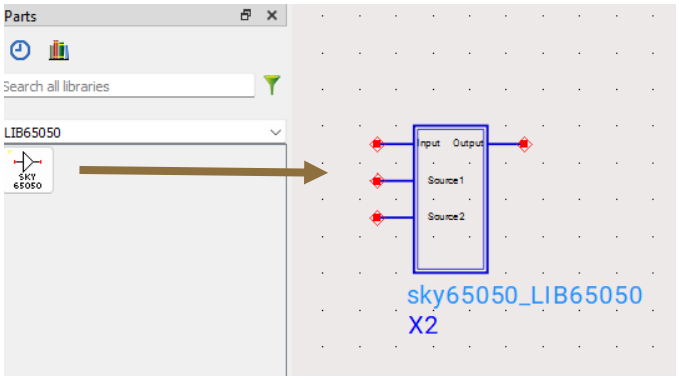


You can view the libraries that are loaded in the workspace by clicking on “DesignKit > Manage Libraries…”.





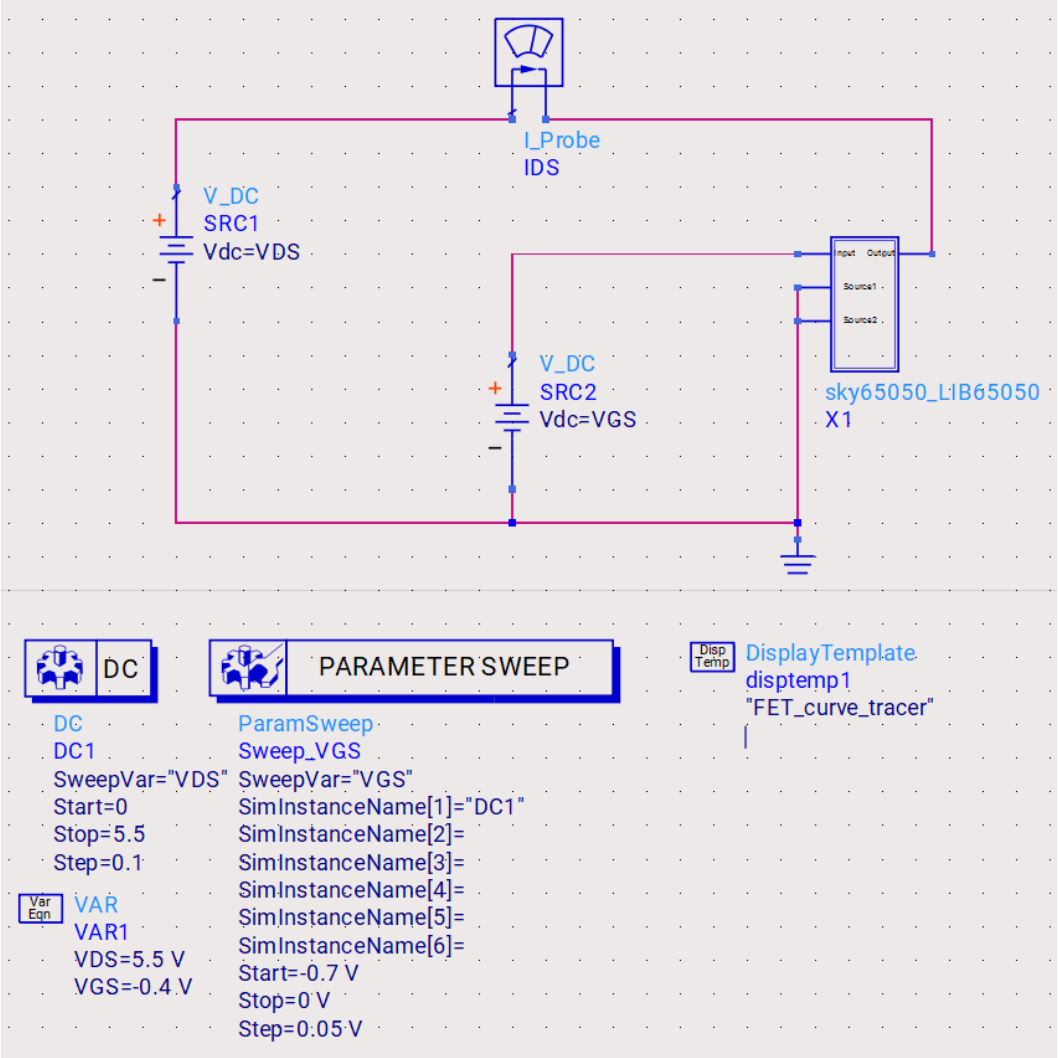
Now, the device will be available for use in the schematic window.



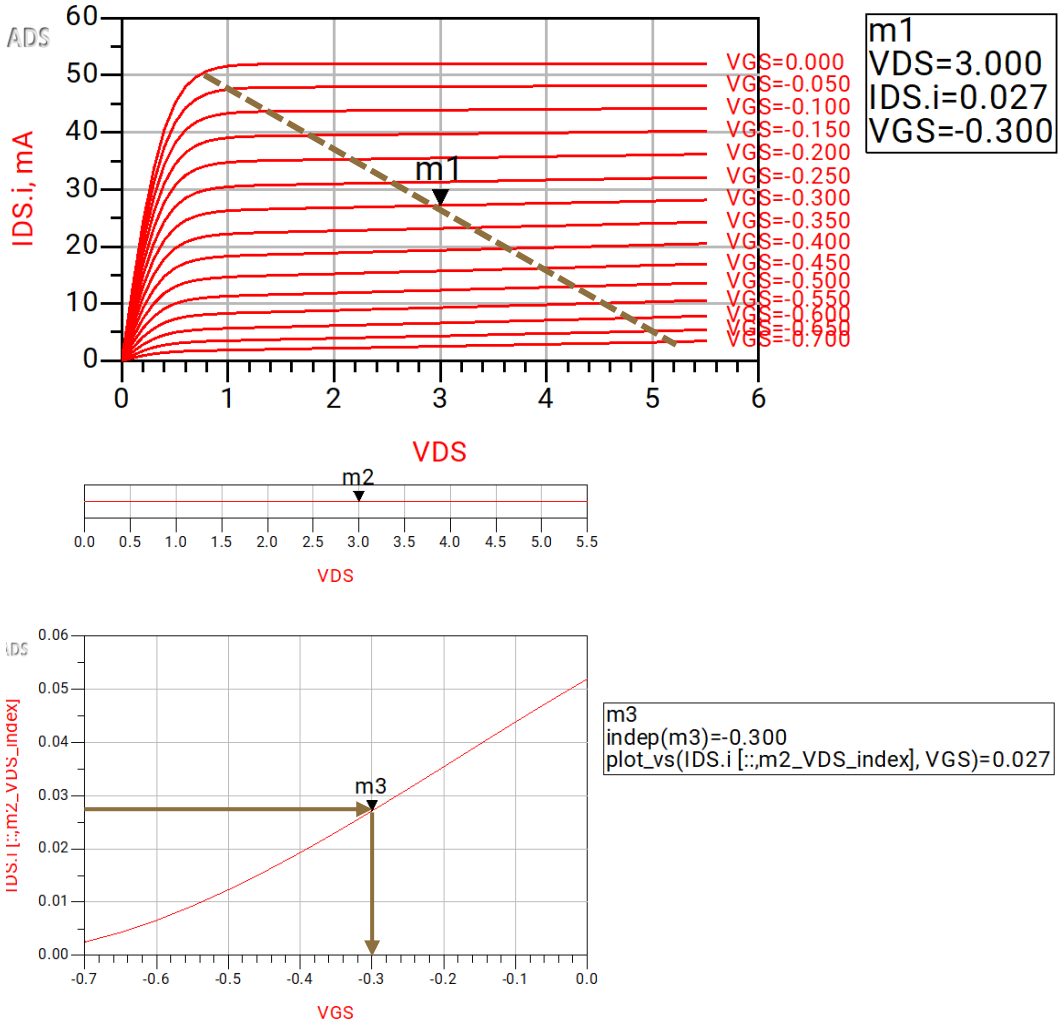
2.2. IV Characterization

To obtain the DC characteristics of the device, we will plot the output transfer characteristics given by the drain current I_{DS} against the drain voltage V_{DS} for several bias voltages V_{GS}. The following schematic has the configuration needed for the DC sweep.

By: Alex D. Santiago-Vargas

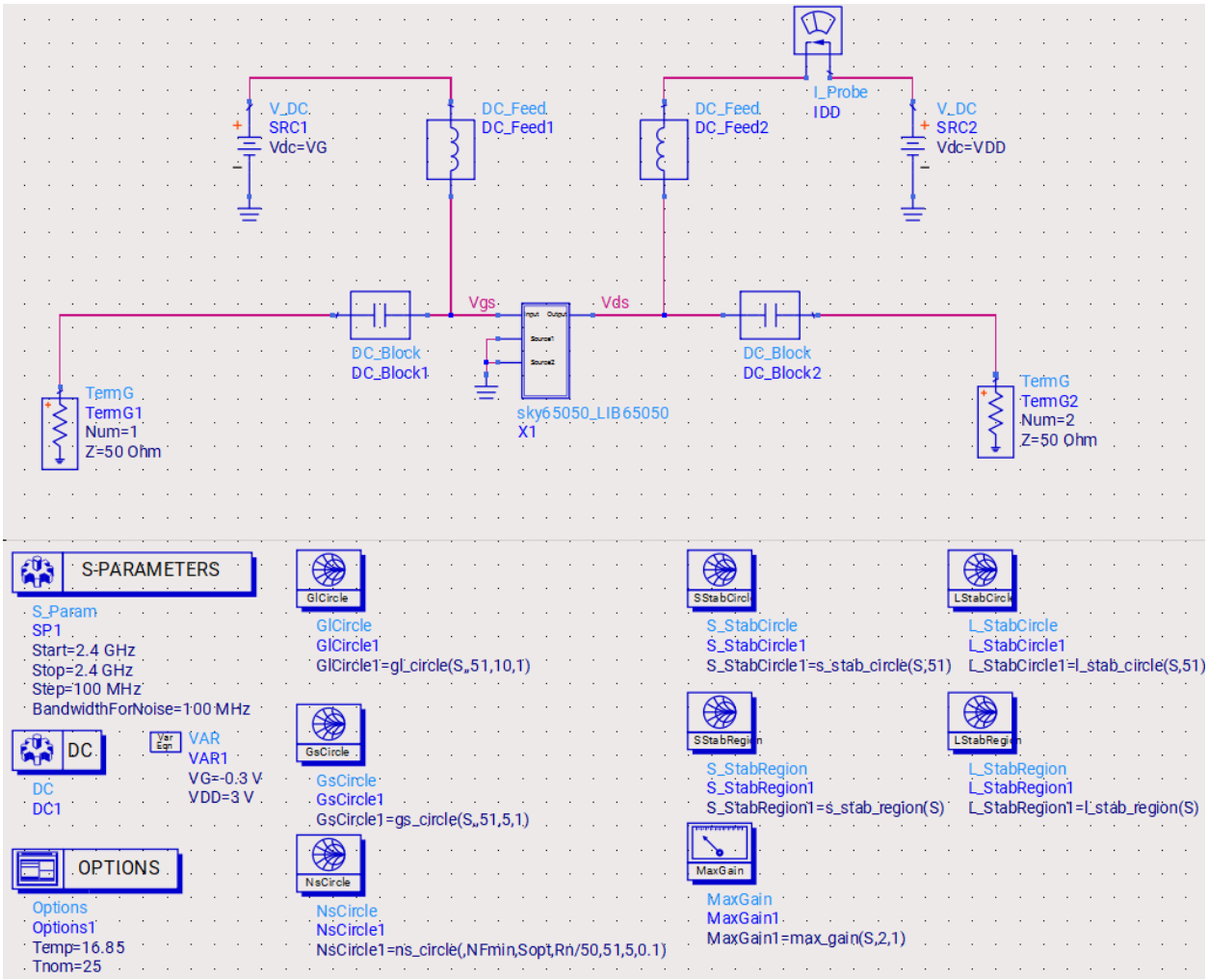


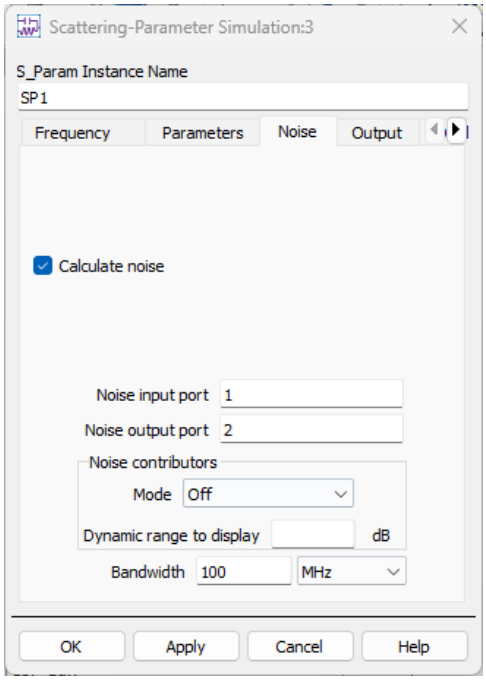
These are the output and input transfer characteristics for the SKY65050-372LF. In this design we will select a Class A quiescent current of 27mA (center of input characteristic, center of DC loadline) which results in a VGS bias voltage of -0.3V.



2.3. Source Pull

One method of performing source and load pulls in ADS is shown in the following schematic. To obtain the noise figure, make sure to enable noise in the S Parameter simulation block. NFmin, Sopt, and Rn data are generated from the device model only when the noise is enabled. The DC Feed and Block are ideal components which do not impact your frequency response.





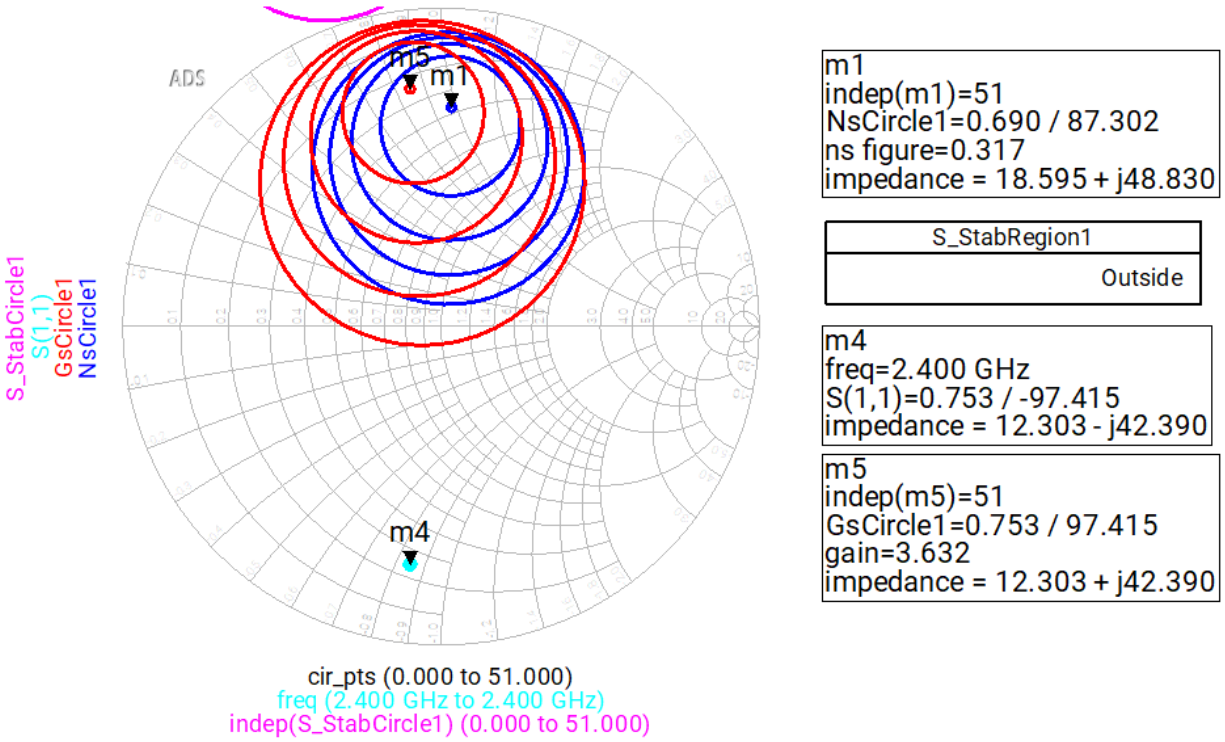
By: Alex D. Santiago-Vargas

By plotting GsCircle, NsCircle, and S_StabCircle the source pull gain, noise figure, and stability circles will be shown. In this example, to make the amplifier unconditionally stable (push the stability circles out) a 200Ω shunt resistor was added to the output port and the source pull simulation was repeated.

The design engineer will choose an impedance to which the impedance matching will target to satisfy the system requirements. In this case, we will perform a minimum noise figure match by targeting the minimum NF shown with the marker m1. This will essentially move the NF circles to be centered around 50Ω. Following the impedance matching Method 2 in Section 1.2, $\Gamma_S = S_{11}^*$ for minimum NF and the S parameters are obtain from the $Z_0 = 50\Omega$ termination.

Γ_S is selected from the S_{11}^* for minimum NF:

$$\Gamma_S = 0.690\angle 87.302°$$



Device S Parameters:

$$S_{11} = 0.753\angle -97.415°$$
$$S_{12} = 0.032\angle 40.022°$$
$$S_{21} = 5.249\angle 102.418°$$
$$S_{22} = 0.480\angle -37.075°$$

Then, the output reflection coefficient can be calculated as

$$\Gamma_{OUT} = S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S} = 0.479\angle -64.653°$$

By: Alex D. Santiago-Vargas

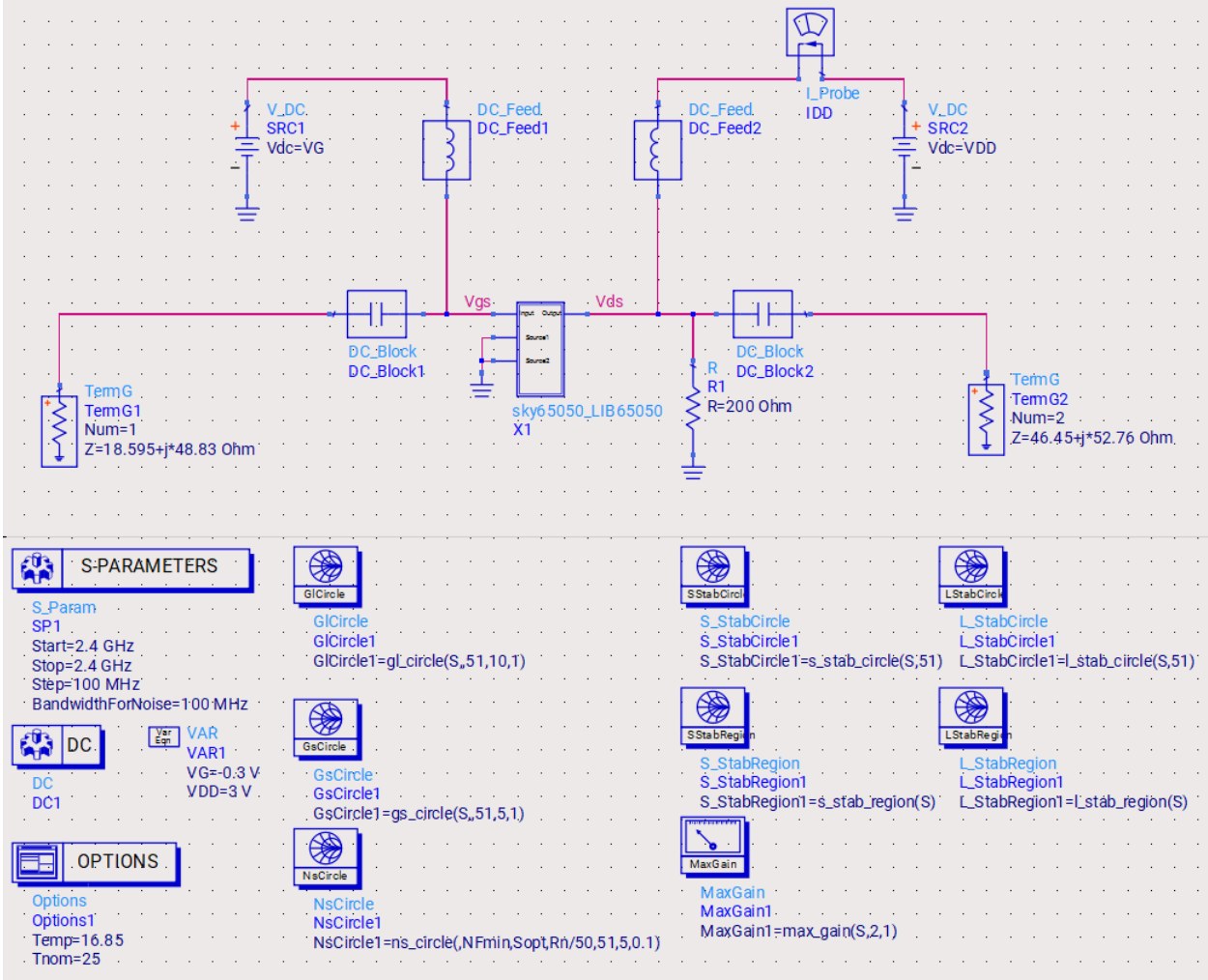
The input impedance will be calculated from Γ_S and the output termination impedance will be calculated from Γ_{OUT}^*.

$$Z_{IN} = 18.595 + j48.830\ \Omega$$
$$Z_{OUT} = 46.450 + j52.760\ \Omega$$

The matching network will be designed to target these impedances.

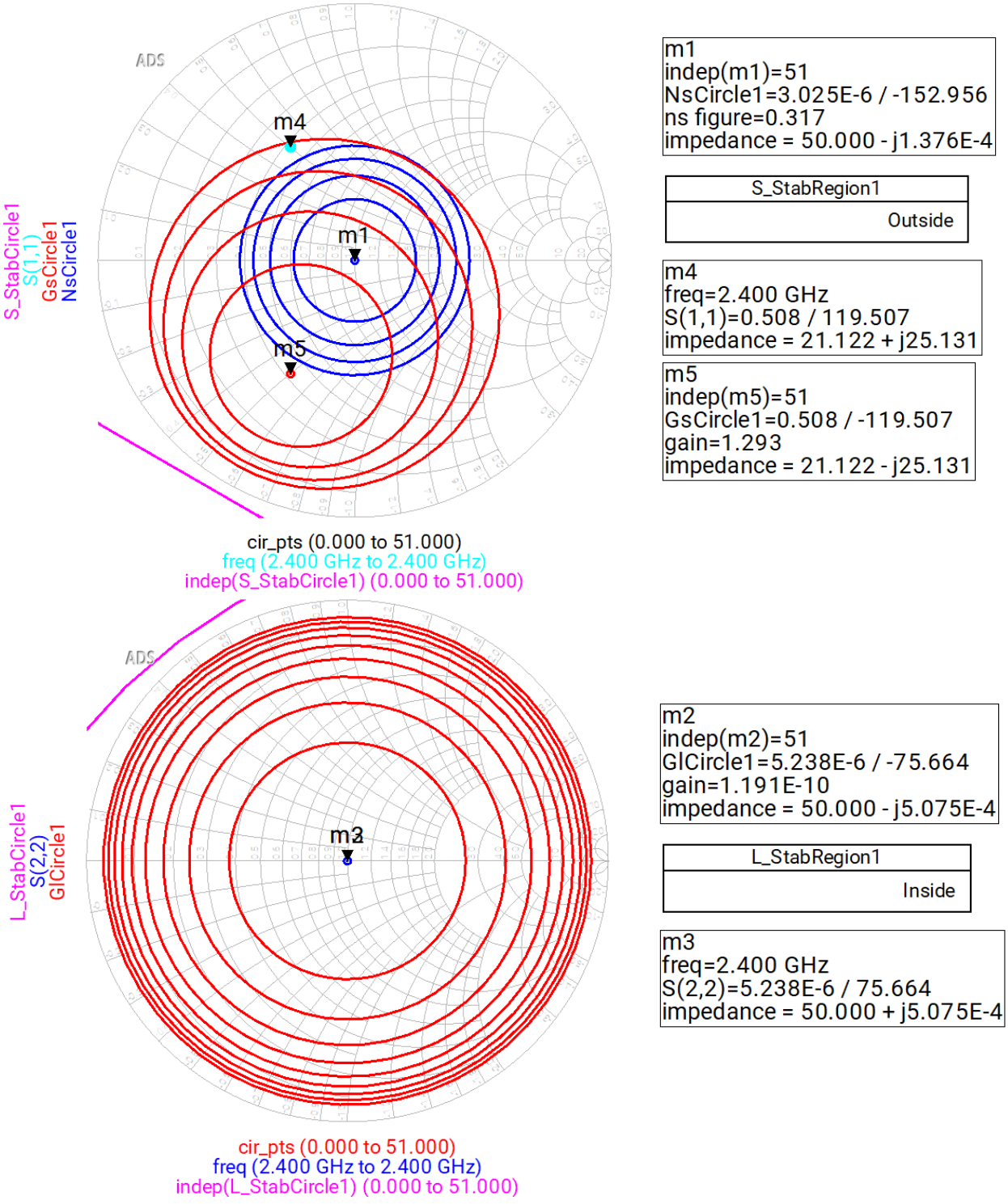
2.4. Load Pull

As a validation, the port impedances can be changed to reflect the selected Z_{IN} and Z_{OUT} before designing the matching network.



By plotting GlCircle and L_StabCircle, the load pull gain and stability circles will be shown. As the input and output are targeting the desired impedances, the performance contours will be moved. At Z_0, on the center of the Smith Chart, the input has the minimum NF and the circles are centered around this point. Which means, a $Z_0 = 50\Omega$ load will create the minimum NF in the amplifier. The gain circles are offset, but at Z_0 is in the regions between the circles at $-1dB$

and $-2dB$ from the peak gain. Which means, the performance tradeoff is about $1.5dB$ of gain. The output in the other hand is matched to peak gain, so it maximizes the gain from the device.



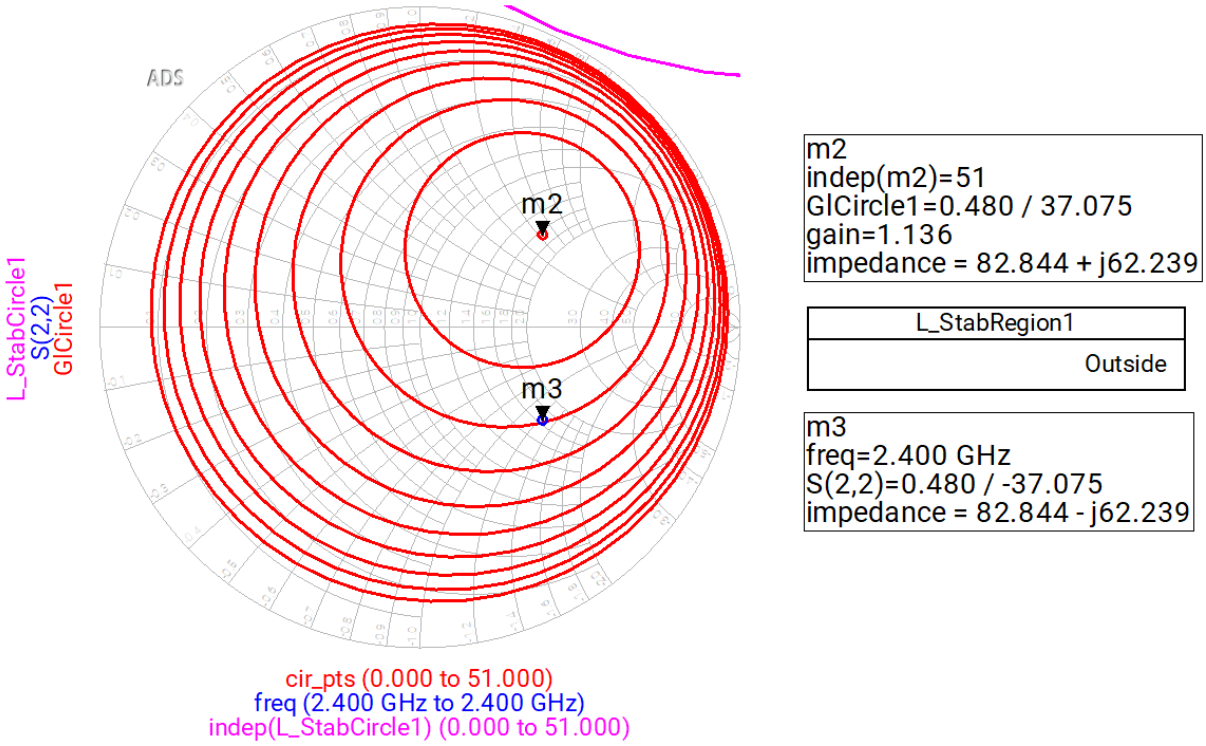
The gain tradeoff at the input and maximum gain at the output seem contradictory. Keep in mind these circles are plotted in the context of the input and output impedance when the

other port is matched. We do have maximum gain at the output, but the input is creating a drop in gain due to the selected $1.5dB$ gain tradeoff.

Another way of interpreting these circles is that for a given mismatch, the amplifier will maintain a given performance. That is, if we have a load that lands in the $-1\ dB$ gain circle, the amplifier will only achieve a gain $1\ dB$ below the peak when matched at Z_0.

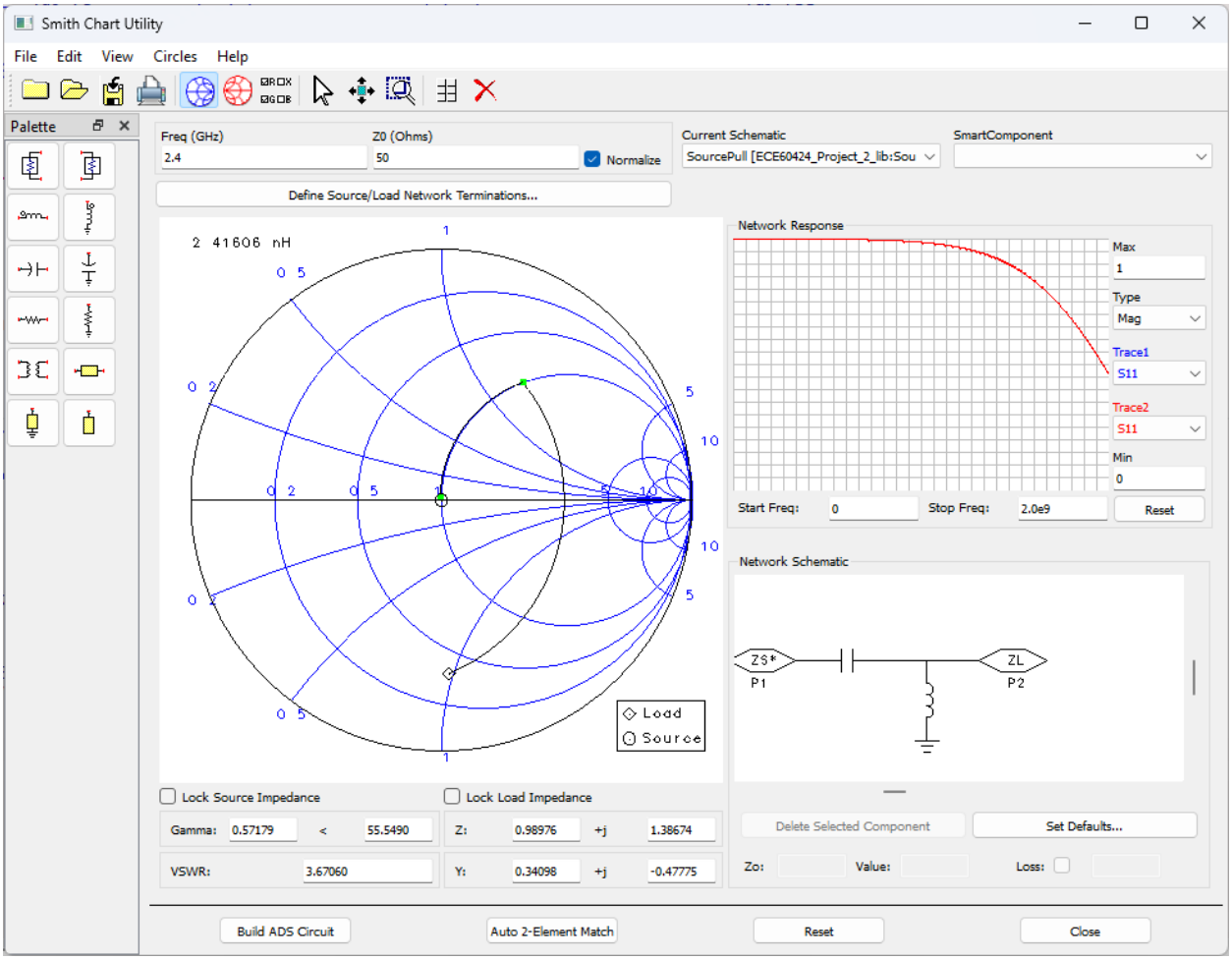
Alternative Method

For the alternative of selecting the output impedance first following Method 1, the design engineer will choose an impedance to which the impedance matching will target to satisfy the system requirements. For example, a maximum gain match by targeting the peak gain shown with the marker m2. Then Γ_{IN} will be calculated in a similar way as Γ_{OUT} was calculated in Section 2.3. This method will essentially move the output gain circles to be centered around 50Ω.



3. Impedance Matching Network Design

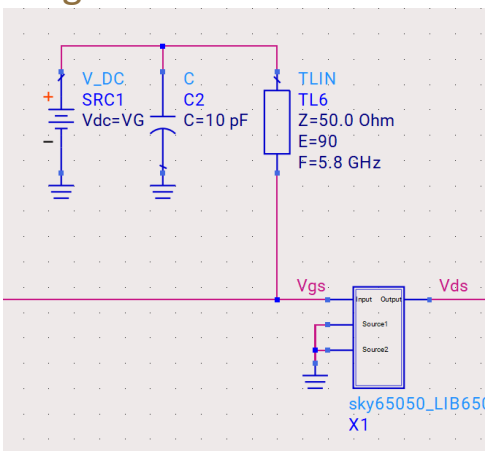
The matching network can be designed as desired, but considering biasing it should either allow for a DC feed or pass DC. In this example, a DC bias can be injected through the shunt inductor and effectively would be a DC short.



4. Biasing Network Design

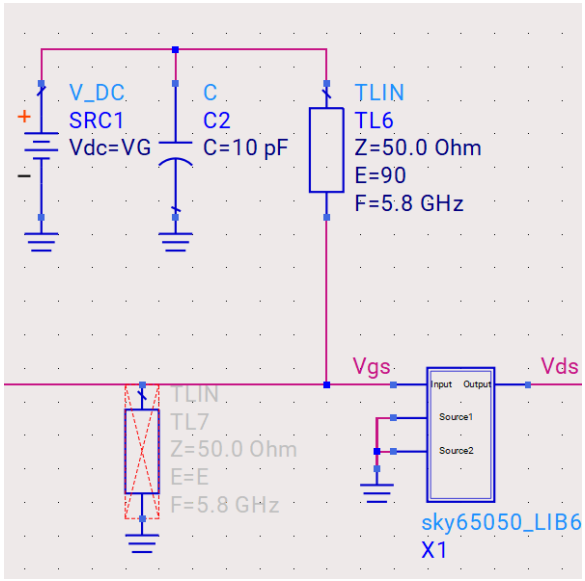
There are different techniques that can be used to bias the device. Two important considerations are that there is DC continuity between the DC feed and the transistor ports and that there is no DC short circuit for the supply. Some valid techniques are shown below.

4.1. Quarter Wavelength Transformer

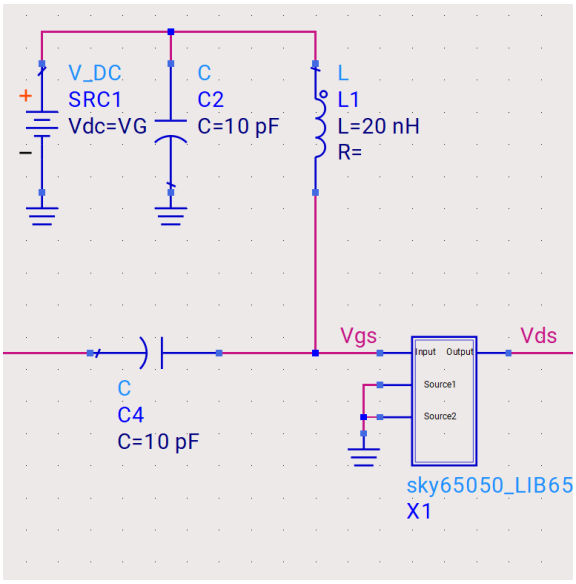


The capacitor and DC supply are effectively an RF short circuit (given that the capacitance has a reactance $> Z_0/10$). Hence, a $\lambda/4$ ($90°$ electrical length) short-circuited stub will look like an open circuit at the transistor pin and should not change the impedance of the device at the center frequency. The capacitor filters out supply noise and provides an alternate RF short to prevent leaked RF from going to the supply. Alternatively, if you have a short-circuited stub in your matching network, you can terminate it like this and use the length you need to provide both matching and DC bias. The disadvantage of transmission lines is that they are limited to small fractional bandwidths. But that is okay for this project since we have a narrowband design.

Be careful if you have an additional shorted stub, as it will short circuit the supply to ground. In real life, the supply will drop the voltage since it cannot provide the infinite current needed to maintain the node voltage. You could add a DC block capacitor with a large reactance (similar to the next example) to prevent a DC short. Essentially, don't use a shorted stub like TL7 (which is disabled in this diagram):



4.2. LC Bias Tee



You could use an inductor instead of a quarter wavelength transformer if the reactance is $> 10Z_0$. Keep in mind, at high frequencies inductors have low Q and low self-resonance frequency which will be hard to design. These are more common in sub-3GHz designs. The series capacitor that follows will block any external DC. More importantly, if you have a shorted stub, this capacitor will provide a DC open circuit, so it doesn't short out the supply. If the matching network has this topology, you could use the values for matching as your elements and provide both matching and biasing through the same network.