TP1 - Introdução aos Sistemas Lógicos

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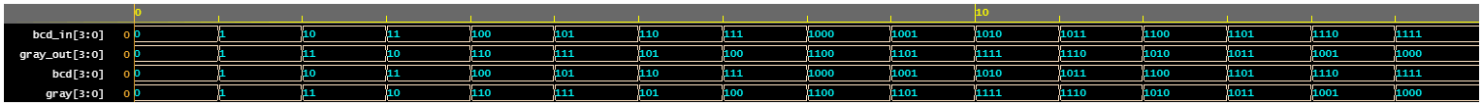
Tabela Verdade, saída do Verilog

```
VCD info: dumpfile dump.vcd opened for output.
bcd <-> gray
0000 <-> 0000
0001 <-> 0001
0010 <-> 0011
0011 <-> 0010
0100 <-> 0110
0101 <-> 0111
0110 <-> 0101
0111 <-> 0100
1000 <-> 1100
1001 <-> 1101
1010 <-> 1111
1011 <-> 1110
1100 <-> 1010
1101 <-> 1011
1110 <-> 1001
1111 <-> 1000
Finding VCD file...
./dump.vcd
```

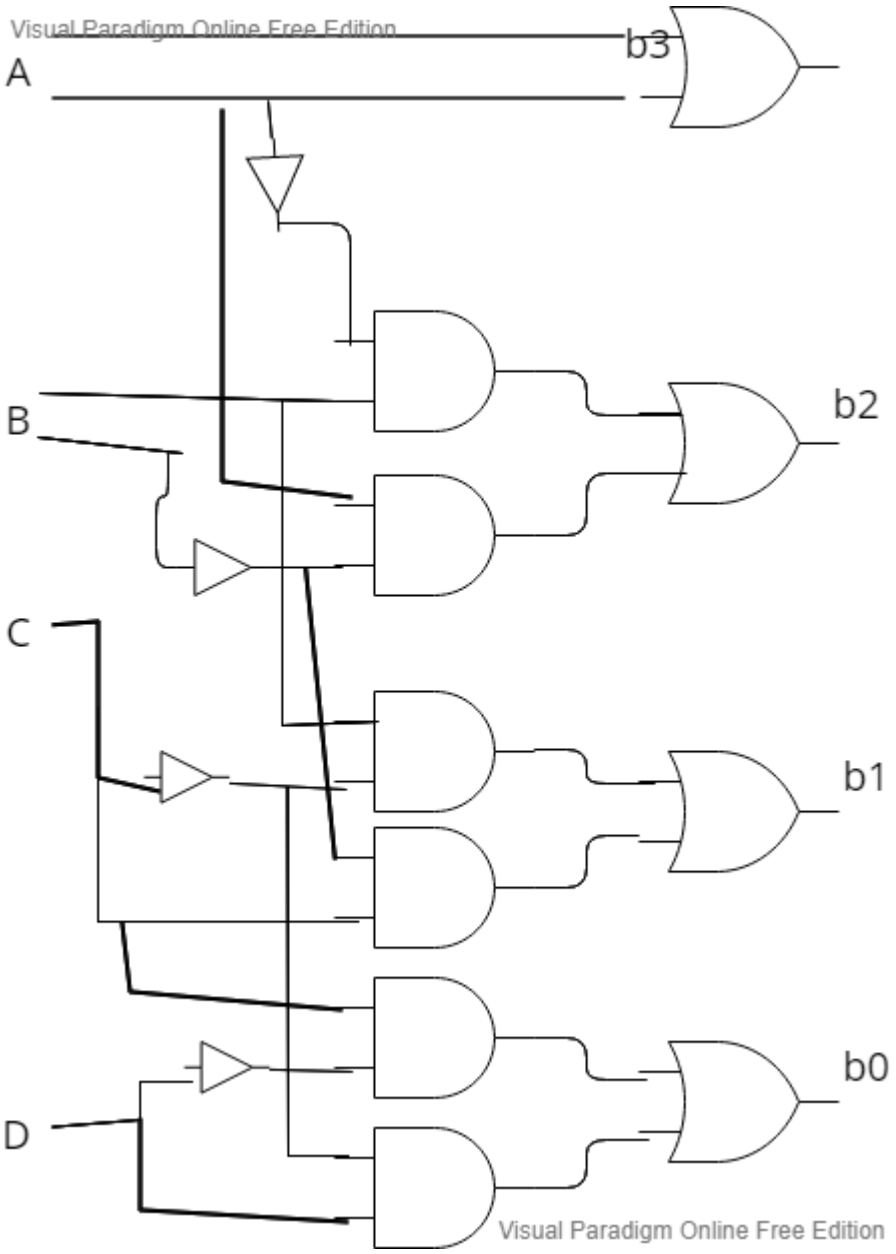
a) b3 = **AB´C´D´+AB´C´D+AB´CD´+AB´CD+ABC´D´+ABC´D+ABCD´+ABCD**
b2 = **A´BC´D´ + A´BC´D + A´BCD´ + A´BCD + AB´C´D´ + AB´C´D + AB´CD´ + AB´CD**
b1 = **A´BC´D´ + A´BCD´ + ABC´D´ + ABCD´ + A´B´C´D + A´B´CD + AB´C´D + AB´CD**
b0 = **A´B´CD´ + A´BCD´ + AB´CD´ + ABCD´ + A´B´C´D + A´BC´D + AB´C´D + ABC´D**

b) b3 = **A**
b2 = **A´B+AB´**
b1 = **BD´+B´D**
b0 = **CD´ + C´D**

c) Forma de Ondas do caso teste



d)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A
b3
B
b2
C
b1
b0
D
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