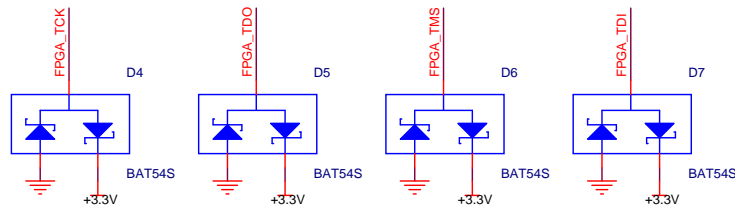
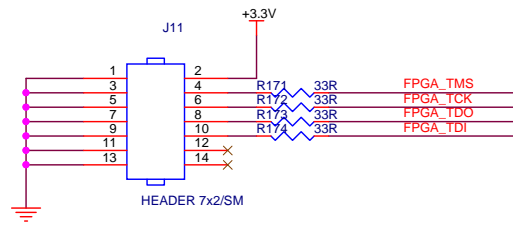
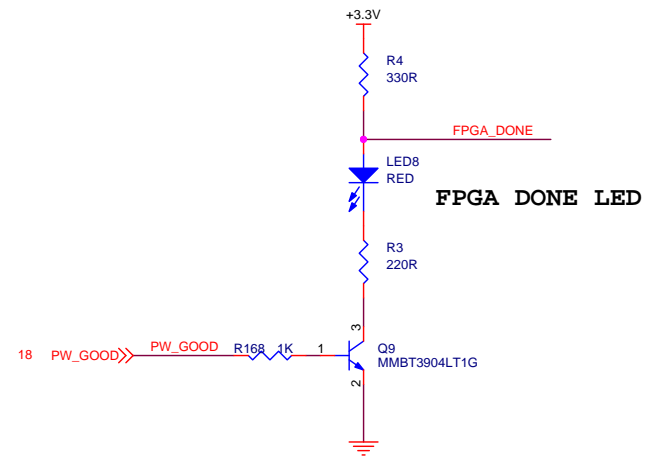


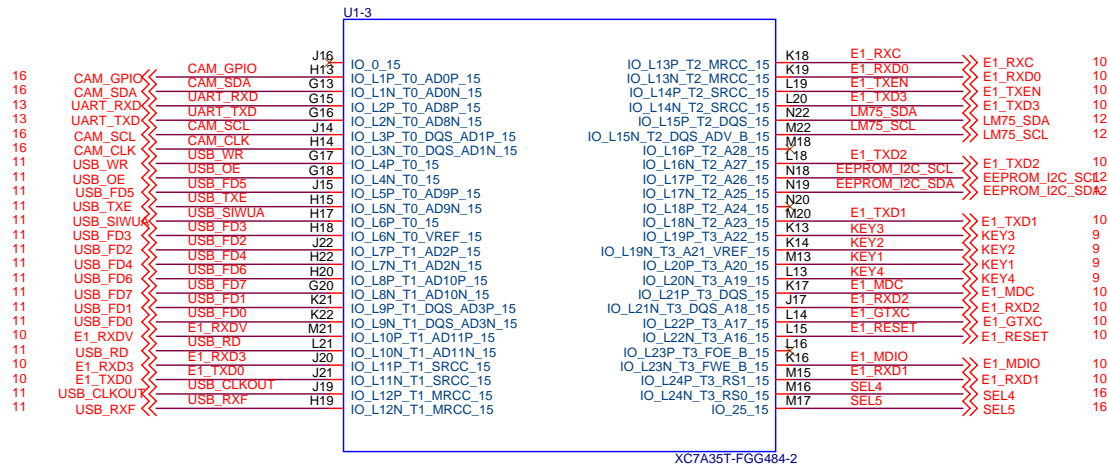
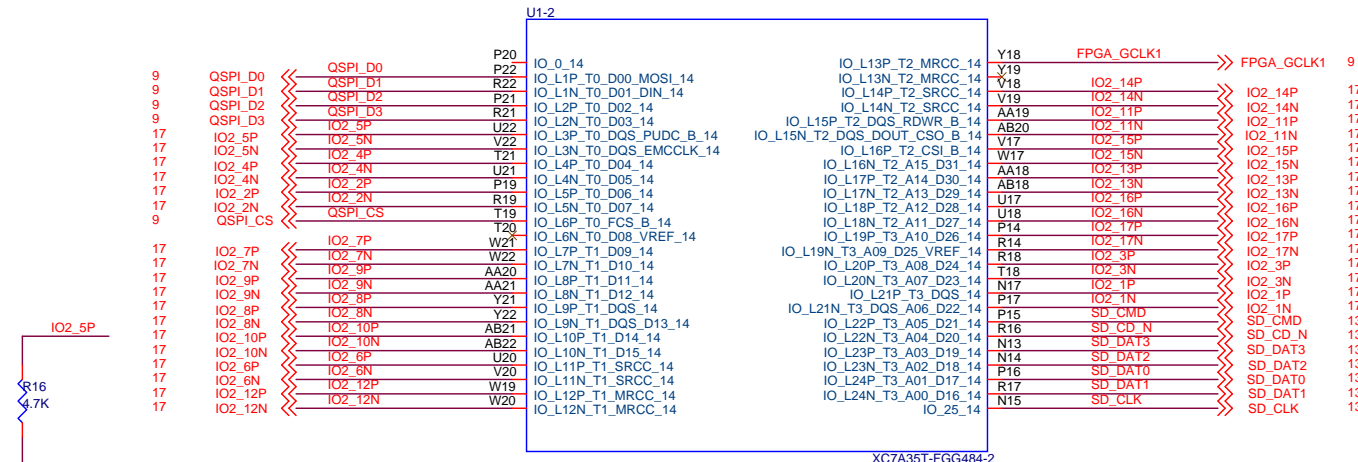
JTAG Connector



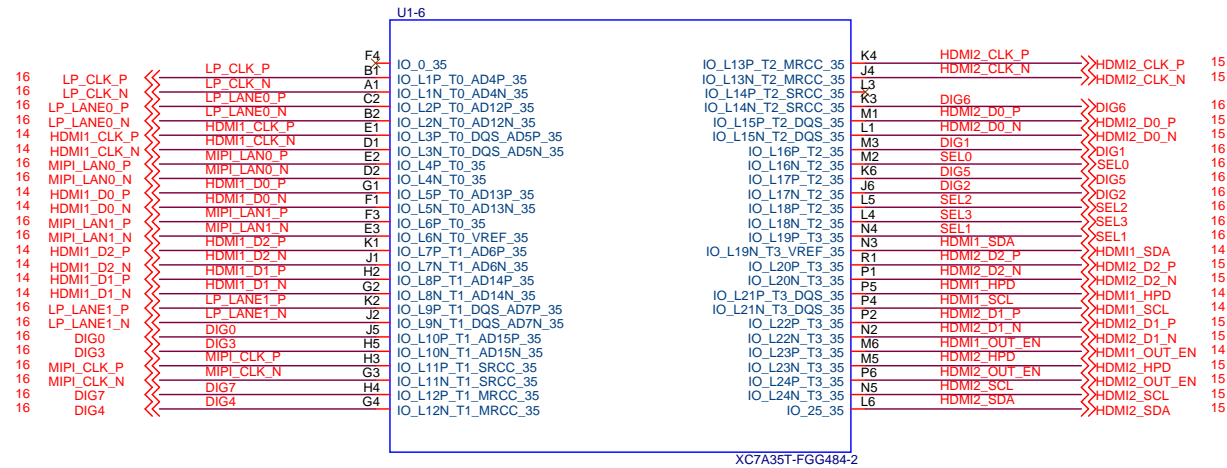
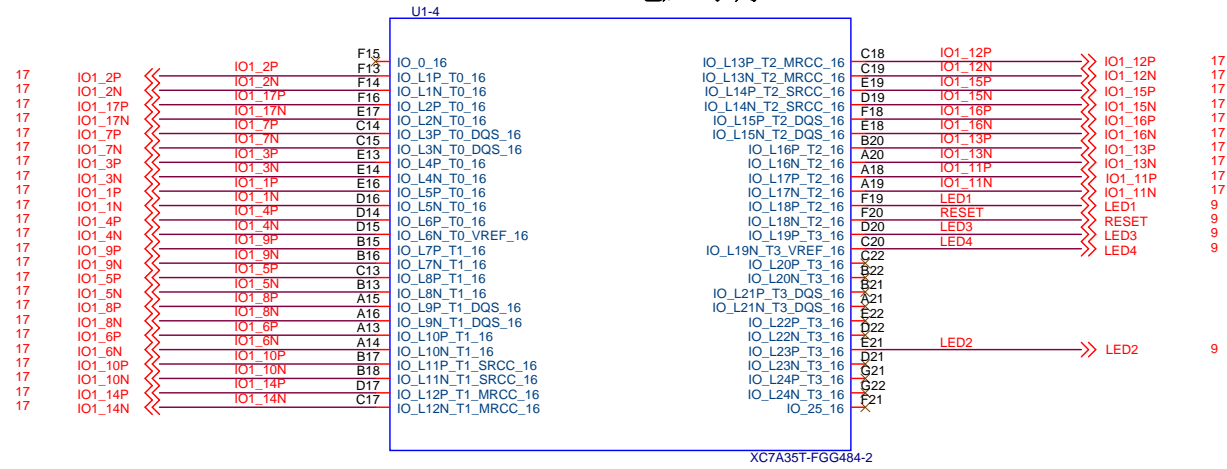
Power LED



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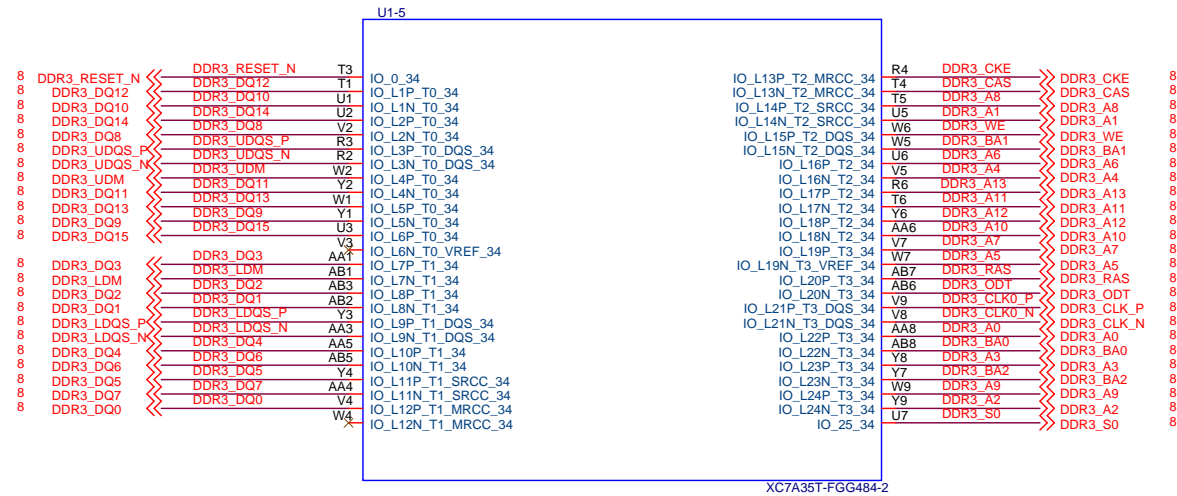


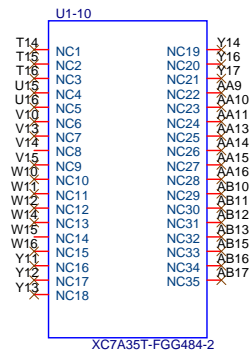
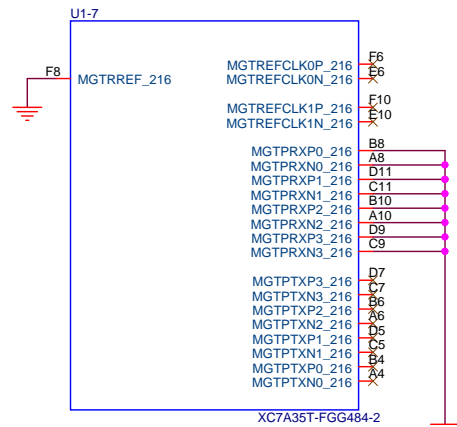
IO 电压可调

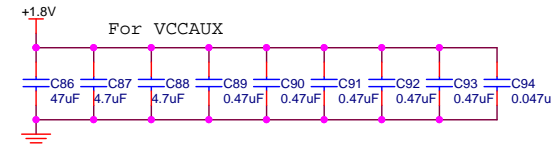
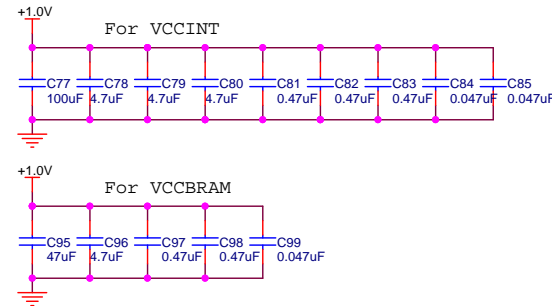
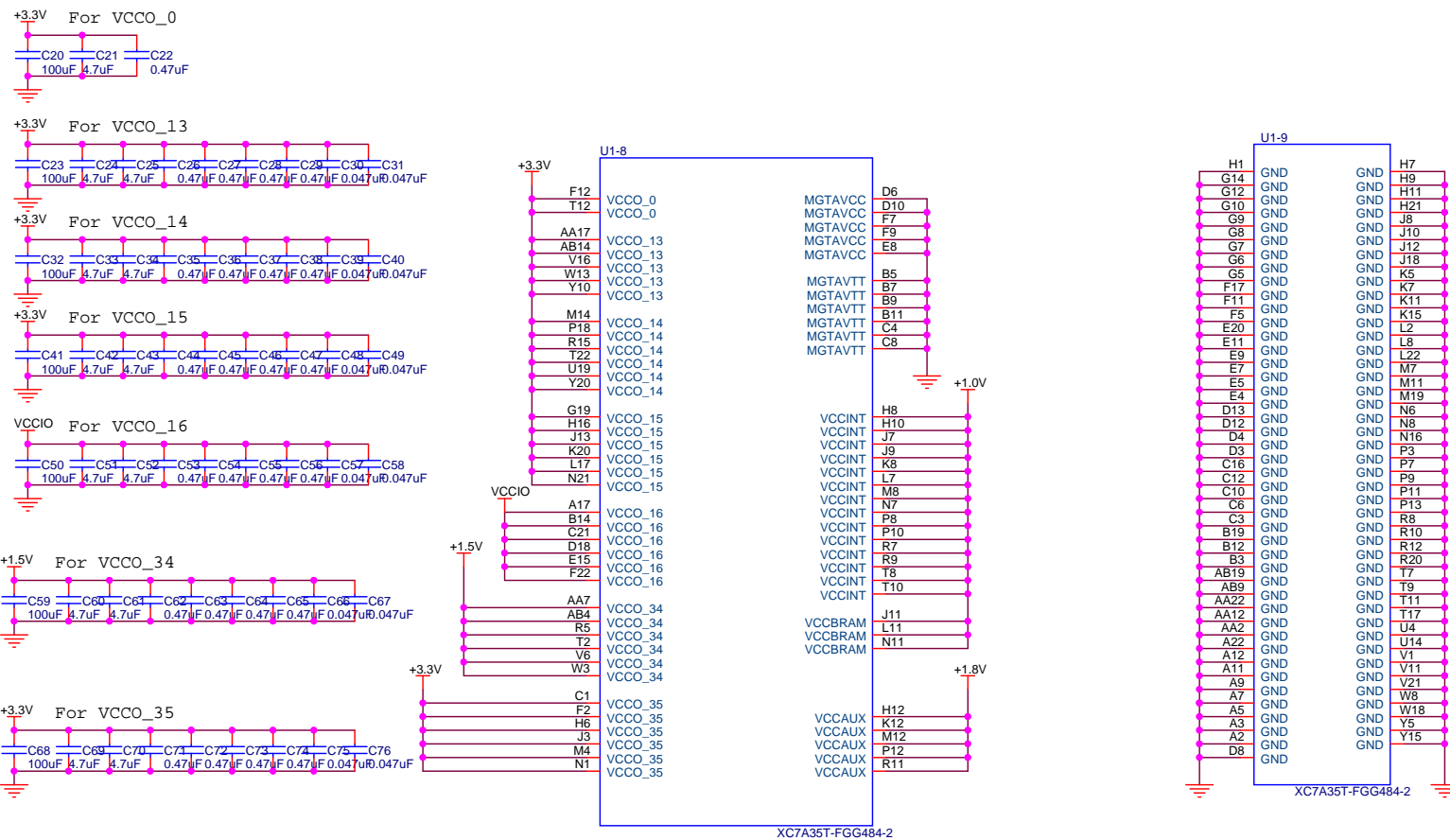


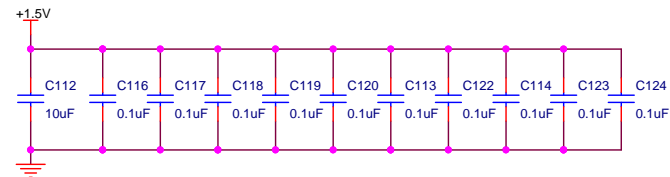
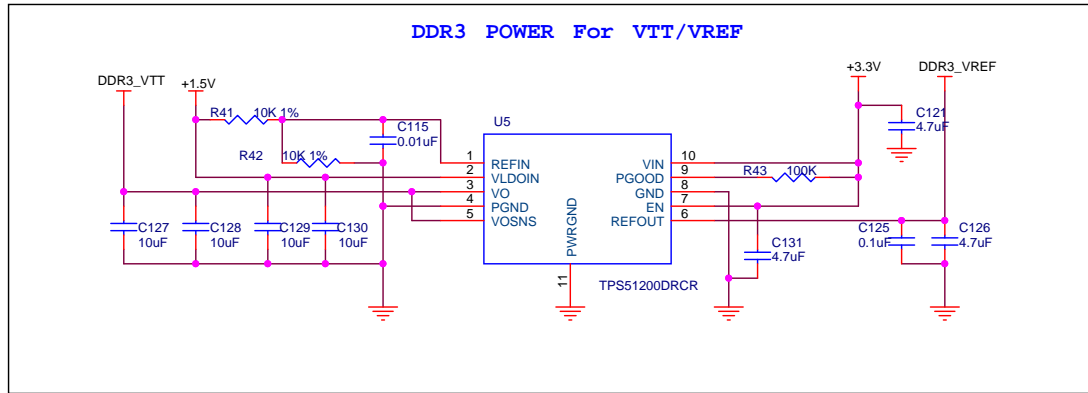
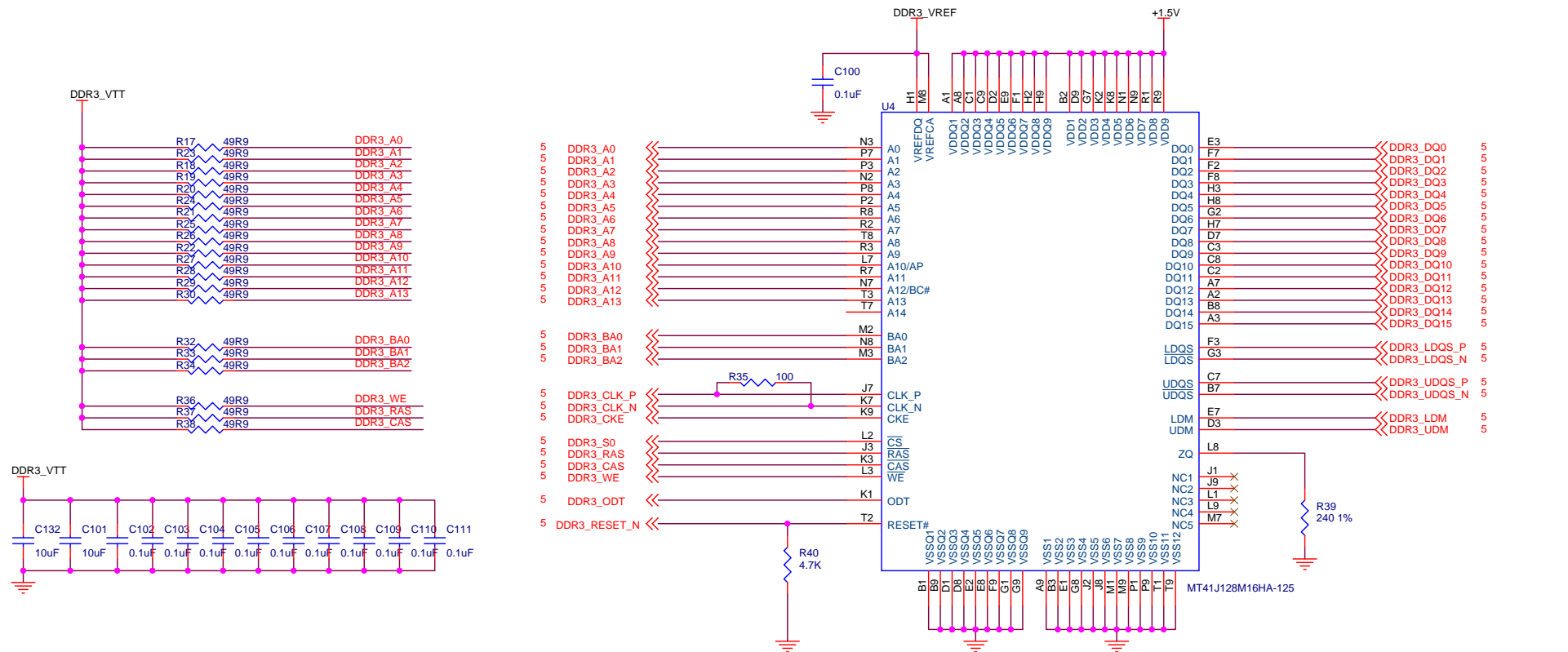
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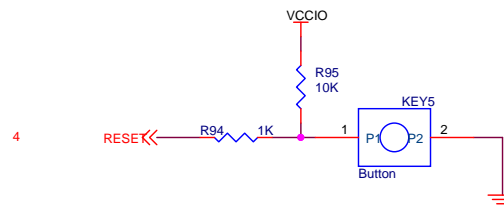
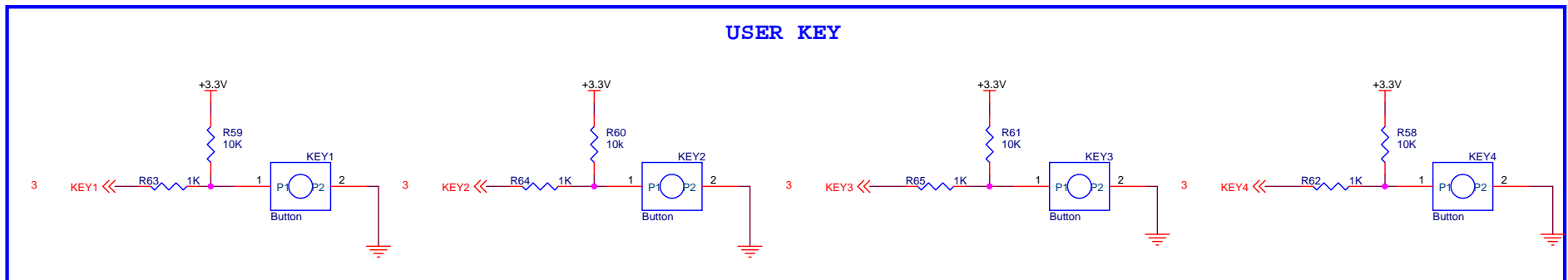
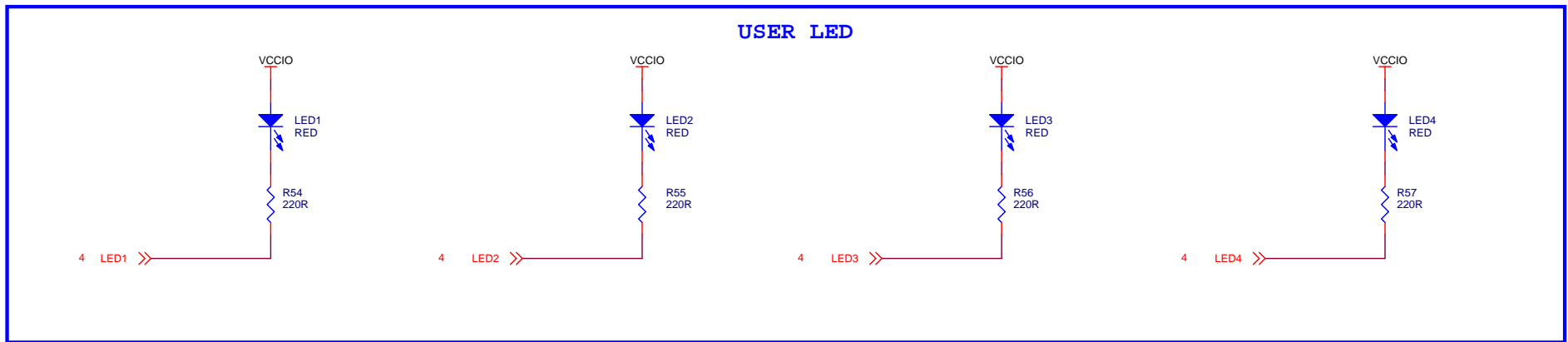
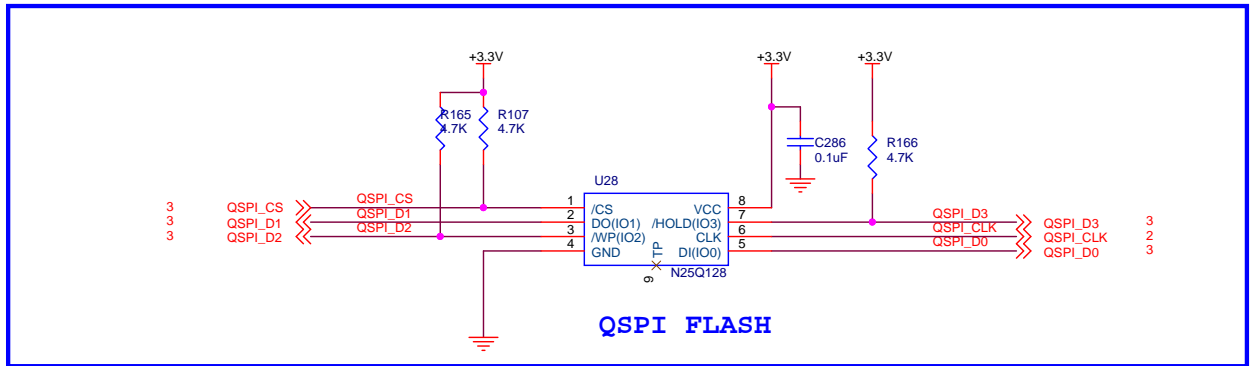
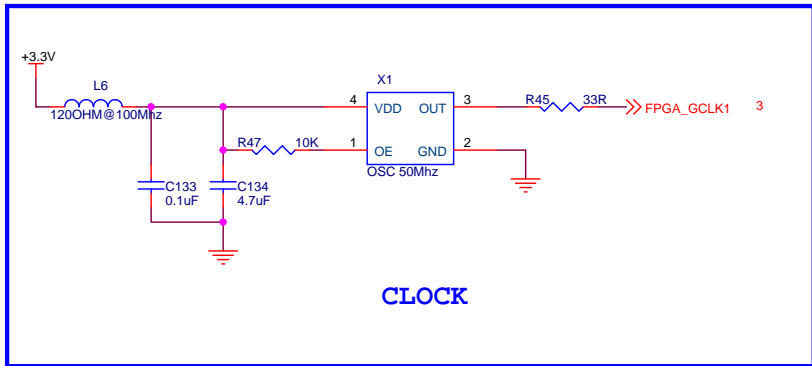
Internal VREF is used in this example



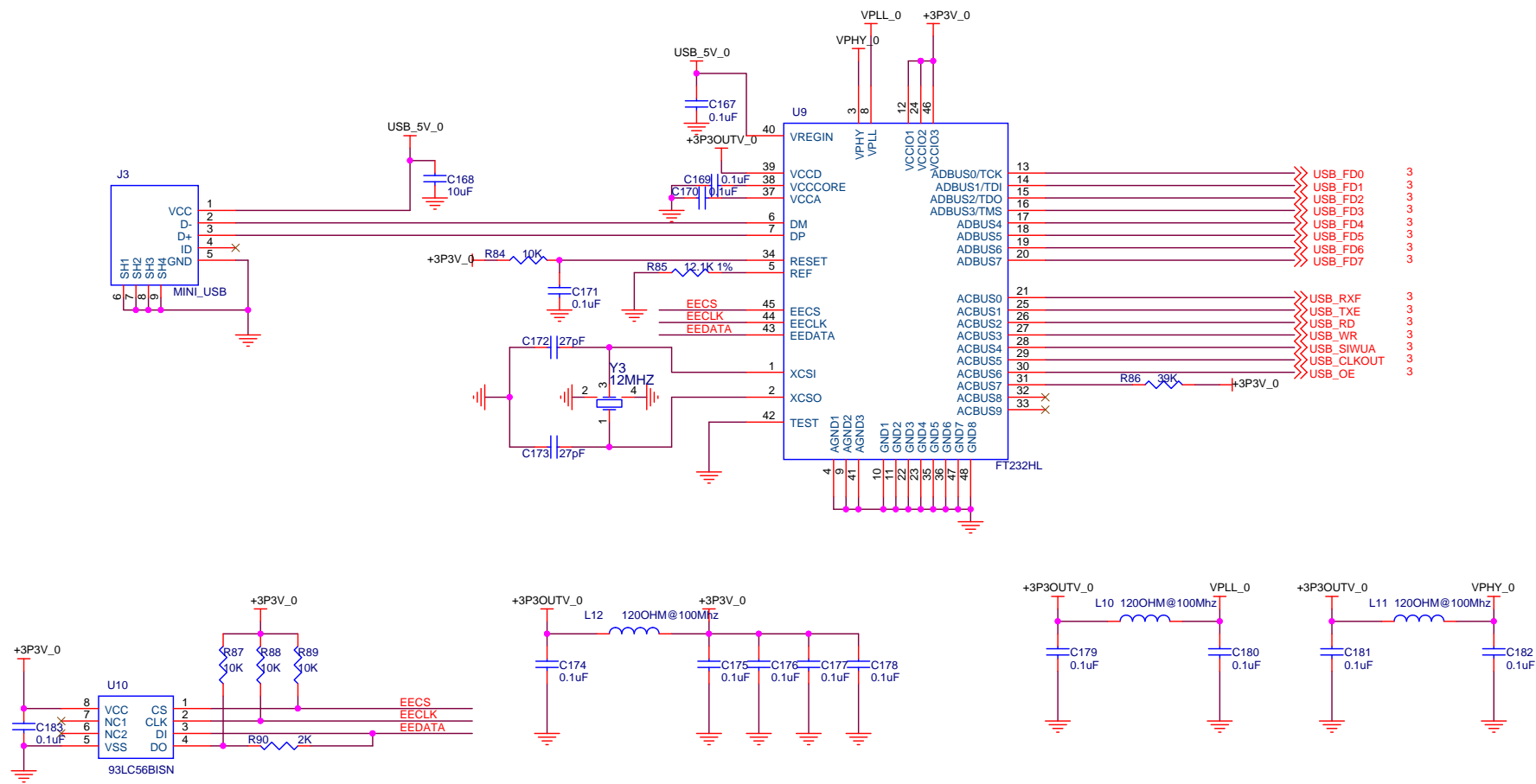


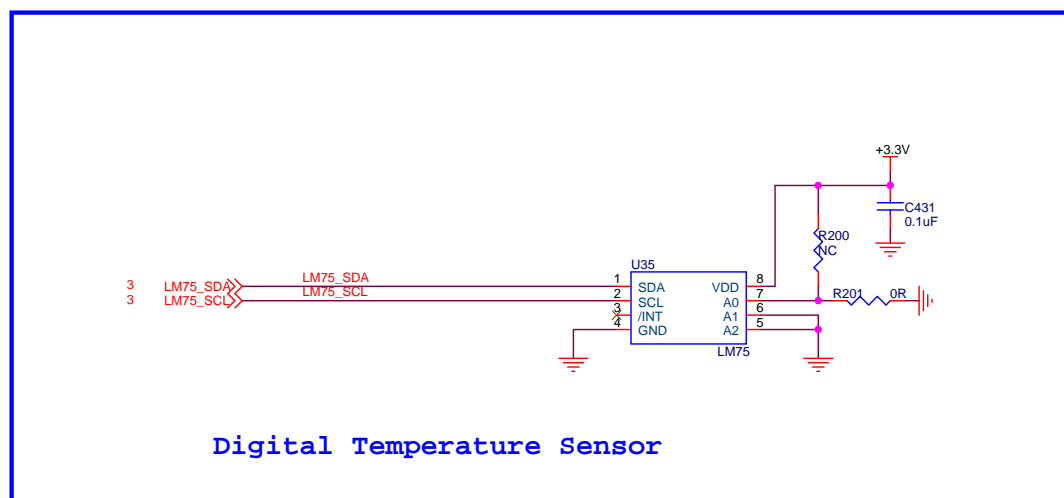
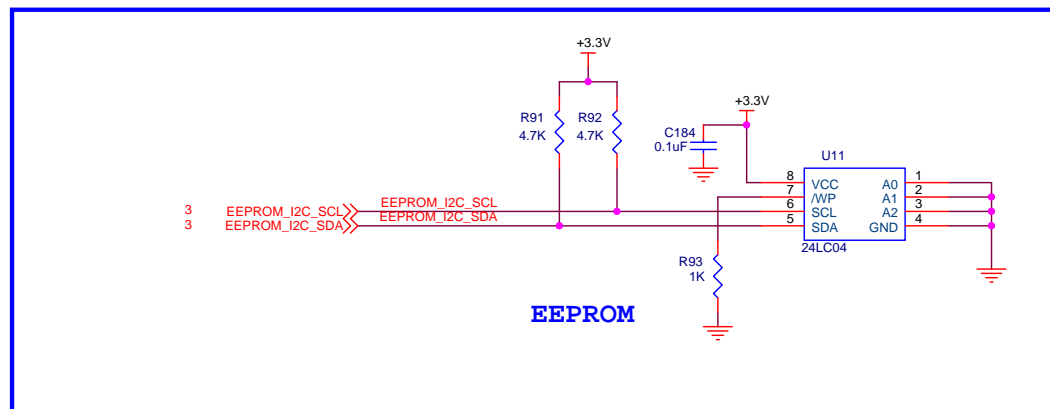


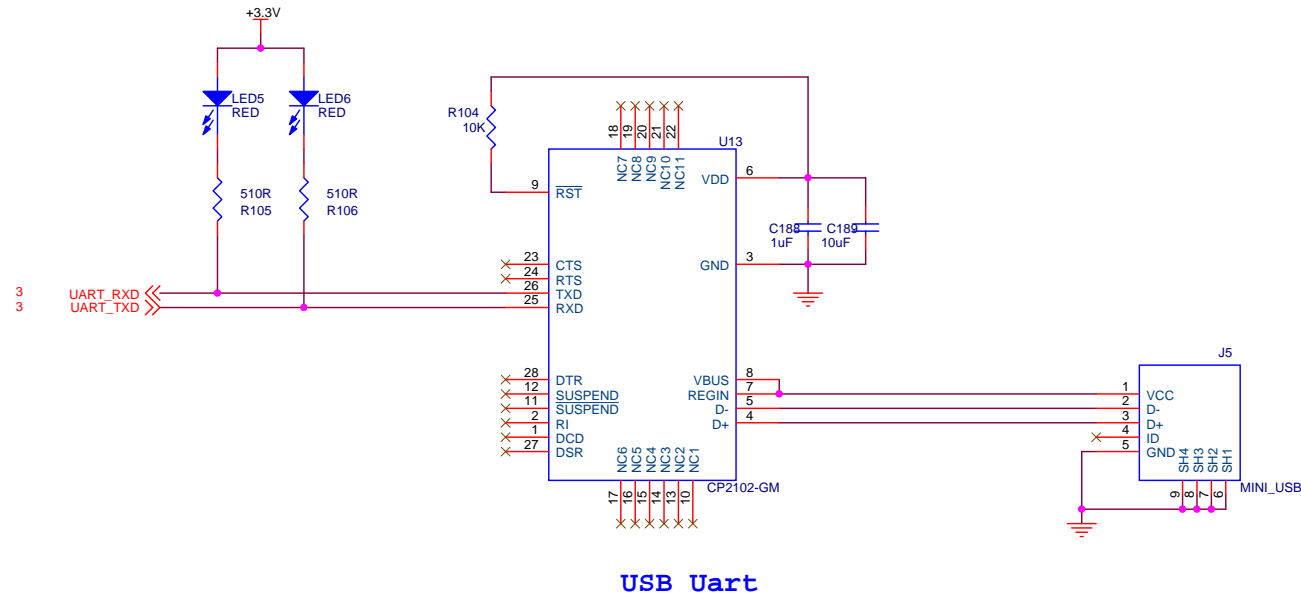
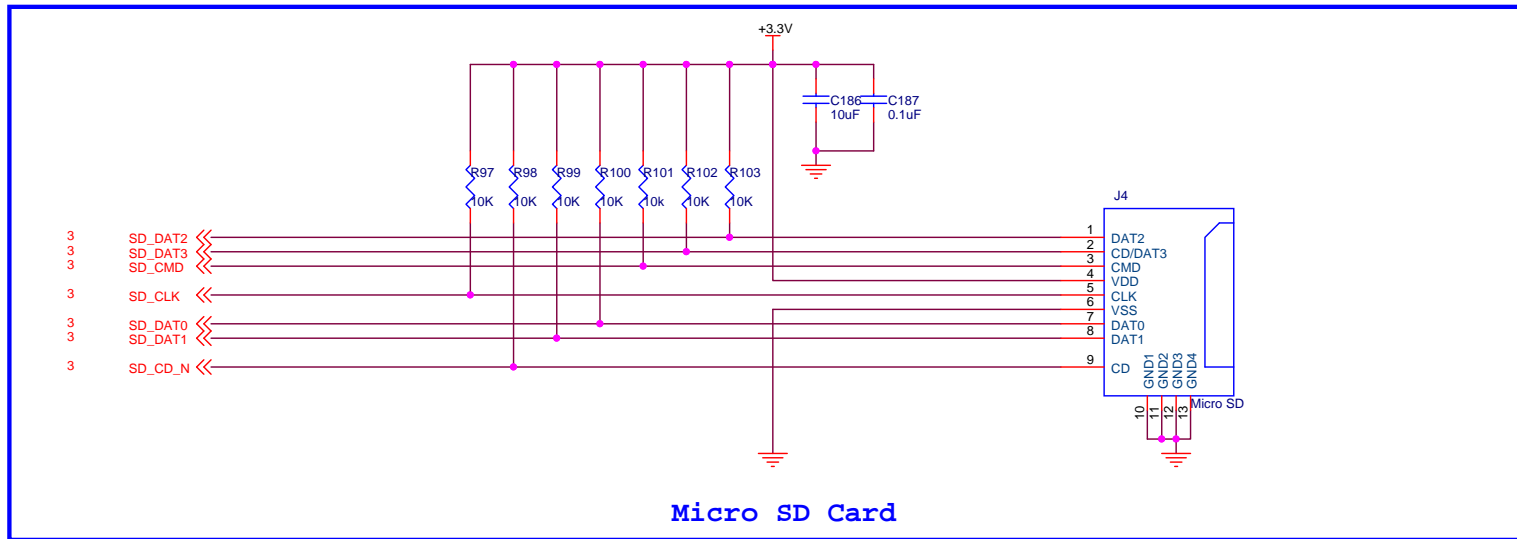


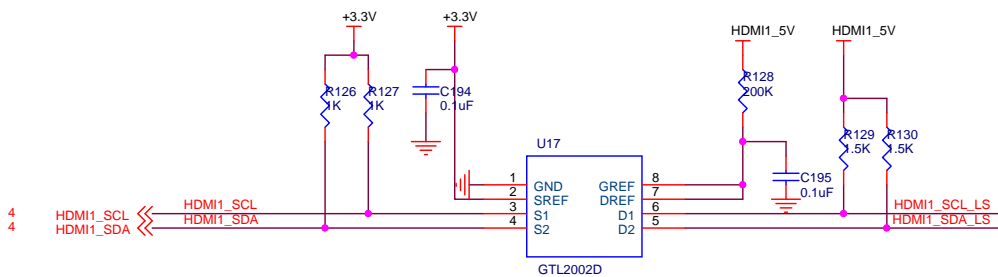
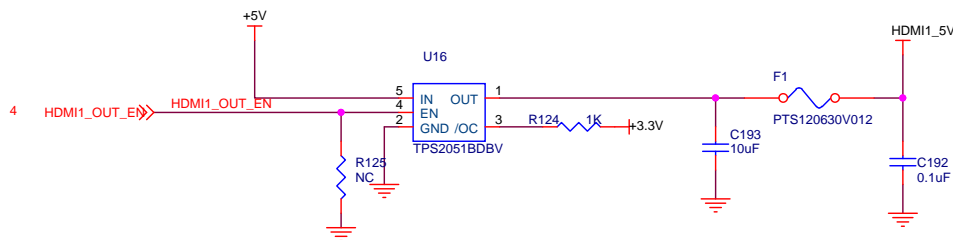
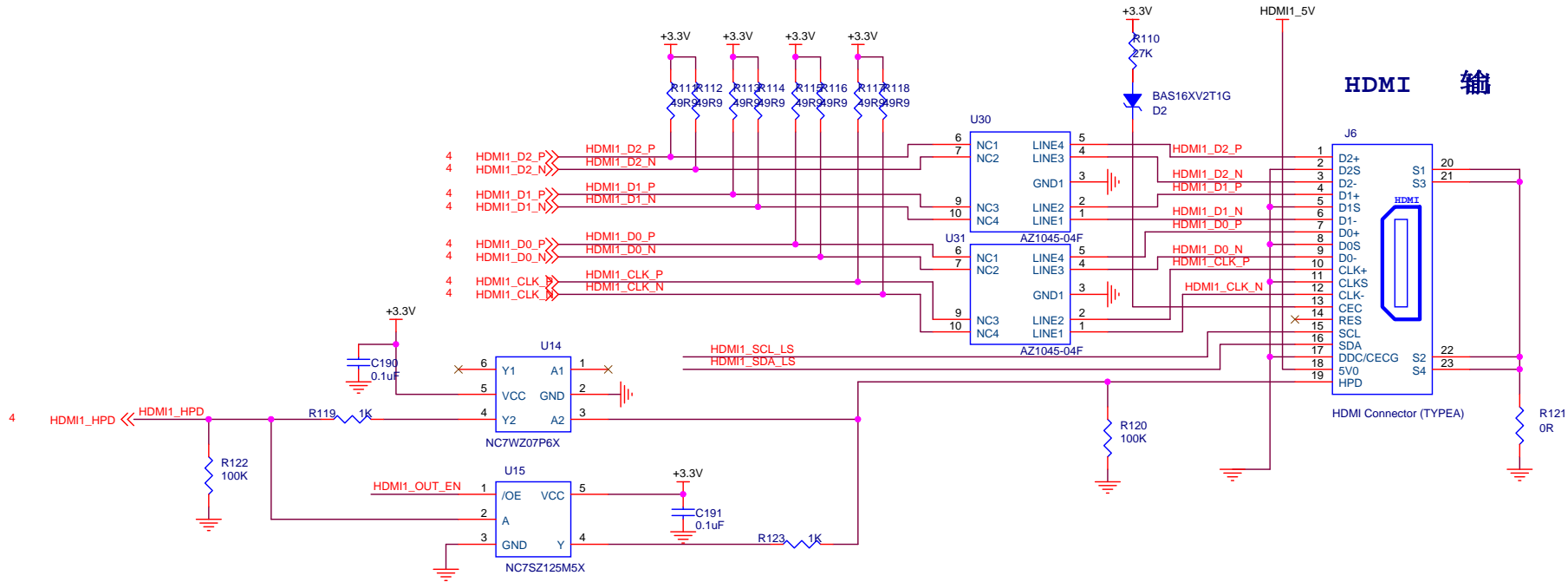


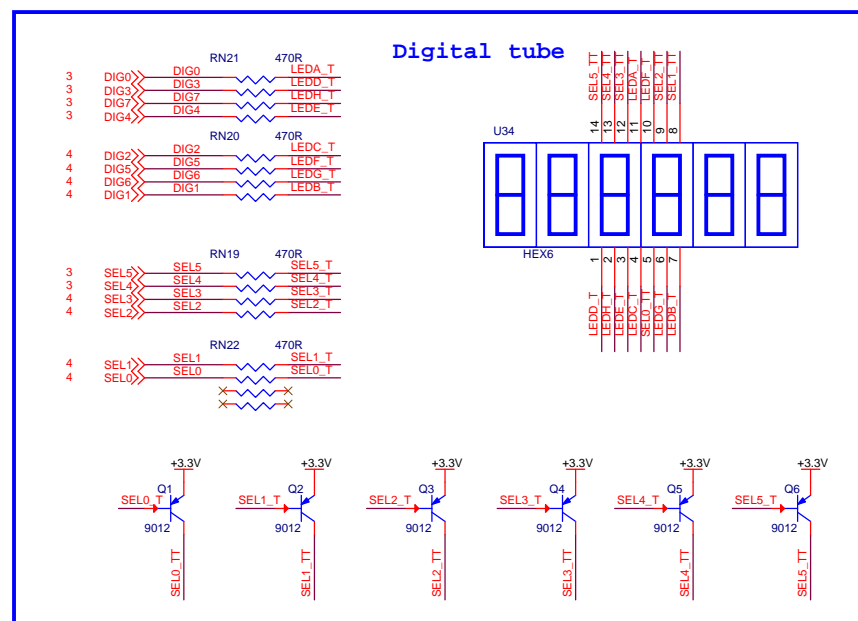
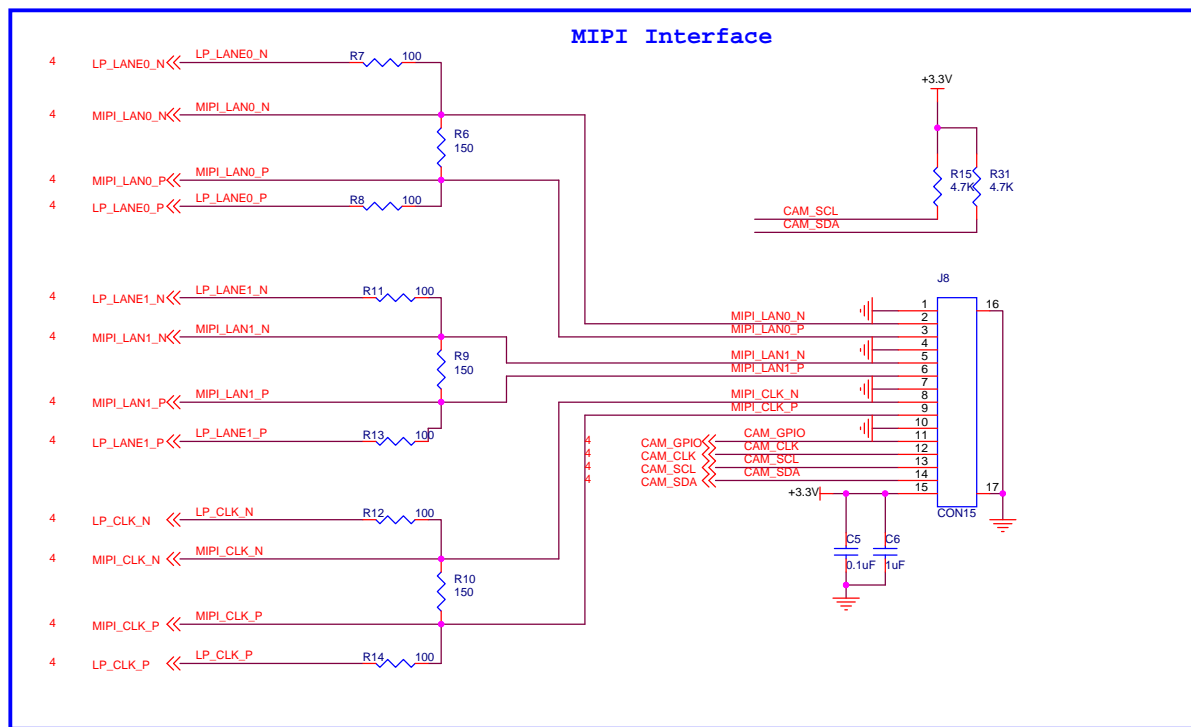
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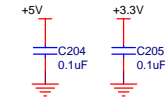
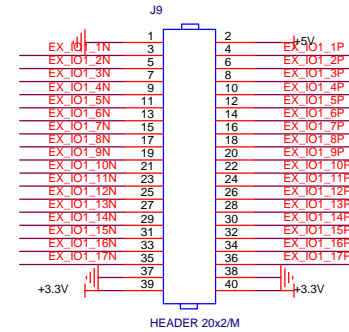




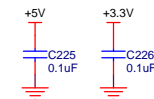
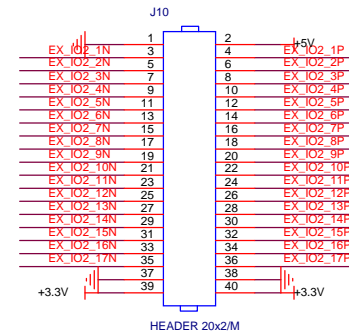




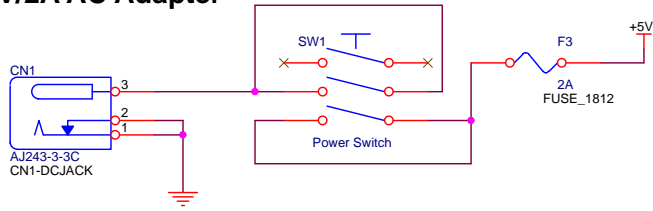
FPGA 40 PIN External IO



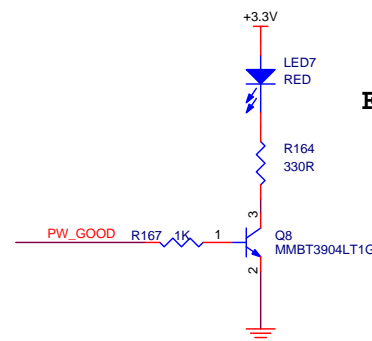
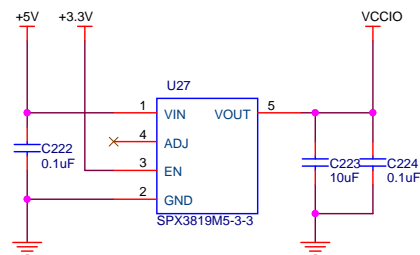
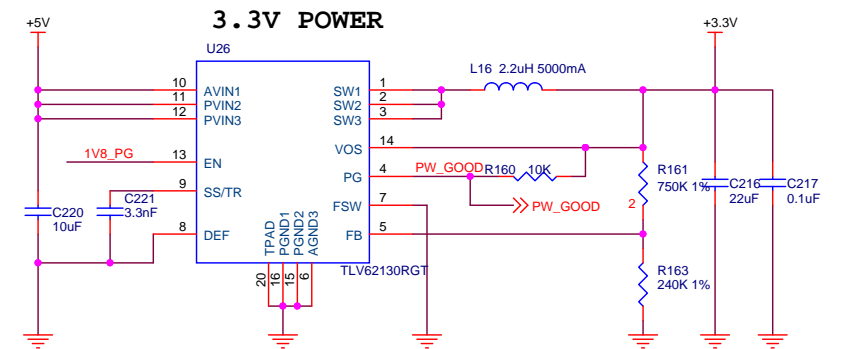
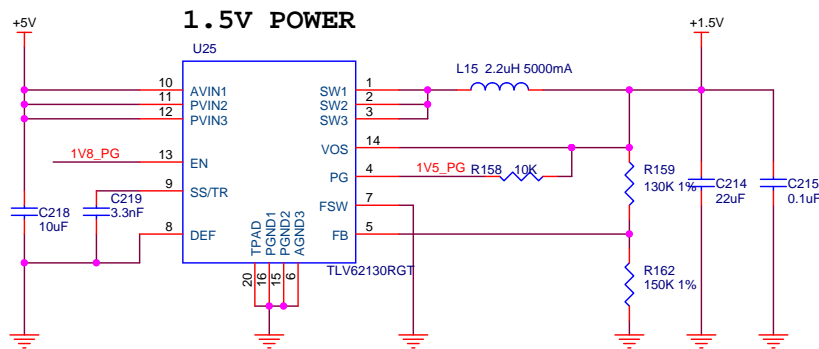
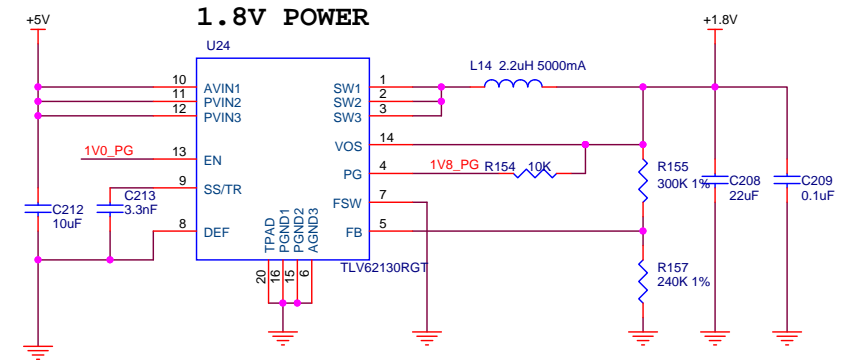
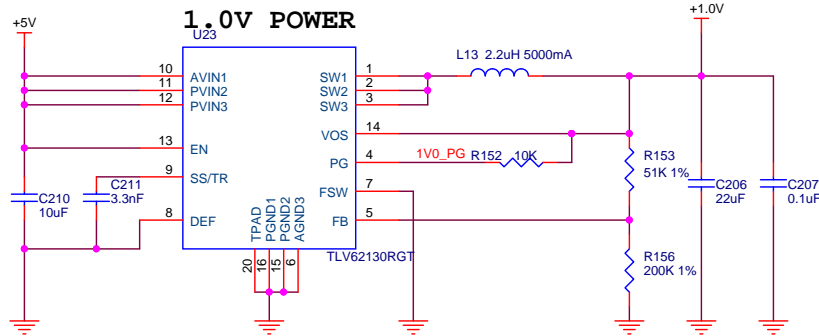
FPGA 40 PIN External IO



5V/2A AC Adapter



POWER ON: VCCINT(1.0V) -> VCCBRAM(1.0V) -> VCCAUX-(1.8V) > VCCO(1.5V and 3.3V)



FPGA Power LED