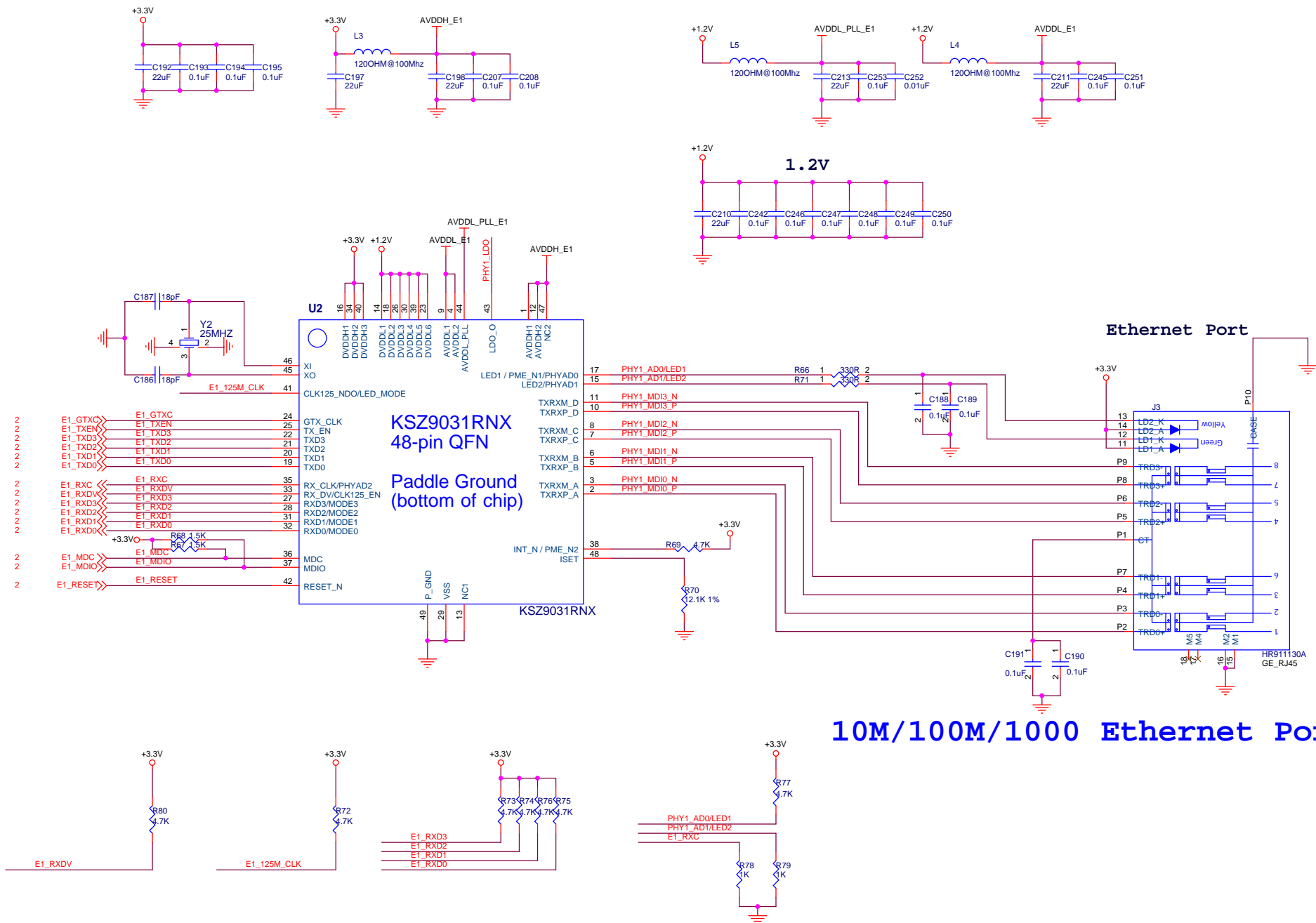
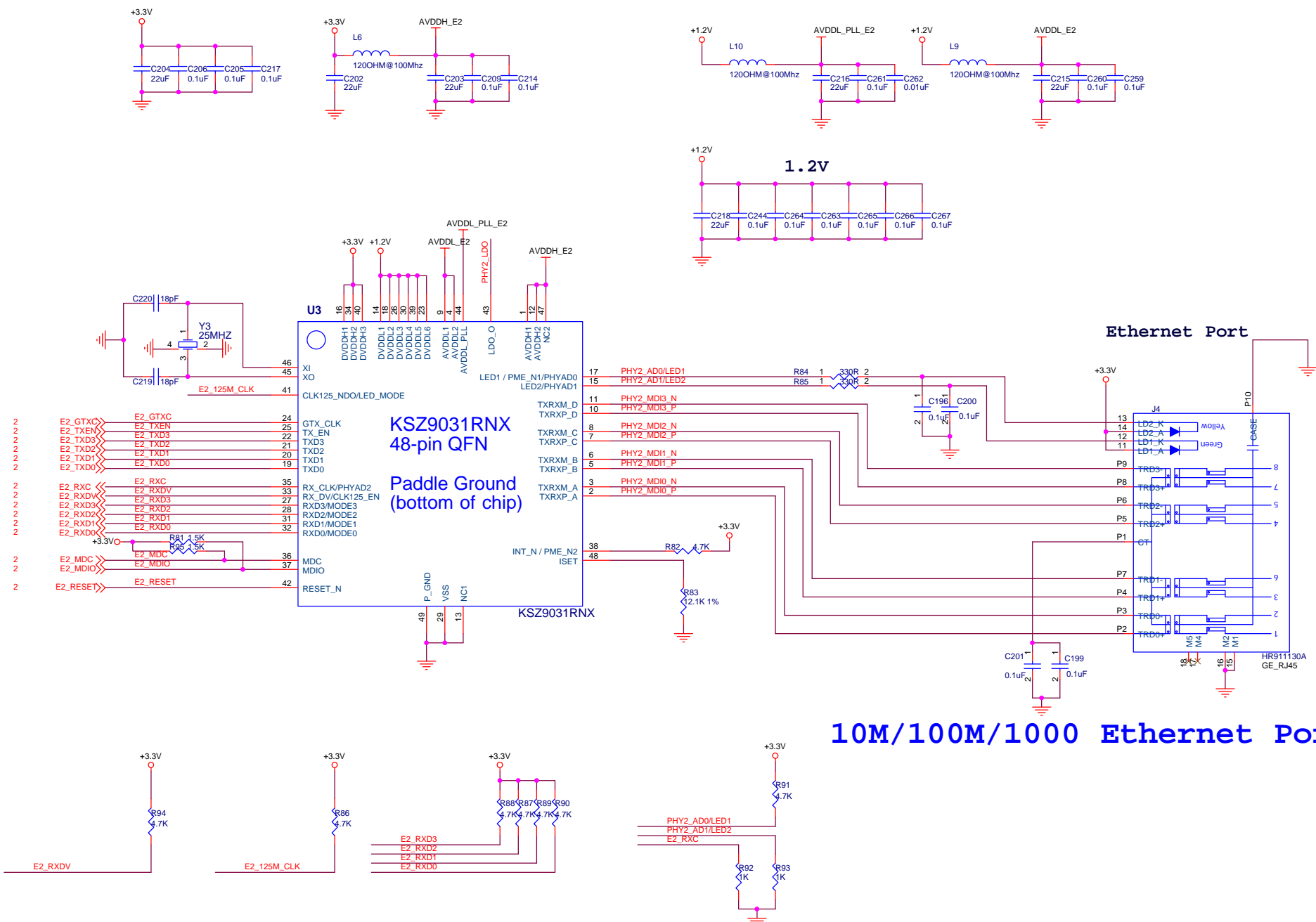
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Rev 1.0	
Date: Tuesday, June 07, 2022	
Sheet 2 of 11	

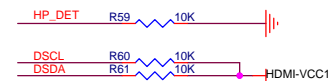
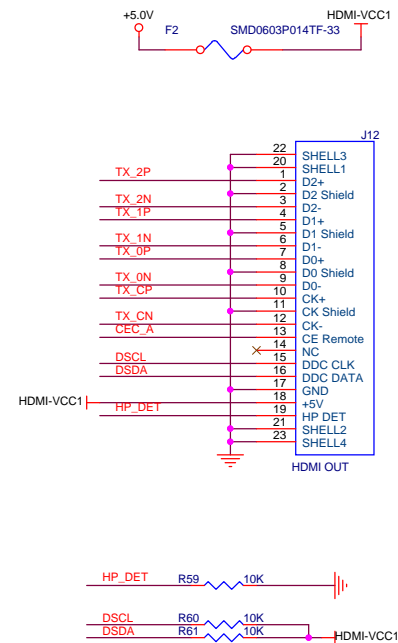
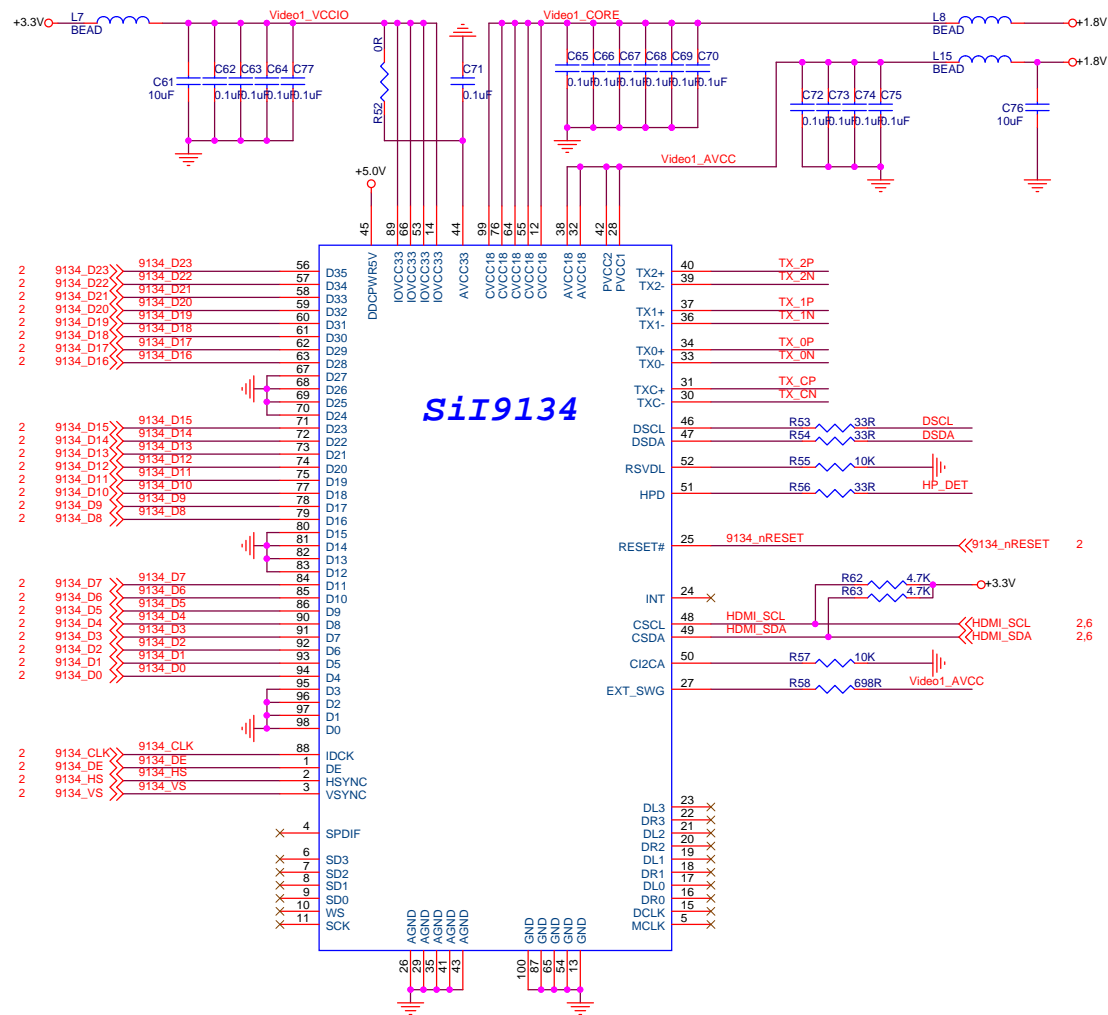


Enable 125Mhz Clock out Single-LED mode RGMII mode - Advertise all capabilities PHY Address is 001

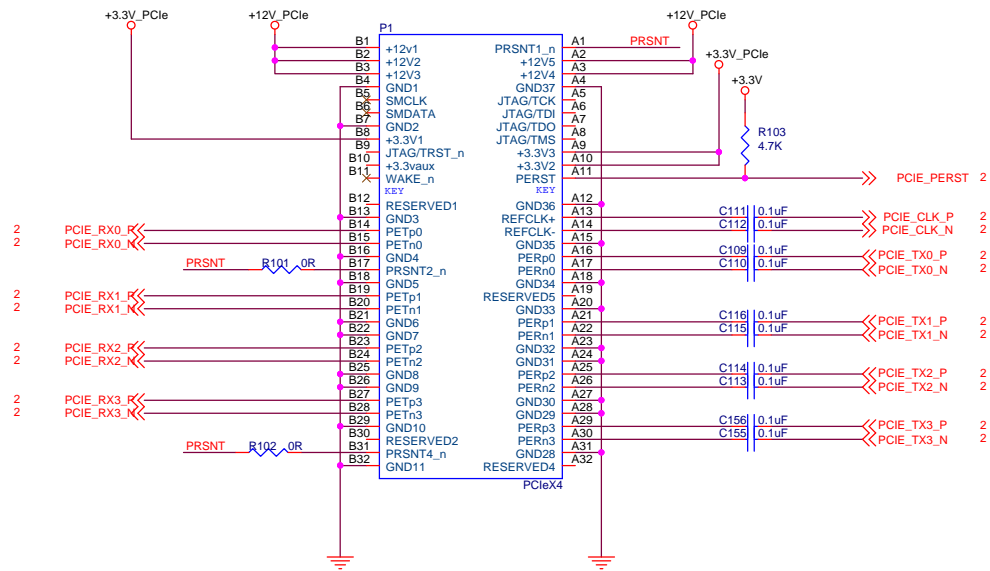
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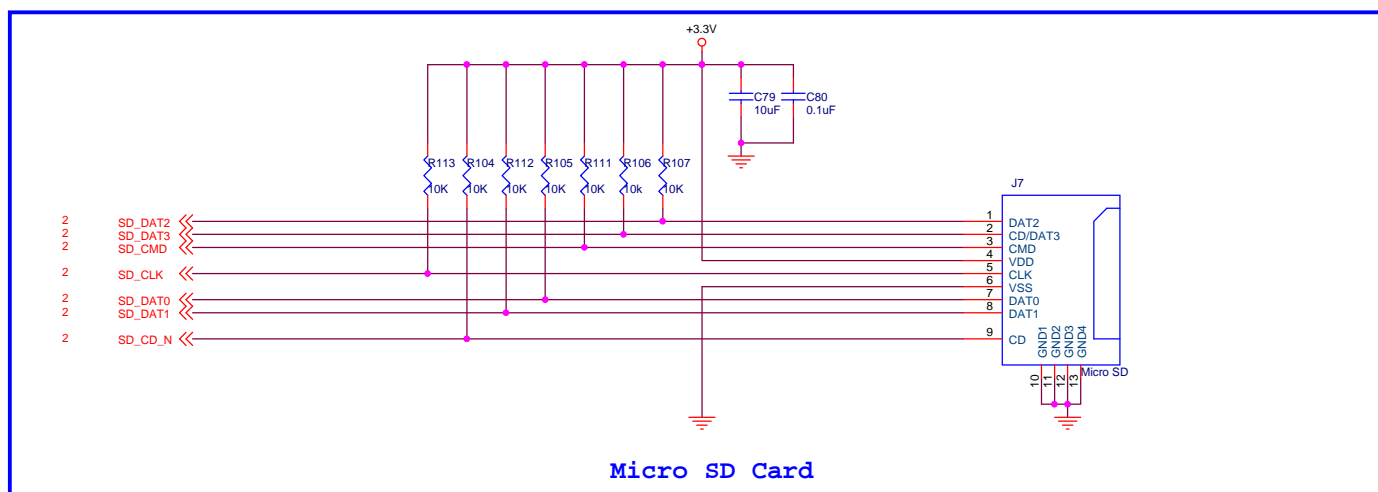
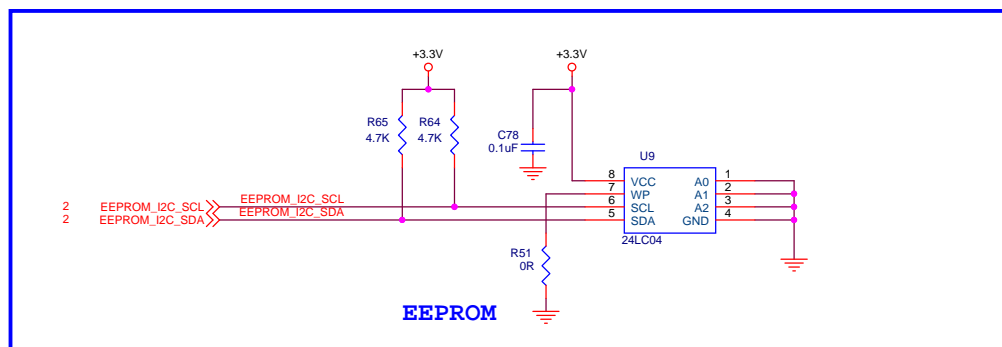


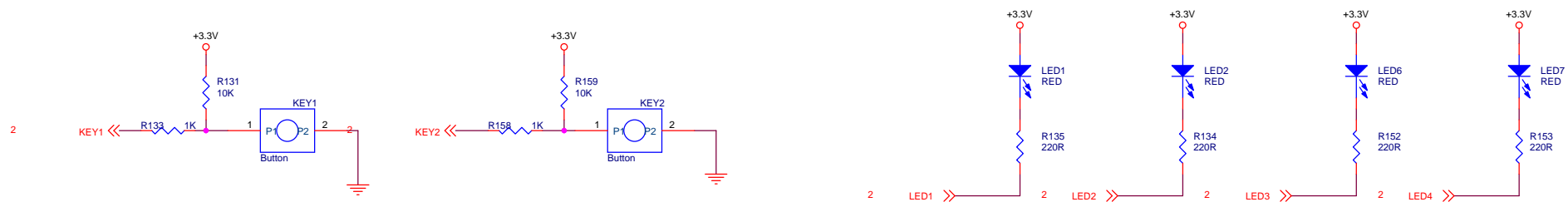
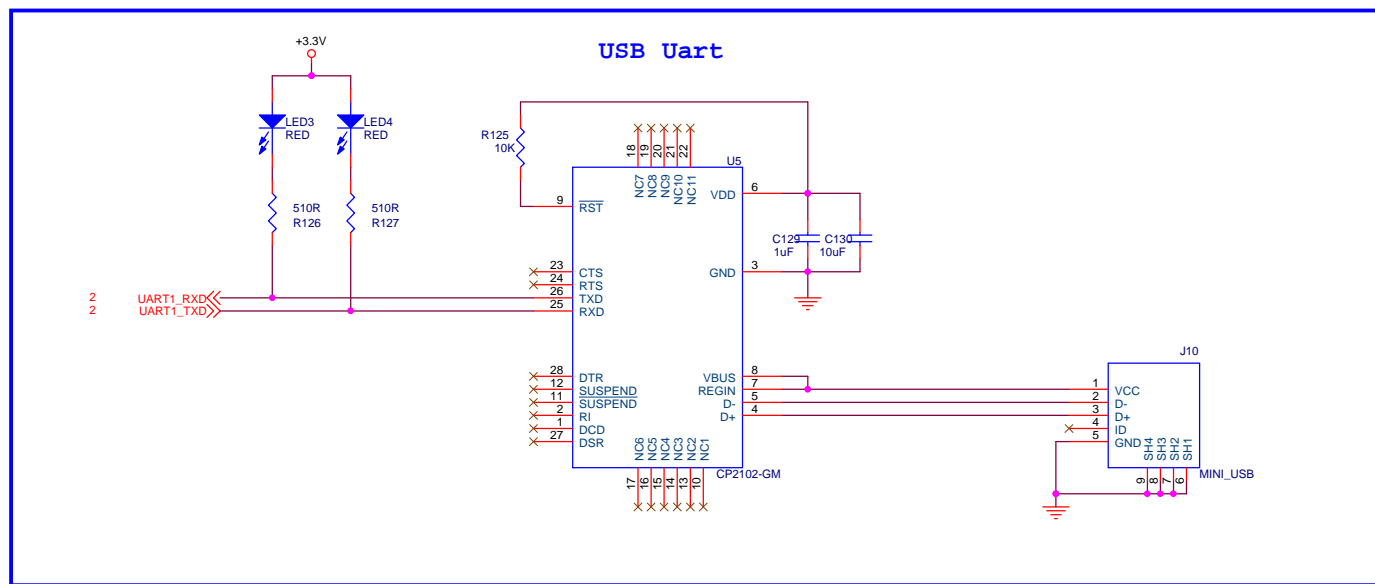
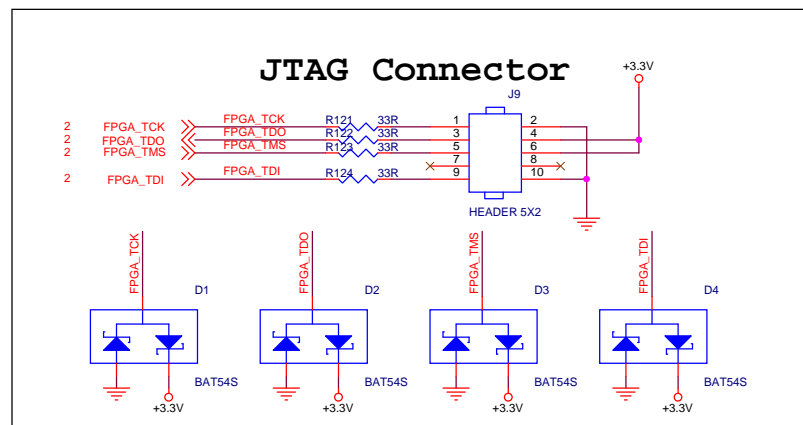
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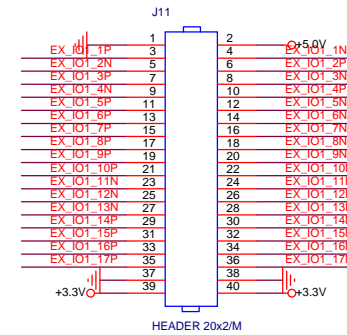
PCIE X4 SLOT



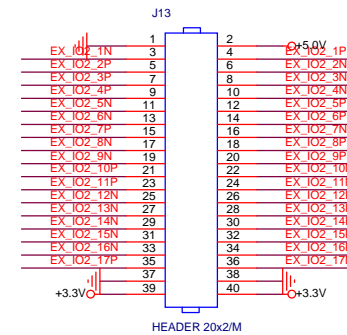




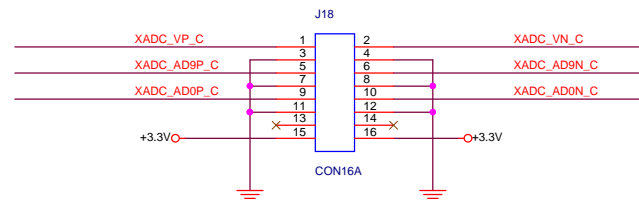
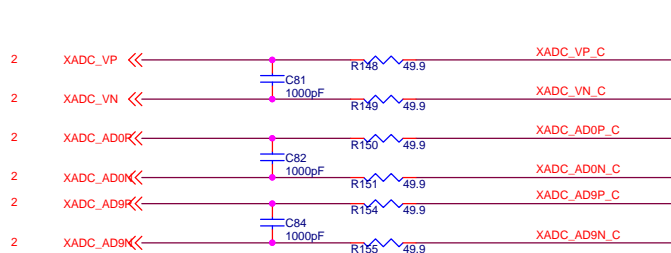
FPGA 40 PIN External IO



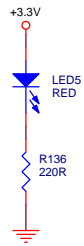
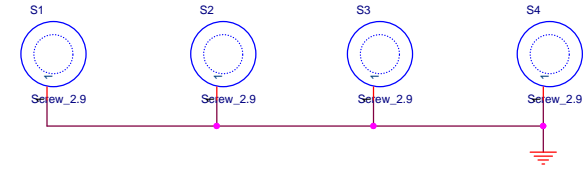
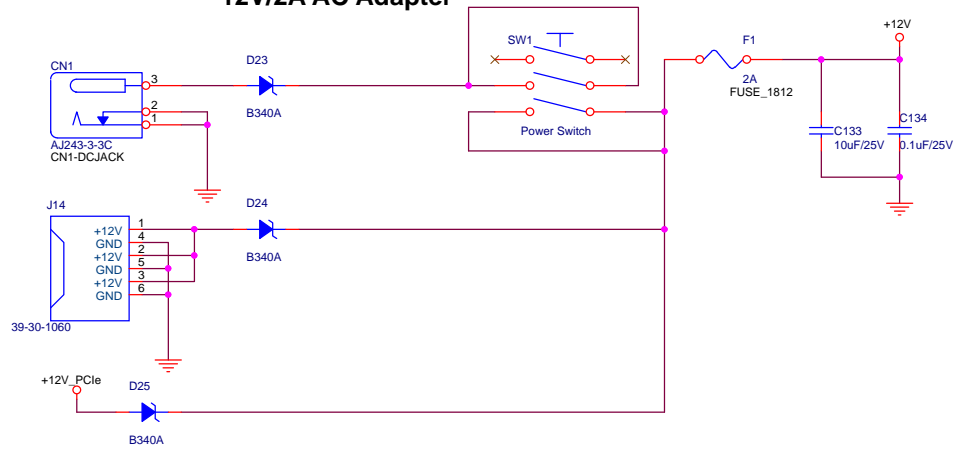
FPGA 40 PIN External IO



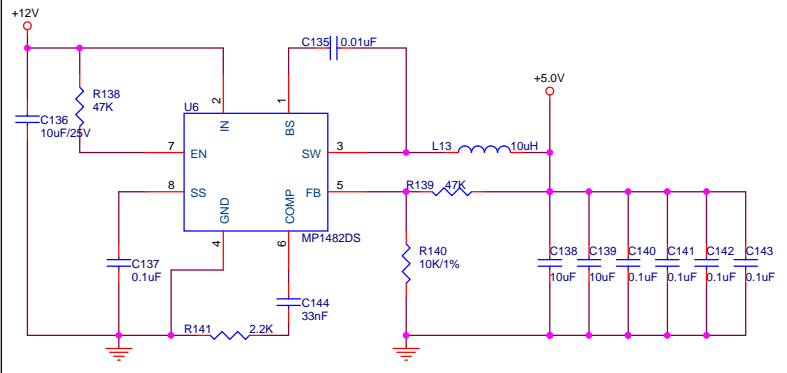
XADC Connector



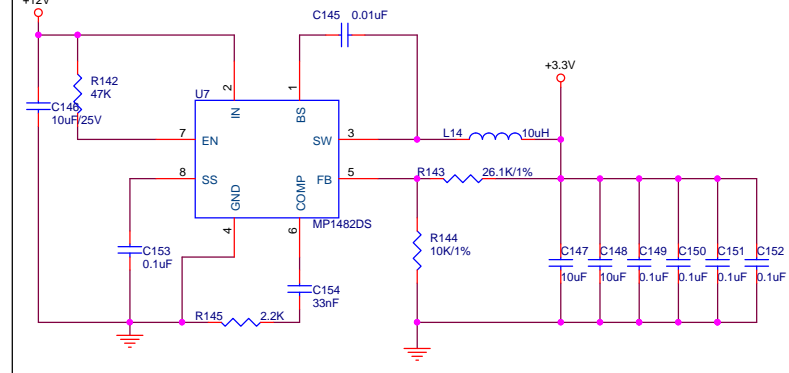
12V/2A AC Adapter



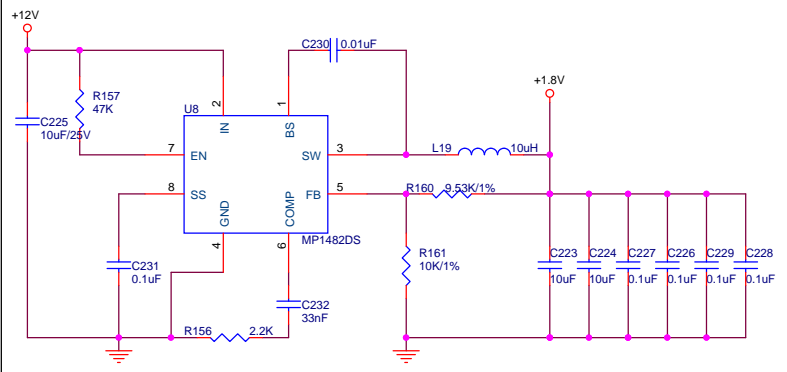
+5.0V POWER



+3.3V POWER



+1.8V POWER



+1.2V POWER

