REV	Description	Date
V1.0	First Release	2018-3-06

FPGA 核 心板

AC7100 Schematics

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Title: Cover Page

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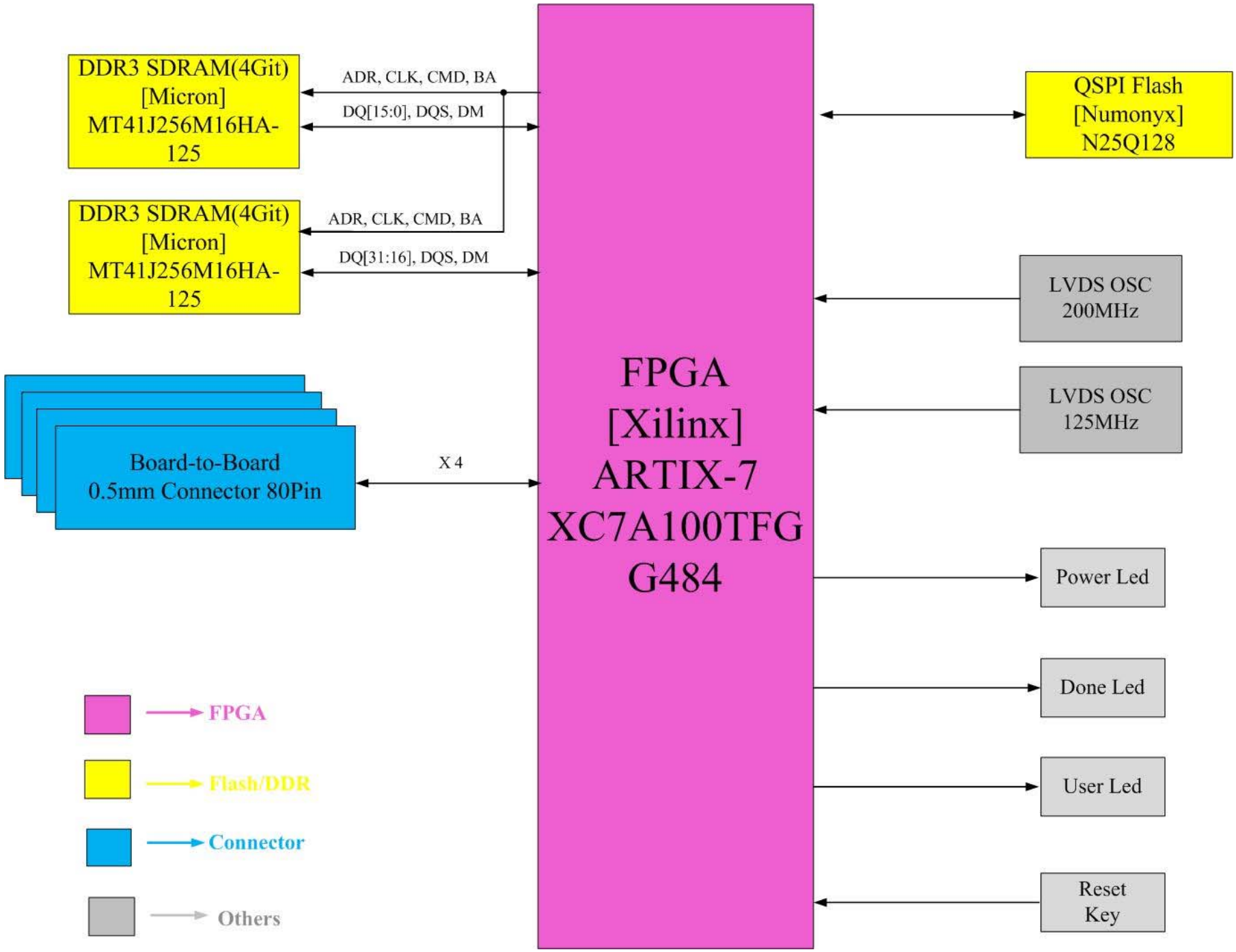

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Title	AC7100 BLOCK DIAGRAM	
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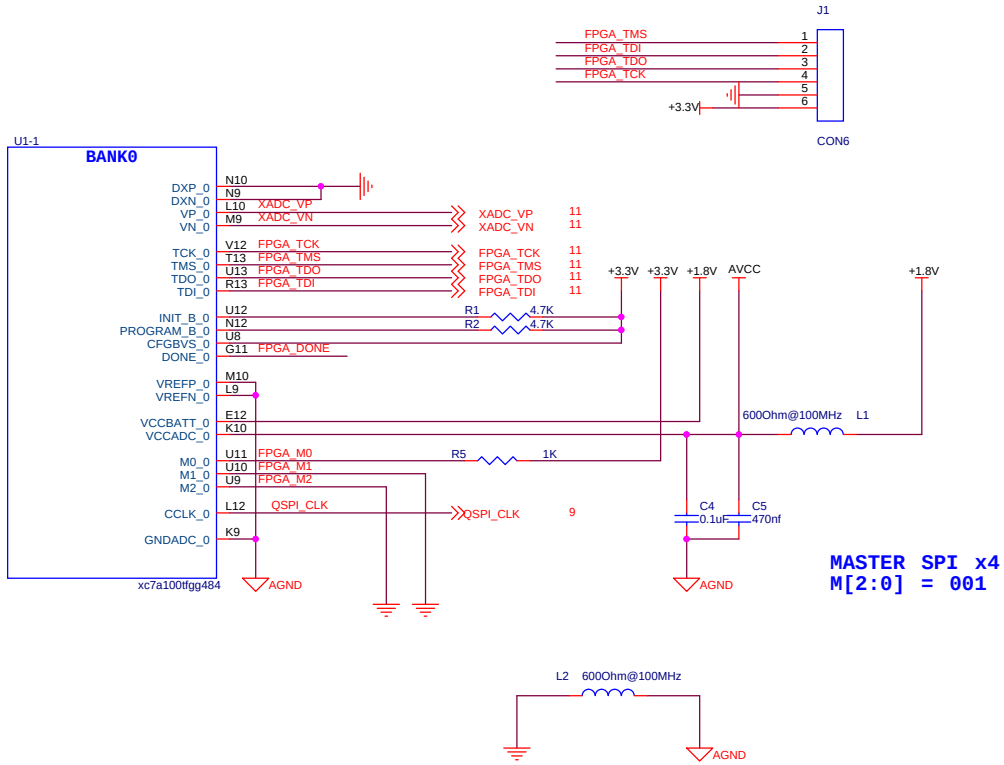

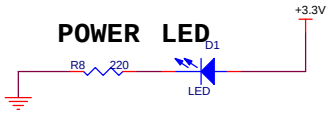

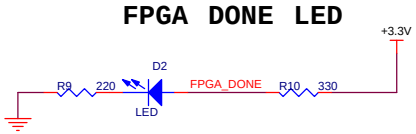

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Title	AC7100 Bank0	
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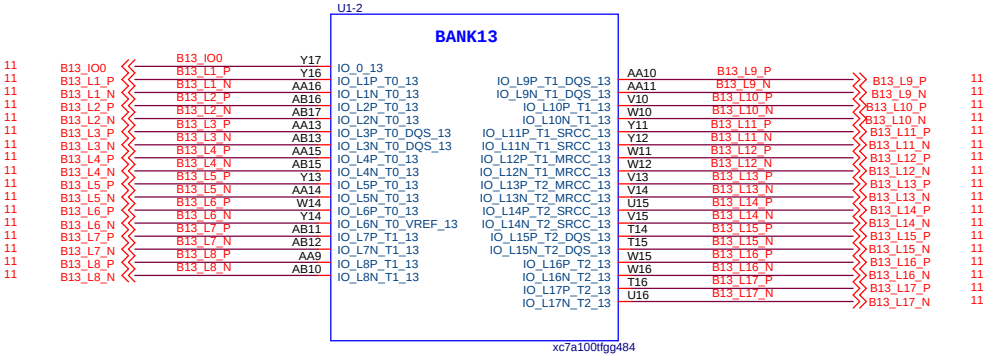
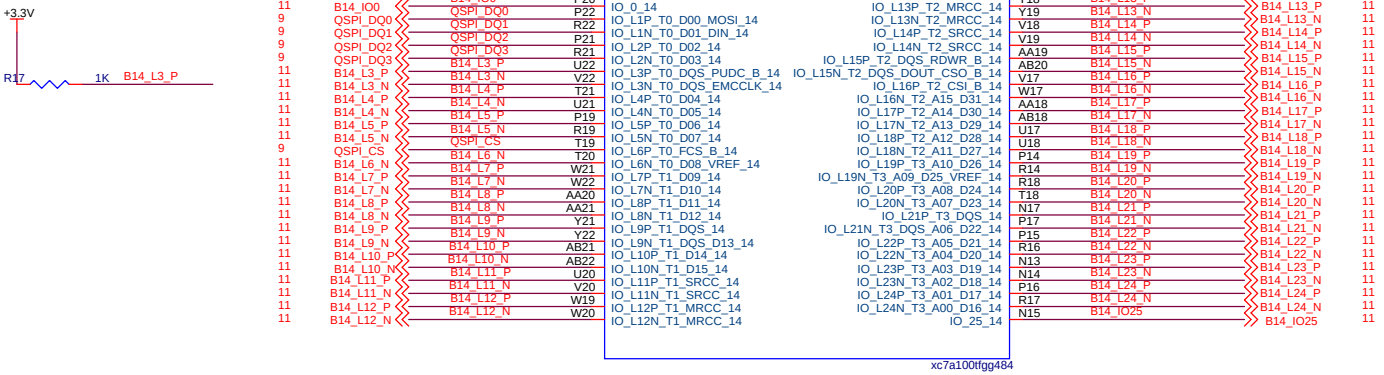


PUDC_B=1: Deactive internal Pull up Resister



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Title	AC7100 Bank13/14
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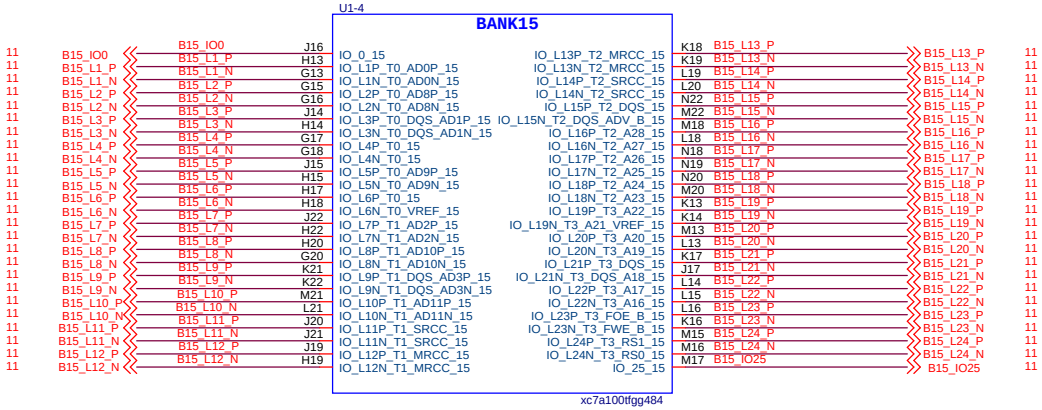

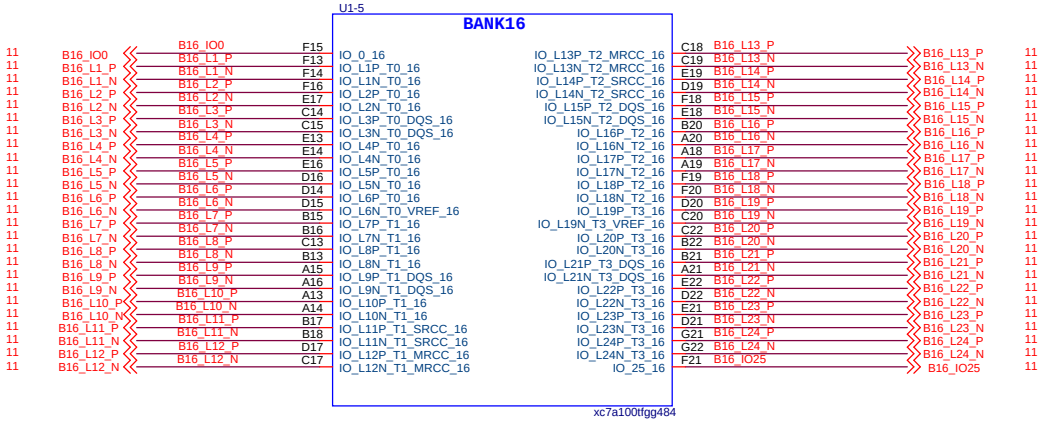

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Title: AC7100 Bank15/16

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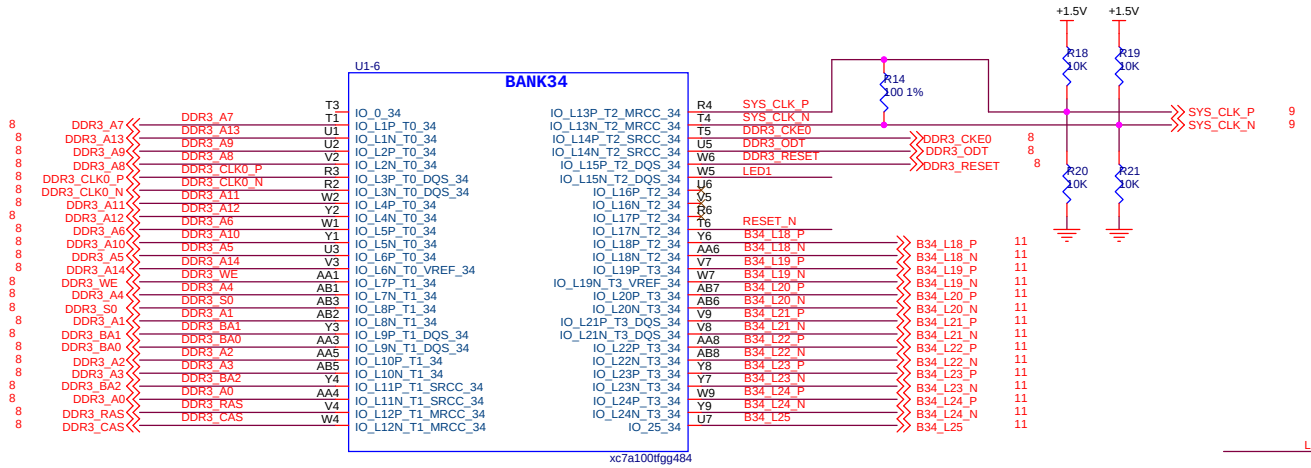
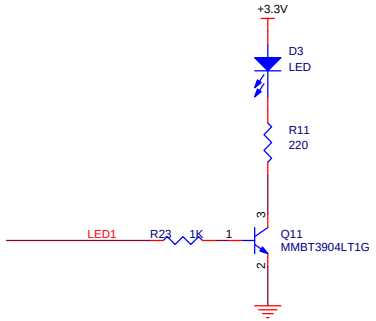
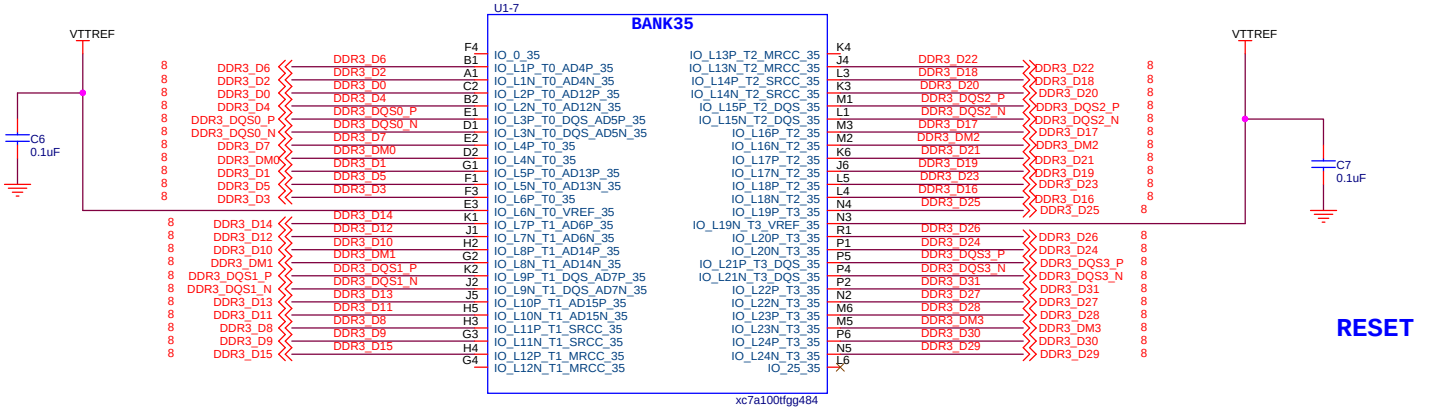
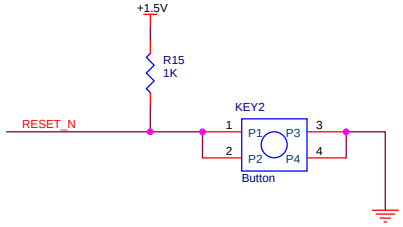


USER LED





RESET KEY



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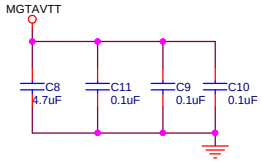
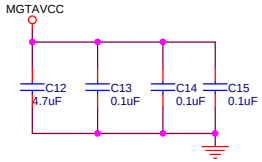
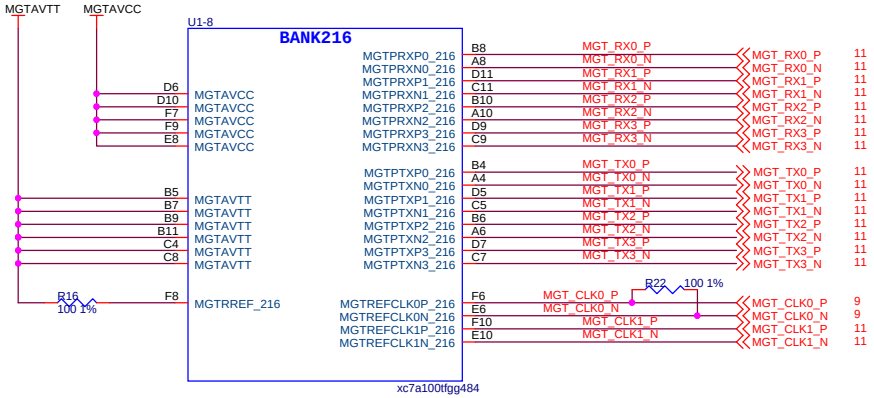
MGTAVTT　　4.7uF(1) 0.1uF(2)



MGTAVCC　　4.7uF(1) 0.1uF(2)





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Title	AC7100 Bank216
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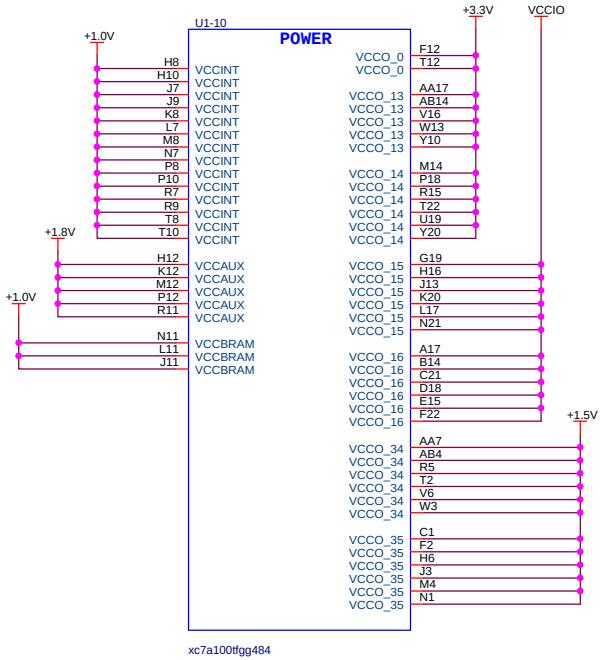

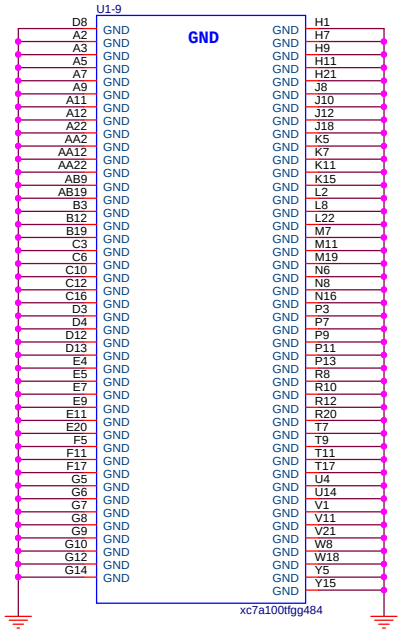

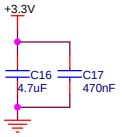

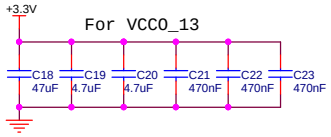

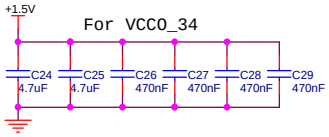

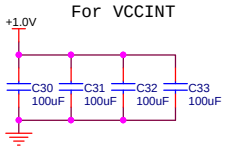

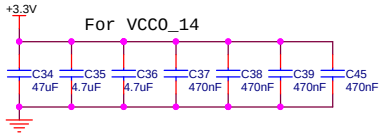

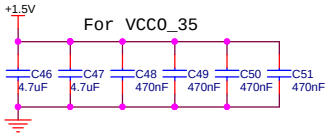

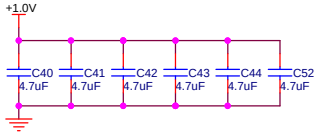

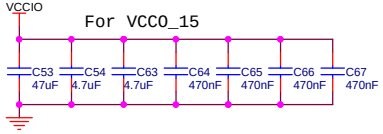

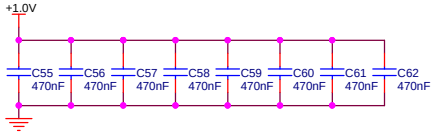

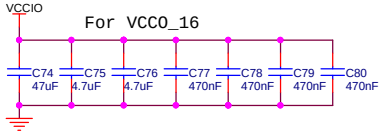

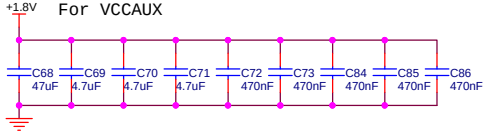

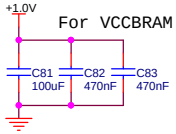

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Title	AC7100 FPGA POWER
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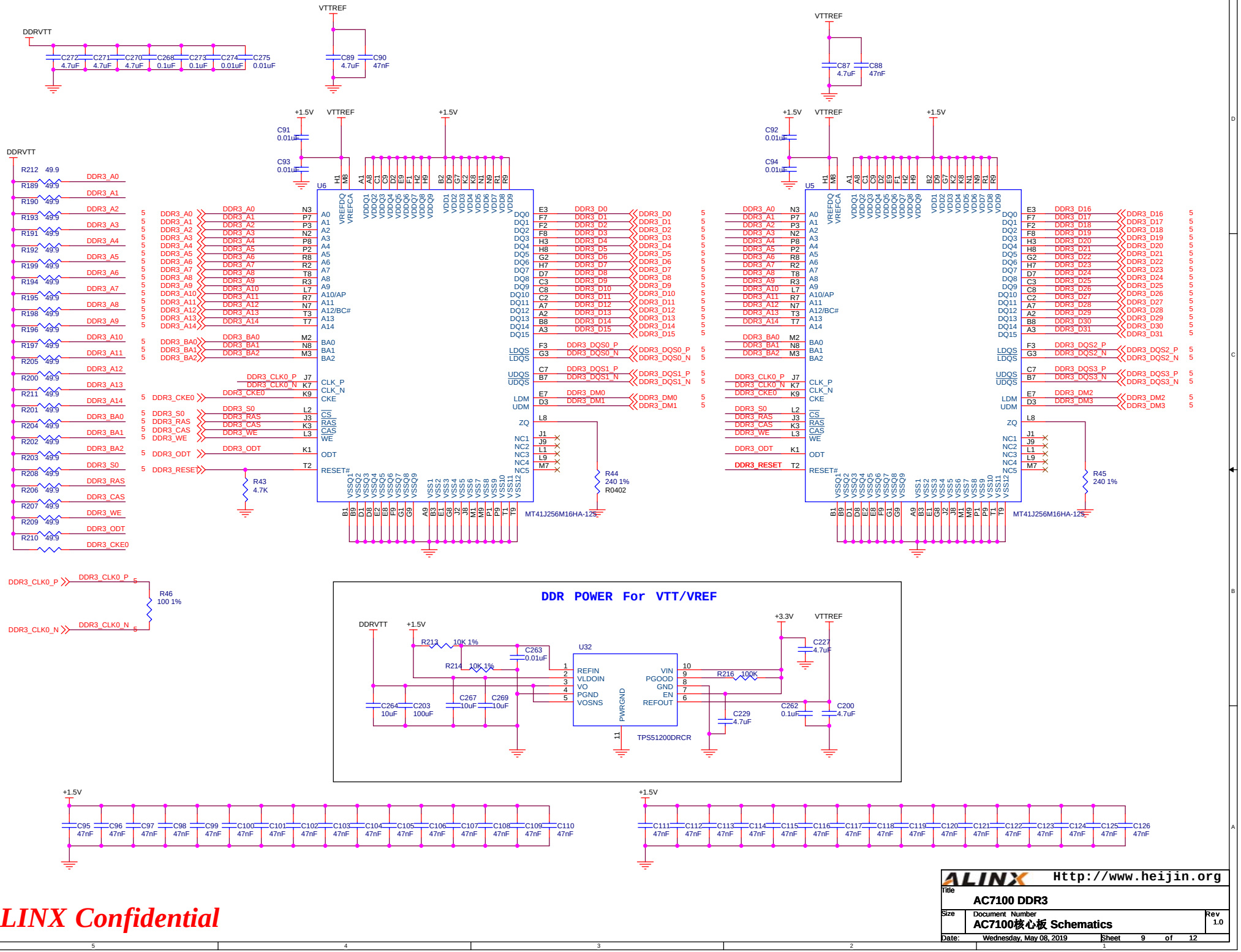

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Title	AC7100 DDR3
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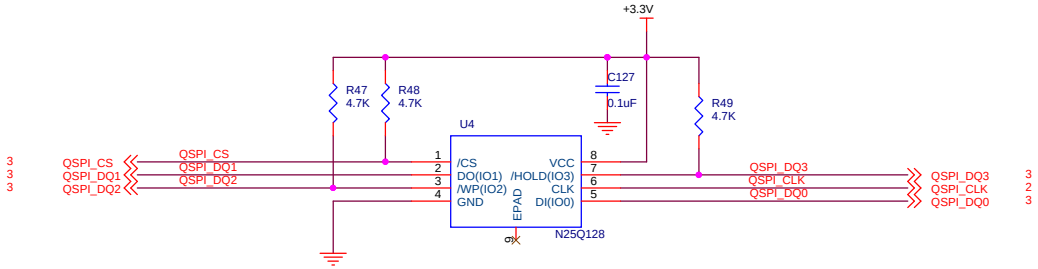
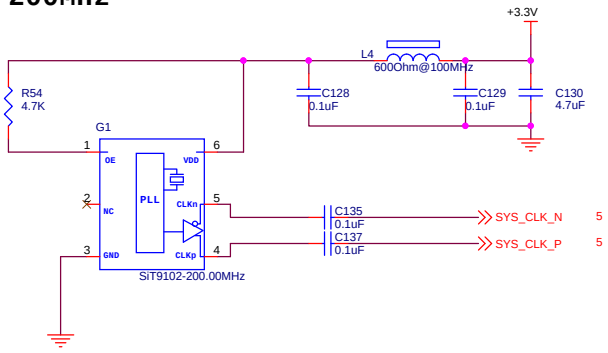
FPGA CONFIG SPI



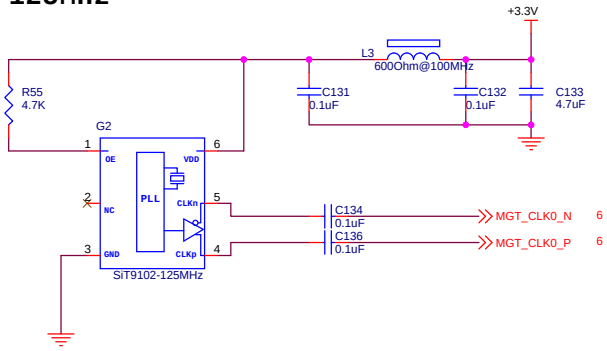
SYSTEM CLOCK

200MHz



GTP CLOCK

125MHz



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Title	AC7100 FLASH&CLOCK	
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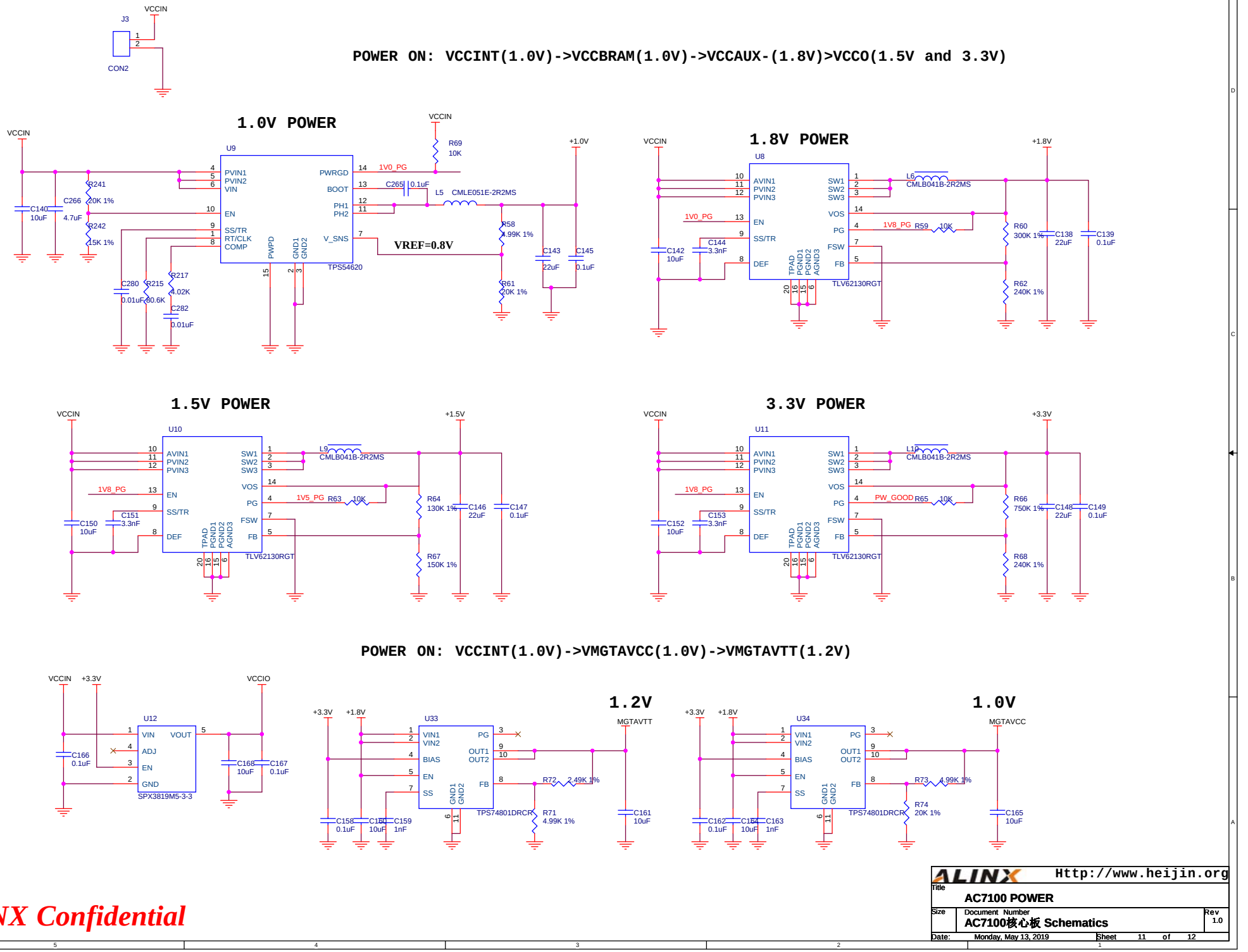
POWER ON: VCCINT(1.0V)->VCCBRAM(1.0V)->VCCAUX-(1.8V)>VCCO(1.5V and 3.3V)
1.0V POWER
1.8V POWER
1.5V POWER
3.3V POWER
VCCIN
J3
CON2
U9
TPS54620
VREF=0.8V
U8
TLV62130RGT
U10
U11
POWER ON: VCCINT(1.0V)->VMGTAVCC(1.0V)->VMGTAVTT(1.2V)
U12
SPX3819M5-3-3
VCCIO
1.2V
MGTAVTT
U33
TPS74801DRCR
1.0V
MGTAVCC
U34
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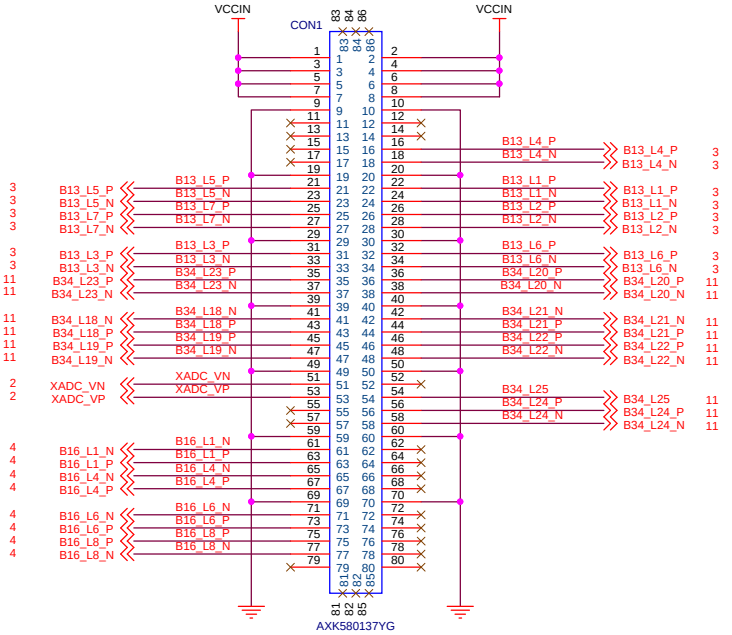
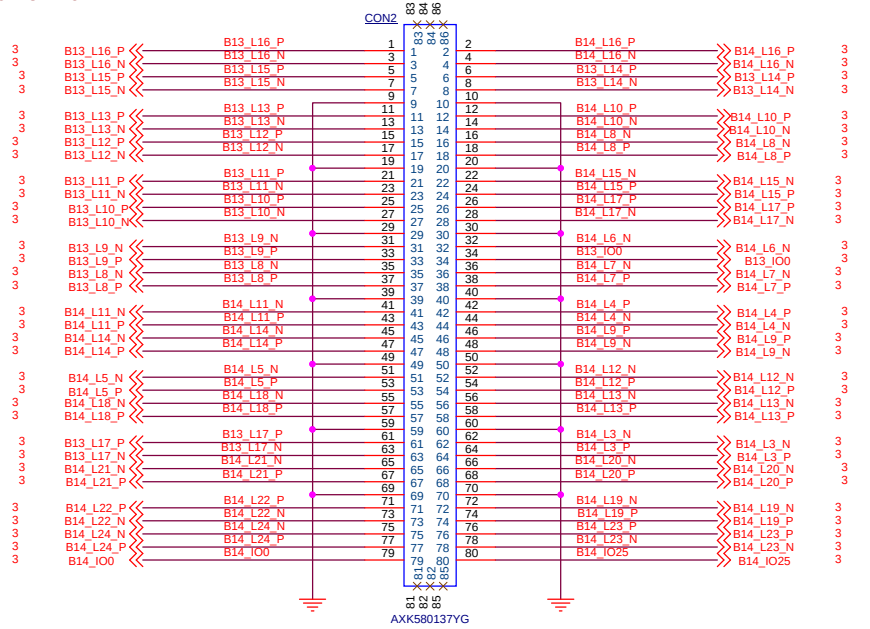
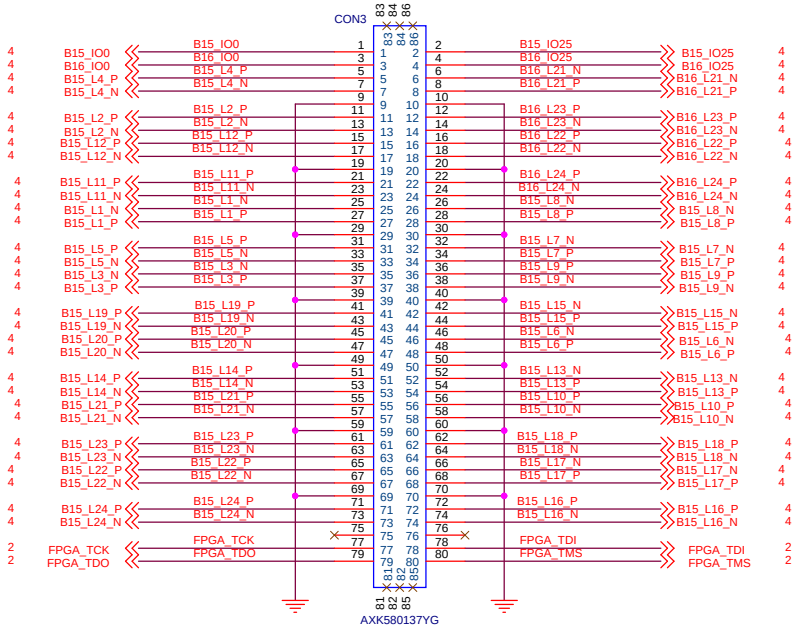
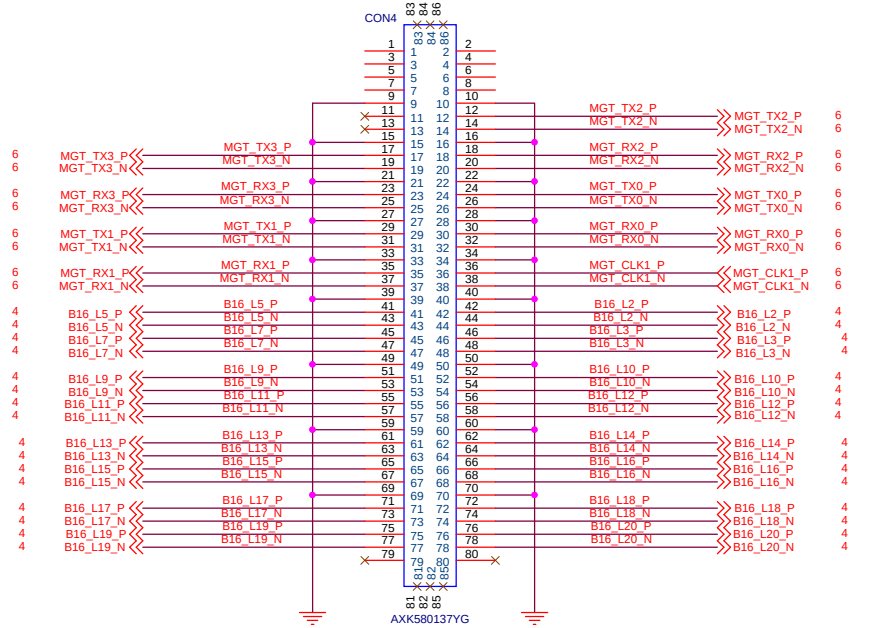
AC7100 POWER
AC7100核心板 Schematics
Monday, May 13, 2019

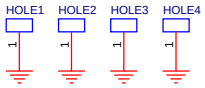
These IOs are on BANK34, Voltage is 1.5V!!!











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Title: AC7100 CONNECTOR

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