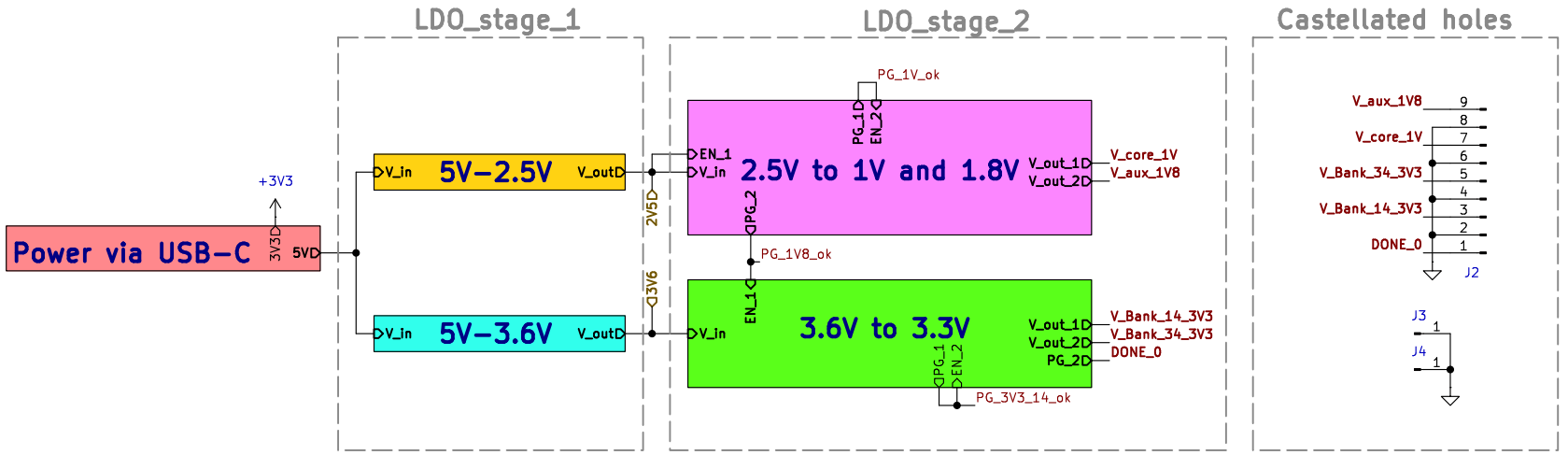
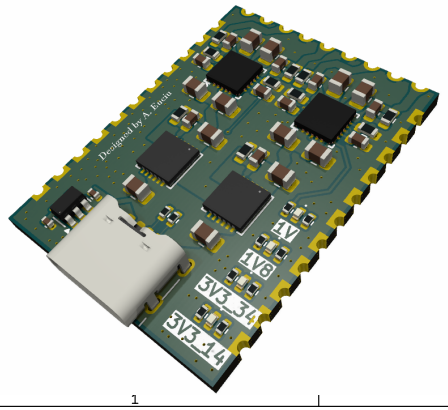
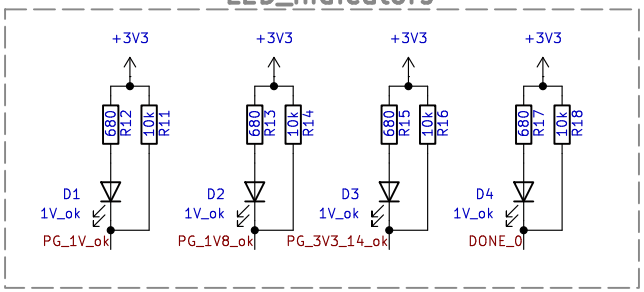
Note: FPGA Power sequence: V_core_1V -> V_aux_1V8 -> V_bank_3V3
Power regulation via LDOs cascade







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Institution: Technische Universität Darmstadt

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Title: PSU Stamp for Spartan7-FTGB196

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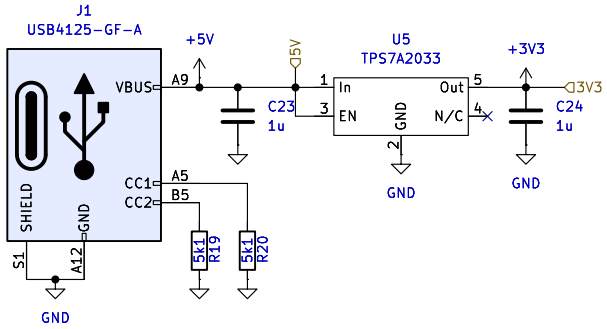

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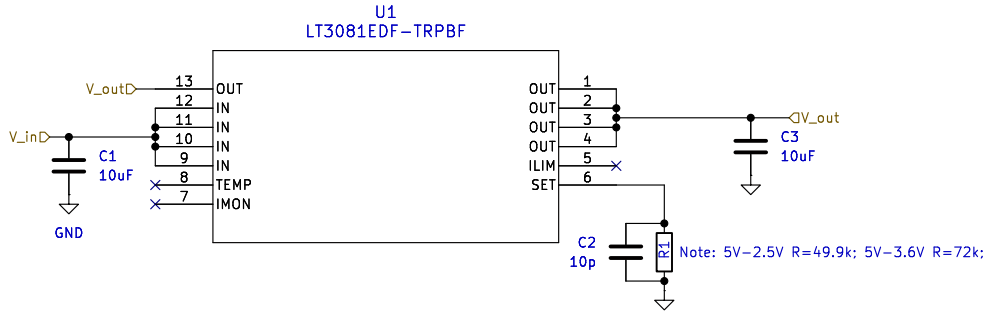
KiCad E.D.A. 9.0.3		Id: 6/6



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Author: Dr. Alexandru Enciu	
Institution: Technische Universität Darmstadt	
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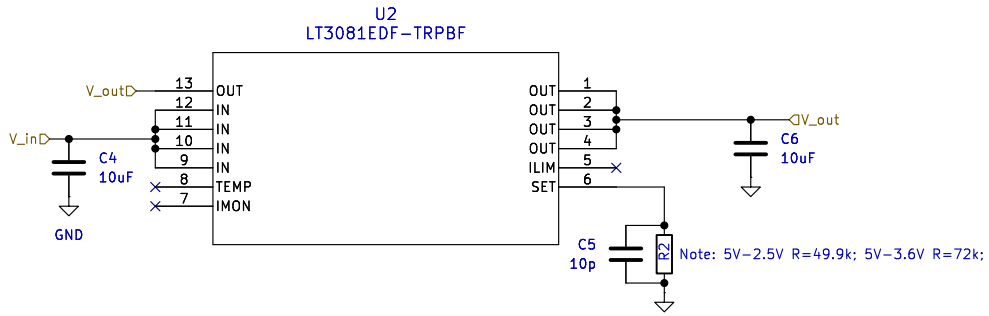
Size: A4 / Date:	**Rev:**
KiCad E.D.A. 9.0.3	Id: 2/6



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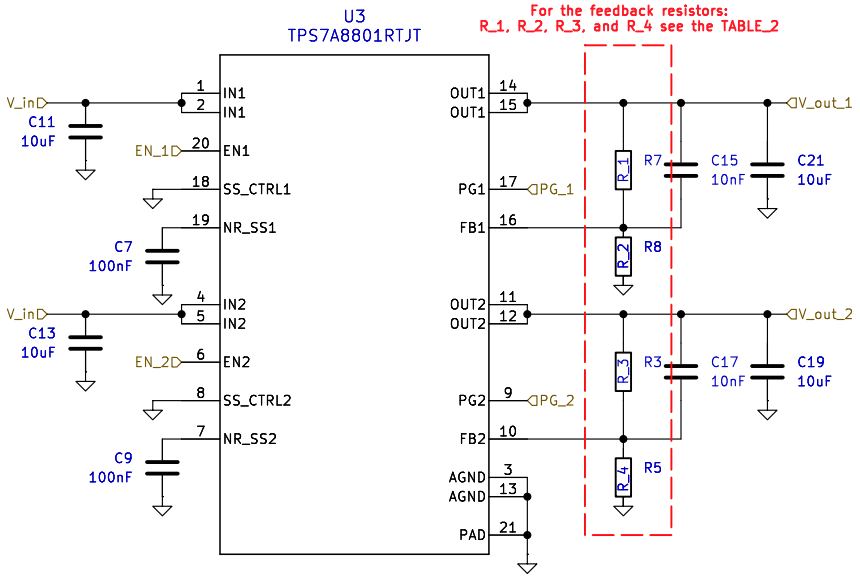

Table 2. Recommended Feedback-Resistor Values

$V_{OUTx(TARGET)}$ (V)	FEEDBACK RESISTOR VALUES(1)	
	R_1, R_3 (kΩ)	R_2, R_4 (kΩ)
0.8	Short	Open
1.00	2.55	10.2
1.20	5.9	11.8
1.50	9.31	10.7
1.80	1.87	1.5
1.90	15.8	11.5
2.50	2.43	1.15
3.00	3.16	1.15
3.30	3.57	1.15
5.00	10.5	2

(1) R_1, R_3 are connected from OUTx to FBx; R_2, R_4 are connected from FBx to GND; see Figure 42.

Project: HYDRA TPC & Fiber Tracker
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Institution: Technische Universität Darmstadt
Sheet: /2.5V to 1V and 1.8V/
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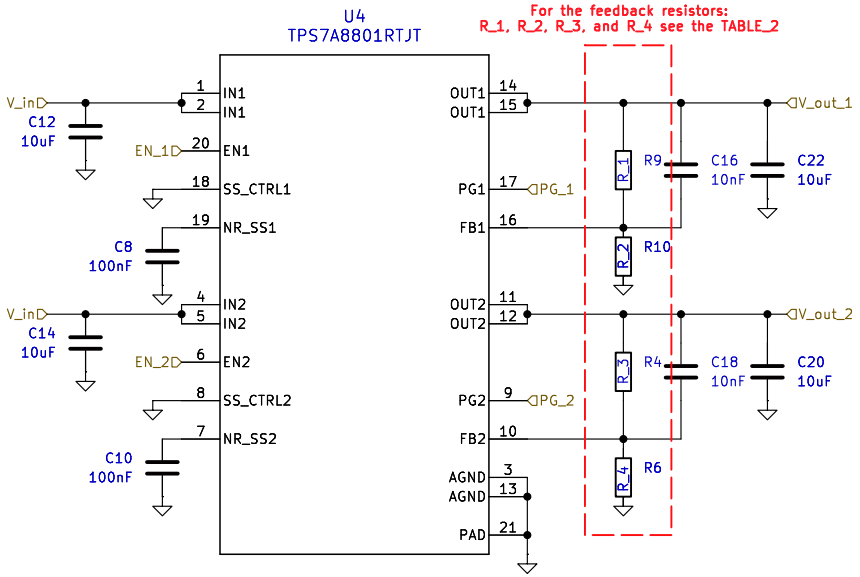

Table 2. Recommended Feedback-Resistor Values

$V_{OUTx(TARGET)}$ (V)	FEEDBACK RESISTOR VALUES(1)	
	R_1, R_3 (kΩ)	R_2, R_4 (kΩ)
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1.80	1.87	1.5
1.90	15.8	11.5
2.50	2.43	1.15
3.00	3.16	1.15
3.30	3.57	1.15
5.00	10.5	2

(1) R_1, R_3 are connected from OUTx to FBx; R_2, R_4 are connected from FBx to GND; see Figure 42.

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Author: Dr. Alexandru Enciu
Institution: Technische Universität Darmstadt

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