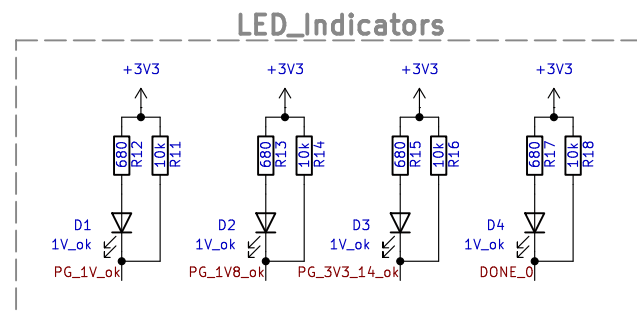
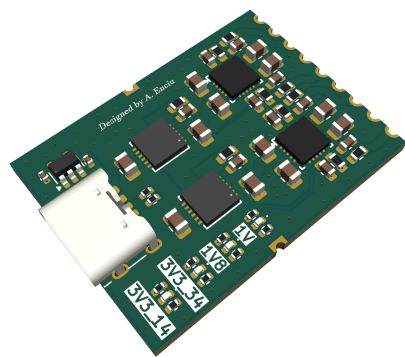
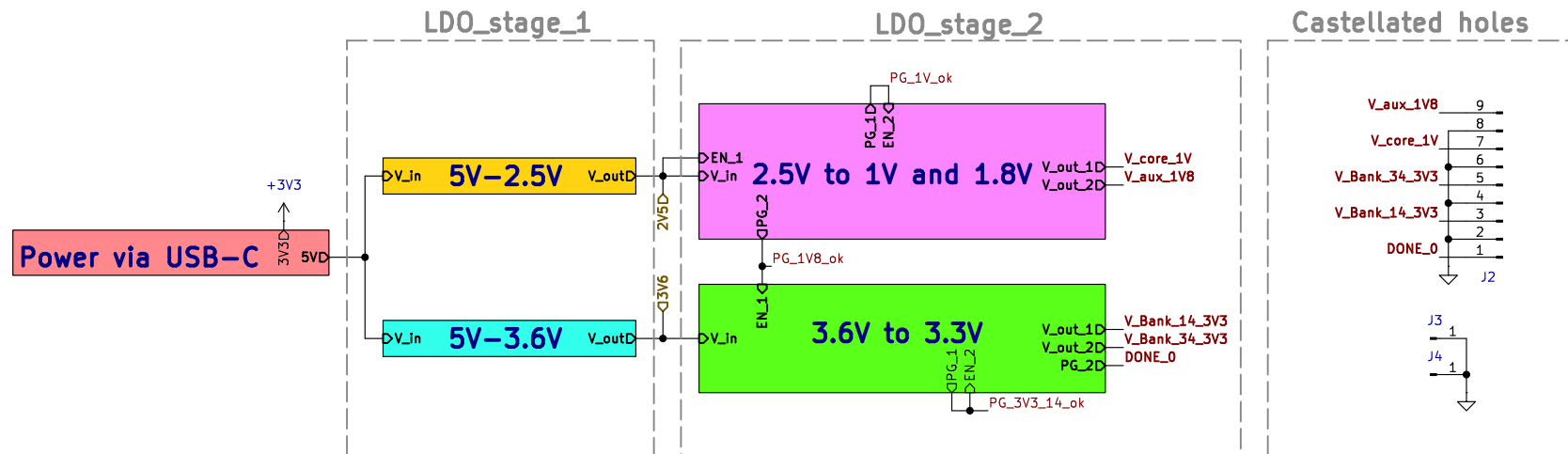


Note: FPGA Power sequence: V_core_1V → V_aux_1V8 → V_bank_3V3
Power regulation via LDOs cascade



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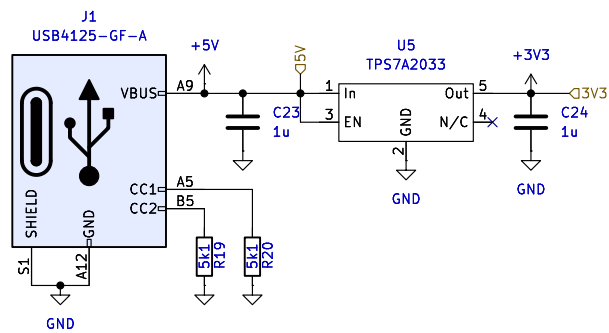
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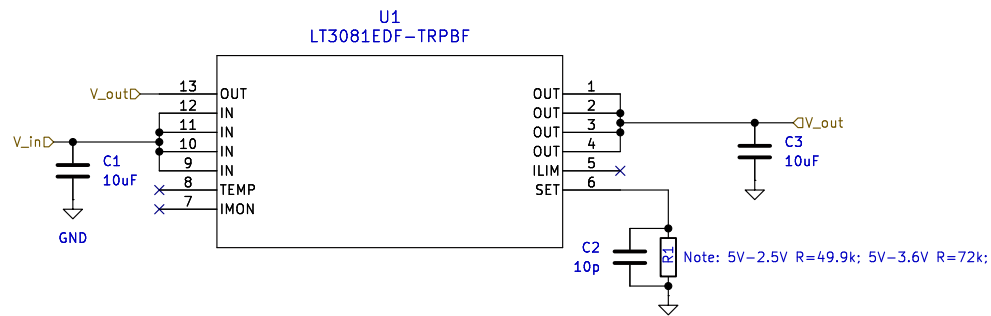
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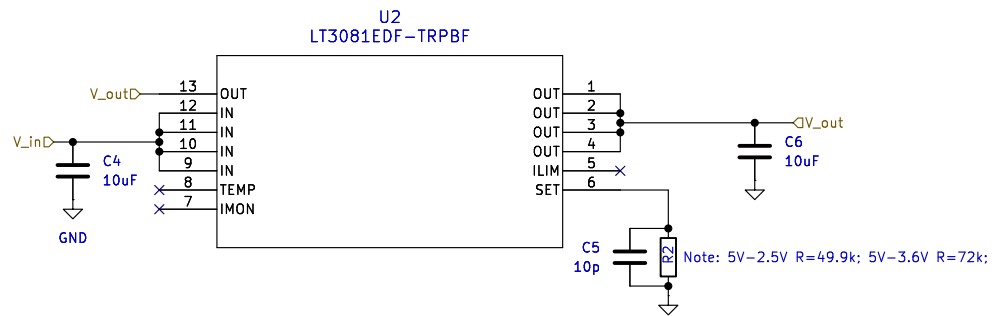
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 Author: Dr. Alexandru Enciu
Institution: Technische Universität Darmstadt
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 File: LT3081EDF.kicad_sch



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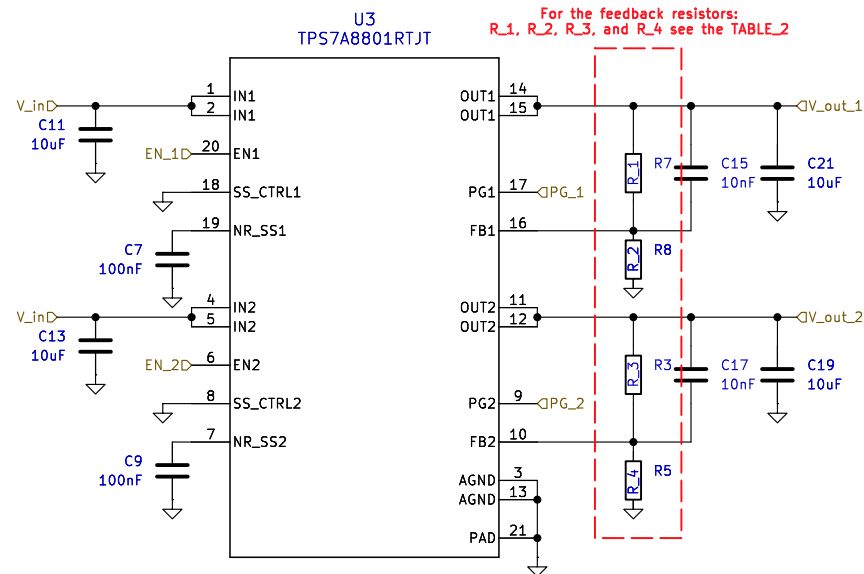


Table 2. Recommended Feedback-Resistor Values

V _{OUTx(TARGET)} (V)	FEEDBACK RESISTOR VALUES ⁽¹⁾	
	R ₁ , R ₃ (kΩ)	R ₂ , R ₄ (kΩ)
0.8	Short	Open
1.00	2.55	10.2
1.20	5.9	11.8
1.50	9.31	10.7
1.80	1.87	1.5
1.90	15.8	11.5
2.50	2.43	1.15
3.00	3.16	1.15
3.30	3.57	1.15
5.00	10.5	2

(1) R₁, R₃ are connected from OUTx to FBx; R₂, R₄ are connected from FBx to GND; see Figure 42.

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