1. 4,8, and 16 bit AND Gates
2. Name of Verilog Module: and.v
3. Inputs
4. in1 – has bit size of 4, 8, or 16
5. in2 – has bit size of 4, 8, or 16
6. Outputs
7. out - has bit size of 4, 8, or 16
8. Interfaces
9. No interfaces were used in this component.
10. Any Controls
11. No controls were used in this component.
12. Description
13. This component is an AND gate which takes two numbers of bit size 4, 8, or 16 and does bitwise AND for both. This means a 1 will be outputted only if both bits in the input are 1 for that bit position.
14. 4,8, and 16 bit XOR Gates
15. Name of Verilog Module: xor.v
16. Inputs
17. in1 – has bit size of 4, 8, or 16
18. in2 – has bit size of 4, 8, or 16
19. Outputs
20. out - has bit size of 4, 8, or 16
21. Interfaces
22. No interfaces were used in this component.
23. Any Controls
24. No controls were used in this component.
25. Description
26. This component is a XOR gate which takes two numbers of bit size 4, 8, or 16 and does bitwise XOR for both. It will only output a 1 in that bit position if one bit is 1 and the other is 0.
27. 16 bit Left Arbiter
28. Name of Verilog Module: leftarbiter.v
29. Inputs
30. A – has bit size of 16
31. Outputs
32. out - has bit size of 4, 8, or 16
33. Interfaces
34. Use 16 bit wire interface ‘cas’.
35. Any Controls
36. No controls were used in this component.
37. Description
38. This component is a left arbiter with a 16 bit input and returns a one hot binary number which is the most significant bit in the input that has a 1.
39. Documentation
40. Dally, WIlliam J., Harting, Curtis, R. *Digital Design, A Systems Approach,* Cambridge, Cambridge University Press, 2012