

## Lesson 14 Practice Problems

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1. The following problems deal with translating from C code to MIPS code. Assume that variables  $x$ ,  $y$  and  $z$  are given and implemented as 32-bit integers in a C program ( $y$  is an even number). Also assume the values of  $x$ ,  $y$  and  $z$  are stored in register  $\$s1$ ,  $\$s2$  and  $\$s3$ , respectively, and the value of result  $f$  is stored in register  $\$s0$ .
  - a.  $f = x*4 + y - z$
  - b.  $f = z + 24 - x + y/2$ 
    - For each C statement above, what is the corresponding MIPS code?
    - How many bits are needed to encode the above instructions for each C statement?
    - How many bits are needed in the register file to store the data for each C statement?
- a. `addi $s0, $s1, -100`
- b. `sll $s0, $s0, 4`
  - How can the two MIPS instructions above be represented using C code?
  - Why are constants in I-type instructions represented in 2's complement format?
  - What is the largest value (in decimal) that can be represented in the immediate field of an I-type instruction?
2. In the following problem, the data table contains bits that represent the opcode of an instruction. You will be asked to translate the entries into assembly code and determine what format of MIPS instruction the bits represent.
  - a. 0010 0001 0001 0111 0000 0000 0001 0000
  - b. 0000 0001 0000 1001 1000 0000 0010 0000
    - For the binary entries above, what MIPS instructions do they represent?
    - What type (I-type, R-type) instruction do the binary entries represent?

3. In the following problems, the data table contains MIPS instructions.
  - a. `sub $s0, $t1, $t2`
  - b. `lw $s0, 8($t0)`
    - For the instructions above, show the hexadecimal representations of the instructions.
    - Indicate the type of each instruction
    - Show the hexadecimal value of each field of each instruction
4. What is the purpose of the sign extend block in the MIPS datapath? Describe how it is used for one MIPS instruction which requires it.
5. Note the pipelined MIPS datapath shown on slide 9 of lecture 17. Redraw the figure to include hardware to support a *j* instruction (hint: examine slide 19 of lecture 12). For the following instructions, indicate which hardware blocks are used for each instructions (e.g. sign extend, shift, ALU, etc). Please include ALL hardware (including control) which is used for the instructions *add*, *lw*, *bne*, and *j* in a list.
6. For this exercise we will examine the affect of pipelining on datapath latency and throughput. Consider the following latencies of the datapath on slide 3 of lecture 16.
  - (a)  $IF=200\text{ps}$ ,  $ID=250\text{ps}$ ,  $EX=400\text{ps}$ ,  $MEM=450\text{ps}$ ,  $WB=150\text{ps}$
  - (b)  $IF=300\text{ps}$ ,  $ID=150\text{ps}$ ,  $EX=450\text{ps}$ ,  $MEM=650\text{ps}$ ,  $WB=200\text{ps}$ 
    - What is the minimum clock cycle time for pipelined and unpipelined versions of these datapaths (one answer for each circuit)?
    - What is the latency of an *sub* instruction in pipelined and unpipelined versions of the datapath? What is the throughput of a series of these instructions if they are executed consecutively.
    - What is the latency of an *sw* instruction in pipelined and unpipelined versions of the datapath? What is the throughput of a series of these instructions if they are executed consecutively.
7. On the datapath shown on slide 3 of lecture 16, add circuitry to allow for data forwarding from the data memory. Please redraw the figure, including the necessary new hardware and wires needed for the forwarding. Only include hardware for memory data forwarding.
8. Consider the instruction `lw $s1, -8($t1)`. Use the datapath shown on slide 3 of lecture 16 for your answer:

- What is this instruction in Hex format?
  - What is the output of the sign extend unit for this instruction as it exits the ID stage
  - What is the input value of "Read Addr 1" in the ID stage? How big is the input?
  - Assuming the instruction is located at address 0x3250, what is the value of the PC after the IF stage?
  - If the longest stage of the pipeline requires 300ps, what is the latency of the instruction? What is the throughput of the pipeline?
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