Half-hour Examination #5 - 30 minutes
Closed Book, one 8.5x11" page of notes (double-sided)

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NAME _____   Pilot ID: w_____   **SCORE** _____ / 20

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SHORT   Each question is worth +2 pts. for a correct answer, 0 pts. for a wrong answer.
ANSWER   Provide justification if you feel it is necessary.

_____

Problem #1 [10]

(a) [2 pts.] The initial contents of a 16-bit shift register is $xBEEF_{16}$. The register is shifted three bits to the left, with the serial input (Left shift in) being the sequence: 010_2. What are the contents (in HEX) of the register after the shift?

(b) [2 pts.] What RTL expression would be used to represent the concept of a data value stored in register R0 being copied to register R1 WITHOUT changing the value of R0 itself?

(c) [2 pts.]   (Fill in the blanks)   A(n) 16 x 8 ROM can be used to implement the functionality of any combinational device consisting of no more than   inputs and   outputs.
                                    _____   _____

(d) [2 pts.] How much data is available in a ROM device with a 16-bit address and an 8-bit output-word? Please provide this capacity in BYTES!

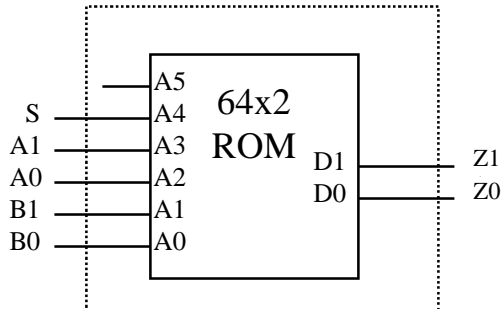(e) [2 pts.] How many 2k x 4 ROM chips would be necessary in order to construct a 16k x 16 ROM?

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Problem #2 [2]
A ROM is used to implement the functionality of a two-to-one, two-line MUX, as shown below. Describe the contents of the ROM for the addresses listed below. When S = 0, Z =A; when S = 1, Z = B.

ADDR	D1	D0
x00		
x01		
x0D		
x19		

Diagram:

```
              A5
         S ───A4   64x2
        A1 ───A3   ROM  D1 ──── Z1
        A0 ───A2        D0 ──── Z0
        B1 ───A1
        B0 ───A0
```
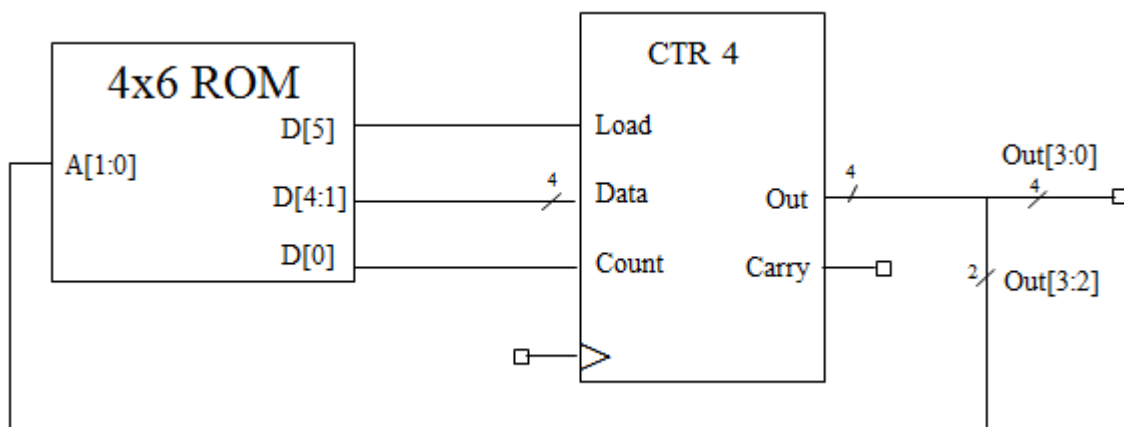
Problem #3 [3]
What is the count sequence for the counter shown below? Assume initial state of x0. Show your work!
For this counter: LOAD: when 1, load from D (if count = 0) or decrement (if count = 1); DATA: value to load into counter; COUNT: when 1, counter increments (decrements if load = 1); OUT: current value of counter; CARRY: 1 if at maximum count (minimum count if decrementing).

4x4 ROM Contents

ADDR	DATA
0	x36
1	x03
2	x2C
3	x29

Diagram:

```
  4x6 ROM                        CTR 4
            D[5] ──────────── Load
  A[1:0]                                        Out[3:0]
            D[4:1] ─────── 4 ─ Data    Out ── 4 ──┐── Out[3:0]
            D[0] ──────────── Count   Carry ─□    │
                         ▷                       2┤ Out[3:2]
```

ANSWER: Values of Out[3:0] in hex, one box per clock tick (the final value in this sequence should be a value that has previously appeared; this implies a repeat back to the previous occurrence)

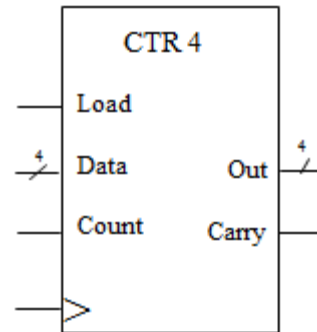| COUNT SEQUENCE:	x0																

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Problem #4 [2]
Answer the following question(s) to the best of your ability in the time available.

Use any combinational functionality that you wish to cause the 4-bit binary counter shown below (details in problem #3) to count the sequence below:

x0	x1	x9	xA	x0 (Repeat)

Problem #5 [3]
Provide a logic diagram for a datapath with a 1-bit control input S, an 32-bit input IN, an 32-bit output OUT, and two registers R0 and R1 that is capable of the following RTL functionality:

S: R0 ← IN, OUT ← IN
S': R1 ← R0, OUT ← R1

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DO NOT BEGIN UNTIL INSTRUCTED TO DO SO

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HONOR CODE: Before the end of the examination, please sign:

In recognition of and in the spirit of the Wright State University policies of academic honesty, I certify that I have neither given nor received unpermitted aid in this examination.

Name (Printed): _____

Signature: _____
_____

_____

DO NOT BEGIN UNTIL INSTRUCTED TO DO SO

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