Lab 5: Sequential Circuit Analysis

PURPOSE

The purpose of this lab is to analyze simple sequential logic circuits implemented with D-type positive edge triggered flip-flops.

LAB 5 - Sequential Circuit Analysis

- Perform the following with each of the provided clocked sequential circuits. need clk, in, q, out for functional timing diagram
  (a) Draw (by hand) a functional timing diagram showing clock signals, state variables, and primary inputs/outputs of the devices eight cycles of CLK. Assume that the circuit starts with all state variables reset to 0. Choose an 'interesting' set of input values, as appropriate.
  (b) What does this circuit do? Construct logic equations, a state table, and a state diagram for this circuit. Consider how the frequencies of the signals at the state variables and primary outputs are related to the frequency of the clock. Comment on how having the clock act as an input to the logic devices in this circuit simplifies/complicates analysis.
  (c) Implement, print, and include in your labbook a simulation schematic for this circuit. Also include simulation results demonstrating the functionality of the device. Simulation results may be logged by hand or by using the simulator's logging function. In Logisim, logging is available in the simulate menu: (a) "add" your selected inputs/outputs to the log before simulation in order to capture the results, (b) view/print the results from the table tab after simulation.
  (d) Provide timing information for the device. If you are unable to provide this information for each figure explain why not. Is critical information missing? Does the timing characteristic not exist due to the details of the device? Include calculated values (show your work) or commentary on the following five standard timing characteristics:
    - Setup time, input to clock:
    - Hold time, input to clock:
    - Propagation delay, clock to output (min):
    - Propagation delay, clock to output (max):
    - Maximum clock rate of device:

- [2 points] Perform the above analysis for Figure 1.
- [2 points] Perform the above analysis for Figure 2.
- [2 points] Perform the above analysis for Figure 3.

LAB 5 - DEMONSTRATION

[2 points] Demonstrate your simulated circuits to your lab instructor. Be prepared to answer questions regarding these circuits and their timing. Be prepared for the TA to analyze a new circuit that the TA might put up in the laboratory as part of the demonstration.

Integrated Writing [2 points]: Refer to "Digital System Design: Engineering Journals & Lab Policies" for details. 0.5 points each for Completeness, Clarity, Organization, and Testing.

Timing Specification Information

Flip flop	DFF	Propagation Delay, Clock to Output (max): Propagation Delay, Clock to Output (min): Setup Time, Data input before Clock: Hold Time, Date input after Clock:	9 ns 7 ns 10 ns 4 ns
Inverter	BUF-1 INV-1	Propagation Delay, Input to Output (max): Propagation Delay, Input to Output (min):	2 ns 1 ns
2 input and/or	AND-2 OR-2	Propagation Delay, Input to Output (max): Propagation Delay, Input to Output (min):	3 ns 1 ns
3 input and/or	AND-3 OR-3	Propagation Delay, Input to Output (max): Propagation Delay, Input to Output (min):	6 ns 4 ns

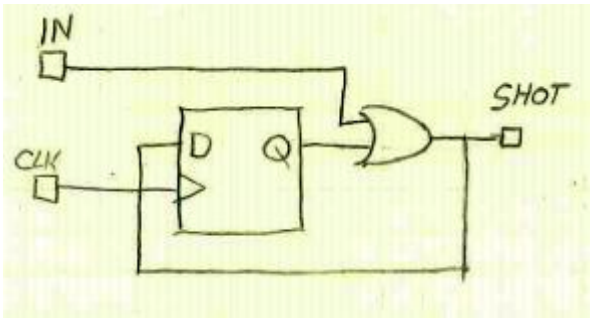

Figure1

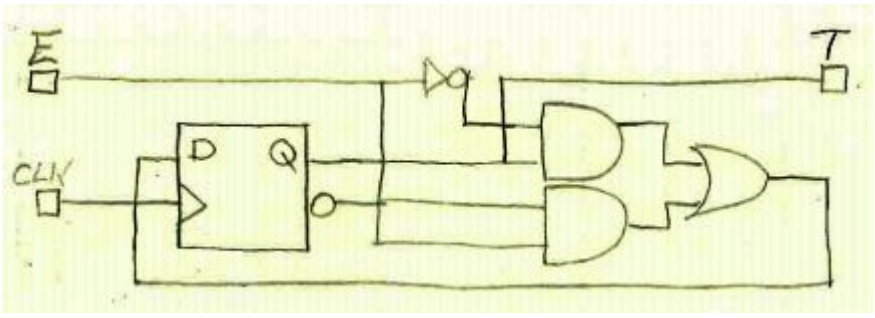

Figure 2

Note, put descriptions of what each device does

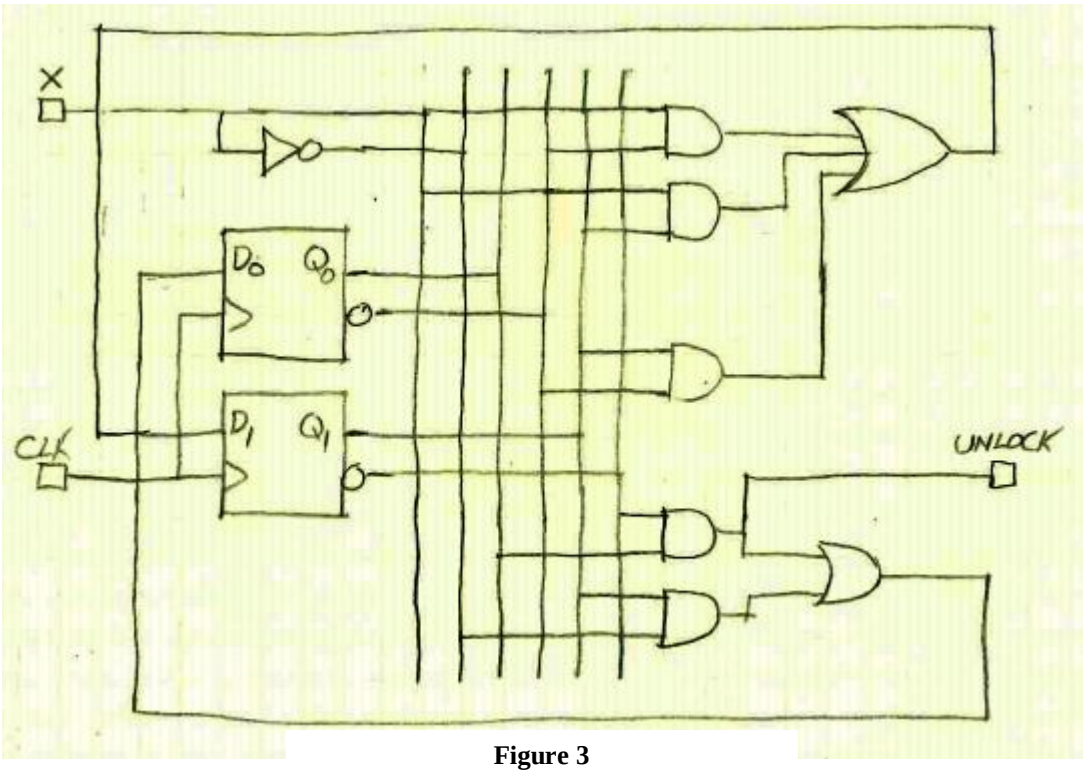

Figure 3