35 pts.

EE 3310/3510 • Exam V • 16 November 2022 NAME SOLUTION

Design a small-signal voltage amplifier using a single 2N3904 bipolar junction transistor that achieves the following specifications into an output load of 10 kΩ in parallel with 1 nF:

- $R_{in} > 2$ kΩ
- $R_{out} < 5$ kΩ
- $A_V = 30$ dB, stabilized with negative feedback
- $V_{out} > 8$ $V_{p\text{-}p}$
- Bandwidth: at least 20 kHz

First, choose an approximate V_{CC}, R_C, and operating point that will achieve the required signal swing, gain, and R_{out}. Explain your choices and design rationale in detail.

10 pts.

+2 R_C consistent with $R_{out} < 5k\Omega$
[i.e., $R_C < 5k$]

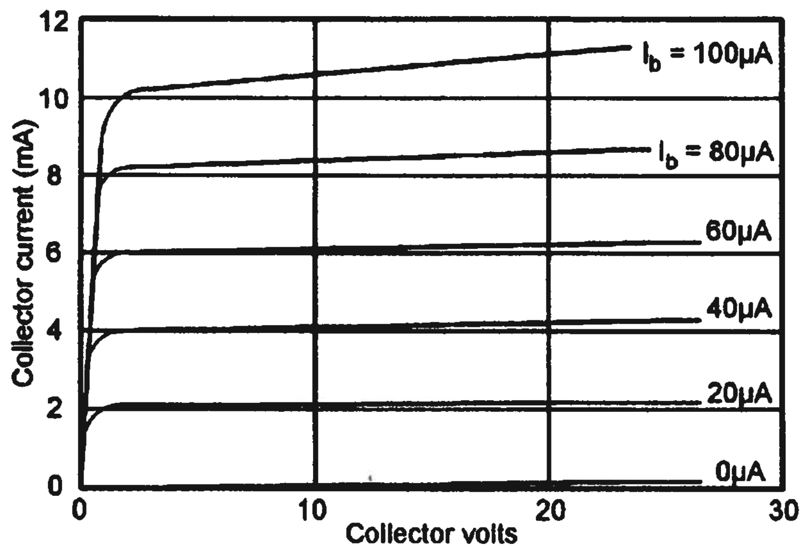
+2 V_{CC} consistent with $V_{out} > 8V_{P\text{-}P}$
→ should be approx. $12V < V_{CC} < 24V$ etc..

+2 quiescent $V_C \approx \frac{1}{2} V_{CC}$; corresponding I_C

+2 if adequately explained/justified

+2 BW addressed

Perform DC and AC load line analysis to determine the optimum quiescent operating point, and design the DC bias network. Draw your load lines on the following characteristic curves.



10 pts.

+2 for D.C. load line

+2 for A.C. load line

+2 V_B consistent w/ choice of Vcc and DC. emitter feedback

+2 Voltage divider bias resistor values

+2 verify R_{in} > 2k Ω

[requires computation of g_m ; r_b]
[OK on next page]

Perform small-signal analysis to determine the mid-frequency gain and input capacitance due to Miller Effect. Verify that the 20 kHz HF spec has been achieved at the input if R_S = 200 Ω.

8 pts.

+4 for A_v computation, including g_m and $R_C \| R_L$

+2 for C_{IN} using Miller's Theorem

+2 for BW

Implement negative feedback in the form of a partially-unbypassed emitter resistor. Show all computations for your beta network and resistor values. You do not have to design the low-frequency portion of this amplifier. Draw your final circuit.

7 pts.

+3 β computation from A_{vo} & final A_v
[including voltage gain from 30dB spec]

+2 R_{E_1} computation and R_{E_2} recomputation

+2 circuit sketch