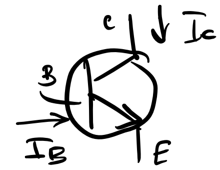
Introduction to Field-Effect Transistors

- like the BJT, the FET is a three-terminal device, but operates under a different principle!
- BJTs are <u>bipolar devices</u> because current flow depends on both holes <u>and</u> electrons, while FETs are <u>unipolar</u> devices whose current flow depends on <u>either</u> holes <u>or</u> electrons
- however, the <u>real</u> distinguishing factor that differentiates them:

BJT: <u>current-controlled current device</u>

$$\underbrace{I_C}_{\text{collector current}} = \beta \underbrace{I_B}_{\text{base current}}$$



FET: <u>voltage-controlled current device</u>

- <u>drain</u> current depends on electric field created by <u>gate-to-source</u> voltage

-- two principal types:

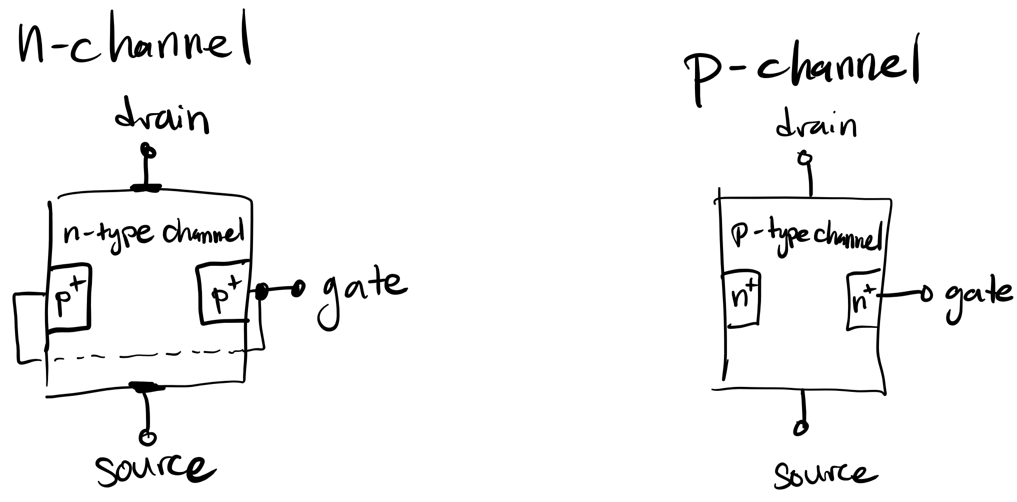
JFET (Junction Field Effect Transistor)

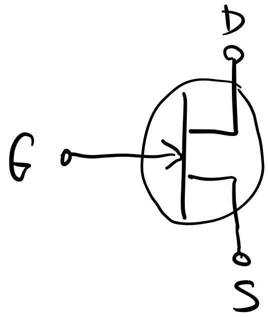
MOSFET (Metal Oxide Semiconductor Field Effect Transistor)

-- MOSFET has superceded the JFET and BJT in many integrated circuit applications; but we'll talk about JFETs first

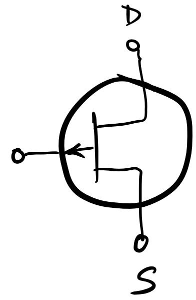
JFET

-- like NPN and PNP transistors, there are two flavors:

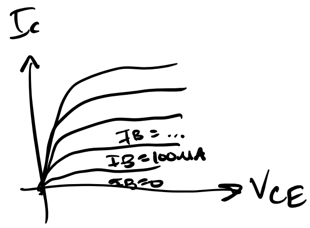




n-channel

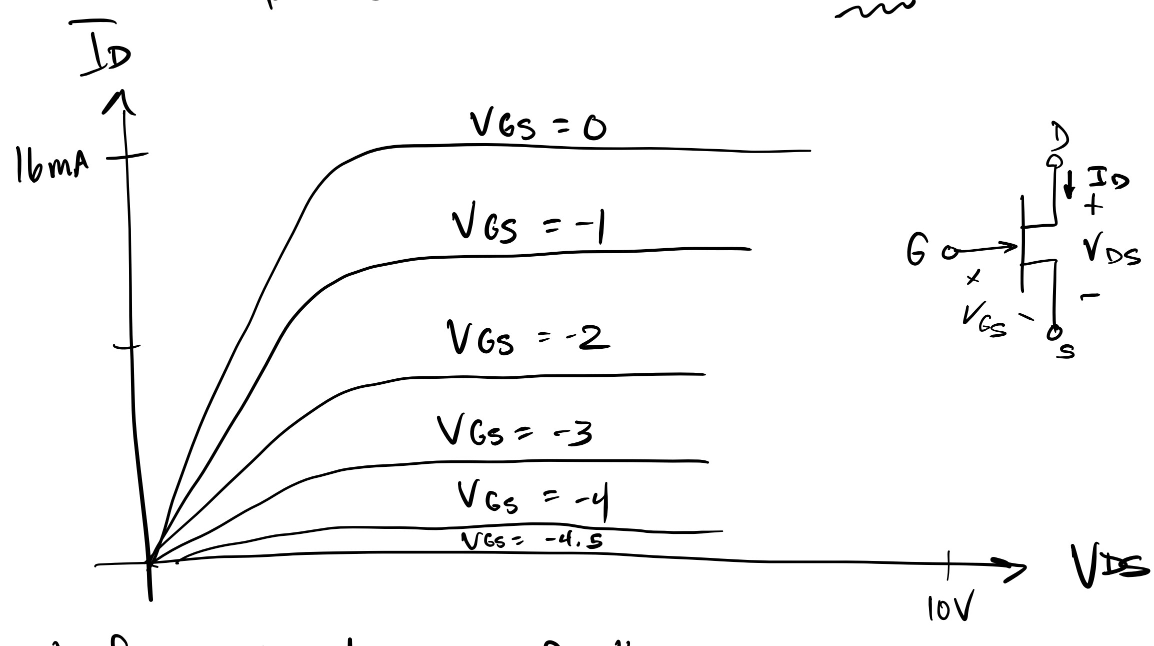


p-channel



drain : analogous to collector
gate : analogous to base
source : analogous to emitter

- consider n-channel JFET curves for V_{DS} vs. I_D for different values of V_{GS}.



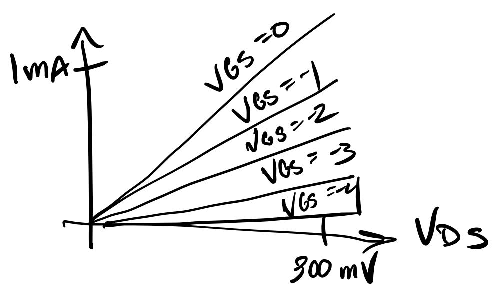
- at first, they look superficially similar to BJT V_{CE} vs. I_C curves, but there are crucial differences!

-- for starters: each curve is a different V_{GS}, not I_B!

-- notice all values of V_{GS} are negative, topping out at $V_{GS}=0$

-- thus, the gate-to-source p-n junction is always reverse-biased and there is no gate current!!! (Nice!)

-- at low levels of V_{DS}, note that the slope of V_{DS} vs. I_D increases with increasing V_{GS}:



-- since the slope $\frac{\Delta I_D}{\Delta V_{DS}}$ is equivalent to conductance or $\frac{1}{R}$, its reciprocal, R, decreases with increasing V_{GS}

-- this is called the ohmic region and it may be used as a voltage-controlled resistance.

-- audio compressors!

-- at higher magnitudes of V_{DS}, the curves flatten and we enter the active region, in which I_D is nearly constant for a given V_{GS}.

- at $V_{GS} = 0$, the JFET is operating at its maximum drain current called I_{DSS}

"drain-source saturation current"

$$I_{DSS} = I_D \Big|_{V_{GS}=0}$$

- I_{DSS} is a parameter associated with a particular device

- as V_{GS} is made more negative, I_D decreases until the channel is totally depleted and $I_D = 0$

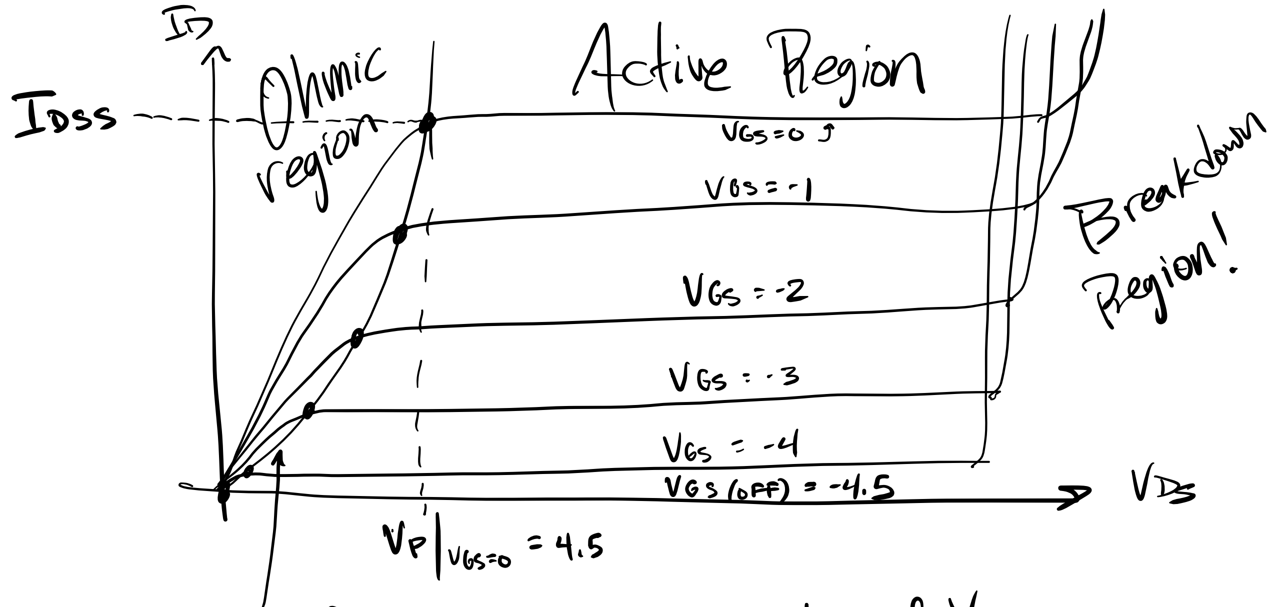
- this happens at the gate-to-source cutoff voltage, $V_{GS(OFF)}$.

$$V_{GS(OFF)} = V_{GS} \Big|_{I_D=0}$$

- it turns out that the value of V_{DS} at which the FET enters the active region is called the pinch-off voltage V_P; and at $V_{GS}=0$,

$$V_P = |V_{GS(OFF)}|$$

- at lower values of V_{GS}, V_P is lower and the family of V_P values forms a parabolic locus



∴ the equation defining this parabola is called

Shockley's Equation:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(OFF)}}\right)^2$$

∴ with I_{DSS} and $V_{GS(OFF)}$ being constants, the Shockley equation tell us that there is a squared relationship between V_{GS} and I_D.

important later!

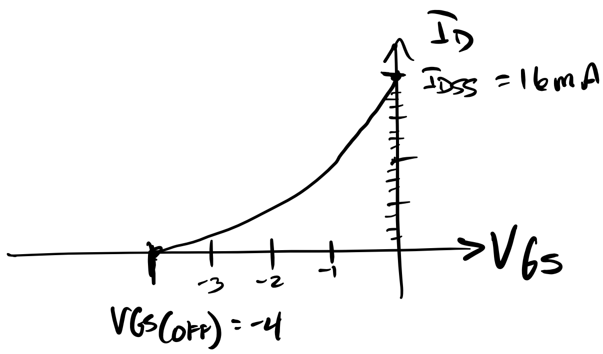
ex: a JFET has a known $I_{DSS} = 16\,mA$ and $V_{GS(OFF)} = -4V$.
∴ determine I_D in the active region @ $V_{GS} = -2V$.

$$I_D\big|_{V_{GS}=-2} = 16\left(1 - \frac{-2}{-4}\right)^2 = 4\,mA$$

- note that this is a little more complicated than the BJT with its $V_{BE} \sim 0.7V$!

- another way of plotting Shockley's Equation:

transfer characteristics :



quite useful !

- for p-channel, V_{GS} is positive and V_{DS} is negative

ex: $I_{DSS} = 12mA$, $V_{GS(OFF)} = +3.6V$, at $V_{GS} = 1.8V$:

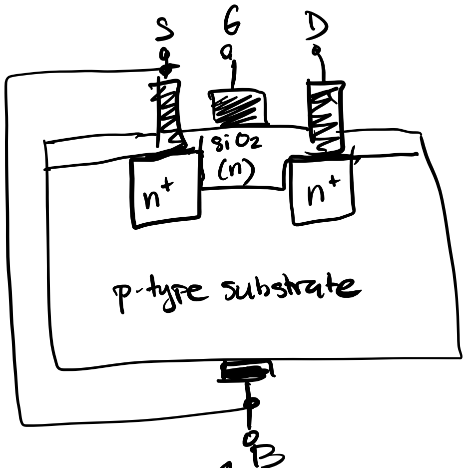
$$I_D = 12\left(1 - \frac{+1.8}{+3.6}\right)^2 = 3mA$$

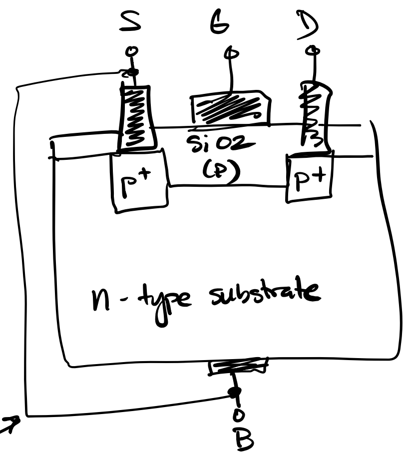
- note: important in circuit design to never let $V_{GS} > 0$ (for n-channel; $V_{GS} < 0$ for p-channel)
  - doing so forward-biases V_{GS}, gate current flows, and damage is likely!

MOSFET

- like JFETs, they come in n-channel and p-channel varieties

- principal distinction: gate is <u>insulated</u> from channel by thin layer of SiO_2, <u>eliminating gate current</u> under all conditions





substrate or "bulk"
usually internally connected to source

- two types of MOSFETS:

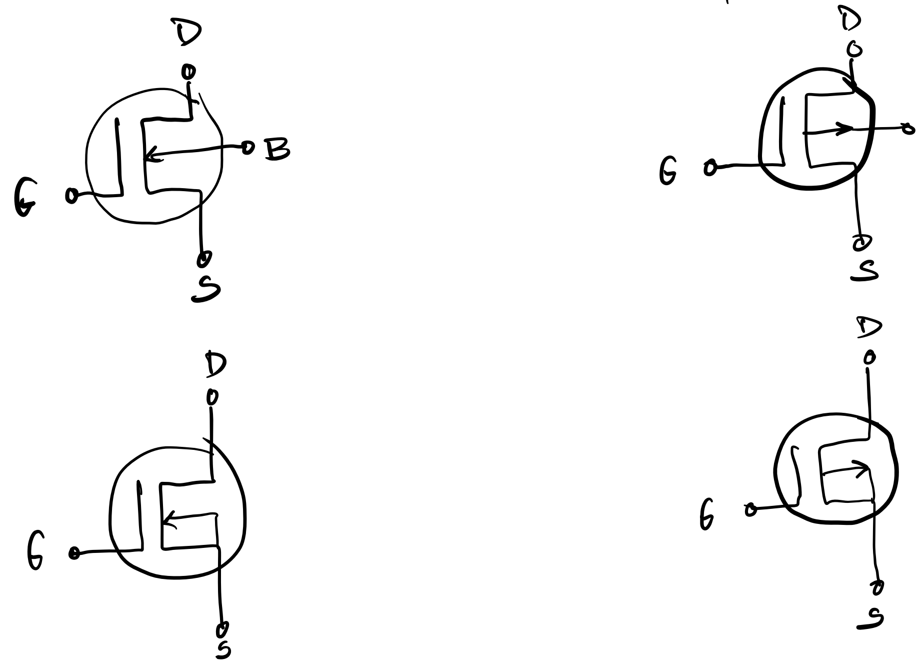
<u>depletion-type</u> or <u>D-MOS</u> and <u>enhancement-type</u> or E-MOS

- we'll talk about D-MOS first.

D-MOS

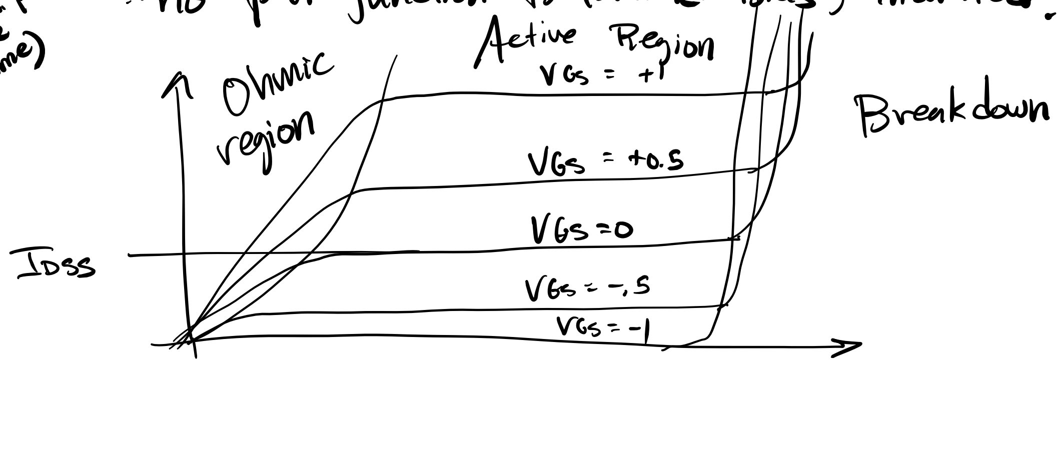
n-channel

p-channel



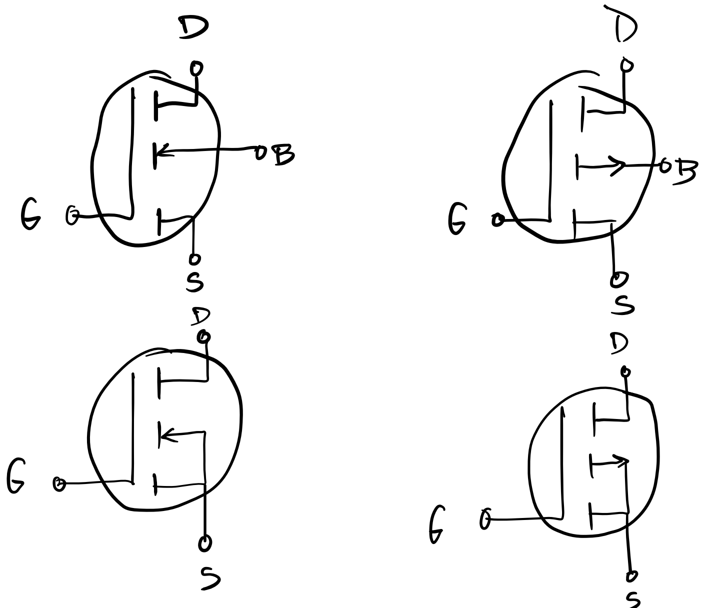
- depletion MOSFETs operate similarly to JFETs; similar curves, Shockley Equation, I_{DSS} and $V_{GS(OFF)}$
- however, unlike JFET, we may operate D-MOS transistors with $V_{GS} > 0$ (n-channel; $V_{GS} < 0$ for p-channel)
  - no p-n junction to forward-bias; insulated!

IGFET
"insulated-gate" FET
(original name)



E-MOS

- rather than having a fixed current I_{DSS} @ $V_{GS} = 0$ and a cutoff voltage $V_{GS(OFF)}$ at which $I_D = 0$, E-MOS transistors have <u>no</u> current @ $V_{GS} = 0$ and drain current will not flow until a <u>positive</u> value of V_{GS} is reached called the <u>threshold voltage</u>, V_t.



n-channel p-channel

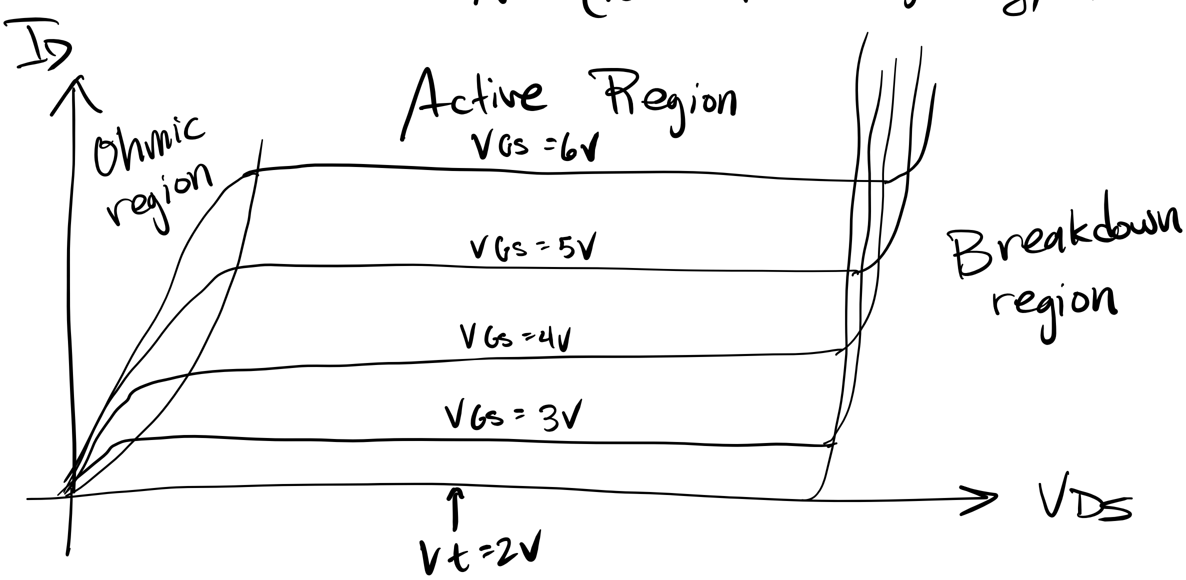
- as V_{GS} is increased past V_t, I_D increases.
- at low levels of V_{DS}: <u>ohmic region</u>, just like JFET and D-MOS
- once V_{DS} is increased to the <u>saturation voltage</u> $V_{D(sat)}$, where $V_{D(sat)} = V_{GS} - V_t$, we enter the active region; same principle as pinch-off voltage in JFET and D-MOS.

∴ these saturation voltages at different values of V_{GS} form a parabolic locus whose equation is:

$$I_D = K(V_{GS} - V_t)^2$$

← similar to Shockley equation!

K : conductivity parameter of particular device in A/V^2 (related to device geometry/aspect ratio)



ex: n-channel enhancement MOSFET in active region with $K = 1\ mA/V^2$, $V_t = 2V$

∴ what is drain current @ $V_{GS} = 3.5V$?

$$I_D = 1(3.5 - 2)^2 = 2.25\ mA$$

∴ for p-channel E-MOS, V_{GS} and V_t are negative quantities; thus, $I_D = K(|V_{GS}| - |V_t|)^2$