Lab 4: Combinational Iterative Design

PURPOSE

The purpose of this laboratory project is to introduce students to the synthesis of a digital device of moderate complexity consisting exclusively of combinational functionality. In this lab, we will practice using MSI combinational components to deal with complexity. In this lab, students will implement larger devices using a general iterative approach under a variety of constraints.

n-BIT MAXIMUM VALUE SELECTOR

Consider a simple device that takes two n-bit unsigned magnitude binary inputs A and B representing two numeric values ranging from zero to 2^n-1. The n inputs for A are represented by input variables A(n-1) through A0. Values for B and C are represented similarly. The n-bit output C of the device will be the *greater* of the two binary values presented on the n-bit inputs A and B.

LAB 4 – DESIGN AND IMPLEMENT

Implement these designs in order. Detail your work in your laboratory notebook.

Design #0 (0 points)

- Consider a 2-bit maximum value selector. There will be four inputs (A1A0B1B0) and two outputs (C1C0). Create a truth table, simplified SOP equations, and an implementation for your solution. [NOTE: If you received full credit for Lab #3 then you may simply refer to your previous work done in that laboratory.]

Design #1 (1 point)

- Realize a new solution for a 2-bit maximum value selector that uses two 1-bit 16-to-1 multiplexers (one to implement C1 and one to implement C0). You may use *no* other discrete logic devices. Simulate your design, test it, and be prepared to demonstrate your simulation/answer questions/implement your design for your TA.

Design #2 (1 point)

- Again consider a 2-bit maximum value selector. Realize a solution to this design that uses only 1-bit 2-to-1 multiplexers. You may use as many of these multiplexers as you wish, but you may use NO other logic device. Simulate your design, test it, and be prepared to simulate it/answer questions/implement it about it for your TA.

Design #3 (1 point)

- Realize a new implementation for your 2-bit maximum value selector that uses only NAND gates. You may use as many NAND gates as you wish, but may use NO other discrete logic devices. Simulate your design, test it, and be prepared to simulate it/answer questions/implement it about it for your TA.

Design #4 (2 points)

- Design a 1-bit maximum value selector designed to be used to solve larger problems using an iterative design approach. This may require your one-bit design to have ADDITIONAL inputs and/or outputs that are used by the 1-bit devices to communicate information about the progress of the overall task to EACH OTHER. What information might one stage of the device need to communicate to other stages of the device? In which direction does information need to follow (MSB->LSB or LSB ->MSB)? Simulate your design, test it, and be prepared to simulate it/answer questions/implement it about it for your TA.

- WARNING: This may be the most difficult part of the laboratory. Do a few examples by hand. What do you need to keep track of? You may want to represent the things that you need to keep track of by additional inputs/outputs to your device! Don't forget to detail your successes, failures, and thoughts in your lab notebook!

Design #5 (1 point)

- Construct a 4-bit maximum value selector (two 4-bit inputs A[3:0] and B[3:0], and one 4-bit output C[3-0]) using YOUR 1-bit bit maximum value selector designed for iterative implementation. Simulate your design, test it, and be prepared to simulate it/answer questions/implement it about it for your TA.

Additional mandatory discussion (0 points)

- In your labbook, discuss what approach you would choose to implement a 32-bit maximum value selector. You do NOT need to implement the device. Comment on why you might choose to use one the above implementation techniques over another. What trade-offs would you consider? [This writing will be considered for IW: Completeness points, below.]

LAB 4 - DEMONSTRATION

[2 points] Demonstrate your simulations to your TA in your e-labbook. Be prepared to address any questions that the TA might have.

Integrated Writing [2 points]: Refer to "Digital System Design: Engineering Journals & Lab Policies" for details. 0.5 points each for Completeness, Clarity, Organization, and Testing.