Lab 7: More Sequential Circuit Analysis and Design

PURPOSE

The purpose of this lab is to design and simulate a simple sequential logic circuit using flip-flops.

Sequence detector

Consider a device with a single input IN and a single output UNLOCK. This device is a sequence detector. The output UNLOCK is to be asserted if and only if a secret 'code' is entered. The code is always considered to be over the last few inputs (depending on the length of the code). Thus, code overlap IS allowed. Correct codes are considered to be entered MSB to LSB. Thus, the first bit entered for the code 11000 would be '1'.

There are two versions of this device. The Moore version of this device considers only inputs that have been successfully read at a clock tick to be part of the code sequence. The Mealy version of this device considers the last (LSB) bit of the code to the CURRENT input – even before the clock event occurs.

Timing assumptions

- For the purposes of this laboratory, assume that all combinational logic gates have a minimum propagation delay (in nanoseconds) equal to the number of inputs to the device. Assume that the maximum propagation delay for all combinational logic gates is twice its minimum propagation delay. Thus, a 3-input AND gate would have a minimum propagation delay of 3ns and a maximum propagation delay of 6 ns.
- For the purposes of this laboratory, all flip-flops should be assumed to have a minimum propagation delay of 6ns, a maximum propagation delay of 10ns, a setup time of 5ns, and a hold time of 1ns.

LAB 7 - Sequential Circuit Analysis

- [2 points] Figure 1 is a logic diagram of a sequence detector. What is the code sequence (or sequences!) that causes UNLOCK to be asserted?!? Is the device Mealy or Moore? What are the relevant timing characteristics necessary to use the overall device? Document your answers with equations, diagrams, tables, and other evidence to demonstrate and support your claims.

LAB 7 - Sequential Circuit Design

Make a sequence detector that detects two sequences. UNLOCK should be asserted for whenever the last four inputs are 1101 and also asserted if the last four inputs are 1010.

- [1 point] Design the Moore version of the device. For this lab, you must use the 'full' synthesis approach (No ad hoc designs – yet!). Include a state diagram, state table, Boolean equations, and fully labeled logic diagram. Your design must use a minimal number of states. Provide evidence that supports this!
- [1 point] Implement the Moore design using the lab simulator. Include an analysis of all relevant timing characteristics for using your implementation under the timing assumptions listed earlier for this laboratory.
- [1 points] Design the Mealy version of the device. For this lab, you must use the 'full' synthesis approach (No ad hoc designs – yet!). Include a state diagram, state table, Boolean equations, and fully labeled logic diagram. Your design must use a minimal number of states. Provide evidence that supports this!
- [1 points] Implement the Mealy design using the lab simulator. Include an analysis of all relevant timing characteristics for using your implementation under the timing assumptions listed earlier for this laboratory.
- [0 points] What are the relative advantages/disadvantages of the Mealy/Moore versions of the device? Which requires more hardware? More memory? More complex timing? Which version is more 'secure' / difficult to code break? Which was easier to design? Include any other observations

that you have regarding the differences between your Moore and Mealy designs and implementations. [This writing will be considered for IW: Completeness points, below.]

LAB 7 - DEMONSTRATION

[2 points] Demonstrate the correct operation of your clocked synchronous state machine design. Completely verify the operation of the circuit or simulation to your laboratory instructor. Be prepared to answer questions regarding your documentation and the design process.

Integrated Writing [2 points]: Refer to "Digital System Design: Engineering Journals & Lab Policies" for details. 0.5 points each for Completeness, Clarity, Organization, and Testing.

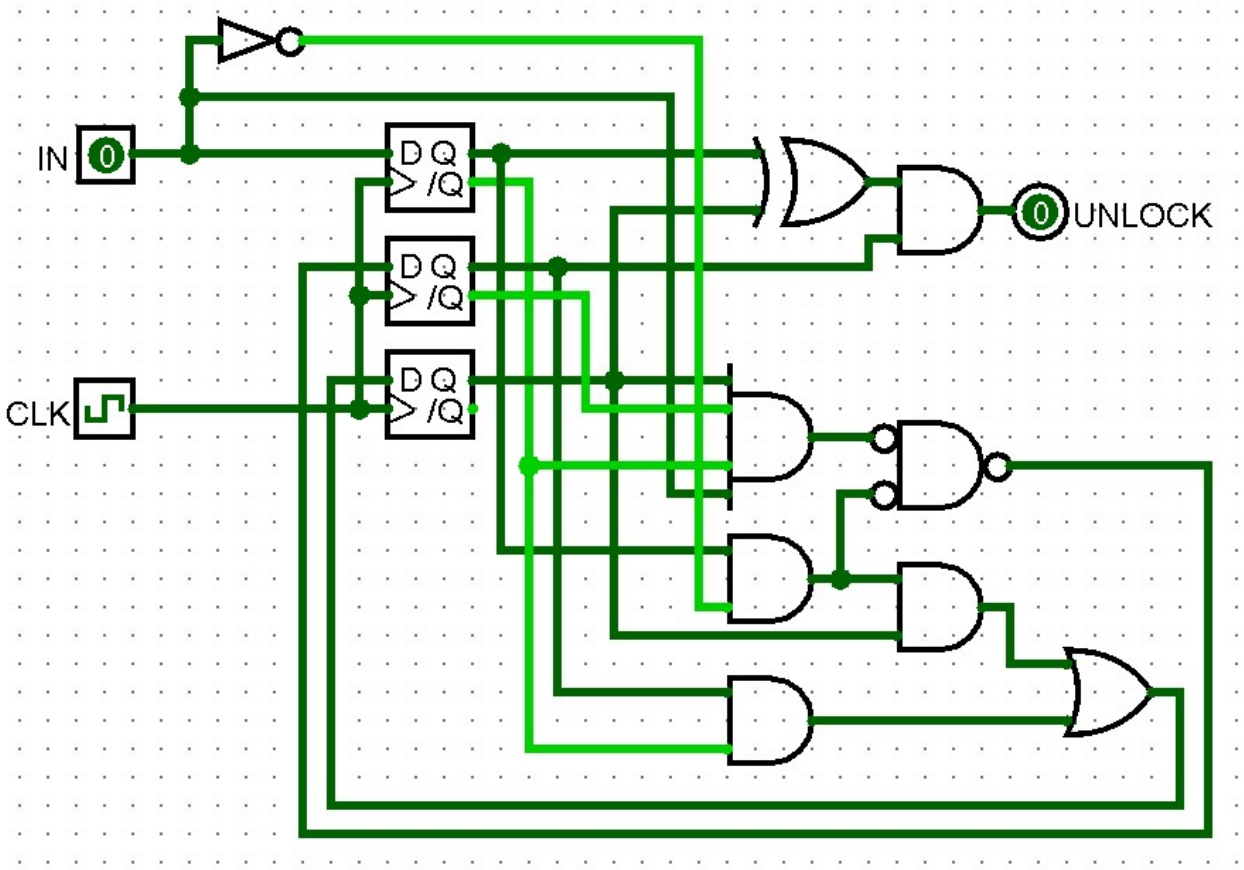

Figure 1: A Sequence Detector