Lab 9: CMOS Differential Amplifier

EE 3310L

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1. Introduction

The purpose of this lab is to construct and test a CMOS differential amplifier in three configurations and to fosters an ability to function effectively on a team whose members together provide leadership, create a collaborative and inclusive environment, establish goals, plan tasks, and meet objectives [1]. Teamwork is especially important in this lab as it contains two labs worth of content in one lab.

2. Experimental Methodology [1]

The first step of the experiment is constructing the circuit following figure 1 below and ensuring that the drain voltages are resting at approximately 3V with respect to ground.
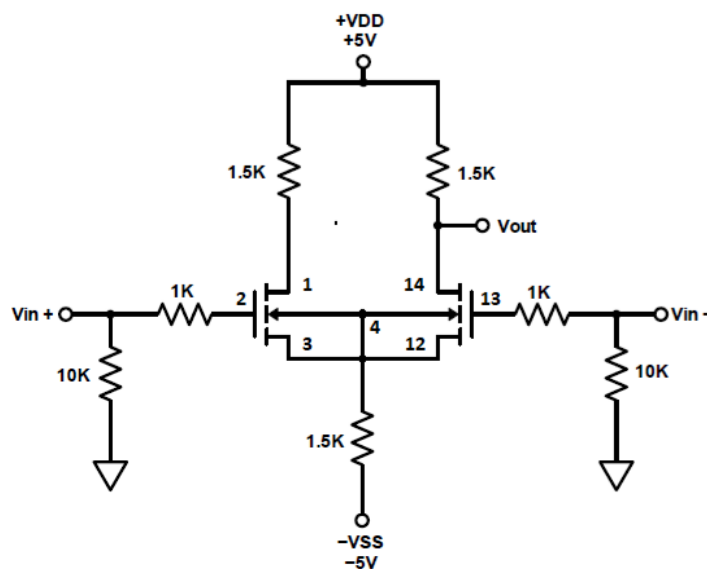

Figure 1: resistive drain loads and sink

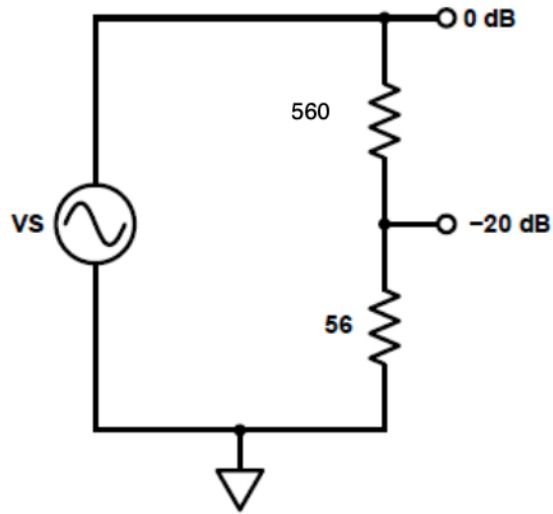The next step is to build the circuit seen below in figure 2.

Figure 2: 20-dB pad

The signal generator is then set to a 100mV$_{p-p}$ and 1kHZ sine wave and connect the 20-dB pad to Vin+ on the circuit in figure 1 above. The peak-to-peak output voltage and peak-to-peak voltage at Vin+ are then measured for the circuit in figure 1. From those values, the positive-input gain is calculated. The steps are then repeated with the 20-dB pad connected to Vin- and peak to peak voltage measured at Vin- instead of Vin+. From those values, the negative-input gain is calculated. With both positive and negative input gain values, the differential-mode gain and differential imbalance are calculated. The signal generator is then directly connected to both Vin+ and Vin- and the peak-to-peak output voltage and peak-to-peak voltage at Vin+=Vin- are then measured. From these values, common-mode gain is calculated.

Circuit 1 is then used to build the circuit seen below in figure 3 again ensuring that the drain voltages are resting at approximately 3V with respect to ground.
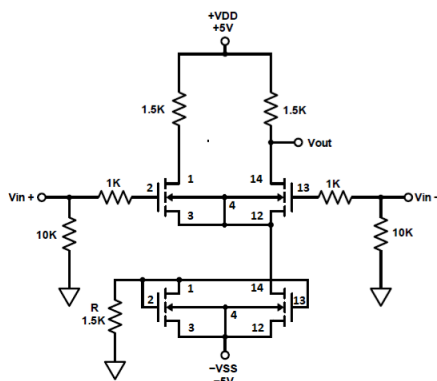

Figure 3: resistive drain loads with electronic current-mirror sink

The same procedure done to the circuit in figure 1 with the circuit in figure 2 is repeated on figure 3.

Circuit 3 is then used to build the circuit seen below in figure 4 again ensuring that the drain voltages are resting at approximately 3V with respect to ground.
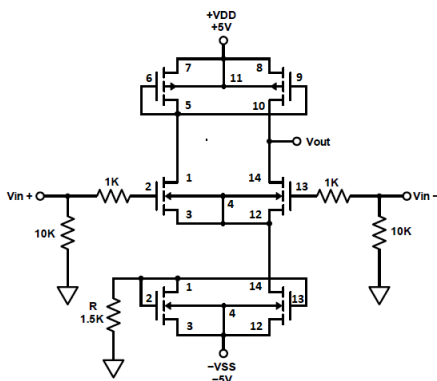

Figure 4: resistive drain loads with electronic current-mirror sink

The same procedure done to the circuit in figure 1 with the circuit in figure 2 is repeated on figure 4.

3. Results and Description

3.1 Resistive Drain Loads and Sink

The measured values of Vin+ and Vout are 120mV and 210mV for the 20-dB pad connected to Vin+ configuration. The positive-input gain can be seen equation 1 below.

$$A_{VIN+} = \frac{V_{OUT}}{V_{IN+}} = \frac{210}{120} = 1.75 = 4.86dB \tag{1}$$

The measured values of Vin- and Vout are 100mV and -280mV for the 20-dB pad connected to Vin- configuration. The negative-input gain can be seen equation 2 below.

$$A_{VIN-} = \frac{V_{OUT}}{V_{IN-}} = \frac{-280}{100} = -2.8 = 8.94dB \ (inverting) \tag{2}$$

The differential-mode gain can be seen equation 3 below.

$$A_{DM} = A_{VIN+} - A_{VIN-} = 1.75 - -2.8 = 4.55 = 13.6dB \tag{3}$$

The differential-imbalance can be seen equation 4 below.

$$A_i = \left|\frac{A_{VIN+}}{A_{VIN-}}\right| = \left|\frac{1.75}{-2.8}\right| = 0.625 = 9.4dB \ (inverting) \tag{4}$$

The measured values of Vin+=Vin- and Vout are 940mV and 450mV for the 20-dB pad connected to Vin+ and Vin- configuration. The common-mode gain can be seen equation 5 below.

$$A_{CM} = \frac{V_{OUT}}{V_{IN+} - V_{IN-}} = \frac{450}{940} = 0.4787 = 6.4dB \ (inverting) \tag{5}$$

3.2 Resistive Drain Loads with Electronic Current-Mirror Sink

The measured values of Vin+ and Vout are 100mV and 228mV for the 20-dB pad connected to Vin+ configuration. The positive-input gain can be seen equation 6 below.

$$A_{VIN+} = \frac{V_{OUT}}{V_{IN+}} = \frac{228}{100} = 2.28 = 7.16dB \tag{6}$$

The measured values of Vin- and Vout are 100mV and -248mV for the 20-dB pad connected to Vin- configuration. The negative-input gain can be seen equation 7 below.

$$A_{VIN-} = \frac{V_{OUT}}{V_{IN-}} = \frac{-248}{100} = -2.48 = 7.89dB \ (inverting) \tag{7}$$

The differential-mode gain can be seen equation 8 below.

$$A_{DM} = A_{VIN+} - A_{VIN-} = 2.28 - -2.48 = 4.76 = 13.55dB \tag{8}$$

The differential-imbalance can be seen equation 9 below.

$$A_i = \left| \frac{A_{VIN+}}{A_{VIN-}} \right| = \left| \frac{2.28}{-2.48} \right| = 0.92 = 0.73dB \ (inverting) \tag{9}$$

The remainder of the lab was not completed due to time constraints.

4. Discussion

This lab fosters an ability to function effectively on a team whose members together provide leadership, create a collaborative and inclusive environment, establish goals, plan tasks, and meet objectives by containing so many steps while each individual step is relatively simple. More specifically, due to the lab being condensed from a multiweek time period to a single week, we decided to divide our roles to more effectively complete the tasks of getting the parts and checking the parts. For example, I would gather all the components while my lab partner gathered the various wires and cables required and while I measured all the resistor values to ensure we would not need to diagnose our circuit to find any bad resistors after the circuit was built, my lab partner started to build the circuit itself with the already measured resistors. Once the circuit itself was built, we reconvened to get the measurements and do the calculation needed for the circuit before repeating the process for the next circuit. Unfortunately, despite our efforts, we were unable to complete two weeks of lab in one week and were only able to fully complete one set of measurements and calculations while we were only able to complete most measurements and calculations for a second circuit.

5. Summary and Conclusions

The lab is not completed due to it originally being a multiweek lab. The instructions for the lab itself are simple and straightforward to complete due to the instructions given.

Reference

[1] Tritschler, Joe. "CMOS Differential Amplifier." N.p., n.d. Web. 17 Mar 2023