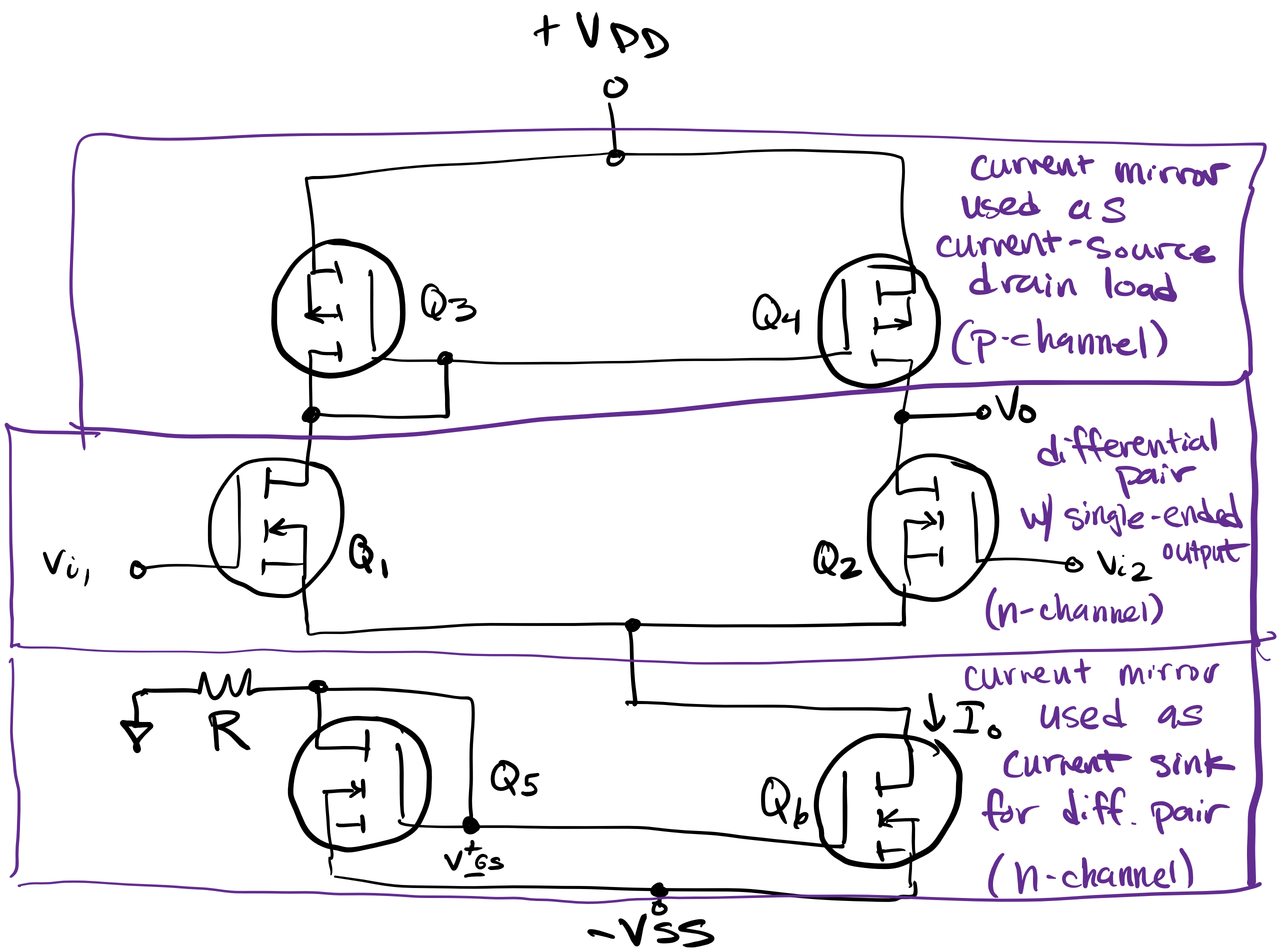
MOSFET Differential Pair with Active Load

- We have discussed the MOSFET differential pair and its performance in differential and common modes with different current sink dynamic resistances (r_{out})

- in this circuit and drain-loaded amplifiers in general, overall gain is dominated by the $g_m R_D$ term ($R_D \lll r_o$)

- R_D also plays a crucial role in the DC operating characteristics of the amplifiers
  - if we try to make R_D large to get more gain, it drops more DC voltage ($I_D R_D$), necessitating either increased V_{DD} (expensive!), or reduced I_D (reduces gain!)

- furthermore, often we really only need a differential input to accept balanced signals or a feedback loop; if we don't need the differential output, using a current-mirror as an active drain load greatly increases gain without increasing V_{DD} or I_D



∴ note: one resistor sets all DC operating conditions!

∴ we can now set the drain current to a much wider choice of values to get the desired performance, without worrying about a drain resistor dropping too much voltage!

∴ effective $r_D = r_o$; much larger than any practical drain resistor R_D!

$$I_{REF} = \frac{0 - (-V_{SS} + V_{GS})}{R}$$

$$R = \frac{|V_{SS}| - V_{GS}}{I_{REF}}$$

if $K = 10\ mA/V^2$, $V_t = 1.2V$, $V_{DD} = \pm 12V$

$$V_{GS} = \sqrt{\frac{I_D}{K}} + V_t$$

$$= \sqrt{\frac{2}{10}} + 1.2 = \underline{1.647V}$$

then $R = \frac{12 - 1.647}{2} = 5.177k$;

use $5.23k\Omega$ 1%

-- what about the diff pair itself?

-- With no drain resistors, how do we know what V_D is and if it provides "wiggle room?"

.. Q_3 is a p-channel MOSFET with its drain connected to its gate; thus, $\underline{V_{DS3} = V_{GS3}}$

.. furthermore, its source is connected to V_{DD}

$\therefore V_{DS3} = V_{D3} - V_{S3}$

$= V_{D3} - V_{DD} = V_{GS3}$

$\rightarrow V_{D3} = V_{DD} + V_{GS3}$

p-channel! each half of diff pair!

.. assuming $K = 10\ mA/V^2$, $V_t = -1.2V$, $I_D = 1mA$

$$V_{GS}\Big|_p = -\sqrt{\frac{I_D}{K}} + V_t$$

$$= -\sqrt{\frac{1}{10}} + -1.2$$

$$= -1.516V$$

then $V_{D3} = 12 + -1.516 = 10.48V$

$\therefore$ this must also equal V_{D2} ← output of diff pair

.. if Q_3 and Q_4 are perfectly matched (same chip!!!)

then $V_{D4} = V_{D3} = V_{D2} = V_{D1} = V_o = 10.48V$

.. note: we are sitting pretty close to V_{DD} and won't have much upward wiggle room; but that's ok, these are usually low-level stages.

Differential Gain of MOSFET Diff Pair w/ Active Load

- we have already established that the differential-mode gain to one output is

$$\frac{V_{o2}}{V_d} = \frac{+g_m R_D \| r_o}{2}$$

$= V_o$; we intentionally chose the non-inverting output!

- now R_D is replaced with $r_D = r_o$ from active current-source load
  - let's call this r_{op} to distinguish it from the r_{on} of the diff pair itself

then $$A_d = \frac{g_m \, r_{op} \| r_{on}}{2}$$

- and finally, if $r_{op} \approx r_{on} = r_o$, then $r_o \| r_o = \frac{r_o}{2}$

$$\boxed{A_d = \frac{g_m r_o}{4}}$$

-- if $g_m = 2\sqrt{K I_D}$

$= 2\sqrt{10 \cdot 1} = 6.325 \text{ mA/V}$

$r_o = \frac{|V_A|}{I_D} = \frac{100}{1} = 100 \text{ k}\Omega$

then $A_d = \frac{6.325 \cdot 100}{4} = 158.1$

or 44 dB

-- pretty good for MOSFETs @ low current!

-- its because we replaced an R_D of 1 or 2 kΩ with $r_o \| r_o$ of $\approx$ 50 kΩ!

-- an actual 100k drain resistor would have dropped 100V!

-- now the problem with increasing I_D to increase g_m is that it decreases r_o faster!

$g_m = 2\sqrt{K I_D}$ (½ power)

$r_o = \frac{|V_A|}{I_D}$ (linear!)

∴ CMRR is still approximated the same way; thus,

$$\text{CMRR} = 20\log_{10}(g_m r_{sink})$$

for current mirror, $r_{sink} = r_o = \frac{|V_A|}{I_D}$

$$= \frac{100}{2} = 50\,k\Omega$$

$$\text{CMRR} = 20\log_{10}(6.325 \cdot 50) = 50\text{ dB}$$

∴ use cascode current sink if you need higher performance

∴ this is entering the realm of CMOS:

Complimentary Metal Oxide Semiconductor technology,

fabrication process for pairs of n-type and p-type MOSFETs on same chip

∴ now 99% of integrated circuits are CMOS!

∴ related to idea of replacing resistors with more transistors and avoiding capacitors; → integrated circuits