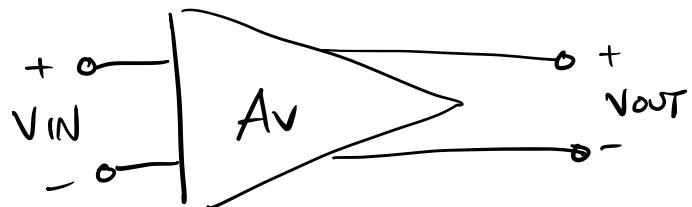


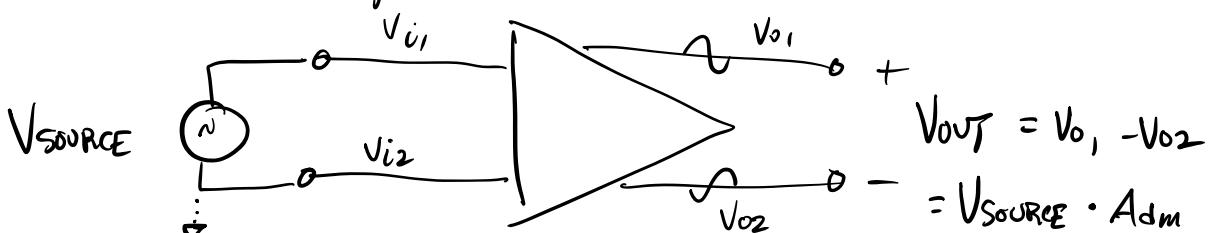
The Differential Amplifier

- this amplifier configuration is crucial to many systems, especially those employing balanced operation, and those utilizing negative feedback
- essential part of op-amp !

block diagram of differential amplifier :

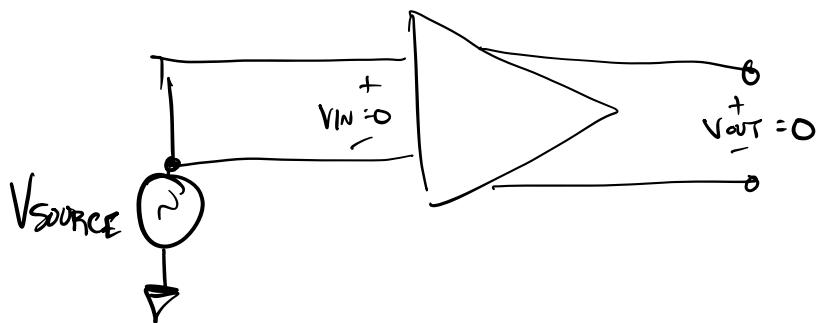


- by definition, a diff amp will amplify the difference between its input terminals by its differential-mode gain A_{dm} , and provide a differential output signal.

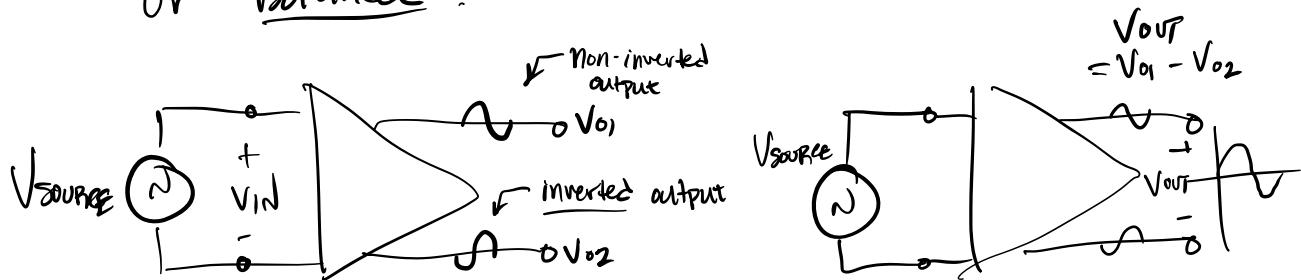


- note : V_S can be a single-ended source with one terminal grounded; or balanced. Either way, its a differential-mode signal.

- if the same signal is connected to both inputs, a perfect differential amplifier will have zero output, as the difference between its input terminals will be zero.
 - this is called a common-mode input signal

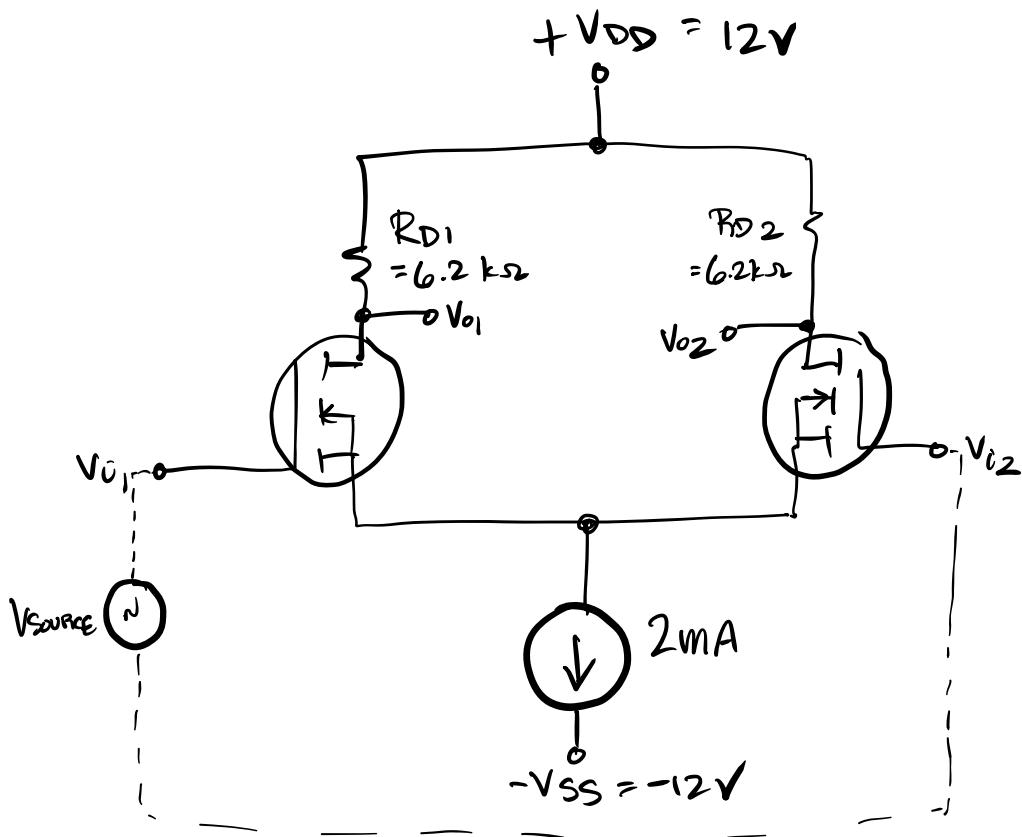


- a practical differential amplifier will not perfectly cancel common-mode input signals; more later!
- the output of a differential amplifier may also be taken single-ended from either V_o , or V_{o2} , or balanced.



The MOSFET Differential Pair

- the heart of most differential amplifiers is the transistor differential pair, which consists of two transistors and a constant-current sink.



Here's how the circuit works:

- assuming perfectly-matched transistors and an ideal constant-current sink of $2mA$, each transistor will have a quiescent current of $1mA$
- if the voltage at V_{i1} increases, I_D increases
→ this causes V_{o1} to decrease

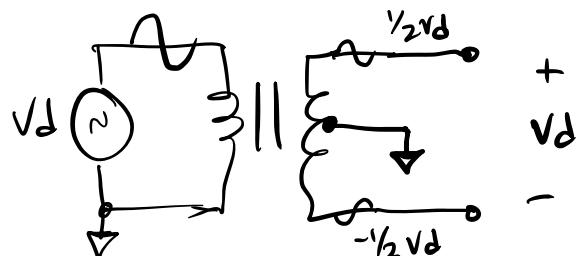
- by KCL, the sum of drain currents must always equal 2mA ; therefore, I_{D2} must decrease by the same magnitude as the increase in I_{D1} !

.. therefore, V_{O2} increases

.. think seesaw action!

- for small-signal differential-mode analysis, let's connect an ideal balanced signal V_d to the inputs such that $V_{i1} = \frac{1}{2} V_d = v_{g1}$, $V_{i2} = -\frac{1}{2} V_d = v_{g2}$

.. in the old days, we did this with a center-tapped transformer winding!



- the two MOSFET source terminals are connected together; thus, $V_{S1} = V_{S2} = V_S$

- if $V_d = V_{g_1} - V_{g_2}$ and $V_g = V_s + V_{gs}$,

$$V_d = V_s + V_{gs_1} - V_s + V_{gs_2}$$

$$V_d = V_{gs_1} - V_{gs_2} = V_{g_1} - V_{g_2} = \frac{1}{2}V_d - \frac{1}{2}V_d$$

$$\underline{V_{gs_1} = \frac{1}{2}V_d}$$

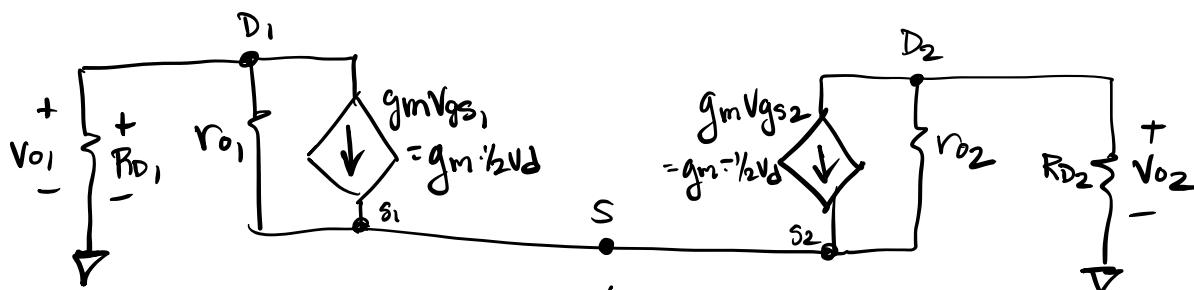
$$\underline{V_{gs_2} = -\frac{1}{2}V_d}$$

- shows that for ideal
balanced input,

$$\underline{V_s = 0}$$

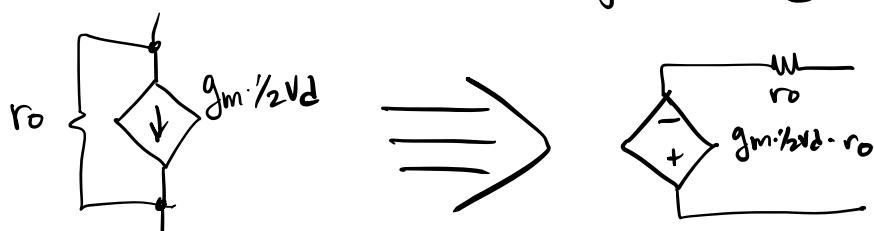
we already
have $V_{gs_1}; V_{gs_2}$

Mid-Frequency Small-Signal Model of Output Section of Diff Amp, Differential Mode



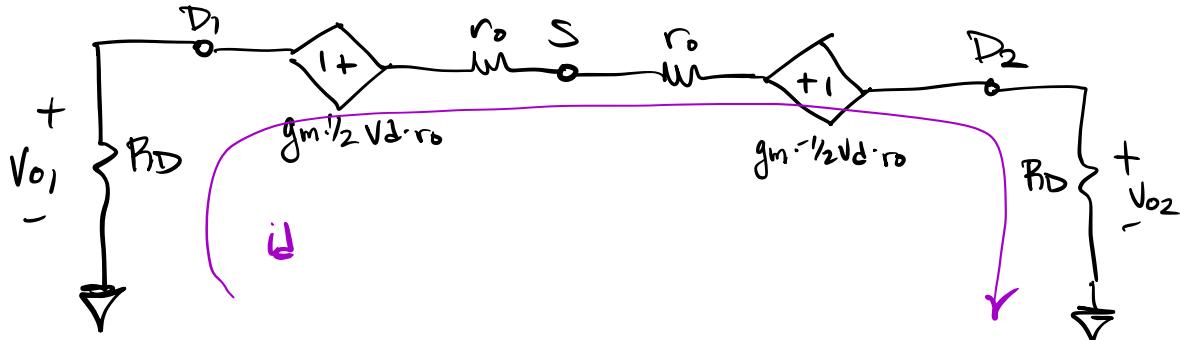
↳ open circuit due to
ideal current sink!

- let's transform the voltage-controlled current source
into a voltage-controlled voltage source



While we're at it : $r_{o1} = r_{o2} = r_o$

$$R_{D1} = R_{D2} = R_D$$



define loop current i_d ; we can show by KVL :

$$i_d R_D - g_m \cdot \frac{1}{2} V_d \cdot r_o + i_d r_o + i_d r_o + g_m \cdot \frac{1}{2} V_d \cdot r_o + i_d R_D = 0$$

$$i_d (2R_D + 2r_o) - g_m V_d r_o = 0$$

$$i_d = \frac{g_m V_d r_o}{2(R_D + r_o)}$$

then $-V_{o1} = i_d R_D = \frac{g_m V_d r_o}{2(R_D + r_o)} \cdot R_D$ $= r_o \parallel R_D$

$$V_{o1} = \frac{-g_m V_d}{2} (R_D \parallel r_o)$$

$$+V_{O2} = i_D R_D = \frac{g_m V_d r_o}{2(R_D + r_o)} \cdot R_D = r_o \parallel R_D$$

$$V_{O2} = \frac{g_m V_d}{2} (R_D \parallel r_o)$$

- We now have the single-ended output voltages with respect to the differential-mode input voltage V_d !

- finally, if $V_{out} = V_{O2} - V_{O1}$ (as drawn),

$$V_{out} = \frac{g_m V_d}{2} (R_D \parallel r_o) - \frac{g_m V_d}{2} (R_D \parallel r_o)$$

$$V_{out} = g_m V_d (R_D \parallel r_o)$$

- define differential-mode voltage gain as

$$A_{dm} = \frac{V_{out}}{V_d} = g_m (R_D \parallel r_o) \quad \leftarrow \text{just like CS !!!}$$

ex: if $K = 10 \text{ mA/V}^2$, $r_o = 50 \text{ k}\Omega$, $I_D = 1 \text{ mA}$ (each),

$$g_m = 2 \sqrt{K I_D} = 2 \sqrt{10 \cdot 1} = 6.325 \text{ mA/V}$$

$$A_{dm} = 6.325 (6.2 \text{ k} \parallel 50 \text{ k}) = 36.58 \text{ or } 31.3 \text{ dB}$$

- for common-mode Signals, we would ideally have zero net differential input signal resulting in zero V_{out}
- in reality, even if the transistors and drain resistors are perfectly matched, a practical current sink with non-infinite Norton impedance causes a non-zero common-mode gain A_{cm}

- Consider the same signal V_C applied to the two input terminals

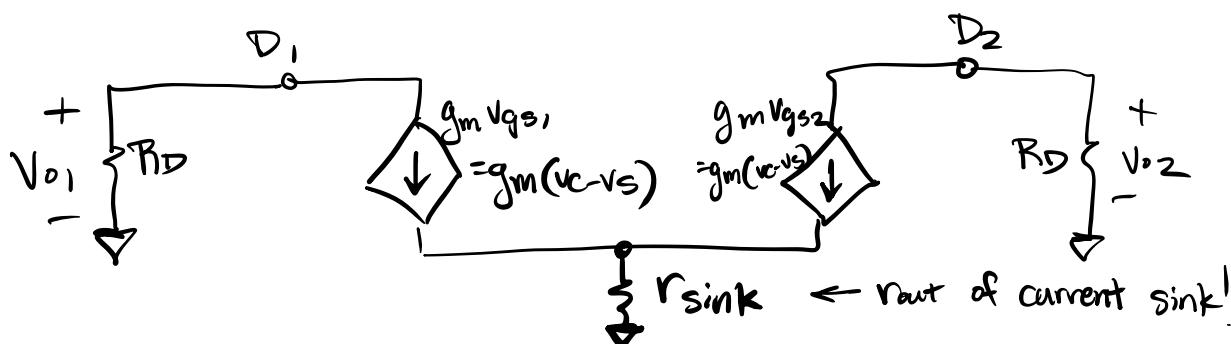
$$V_C = V_{g_1} = V_{g_2} \quad \text{↑ common-mode}$$

this is no longer zero!

$$\rightarrow V_{gs_1} = V_{gs_2} = \underbrace{V_C - V_S}_{}$$

Mid-Frequency SSM of Output Section, Common Mode

Note : assume $r_o \gg R_D$



- note similarity to common-source with unbypassed R_S !
- drain currents in common-mode will be equal, resulting in equal output voltages (not balanced!)

thus, $V_{o1} = V_{o2} = V_o$
- then each drain current will have magnitude

$$-\frac{V_o}{R_D} = g_m (V_C - V_S)$$
- both drain currents flow through r_{sink} , resulting in

$$V_S = 2 \cdot \frac{-V_o}{R_D} \cdot r_{sink}$$
- if $-V_o = R_D \cdot g_m (V_C - V_S)$

$$V_o = -R_D g_m \left(V_C - 2 \cdot \frac{-V_o}{R_D} \cdot r_{sink} \right)$$

$$V_o = -R_D \cdot g_m V_C - \cancel{R_D \cdot g_m} \cdot 2 \frac{V_o}{R_D} \cdot r_{sink}$$

$$V_o (1 + 2 g_m r_{sink}) = -R_D \cdot g_m V_C$$

$$V_o = \frac{-R_D \cdot g_m V_C}{1 + 2 g_m r_{sink}}$$
- assuming $1 + 2 g_m r_{sink} \approx 2 g_m r_{sink}$

$$V_o \approx \frac{-R_D \cdot g_m V_c}{2 g_m r_{sink}}$$

• define common-mode voltage gain

$$A_{cm} = \frac{|V_{out}|}{V_c} \quad \leftarrow \text{we don't care about the inversion!}$$

$$A_{cm} = \frac{R_D}{2 r_{sink}}$$

\leftarrow just like unbypassed source resistor gain equation, except "2" in denominator from two transistors!

• now define common-mode rejection ratio

$$CMRR = \frac{A_{dm}}{A_{cm}}$$

• since common-mode gain was defined with respect to one output, consider single-ended differential-mode gain:

$$CMRR = \frac{g_m (R_D \parallel r_o) / 2}{R_D / 2 r_{sink}}$$

- if $r_o \gg R_D$, then $R_D \parallel r_o \approx R_D$

$$CMRR = \frac{g_m \cdot R_D / 2}{R_D / 2 r_{sink}} = g_m r_{sink}$$

in dB:

$$CMRR (\text{dB}) = 20 \log_{10} (g_m r_{sink})$$

- we want CMRR to be as high as possible to reject unwanted common-mode signals; that's why we explored all those electronic current sinks!
- yes, this relied on many assumptions regarding g_m and r_o ; but it's accurate within a couple dB!
- given our example diff amp w/ $g_m = 6.325 \text{ mA/V}$, we can compute CMRR for various 2mA current sinks, from best to worst.

1) MOSFET cascode current mirror

$$r_{out} = 22.36 \text{ M}\Omega$$

$$CMRR = 20 \log_{10} \left(6.325 \times 10^{-3} \cdot 22.36 \times 10^6 \right)$$

$$\overbrace{CMRR = 103 \text{ dB}}$$

- this is excellent! 100 dB is often a good target
- BJTs w/ high g_m can do even better

2.) Basic MOSFET Current Mirror

$$r_{out} = \frac{|V_A|}{I_D} = \frac{100}{2} = 50 \text{ k}\Omega$$

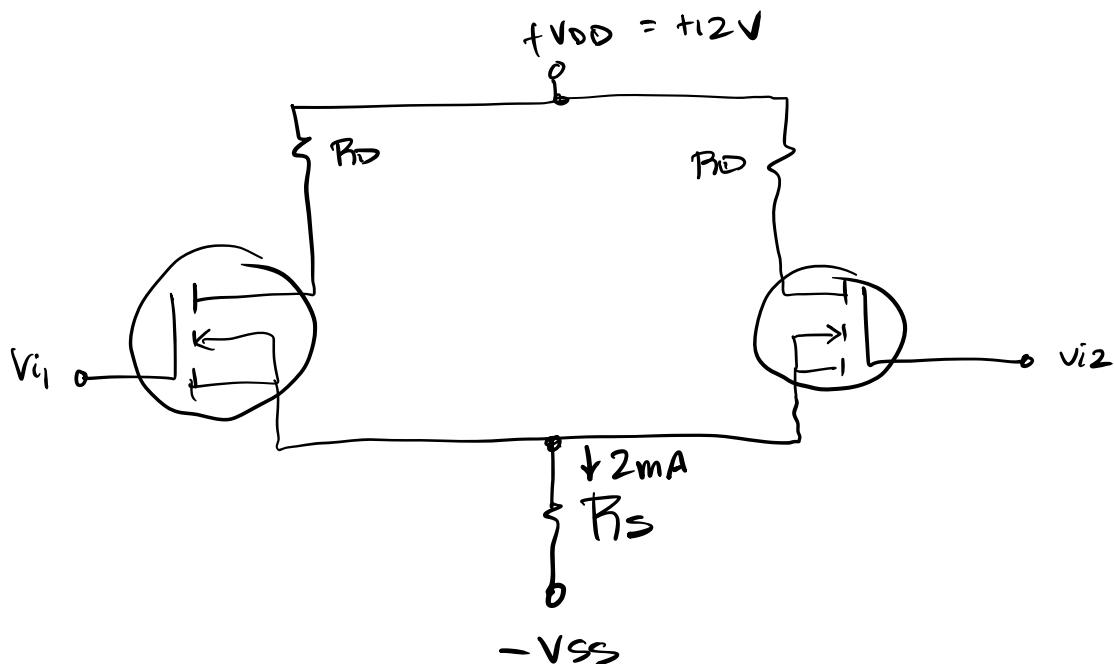
$$CMRR = 20 \log_{10} \left(6.325 \mu\text{A} \cdot 50 \text{ k}\Omega \right)$$

$$\overbrace{CMRR = 50 \text{ dB}}$$

- probably OK for many applications

3) Resistor to $-V_{SS}$ not electronic current sink!

- We used to call this a "long-tail pair"



- to calculate value of R_S for 2mA , need V_{GS}

$$\text{if } K = 10 \text{ mA/V}^2, V_t = 1.2 \text{ V}$$

$$I_D = K (V_{GS} - V_t)^2 \rightarrow V_{GS} = \sqrt{\frac{I_D}{K}} + V_t$$

per transistor!

$$V_{GS} = \sqrt{\frac{I}{10}} + 1.2 = \underbrace{1.516}_{\text{no bias network on gates!}} \text{ V}$$

$$\therefore V_S = V_G - V_{GS} = 0 - 1.516 = \underbrace{-1.516}_{\text{use } 5.23 \text{ k } 1\%} \text{ V}$$

$$R_S = \frac{V_S - -V_{SS}}{2 \text{ mA}} = \frac{-1.516 - 12}{2} = 5.242 \text{ k}\Omega$$

$$CMRR = 20 \log_{10} \left(\frac{6.325_m}{5.23_k} \right)$$

$$CMRR = 30.4 \text{ dB}$$

.. probably inadequate!