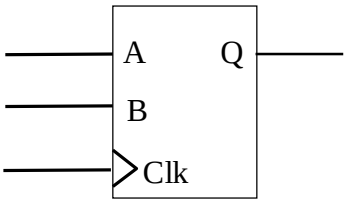
Half-hour Examination #3 - 30 minutes
Closed Book, one 8.5x11" page of notes (double-sided)

NAME _____ Pilot ID: w_____ **SCORE** _____ / 20

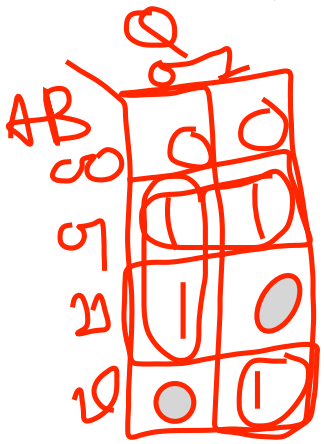
Problem #1 [4]
The questions on this page refer the 'fictional' AB-type flip-flop, described below:

A	B	Q(t+1)
0	0	0
0	1	1
1	0	Q
1	1	Q'



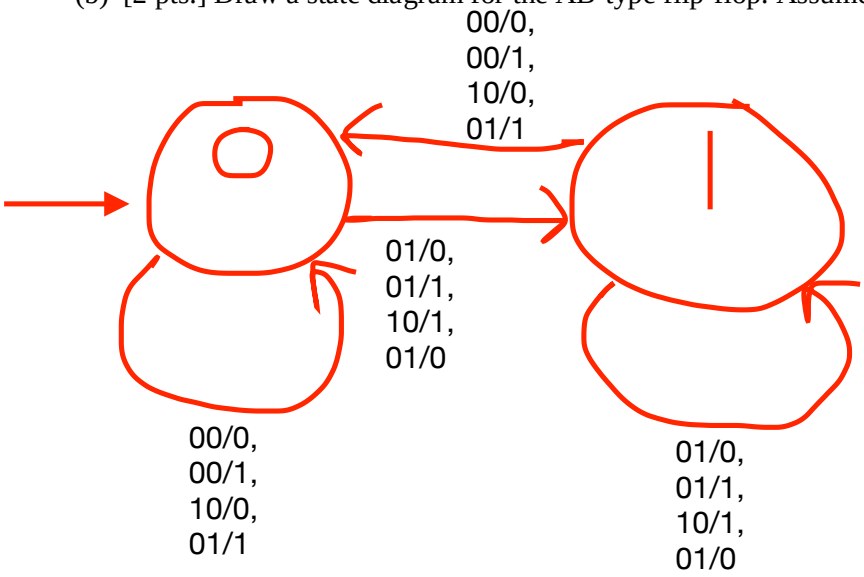
(a) [2 pts.] Determine the characteristic equation (function) of the AB-type flip-flop. Present the equation in simplified/minimized SOP form (show your work).

if a = 0, return b; else if a = 1 && b = 0, return Q, else return Q'



Q(t+1)=A'B + BQ'+AB'Q

(b) [2 pts.] Draw a state diagram for the AB-type flip-flop. Assume initial state is 0 (i.e., Q(0) = 0).



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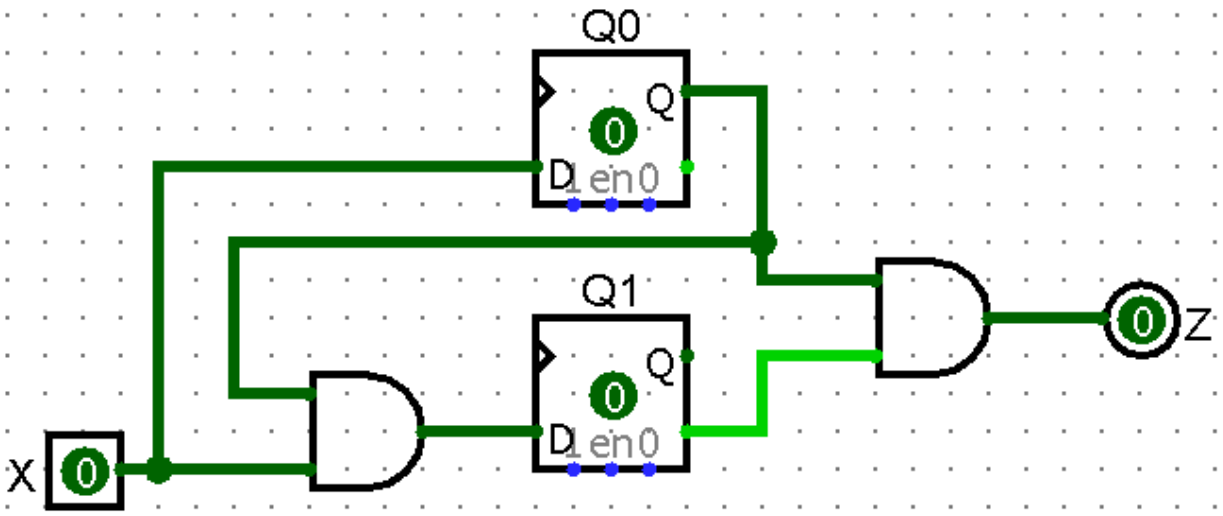
Problem #2 [12]
Analyze the clocked synchronous state machine show below. Assume that unconnected or unshown inputs are wire appropriate to allow normal functionality. [For example, the clock is not shown (for clarity), but should be assumed to be present.]



Simplify all equations

(a) [4 pts.] Input Equations

D1 = X*Q0

D0 = X

(b) [2 pt.] Output Equation

Z = Q1'Q0

(c) [1 pt.] Circle One

Z is **Mealy** or Z is **Moore**

This design is implemented with LS devices having the following characteristics:

Comb. gates propagation delay,	
input to output (min):	1 ns
input to output (max):	2 ns
DFF propagation delay,	
clock to output (min):	4 ns
clock to output (max):	6 ns
input to output (min, max):	∞
DFF setup time,	
data input before clock:	5 ns
DFF hold time,	
data input after clock:	3 ns

Calculate the timing parameters for the design.

(d) [1 pts.] Prop. delay, clock to output (min):

5ns

(e) [1 pts.] Prop. delay, input to output (max):

(f) [1 pts.] Setup time, data input before clock:

5ns

(g) [1 pts.] Hold time, data input after clock:

2ns

(h) [1 pts.] Maximum clock rate:

1/(11ns)

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Problem #3 [4]
Consider a sequential device with one synchronous input (X) and one synchronous output (Z). An initial inspection of the device determines that it has two D-type positive-edge-triggered flip-flops (D1 and D0). Furthermore, the following equations describe the combinational behavior of the circuit.

D1 = Q0X + Q0'X'

D0 = XQ0' + X'Q0

Z = Q1

(a) [2 pt.] Draw a state diagram that represents the sequential functionality of the device. You may assume that the state variables all have an initial value of "0" on reset. Don't forget to label your arcs/nodes clearly!

(b) [2 pt.] Build/Implement/Synthesize this device using D-type flip-flops and any number of AND, OR, and NOT gates. Use good design practices, including proper labeling of all wires/network connections.

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DO NOT BEGIN UNTIL INSTRUCTED TO DO SO

HONOR CODE: Before the end of the examination, please sign:

In recognition of and in the spirit of the Wright State University policies of academic honesty, I certify that I have neither given nor received unpermitted aid in this examination.

Name (Printed): _____

Signature: _____

DO NOT BEGIN UNTIL INSTRUCTED TO DO SO
