Half-hour Examination #6 - 30 minutes
Closed Book, one 8.5x11" page of notes (double-sided)

NAME _____ Pilot ID: w_____ **SCORE** _____ / 20

Print your final answer neatly in the space provided below.

	A	**B**	**C**
Problem #1: @2			
Problem #2: @2			
Problem #3: @2			

Problem #4: @1			**scratch space**

HONOR CODE: At the end of the examination, please sign:

In recognition of and in the spirit of the Wright State University policies of academic honesty, I certify that I have neither given nor received unpermitted aid in this examination.

Signature:

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Unless otherwise specified all questions on this page refer to the datapath described for use in the DDmini as shown in Figure 1.

Problem #1: [6 pts.] The datapath consists of a Register file ($t_{pd(min)}$ = 4 ns, $t_{pd(max)}$ = 6 ns, t_{setup} = 3 ns, t_{hold} = 2 ns) which is connected to MUX B ($t_{pd(min)}$ = 1 ns, $t_{pd(max)}$ = 2 ns). MUX B is connected to a function unit ($t_{pd(min)}$ = 2 ns, $t_{pd(max)}$ = 4 ns). The function unit is connected to MUX F ($t_{pd(min)}$ = 1 ns, $t_{pd(max)}$ = 2 ns). A proposal is made to modify the datapath using registers ($t_{pd(min)}$ = 1 ns, $t_{pd(max)}$ = 2 ns, t_{setup} = 1 ns, t_{hold} = 1 ns) so that it is partially pipelined.
One register is placed on BUS A and BUS B at the horizontal line indicated by the number 1 on Figure 1 (after the register file, before MUX B and the function unit). Anther register is placed at the horizontal line indicated by the number 3 on Figure 1 (after the function unit, before MUX F).
(a) What is the **minimum clock period** that can be used for this datapath **without pipelining**?
(b) What is the **minimum clock period** for the proposed **pipelined** datapath?
(c) What is the (minimum) microinstruction **turn-around time with pipelining**?

Problem #2: [6 pts.] Specify a 16-bit control word IN HEX that could be applied to the datapath to implement each of the following microoperations. In order to receive credit you MUST use zero values for don't care values of the control word. Also indicate if there are any signals from the control unit that must ALSO be asserted in order for your control word to implement the RTL command. For example, if the Memory Write signal to RAM must be asserted, note this in your answer.
(a) R1 ← R1 + R3
(b) M[R3] ← R2
(c) R0 ← constant in

Problem #3: [6 pts.] The following sequence of 16-bit control words are presented to the datapath. For each, identify the *microoperation* that is executed as an **RTL expression**. Assume that Memory Write (to the RAM) is NOT asserted unless it is explicitly indicated.
(a) x0081
(b) x9209
(c) x8F38, MW asserted

Problem #4: [2 pts.] Consider the following machine instructions. These instructions are to be implemented on the simple computer system built in Lab. Construct a sequence of RTL commands for the DDmini datapath that will allow the execution of the instruction. Do **not** convert the RTL commands into hex microinstructions - just provide the RTL microroutine.
(a) M[A] ← x0
(b) M[C] ← M[A] + M[B]

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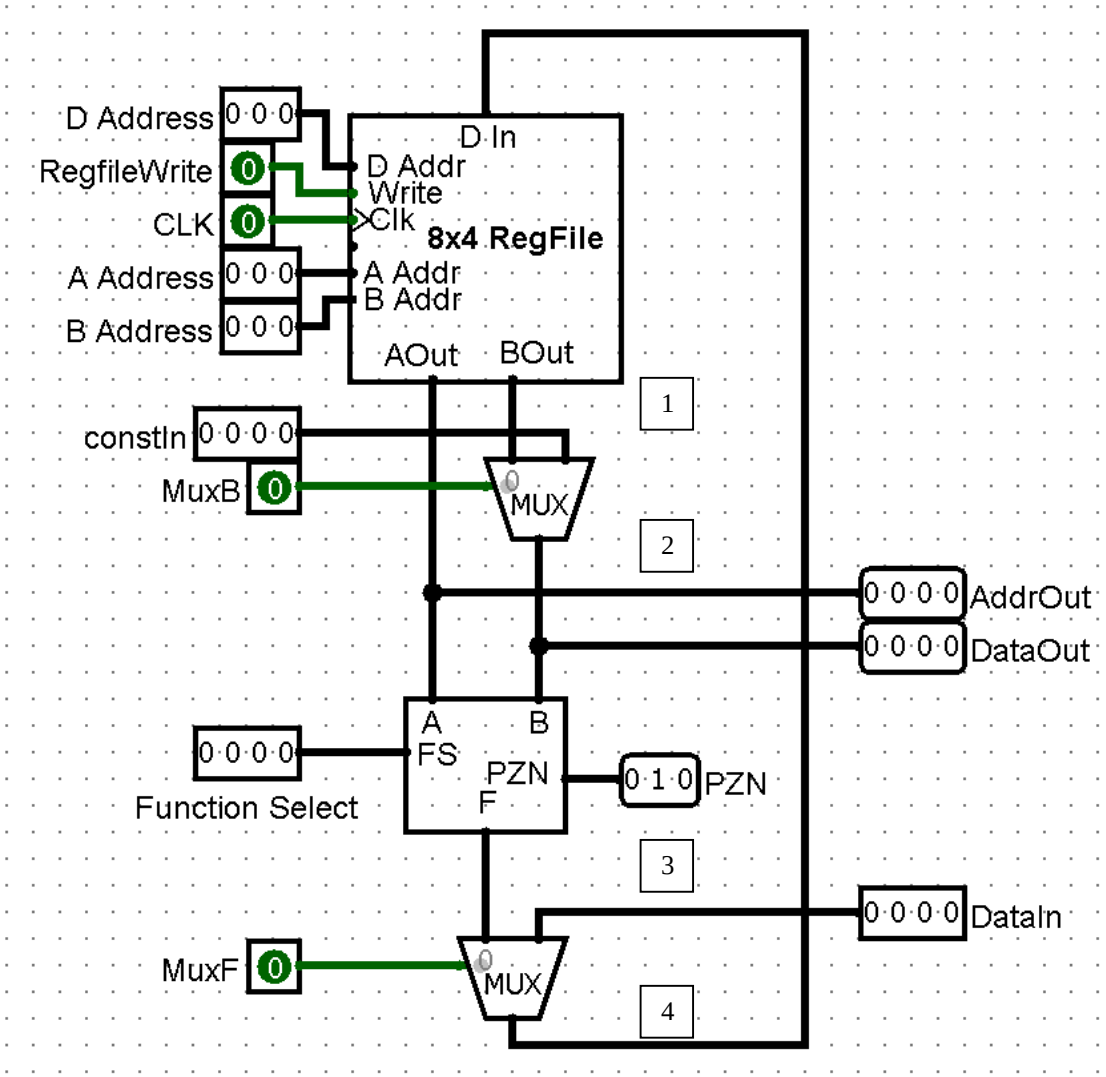

FS	Microoperation
x0	F = 0
x1	F = 1
x2	F = A
x3	F = B
x4	F = A + B
x5	F = A – B
x6	F = A * B
x7	F = A / B
x8	F = NOT(A)
x9	F = A AND B
xA	F = A OR B
xB	F = NOT(A) + 1
xC	F = A >> 1
xD	F = A << 1
xE	F = A >>> 1
xF	Reserved

15:13	12	11:9	8	7:4	3:1	0
AA (3)	MB (1)	BA (3)	MF (1)	FS (4)	DA (3)	RW (1)

Figure 1