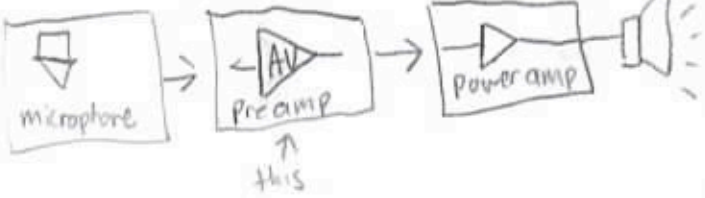
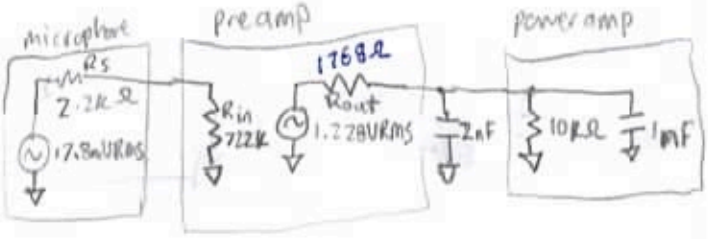
Step 1: determine required
- gain
- input & output impedences
- frequency response
- output signal swing
- Sometimes ↑ must be deduced

ex: design a small-signal preamplifier
for a panasonic WM-61A
electret condenser microphone to
drive a commercial audio power amplifier





microphone specs:
"nominal" signal level: 17.8 mVRMS @ 94 dB SPL
output impedence: 2.2kΩ
↳ ∴ R_{in} should be "much higher" than 2.2kΩ
to avoid voltage dividing an already small signal
∴ Perhaps try for $R_{in} > 22k\Omega$

frequency range: 50 Hz to 15 kHz
↳ amplifier response should exceed this on both sides
↳ -3dB @ 30 kHz ≈ -1dB @ 15kHz
so perhaps shoot for 25 Hz to 30kHz
(f_L) (f_H)

Power-amp specs:
nominal input sensitivity: 1.228 VRMS
input impedance: R_{in} = 10kΩ in parallel w/ 1nF
↳ let's add a worse-case cable capacitance of 2nF (fool proof it)
∴ C_L (total) = 3nF

Calculations

Gain calc

$A_V = \frac{1.228}{0.0178} = 68.99 = 36.78\text{dB}$

∴ this needs a high gain, I tend towards BJT for high g_m ← (thing for gain)

→ But FETs have higher input impedance

in order to drive 3nF to at least 30kHz, we need Rout less than

$f_{Hout} = \frac{1}{2\pi R_{out} C_L} \rightarrow R_{out} = \frac{1}{2\pi f_H C_L}$

$= \frac{1}{2\pi \cdot 30\text{kHz} \cdot 3\text{nF}} = 1768\,\Omega$ ← collector or drain resistor in this ballpark?

"Nominal" usually means "normal" or "average"

↳ could mean peak values well in excess of this

↳ so if our preamp must create nominal 1.228VRMS, but could be asked to provide more, how much more?

∴ let's assume we'd like 10dB of headroom

factor of $10^{10/20} = 10^{1/2} = 3.16$

↳ so max output voltage might be $1.228 \cdot 3.16 = 3.883\,V_{RMS}$

$3.883 \cdot \sqrt{2} \cdot 2 = 11\,V_{pp}$

In summary: our amplifier needs

- $A_V \gtrsim 37\text{dB}$
- $R_{in} \geq 22k\,\Omega$
- $R_{out} \leq 1768\,\Omega$
- output swing $> 11\,V_{p\text{-}p}$ into 10k‖3nF load
- bandwidth better than $f_L = 25\,Hz$, $f_H = 30kHz$

Step 2: choose suitable electronic device & amplifier config. for specs.

Specs
BW: 25-30k
AV=37 dB
$R_{in} \geq 22k\Omega$
$R_{out} \leq 1768\Omega$
$V_{out} \geq 11V_{p-p}$

∴ R_{in} is fairly high; suggests FETs
↳ however, we also need high gain → BJTs

suggest using a Darlington transistor (high g_m of BJT w/ very high equivalent β)
↳ use common-emitter amplifier (have to check if inversion is OK)
also have to check how much input capacitance we can tolerate (if $R_S = 2.2k\Omega$)

Step 3:

↳ $f_{H(in)} \approx \frac{1}{2\pi R_S C_{in}} \rightarrow C_{in} = \frac{1}{2\pi R_S f_{H(in)}} = \frac{1}{2\pi \cdot 2.2k \cdot 60kHz} = 1.2nF$

↑ doubled to be safe

Choose an approximate operating point and actual device that achieves signal swing, gain, and R_{out}

Common-emitter: $R_{out} \approx R_C$
∴ to achieve $R_{out} \leq 1768$, choose $R_C = 1.5k\Omega$
∵ for low distortion, $R_L > 2R_C$ [minimum]
↳ check $10k > 2 \cdot 1.5k$, OK

Common-emitter: $A_{V_2} \approx -g_m(R_C \| R_L)$

$R_C \| R_L = 1.5k \| 10k = 1.3k$

∴ need $g_m > \frac{68.99}{1.3k} = 53.07 \frac{mA}{V}$ ← required gain

↳ consistant w/ BJTs!

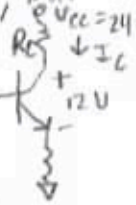
Ebers-Moll: $g_m = 35 I_C$

∴ $I_C > \frac{g_m}{35} = \frac{53}{35} = 1.5mA$ ← Probably doable

we need > $11V_{p-p}$ signal swing
∴ $V_{CC} > 11V$; but how much more?
∵ plan to lose a couple volts across R_E
∵ plan to stay a couple volts away from ground
∵ plan to stay a couple volts away from V_{CC}

avoid saturation ↓
↑ avoid cutoff

∵ choose $V_{CC} = 24V$ (a common voltage regulator value)
∵ determine approx. V_{CE} max and P_{diss}
↳ under extreme conditions, $V_{CE} \rightarrow V_{CC}$
∴ $V_{CE\ max} > 24V$
↳ we don't know our exact V_{CE}, but it'll likely be $\approx V_{CE} = 12V$



∵ approx $I_C \approx \frac{24-12}{1.5k} \rightarrow$ b/c $= 8mA > 1.5mA$ ok

$P_{diss} \approx V_{CE} \cdot I_C = 12 \cdot 8 = 96mW$

∴ we need to choose a Darlington w/ $V_{CE} \geq 24V$, $P_{diss} > 96mW$

Step 4: select device and perform load line analysis to determine optimum quiescent operating point

chosen device: MPS A14

NPN darlington

Si

NPN

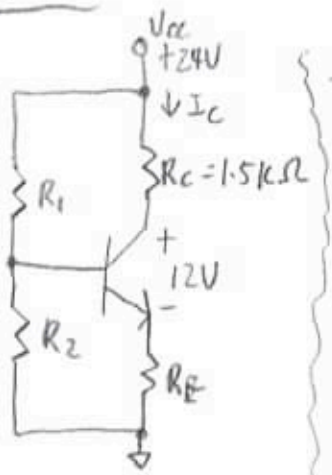
$V_{CE(max)} = 30V$

$h_{fe(min)} = 10,000$ (this is β)

$P_{max} = 625mW$

$C_{ibo} = 5.6pF \approx C_{be}$

$C_{obo} = 5.2pF \approx C_{bc}$



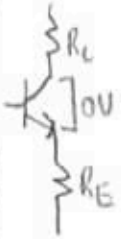
→ let's pick 2V across R_E for DC stability (10% of V_{cc} (loss?) is not uncommon)

∴ $R_E \approx \frac{2V}{8mA} = 0.25k\Omega$, pick $R_E = 220\Omega$

∴ Introduce DC load line

∴ at DC, net load across transistor is $R_C + R_E$ = 1.5k + 0.22k = 1.72kΩ

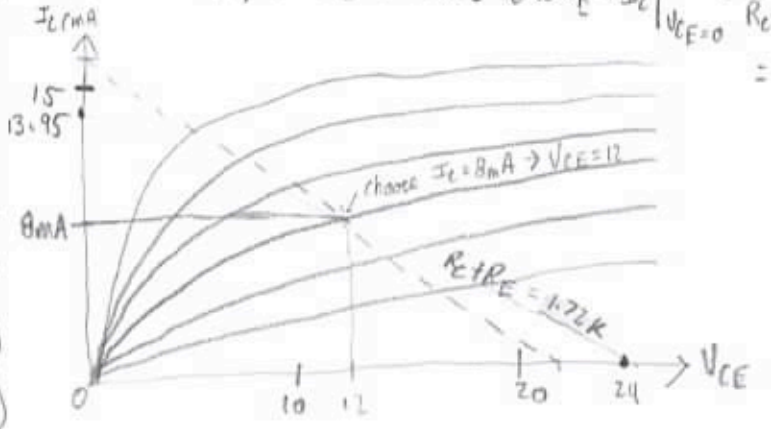
∴ we can plot this against MPSA14 curves to show possible operating points!



$I_{C|max} = \frac{V_{cc}}{R_C + R_E} = \frac{24}{1.72k}$

@ Zero I_C → no drop across R_C & R_E → $V_{CE}|_{I_C=0} = V_{cc}$

@ Zero V_{CE}, all V_{CE} is across R_C & R_E → $I_C|_{V_{CE}=0} = \frac{V_{cc}}{R_C + R_E} = \frac{24}{1.72k}$ = 13.95mA



Continue

∴ steeper AC loadline reduces signal swing

↳ that's why you want $R_L \gg R_C$

↳ final available signal swing is ≈ 20.64 − 2 > 11 V_{p-p} (still ok)

For AC signals need to factor in R_L

↳ AC load line superimposed on D.C. one

actual $V_{CE} = V_{cc} - I_C(R_C + R_E) = 24 - 8(1.5 + 0.22) = 10.24V$

Ac collector load = $R_C \| R_L = 1.5k \| 10k = 1.3k$

↳ we can draw AC Load line with this steeper slope

↳ start w/ quiescent point at $I_C = 8mA$

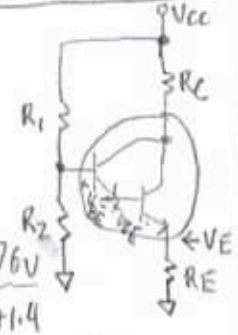
$V_{CE}|_{\Delta I_C = 8mA} = 10.24 + 8(1.3k) = 20.64V$

$I_C|_{\Delta V_{CE} = -10.24V} = 8 + \frac{10.24}{1.3k} = 15.87mA$

See continue to the left

Step 5

use quiescent point determined in step 4 to design D.C. bias network for amplifier



•• Darlington

∴ $I_C \simeq I_E$ (very low base current)

$\therefore V_E = R_E \cdot I_E = 0.220k \cdot 8m = 1.76V$

Darlington: $V_{BE} \simeq 1.4V$ $V_B = V_E + 1.4$

$= 1.76 + 1.4 = 3.16V$

Pick $R_2 = 47k\Omega$

$$V_B = V_{cc}\left[\frac{R_2}{R_1+R_2}\right]$$

$$3.16 = 24\left[\frac{47}{47+R_1}\right] \rightarrow R_1 = 318k \quad \text{use } 300k = R_1$$

Check R_{in}

$R_{in} \simeq R_1 \| R_2$

$= 47k \| 300k$

$= 40.63k > 22k\Omega$ (ok)

Step 6 Mid frequency SS analysis

C_E: $A_{V_2} = -g_m(R_C \| R_L)$

$g_m = 35 I_C = 35 \cdot 8 = 280 \, mA/V$

$A_{V_2} \simeq -280(1.3k) = -364$ or $51dB$ $>> 37dB$ (too much gain)

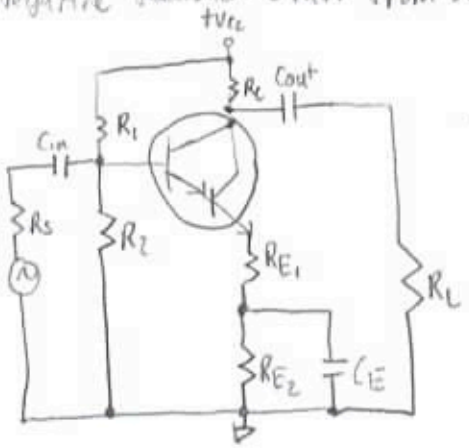
∴ check input capacitance (miller time)

$C_{BC(in)} = C_{BC}(1 - A_V) = 5.2(1 - -364) = 1896\,pF / 1206\,pF$ (not good, too high)

∴ the solution? Negative feedback

1) external shunt/shunt loop
2) unbypassed emitter resistor
   1) works better, but harder to implement
   ∴ choose 2)

Negative feedback stuff from step 6



∴ Set $R_{E_1} + R_{E_2}$ to 220k for D.C. characteristics

∴ Set R_{E_1} for desired feedback factor (for A.C.)

want $A_V = 68.99$ } ignoring polarity inversion

have $A_{V_0} = 364$ }

$$A_V = \frac{A_{V_0}}{1+\beta A_{V_0}} \rightarrow A_V + \beta A_{V_0} A_V = A_{V_0} \rightarrow \beta = \frac{A_{V_0} - A_V}{A_{V_0} \cdot A_V}$$

$$\beta = \frac{364 - 69}{364 \cdot 69} = 0.01175$$

∴ for local-emitter feedback

$$\beta = \frac{R_E}{R_C \| R_L} = \frac{R_{E_1}}{1.3k} = 0.01175 \rightarrow R_{E_1} = 0.01175 \cdot 1.3k = 0.01528k\Omega$$

use $R_{E_1} = 15\Omega$

high-A_{V_0} approximation:

$$A_V \simeq \frac{R_C \| R_L}{R_E} \rightarrow R_{E_1} = \frac{1.3k}{69} = 18.84\,\Omega$$ (might have made Av too lo

because $364 \not\gg 69$

∴ what's left?

•• recheck HF response

∴ design LF components to achieve $f_L < 25Hz$

↑ make most expensive cap dominant pole → (CE)