1. Write VHDL code to implement the function expressed in the following truth table.

A	B	C	F
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

a) Use ***concurrent VHDL code*** (Boolean expression)

```
entity function_F is
        port ( A,B,C : in std_logic;
                F : out std_logic);
end function_F;

architecture concurrent of function_F is
begin
        F <= (NOT A AND NOT B AND NOT C) OR (NOT A AND B AND NOT C) OR (A AND
NOT B AND C) OR (A AND B AND NOT C);

end concurrent;
```

b) Use ***if*** statement

```
entity function_F is
        port ( A,B,C : in std_logic;
                F : out std_logic);
end function_F;

architecture behavior_1 of function_F is
begin
proc1: process(A,B,C)
        Begin
         IF (A='0' And C='0') THEN
                F <= '1';
         ELSIF (A='1' AND B='0' AND C='1') THEN
                F <= '1';
         ELSIF (B='1' AND C='0') THEN
                F <= '1';
         ELSE
                F <= '0';
         END IF;

        end process proc1;
end behavior_1;
```