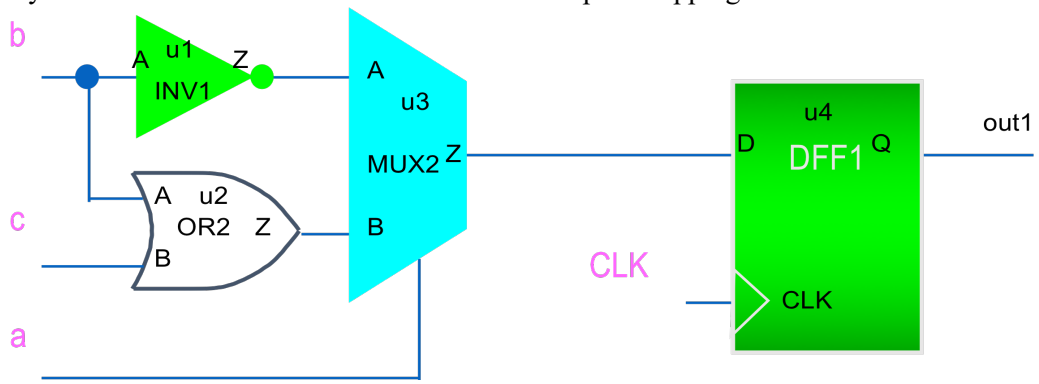
1. Write an entity and architecture pair of VHDL structural description for a structural representation of a circuit sequential_1 shown below. You need to declare the components (i.e., **DFF1** for D flip-flop, **OR2** for 2-input OR gate, **INV1** for inverter gate, and **MUX2** for 2x1 MUX gate) used in the schematic diagram. Assume these basic components have been compiled. Ensure all signals and ports of **STD_LOGIC** type and labeled in the schematic diagram match your VHDL code. Use **BY-NAME** method of port mapping.




```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.all;
ENTITY sequential_1 IS
                    PORT (a, b, c, clk : in std_logic;
                          out1 : out std_logic);
END ENTITY buzzer;
    architecture sequential_structure of sequential_1 is

    -- Component and signal declarations
        component INV1
            port (a: in std_logic;
                z: out std_logic);
        end component;
        component OR2
            port (a,b: in std_logic;
                z: out std_logic);
        end component;
        component MUX2
            port (a,b,sel: in std_logic;
                z: out std_logic);
        end component;
        component DFF1
            port (d, clk: in std_logic;
                q: out std_logic);
        end component;

    -- declaration of signals used to interconnect gates
    signal s1, s2, s3: std_logic;

    begin
    -- Component instantiations statements
    u1: INV1
            port map (a=>b, z=>s1);
    u2: OR2
            port map (a=>b, b=>c, z=>s2);
    u3: MUX2
            port map (a=>s1, b=>s2, sel=>a, z=>s3);
    u4: DFF1
            port map (d=>s3, clk=>clk, q=>out1);

    end sequential_structural;
```