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**EE 4540L/6540L/CEG4322L/CEG6322L**

**FALL 2023**

**TA: Kanchan Vissamsetty**

**Lab section: 01**

**Name: Alex Yeoh**

**“I have neither given nor received aid on this assignment, nor have I observed any violation of the Honor code”**

**Signature: Alex Yeoh Date: 6 December 2023**

**Report due date: 6 December 2023**

1. **OBJECTIVE**

To learn how to design a circuit with EDP in mind.

1. **PROCEDURE**

I calculated the path delay for this circuit with various number of stages. I then built the circuit with the least path delay and simulated it. I then modified the components to minimize the difference in rising and falling propagation delay and simulated it. I then found the highest frequency where the circuit still works properly and simulated it and repeated this for various given voltages. I then calculated the EDP for all those simulations and determined which had the best EDP

1. **RESULT**

F=GBH, G = 1, B = 8\*3/6=4, H = 60/10=10, F = 1\*4\*10=40,

Calculations for F and N

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| n | stages | Path Logical Effort (G) | Path Effort Delay (DF) | Path Parasitic delay (P) | Path delay (D) |
| 1 | nor3 | 2.33 | 93.33 | 3 | 96.33 |
| 2 | nand3, inv | 1.67 | 16.33 | 4 | 20.33 |
| 2 | inv, nor3 | 2.33 | 19.32 | 4 | 23.32 |
| 3 | nor3, inv, inv | 2.33 | 13.61 | 5 | 18.61 |
| 3 | inv, nand3, inv | 1.67 | 12.16 | 5 | 17.16 |
| 4 | nand3, inv, inv, inv | 1.67 | 11.43 | 6 | 17.43 |
| 4 | inv, nor3, inv, inv | 2.33 | 12.43 | 6 | 18.43 |

Calculation for comparing different designs

A screenshot of a computer

Description automatically generated

Schematic of the decoder

A diagram of a computer

Description automatically generated with medium confidence

Simulation of decoder with standard gates

A graph with red lines

Description automatically generated

Average power of decoder with standard gates

A black screen with many colorful lines

Description automatically generated

Simulation of decoder with gates optimized for output 4

A graph with red lines

Description automatically generated

Average power of the simulation above

A black screen with colorful lines

Description automatically generated

Simulation of decoder with gates optimized for output 4 with fastest period

A graph with red lines

Description automatically generated

Average power of the simulation above

A diagram of a computer

Description automatically generated with medium confidence

Simulation of decoder with gates optimized for output 4 with fastest period and 2v power

A graph of a graph

Description automatically generated with medium confidence

Average power of the simulation above

A graph with colorful lines

Description automatically generated with medium confidence

Simulation of decoder with gates optimized for output 4 with fastest period and 1.8v power

A graph of a graph

Description automatically generated

Average power of the simulation above

A black screen with colorful lines

Description automatically generated

Simulation of decoder with gates optimized for output 4 with fastest period and 1.5v power

A graph of a graph

Description automatically generated with medium confidence

Average power of the simulation above

A black screen with colorful lines

Description automatically generated

Simulation of decoder with gates optimized for output 4 with fastest period and 1.2v power

A graph of a graph showing a number of purple lines

Description automatically generated with medium confidence

Average power of the simulation above

A black screen with colorful lines

Description automatically generated

Simulation of decoder with gates optimized for output 4 with fastest period and 1v power

A graph of a graph

Description automatically generated with medium confidence

Average power of the simulation above

A table with numbers and numbers

Description automatically generated

EDP calculations

1. **CONCLUSION**

My results satisfy the requirements of lab, and I have found that a period of 1ns at a voltage of 1.2v has the best EDP. It is likely possible to improve my design by finding better PMOS and NMOS sizes that are less skewed across all outputs for the decoder. I have learned how to calculate EDP from this lab.