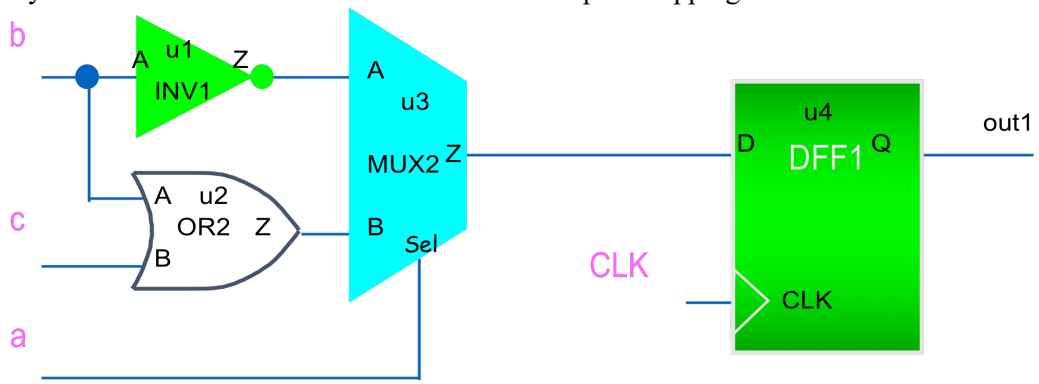
1. Write an entity and architecture pair of VHDL structural description for a structural representation of a circuit sequential_1 shown below. You need to declare the components (i.e., **DFF1** for D flip-flop, **OR2** for 2-input OR gate, **INV1** for inverter gate, and **MUX2** for 2x1 MUX gate) used in the schematic diagram. Assume these basic components have been compiled. Ensure all signals and ports of **STD_LOGIC** type and labeled in the schematic diagram match your VHDL code. Use **BY-NAME** method of port mapping.




```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.all;
ENTITY sequential_1 IS
                PORT ( a,b,c,CLK: in STD_LOGIC; out1: out STD_LOGIC;

                                                                );
END ENTITY buzzer;
    architecture sequential_structure of sequential_1 is

-- Component and signal declarations
                                component INV1
                                port (A: in STD_LOGIC; Z: out STD_LOGIC);
                                end component;
                                component OR2
                                port (A,B: in STD_LOGIC; Z: out STD_LOGIC);
                                end component
                                component MUX2
                                port (A,B,Sel: in STD_LOGIC; Z: out STD_LOGIC);
                                end component
                                component DFF1
                                port (D, CLK: in STD_LOGIC; Q: out STD_LOGIC);
                                end component
-- declaration of signals used to interconnect gates
                                Signal s1, s1, s3: in STD_LOGIC;

begin
-- Component instantiations
```

```
end sequential_structural;
```