WRIGHT STATE UNIVERSITY

EE4620/6620, CEG4324/6324
Digital Integrated Circuit Design
with PLDs and FPGAs

Lab 1 (Summer 2024)

Xilinx Vivado Combinational Circuit Design, Simulation, and Test in FPGA

A. Objective

The main objective of this lab is for you to explore the design space for combinational circuit design and to become familiar with the Xilinx Vivado simulation environment. Read all directions carefully. You will design a VHDL project in Xilinx Vivado and functionally verify and validate your design along with the implementation steps to upload the design through the Vivado simulation environment.

B. Instruction

1. In this lab, the VHDL design code (rca.vhd) describes an n-bit, Ripple-Carry Adder (RCA). It comprises of two parts: subcomponent 1-bit full adder (FA) and top-level entity RCA. Using the number of basic gates as an area estimator, determine the estimated size (by the number of basic logic gates) required for an n-bit RCA where n = 16 in rca.vhd. Using gate delay as a timing estimator, estimate the worst propagation delay, WPD, # of unit gate delays between the time any input changes and the time all outputs are valid. For this lab, use logic gates and delays as follows:

   2 ns for inverter

   4 ns for 2-input logic gates such as AND, NAND, OR, NOR

   5 ns for 3-input logic gates such as AND, NAND, OR, NOR

   6 ns for 4-input logic gates such as AND, NAND, OR, NOR

   Note: Do not use XOR or XNOR or any other logic gates except the above ones.

2. For this step, you simulate the design code from part 1. Look at the test bench file, tb_rca.vhd. In this file, you see the test bench code for simulating the **16-bit** RCA adder described in step 1. In the test bench, note the "wait for WPD" statement. The WPD time given on this line must correspond to the worst-case propagation delay found in step 1. If the time is too short, the simulation will fail. You must adjust the WPD value in the test bench file (i.e., initial **WPD = 32 ns**) to the correct value you calculated in step 1. To simulate the design circuit (rca.vhd) using the test bench file (tb_rca.vhd).
3. Now that you have simulated and validated a Ripple Carry Adder circuit, you will modify the design code to improve the propagation delay. Note: you can reduce the WPD through logic optimization by combining adjacent FA blocks into a combinational two-level logic circuit. In this lab, you combine **two 1-bit FAs** into a **2-bit combinational two-level FA** (2-bit FA). Below is the 2-bit FA truth table where Cin, A1, A0, B1, B0 are the five inputs, and Cout, S1, S0 are the three outputs.

Cin	A1	A0	B1	B0	Cout	S1	S0
0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	1
0	0	0	1	0	0	1	0
0	0	0	1	1	0	1	1
0	0	1	0	0	0	0	1
0	0	1	0	1	0	1	0
0	0	1	1	0	0	1	1
0	0	1	1	1	1	0	0
0	1	0	0	0	0	1	0
0	1	0	0	1	0	1	1
0	1	0	1	0	1	0	0
0	1	0	1	1	1	0	1
0	1	1	0	0	0	1	1
0	1	1	0	1	1	0	0
0	1	1	1	0	1	0	1
0	1	1	1	1	1	1	0
1	0	0	0	0	0	0	1
1	0	0	0	1	0	1	0
1	0	0	1	0	0	1	1
1	0	0	1	1	1	0	0
1	0	1	0	0	0	1	0
1	0	1	0	1	0	1	1
1	0	1	1	0	1	0	0
1	0	1	1	1	1	0	1
1	1	0	0	0	0	1	1
1	1	0	0	1	1	0	0
1	1	0	1	0	1	0	1
1	1	0	1	1	1	1	0
1	1	1	0	0	1	0	0
1	1	1	0	1	1	0	1
1	1	1	1	0	1	1	0
1	1	1	1	1	1	1	1

You may use 5-input K-map to optimize the three outputs in sum-of-products or use the online K-map solvers (for example, http://www.32x8.com/index.html).

4. The 16-bit RCA can be constructed by 3 cases. They are:

   (Case 1) 16 1-bit, i.e. the 16-bit adder is constructed by

   1 + 1 + 1 + 1 + 1 + 1 + 1 + 1 + 1 + 1 + 1 + 1 + 1 + 1 + 1 + 1 from MSB to LSB.

   (Case 2) 4 2-bit + 8 1-bit, i.e. the 16-bit adder is constructed by

   2 + 2 + 2 + 2 + 1 + 1 + 1 + 1 + 1 + 1 + 1 + 1 from MSB to LSB.

   (Case 3) 8 2-bit, i.e. the 16-bit adder is constructed by

   2 + 2 + 2 + 2 + 2 + 2 + 2 + 2 from MSB to LSB.

   For each case of the 16-bit adder, simulate your design to validate your WPD value and the functionality.

C. Report [100 pts] (Submitted to your Lab Pilot Dropbox by 11:30 pm, Monday, May 20, 2024)

1. [10 pts] Your detailed approach to derive Boolean expressions for the ouputs of 1-bit FA and 2-bit FA.
2. [30 pts] Your VHDL and testbenches of the ***three*** cases of 16-bit RCA.
3. [60 pts] Your VHDL and simulation waveforms for each case to validate your design. Your functional verification must include the following test cases:

Test cases for 3
a, b, cin
57,0,0
57,0,1
12345,0,0
12345,0,1
0,129,0
0,129,1
0.54321,0
0.54321,1

A_{10} = (57, 12345)

B_{10} = (129, 54321)

You must test for all A+B cases with initial carry-in C_0 = 0 and 1, which means you should verify a total of 4 x 2 = 8 input and output values. Note: All answers in the waveforms must be labeled to show correct answers. Annotate the inputs and outputs in hexadecimal values next to their binary equivalents in the simulation waveform. Include all waveform snapshots.

1 part 1: by reading the behavioral expression written for Co and S
1 part 2: by making input and output pins in logisim, I analyzed the circuit which generated a blank truth table as seen in figure 1, which I then filled as seen in figure 2, after which I can go to the expression tab where simplified equations are generated. The generated equations are then modified so the gates don't exceed the input limits.