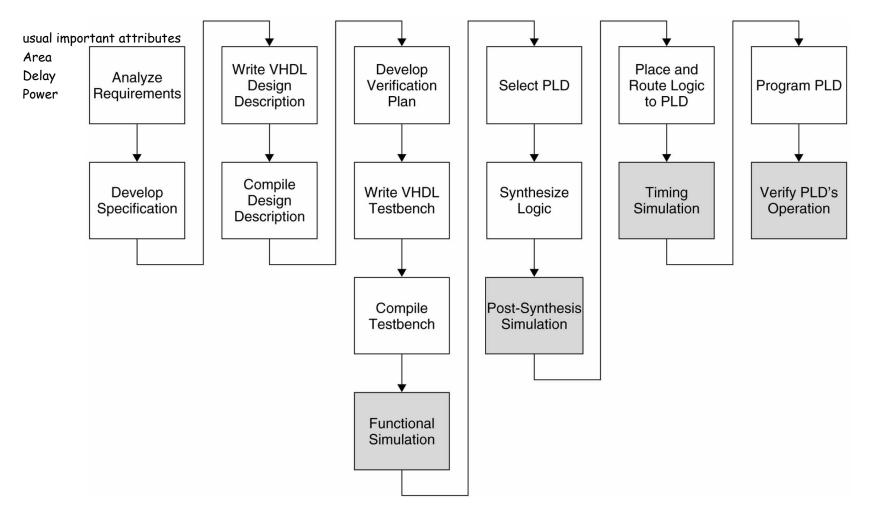
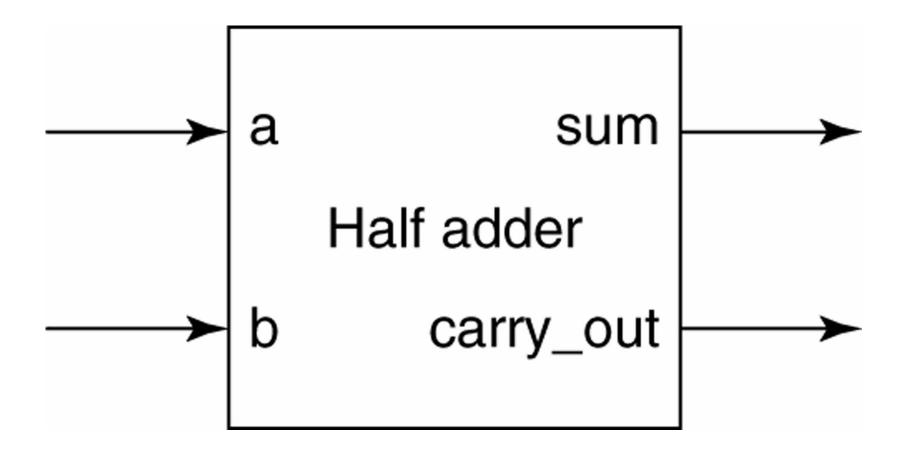
Chapter 1

Digital Design Using VHDL and PLDs



Design flow for the VHDL/PLD design Methodology

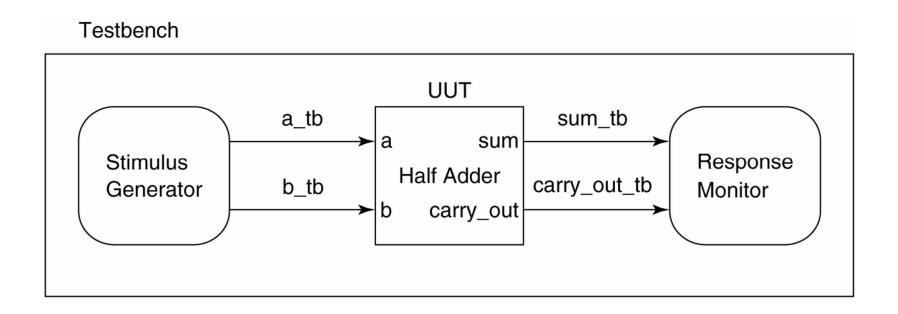


Block diagram of a half adder

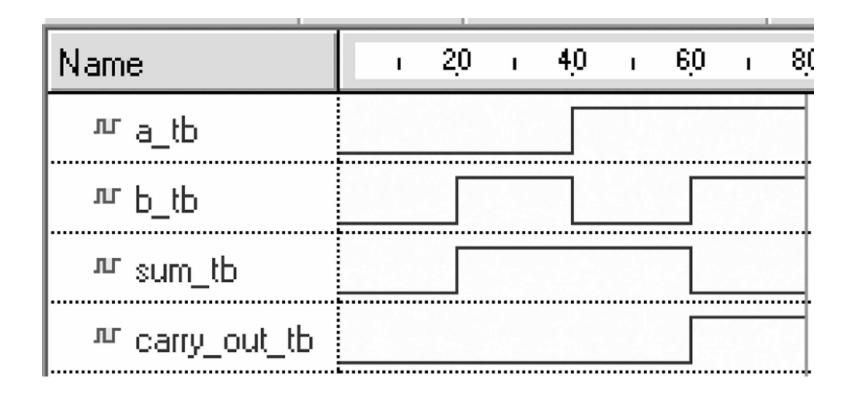
Table 1.3.1

Half-adder truth table and minterms.

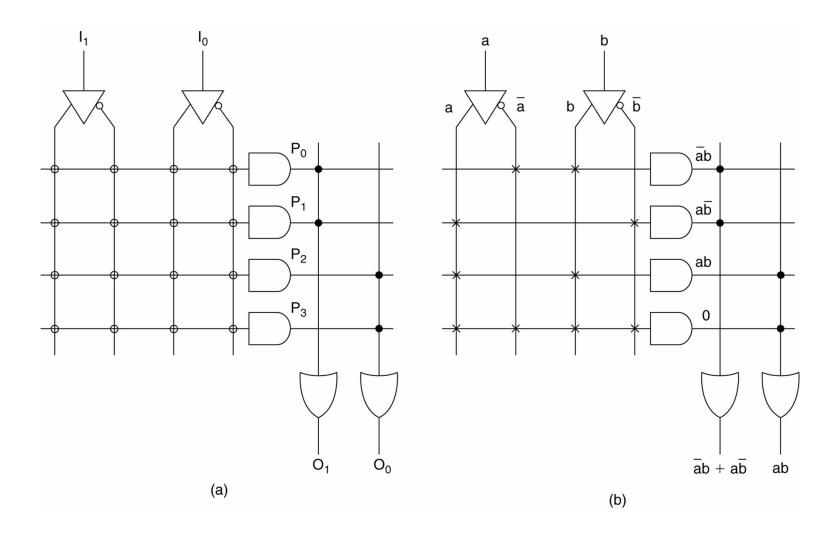
а	b	sum	carry_out		y_out terms
0	0	0	0		
0	1	1	0	ab	
1	0	1	0	ab	
1	1	0	1	ć	ab



Half-adder to its testbench

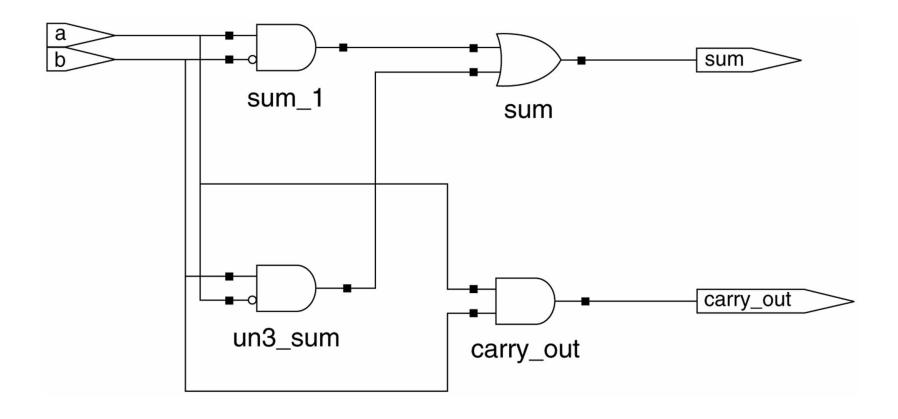


Functional simulation of half-adder

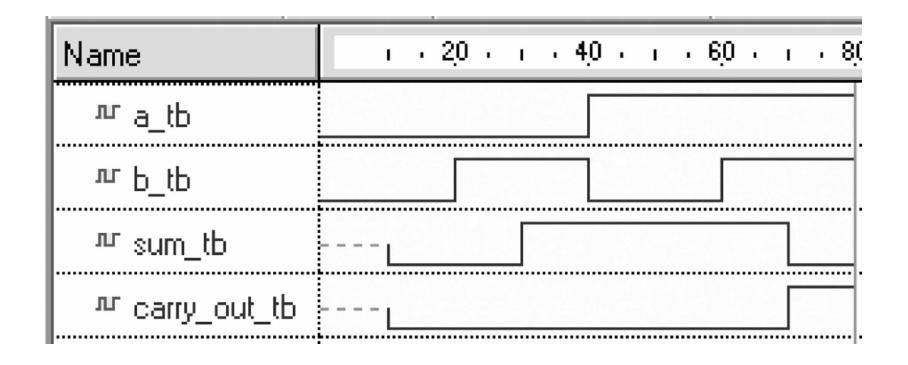


PLD (unprogrammed)

Programmed for half-adder

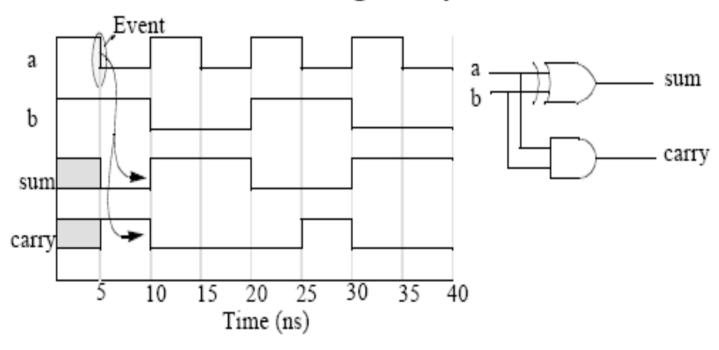


Technology independent view of RTL half-adder synthesized from Boolean equations



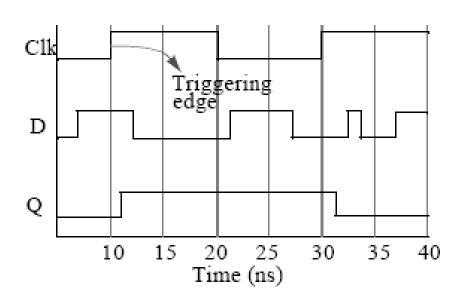
Timing simulation output of half-adder

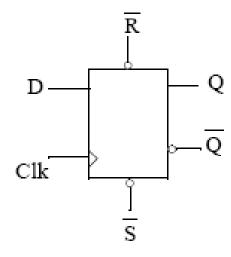
Attributes of Digital Systems



- Digital systems are about signals and their values
- Events, propagation delays, concurrency
- Time ordered sequence of events produces a waveform

Attributes of Digital Systems: Timing

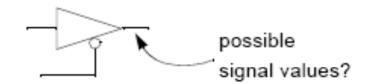




- Timing: computation of events takes place at specific points in time
- Need to "wait for" an event: in this case the clock
- Timing is an attribute of both synchronous and asynchronous systems

Attributes of Digital Systems: Signal Values

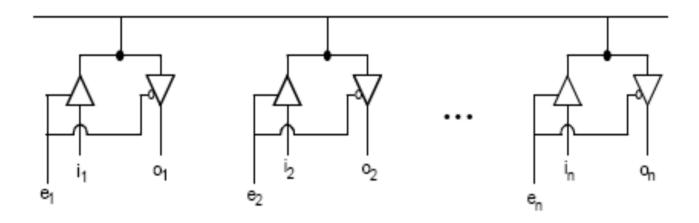
We associate logical values with the state of a signal



Signal Values: IEEE 1164 Value System

Value	Interpretation	
U	Uninitialized	
X	Forcing Unknown	
0	Forcing 0	
1	Forcing 1	
Z	High Impedance	
W	Weak Unknown	
L	Weak 0	
H	Weak 1	
-	Don't Care	

Attributes of Digital Systems: Shared Signals

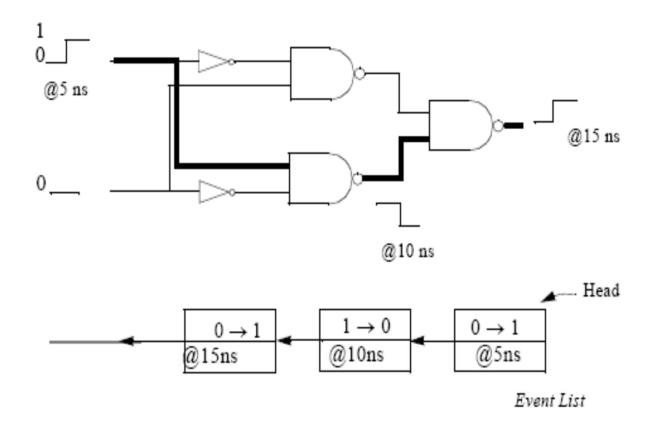


- Shared Signals
 - multiple drivers
- How is the value of the signal determined?
 - arbitration protocols
 - wired logic

Execution Models for VHDL Programs

- Two classes of execution models govern the application of VHDL programs
- Simulation
 - discrete event simulation
 - understanding is invaluable in debugging programs
- Synthesis
 - inference of hardware
 - a function of the building blocks used for implementation

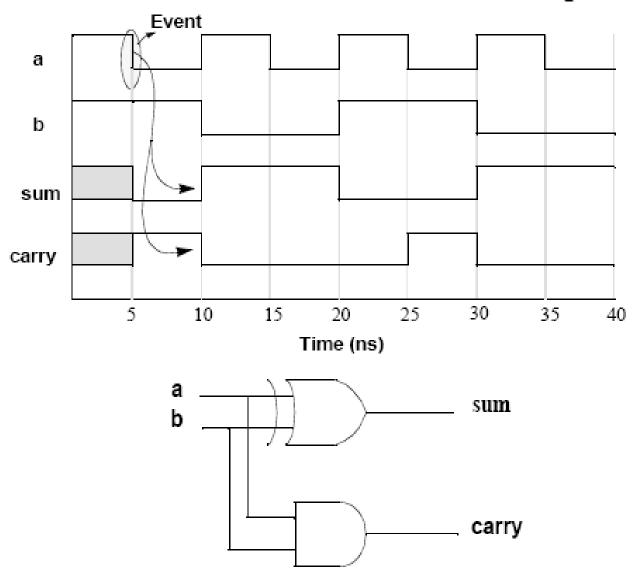
Simulation of Digital Systems



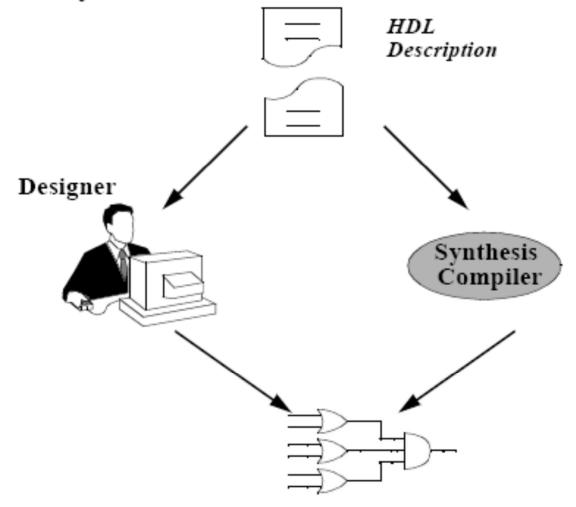
- Digital systems propagate events
- Discrete event simulations manage the generation and recording of events

Introduction- P. 15

Discrete Event Simulation: An Example



Synthesis and Hardware Inference



Both processes can produce very different results!