EE4620L/6620L, CEG4324L/6324L

Digital Integrated Circuit Design with PLDs and FPGAs

Henry Chen / Russ 325 / henry.chen@wright.edu **Summer 2024**

Lab TA: Bilal Abdulhamed < abdulhammed.2@wright.edu>

Lab Sessions

Tue	**2:00 - 4:00 pm**	Russ 434
Thur	**2:00 - 4:00 pm**	Russ 434

TA Office Hours

Mon	**2:00 - 3:00 pm**	Russ 434
Wed	**2:00 - 3:00 pm**	Russ 434
Fri	**2:00 – 3:00 pm**	Russ 434

Course Description
The lab covers the modeling of digital systems using VHSIC hardware description language (VHDL). Designs will be implemented and tested on field-programmable gate arrays (FPGAs). The course covers combinational, synchronous sequential, and pipeline digital circuits. The course is broken into labs and project. Students are required to demonstrate each lab and project. Prerequisite: EE 2010 and EE 2010L.

Software: Xilinx Vivado.

Hardware: FPGA development board, ZedBoard.

Course Learning Objectives
Student will:

- Understand digital design with behavioral hardware description language (VHDL)
- Understand VHDL based digital design flow to include: design, simulation (test), and synthesis
- Understand FPGA programmable hardware to include: logic units (PLBs) and routing resources
- Understand FPGA configuration memory and types of configuration memory
- Understand how a FPGA is programmed
- Understand commercial CAD tools and design flow for mapping circuit to FPGAs
- Understand basic concepts and steps related to mapping circuits to FPGAs
- Design circuits and systems for FPGA implementation
- Simulate circuits during the design process to include: design, mapping, and post-PAR
- Download and demonstrate circuits on a FPGA

Lab/Project

Week 1 Tutorial and Lab 0: Xilinx Vivado Simulation Environment Using VHDL and Testbench
(Lab 0 *Due: Lab Pilot Dropbox by **11:30 pm, Sunday, 5/12/2024***)
Week 2 Lab 1: Combinational Circuit Design, Simulation, and Test in FPGA
(Lab 1 *Due: Lab Pilot Dropbox by **11:30 pm, Sunday, 5/19/2024***)

Week 3	Lab 2: Sequential Circuit Design, Simulation, and Test in FPGA (Lab 2 *Due: Lab Pilot Dropbox by* ***11:30 pm, Sunday, 5/26/2024***)
Week 4	Lab 3: Booth Multiplier and Hardware Security in FPGA (Lab 3 *Due: Lab Pilot Dropbox by* ***11:30 pm, Sunday, 6/2/2024***)
Week 5	Project: Synchronous Pipeline Circuit Design, Simulation, and Test in FPGA
Week 6	Project: Synchronous Pipeline Circuit Design, Simulation, and Test in FPGA (Project *Due: Lab Pilot Dropbox by* ***11:30 pm, Tuesday, 6/12/2024***)

Grading: Letter grade (ABCDF).

EE4620L/CEG4324L		**EE6620L/CEG6324L**	
Lab 0	50 pts	Lab 0	50 pts
Lab 1	100 pts	Lab 1	100 pts
Lab 2	100 pts	Lab 2	100 pts
Lab 3	100 pts	Lab 3	100 pts
Project	150 pts	Project*	200 pts
TOTAL	500 pts	TOTAL	550 pts

***EE6620L/CEG6324L student must complete the additional assigned project in FPGA, which has greater depth than the project of the undergraduate student.**

Note: All the lab exercises must be performed individually unless explicitly mentioned as a group project. The final grade scale will be determined late in the semester. The tentative grading scale is shown below:

EE4620/CEG4324: 500 pts = 100%
EE4620/CEG4324: 550 pts = 100%

A for an overall score equal to or above 90%
B for an overall score between 80% and less than 90%
C for an overall score between 70% and less than 80%
D for an overall score between 60% and less than 70%
F for an overall score of less than 60%

Labs/Project Policies:
It is a violation of the honor code for students to submit their work or documents, which are not the result of their labor and thoughts. It is a violation of the honor code for students who fail to report observed violations by other students. For each assignment that is not explicitly assigned as a group effort, ***each student must write and sign the honor pledge on the lab/project report's front cover page.***

"I have never given nor received aid on this assignment, nor have I observed any violation of the Honor Code."

Consequences of violations:
Failure to strictly adhere to the honor code will result in the submission of an academic integrity violation to the office of Judicial Affairs, and may result in: a grade of '**0'** in the assignment or project; a grade of "**F**" for the course; or dismissal from the university.

Late lab/project reports: Will be deducted by **10%** of total marks per day.

Attendance: In the lab, attendance is mandatory. **If you arrive after the sign-in sheet has gone around, it will count as absent; if you leave early, it will count as an absence**. **Missing three lab sessions will result in the student earning an "F" for this lab course. Signing someone else into class counts as a violation of the student code of conduct and will automatically fail the course.**

Student Learning Outcomes:
Students who successfully complete the course can:

1. Identify, formulate, and solve complex engineering problems by applying principles of engineering, science, and mathematics
2. Develop and conduct appropriate experimentation, analyze and interpret data, and use engineering judgment to draw conclusions