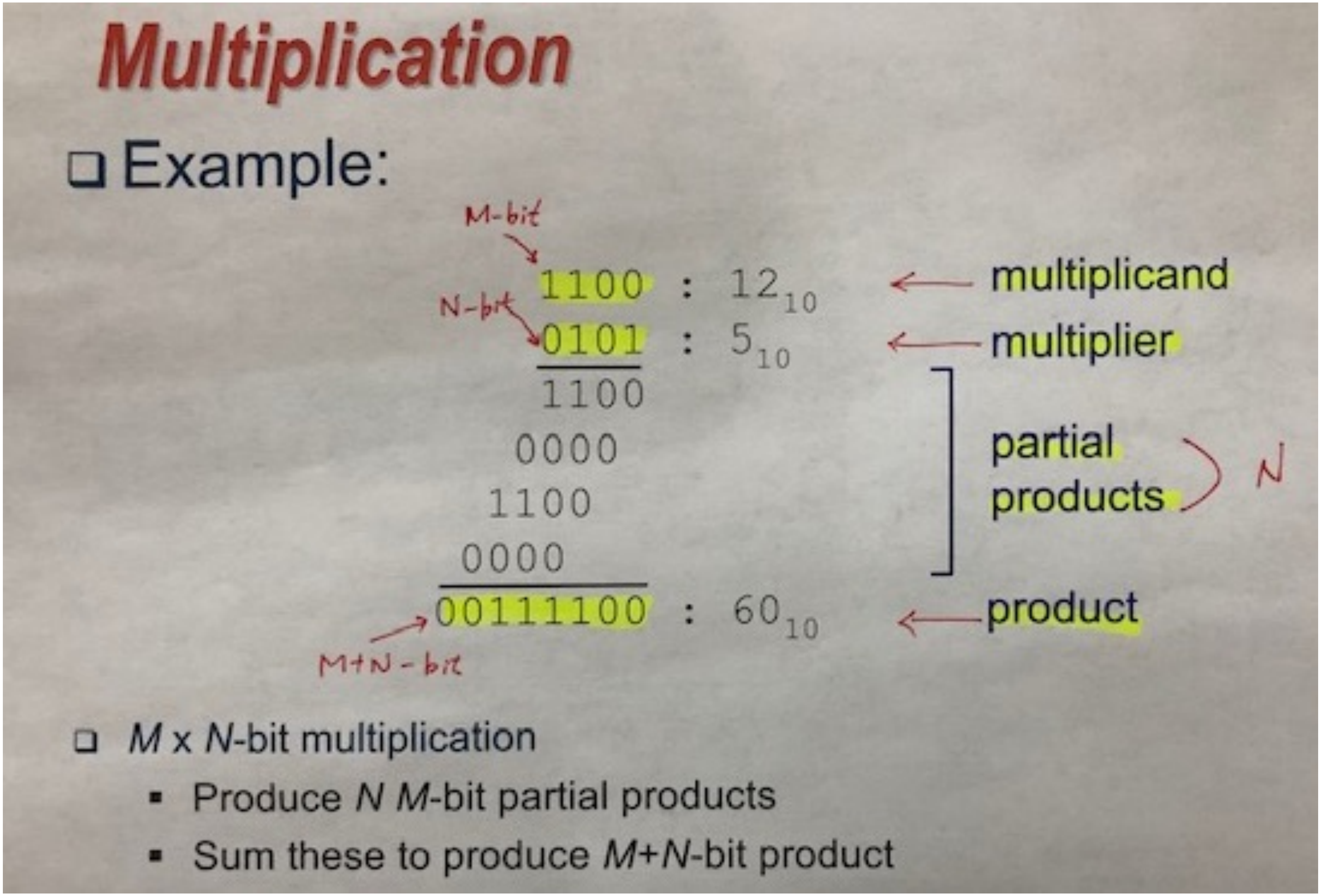
Booth Multiplier



Multiplication

- Example:

M-bit

N-bit

$$\begin{array}{rl}
1100 & : \ 12_{10} \\
0101 & : \ 5_{10} \\
\hline
1100 & \\
0000 & \\
1100 & \\
0000 & \\
\hline
00111100 & : \ 60_{10}
\end{array}$$

M+N-bit

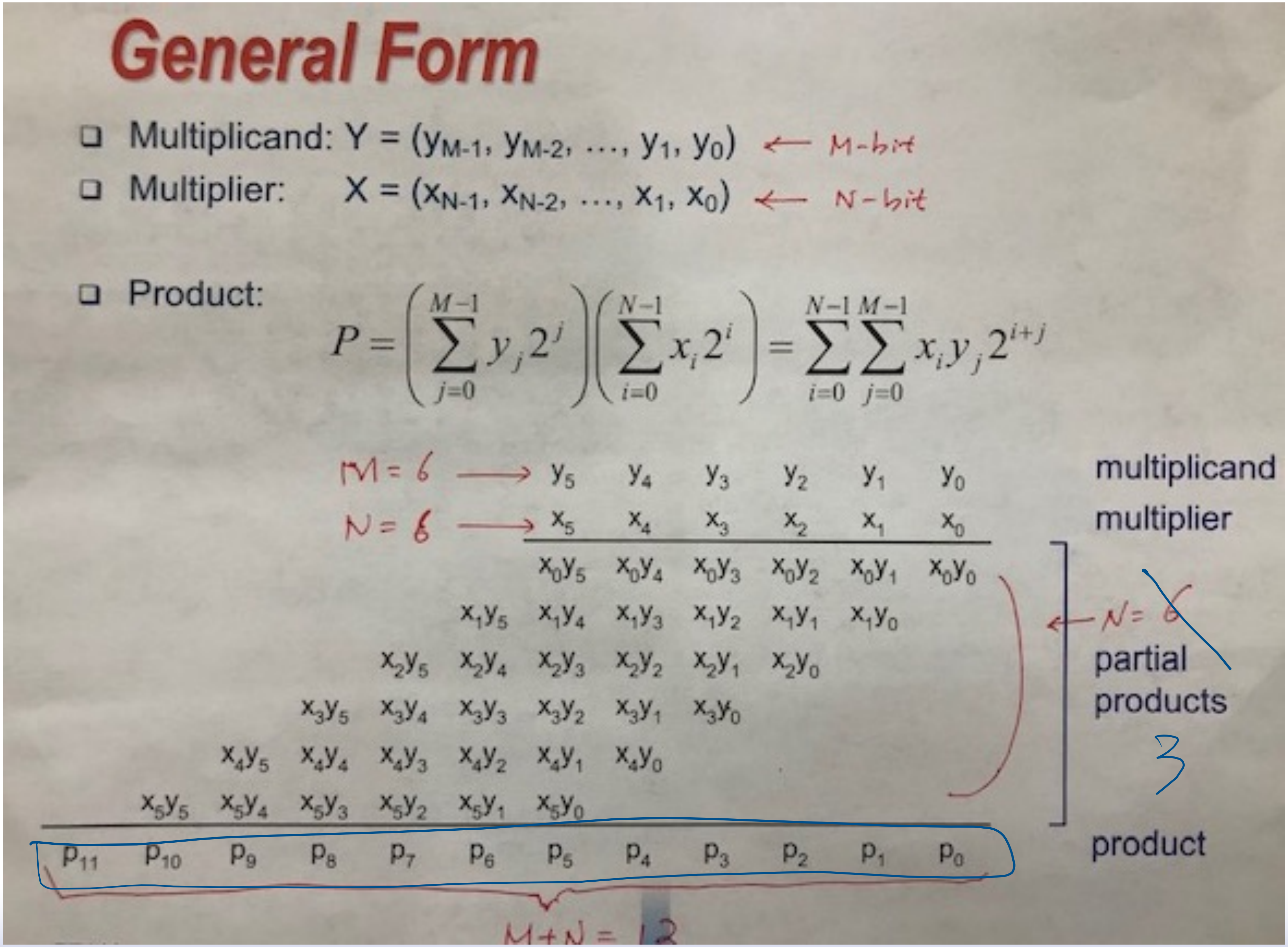
← multiplicand

← multiplier

partial products } N

← product

- M x N-bit multiplication
  - Produce N M-bit partial products
  - Sum these to produce $M+N$-bit product



General Form

- Multiplicand: Y = (y_{M-1}, y_{M-2}, …, y_1, y_0) ← M-bit
- Multiplier: X = (x_{N-1}, x_{N-2}, …, x_1, x_0) ← N-bit
- Product:

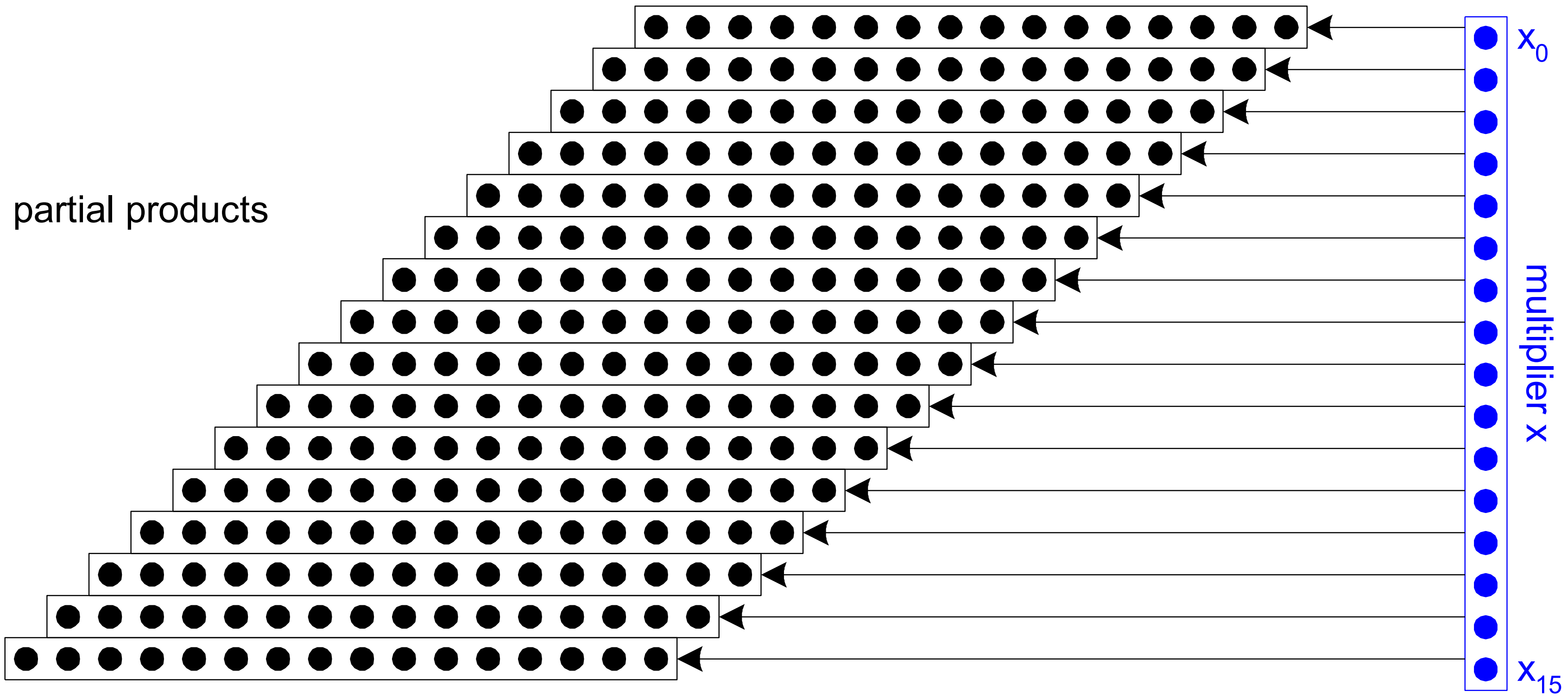
$$P = \left(\sum_{j=0}^{M-1} y_j 2^j\right)\left(\sum_{i=0}^{N-1} x_i 2^i\right) = \sum_{i=0}^{N-1}\sum_{j=0}^{M-1} x_i y_j 2^{i+j}$$

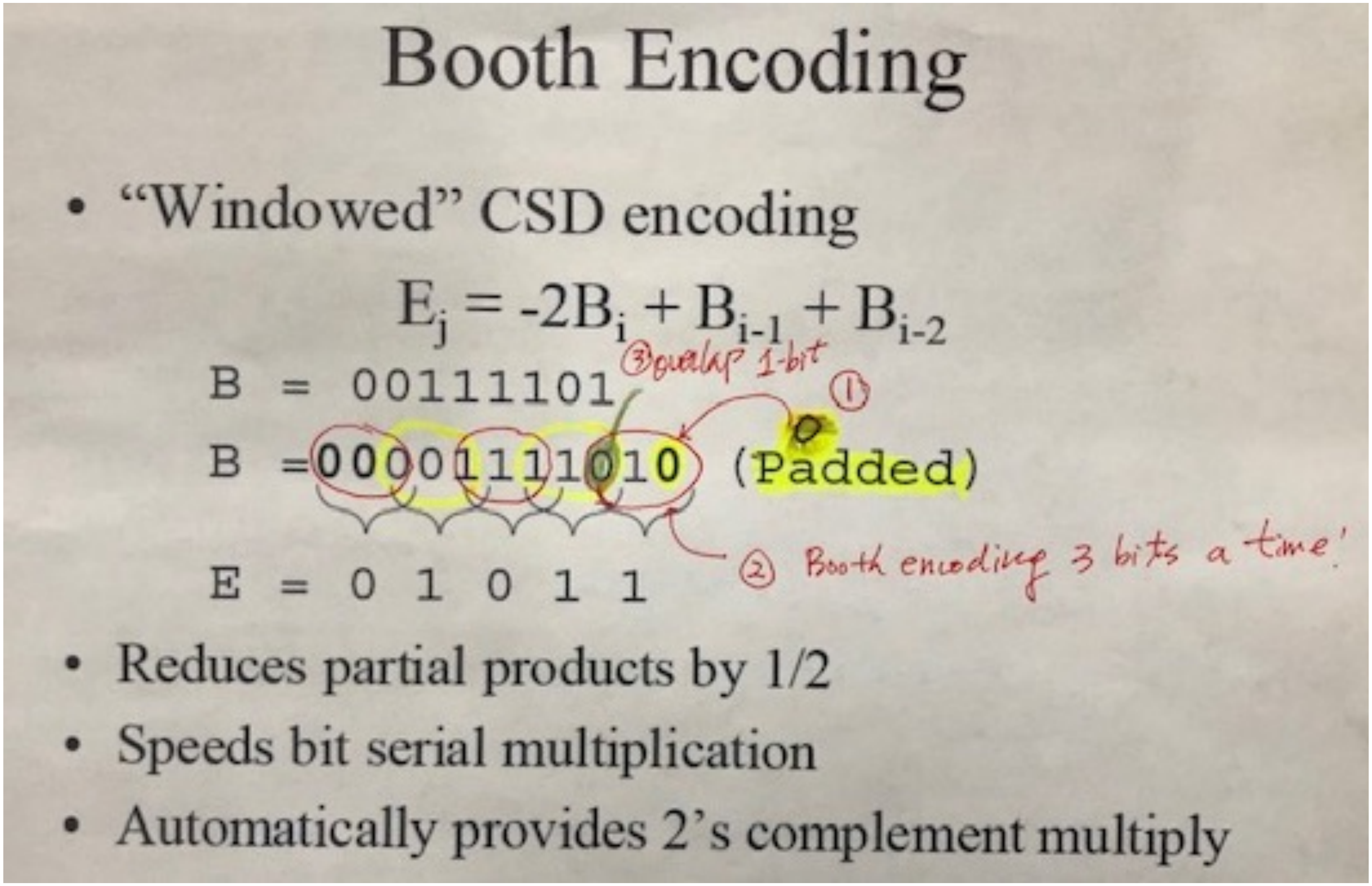
				M = 6	→	y_5	y_4	y_3	y_2	y_1	y_0	multiplicand
				N = 6	→	x_5	x_4	x_3	x_2	x_1	x_0	multiplier
						x_0y_5	x_0y_4	x_0y_3	x_0y_2	x_0y_1	x_0y_0	
					x_1y_5	x_1y_4	x_1y_3	x_1y_2	x_1y_1	x_1y_0		← N = ~~6~~
				x_2y_5	x_2y_4	x_2y_3	x_2y_2	x_2y_1	x_2y_0			partial
			x_3y_5	x_3y_4	x_3y_3	x_3y_2	x_3y_1	x_3y_0				products
		x_4y_5	x_4y_4	x_4y_3	x_4y_2	x_4y_1	x_4y_0					3
	x_5y_5	x_5y_4	x_5y_3	x_5y_2	x_5y_1	x_5y_0						
p_{11}	p_{10}	p_9	p_8	p_7	p_6	p_5	p_4	p_3	p_2	p_1	p_0	product

M+N = 12

16X16 Mult. Dot Diagram

- Each dot represents a bit





Booth Encoding

- “Windowed” CSD encoding

$$E_j = -2B_i + B_{i-1} + B_{i-2}$$

```
B = 00111101
B = 00001111010 (Padded)
E =  0 1 0 1 1
```

③ overlap 1-bit

① 0

② Booth encoding 3 bits a time!

- Reduces partial products by 1/2
- Speeds bit serial multiplication
- Automatically provides 2’s complement multiply

Booth actions

$y_i\ y_{i-1}\ y_{i-2}$	increment
0 0 0	0
0 0 1	x
0 1 0	x
0 1 1	2x
1 0 0	-2x
1 0 1	-x
1 1 0	-x
1 1 1	0

Booth example Algorithm

- $x = 011001\ (25_{10})$, $y = 101110\ (-18_{10})$.
- $y_1y_0y_{-1} = 100$, $P_1 = P_0 - (10 \cdot 011001) = 11111001110$.
- $y_3y_2y_1 = 111$, $P_2 = P_1 + 0 = 11111001110$.
- $y_5y_4y_3 = 101$, $P_3 = P_2 - 0110010000 = 11000111110$.

y_i y_{i-1} y_{i-2}	increment
0 0 0	0
0 0 1	x
0 1 0	x
0 1 1	2x
1 0 0	-2x
1 0 1	-x
1 1 0	-x
1 1 1	0

Hardware Bit Operation
Step 0: 0 padding

x = 011001 (25_{10}), y = 101110 (-18_{10}).

Hardware Bit Operation
Step 1: First 3 bits Y (100) booth encoding

x = 011001 (25_{10}), y = 101110 (-18_{10}).

y_i y_{i-1} y_{i-2}	increment
0 0 0	0
0 0 1	x
0 1 0	x
0 1 1	2x
1 0 0	-2x
1 0 1	-x
1 1 0	-x
1 1 1	0

Hardware Bit Operation
Step 2: Next 3 bits Y (111) booth encoding

x = 011001 (25_{10}), y = 101110 (-18_{10}).

y_i y_{i-1} y_{i-2}	increment
0 0 0	0
0 0 1	x
0 1 0	x
0 1 1	2x
1 0 0	-2x
1 0 1	-x
1 1 0	-x
1 1 1	0

Hardware Bit Operation
Step 3: Next 3 bits Y (101) booth encoding

x = 011001 (25_{10}), y = 101110 (-18_{10}).

y_i y_{i-1} y_{i-2}	increment
0 0 0	0
0 0 1	x
0 1 0	x
0 1 1	2x
1 0 0	-2x
1 0 1	-x
1 1 0	-x
1 1 1	0