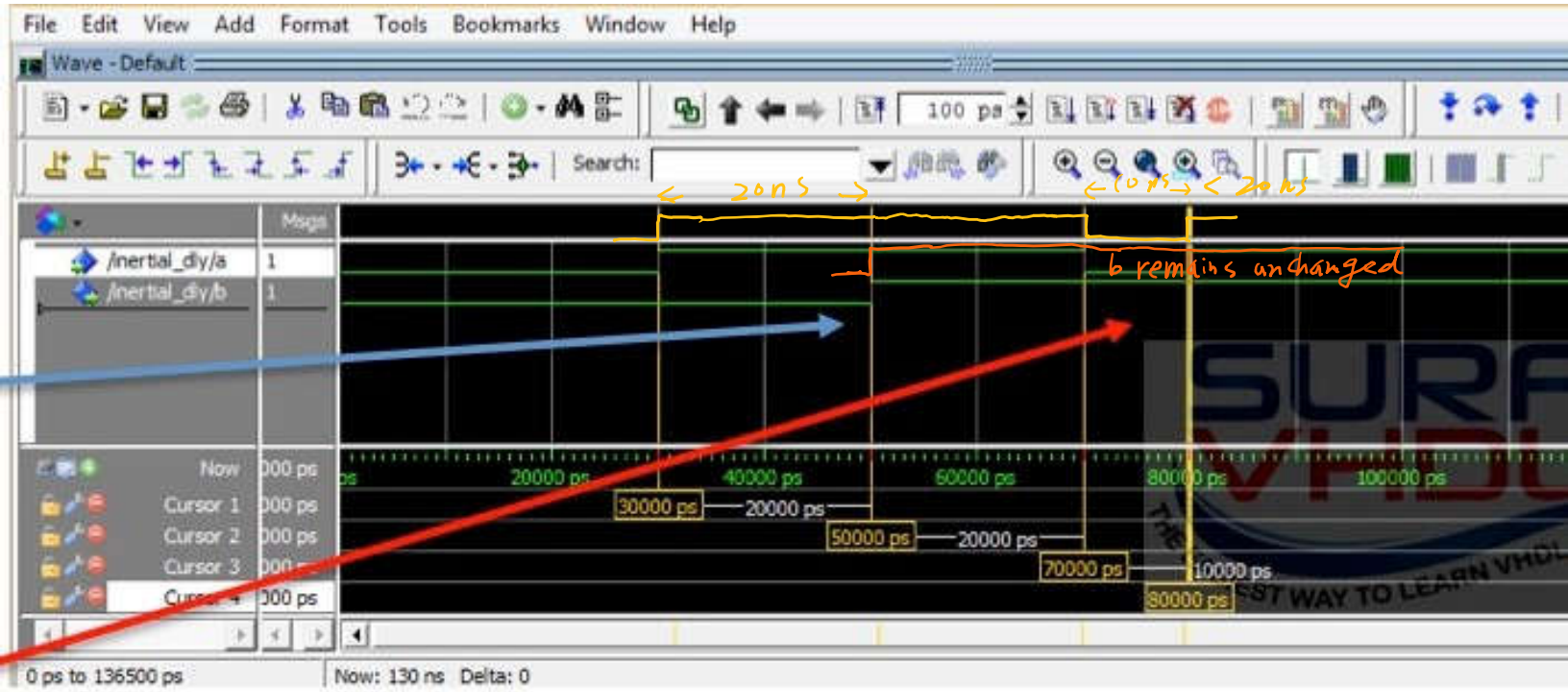
The **inertial delay** model is the default delay implemented in VHDL because it's behavior is very similar to the delay of the device. The delay assignment syntax is:

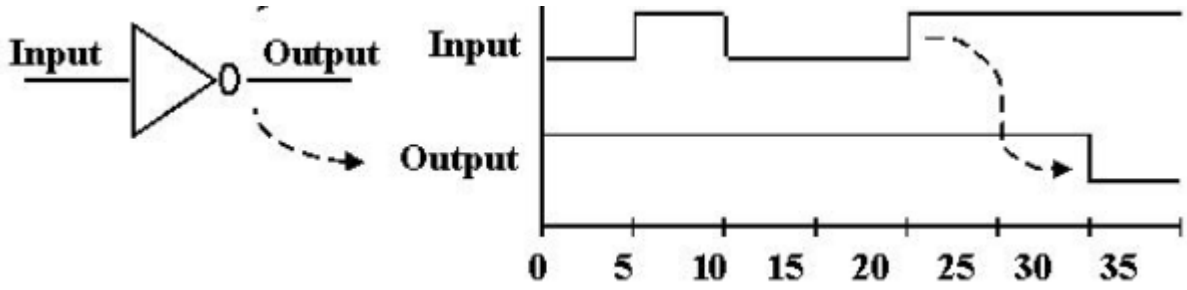
b <= a **after** 20 ns;

In this example **b** take the value of **a** **after** 20 ns second of inertial delay.

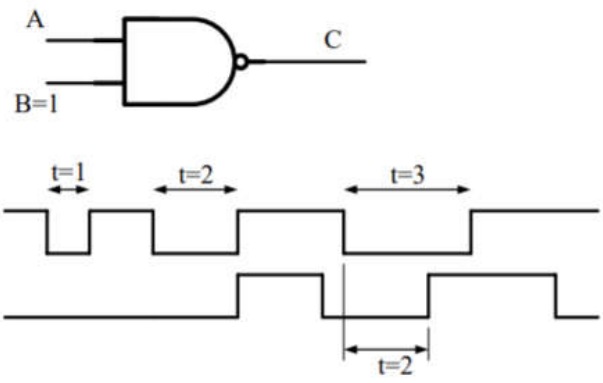
This means that if a value varies **faster** than 20 ns then **b** remain **unchanged**. This simulation should clarify the concept.



Example: Output <= NOT Input after 10 ns

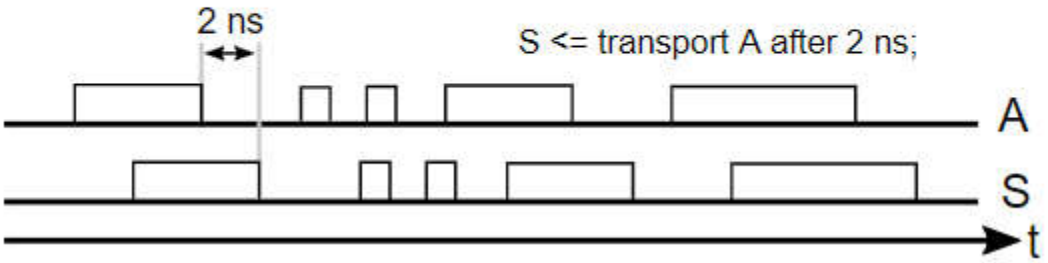


Example:



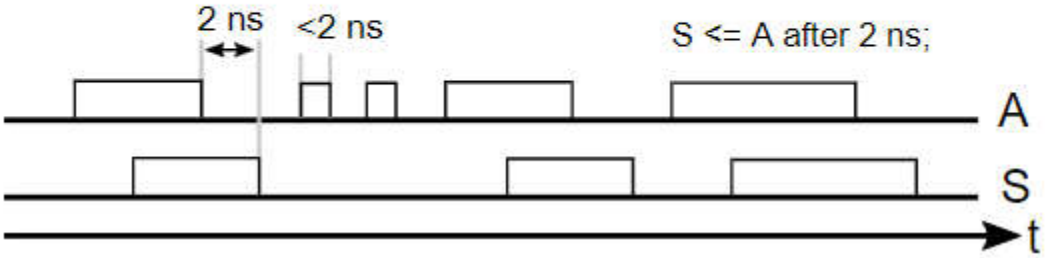
Transport delay:

- models the current flow through a wire (everything is transferred)



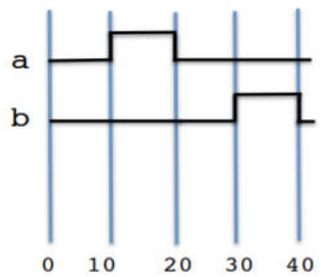
Inertial delay: (default delay mechanism)

- models spike-proof behavior → a value is transferred only if it is active for at least 2 ns



Example:

```
ARCHITECTURE beh OF delay_line
BEGIN
  b <= TRANSPORT a AFTER 20 ns;
END beh;
```




```
ARCHITECTURE beh OF buf
BEGIN
  b <= a AFTER 20 ns;
END beh;
```