WRIGHT STATE UNIVERSITY

EE4620/6620, CEG4324/6324
Digital Integrated Circuit Design
with PLDs and FPGAs

Lab 0 (Summer 2024)

Xilinx Vivado Simulation Environment Using VHDL and Testbench

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A. Introduction

The main objective of this lab is for you to become familiar with the Xilinx Vivado simulation environment. Read all directions carefully. You will follow the Vivado tutorial to create a VHDL project in Xilinx Vivado and functionally verify and validate your design through Vivado simulation environment. Read through all of the steps before you begin the lab.

B. Create a Project

1. In this lab, the VHDL design code (comb_function.vhd) describes a combinational circuit with three inputs, A, B, and C, and two outputs, F and G.

```
 --  A B C  |  F  G
 ----------------------
 --   0  0  0  |  1  0
 --   0  0  1  |  1  0
 --   0  1  0  |  0  0
 --   0  1  1  |  0  1
 --   1  0  0  |  0  1
 --   1  0  1  |  0  0
 --   1  1  0  |  1  0
 --   1  1  1  |  1  0
```

   Note the synthesis off and on comment lines. These lines turn the circuit synthesizer OFF and ON, so it skips the code in between. The timing simulation information is not synthesized, only for simulation purposes. **For this example circuit, we use unit delays of 1 ns for all logic gate function, i.e., INV, AND, NAND, OR, NOR, etc.**

2. Simulate the design code from part 1. Look at the test bench file, tb_comb_function.vhd. In this file, you see the test bench code for simulating a simple three input combinational function. It exhaustively simulates the functionality of the circuit. It uses a generic set at the beginning of the file, i.e., WPD (Worst Propagation Delay) = **2 ns**, to set the amount of time that each vector is applied to the circuit. Follow the Vivado tutorial to simulate the design (comb_function.vhd) using the test bench file (tb_comb_function.vhd). Verify your simulation waveform if there are any simulation errors. Note: It takes time to simulate circuits with more inputs exhaustively.
3. Generate bitstream, program the ZedBoard, and load your design onto the FPGA board. Follow TA's instruction to verify your FPGA design by switching inputs and demonstrating your outputs from on-board OLED.

C. Report [50 pts] (Submitted to your Lab Pilot Dropbox by 11:30 pm, Sunday, May 12, 2024)

1. [10 pts] Set WPD = 2 ns in the tb_comb_function.vhd. Simulate the comb_function.vhd design. Mark on your simulation waveform if there are any simulation errors. Explain why these errors are.
2. [10 pts] Set WPD = 4 ns in the tb_comb_function.vhd. Simulate the comb_function.vhd design. Mark on your simulation waveform if there are any simulation errors. Explain why these errors are.
3. [30 pts] Consider a new truth table

```
-- A B C | F  G
----------------------
--  0 0 0 | 1  0
--  0 0 1 | 1  1
--  0 1 0 | 0  0
--  0 1 1 | 0  1
--  1 0 0 | 1  1
--  1 0 1 | 0  1
--  1 1 0 | 0  0
--  1 1 1 | 1  0
```

Write your new VHDL design code (*new_comb_function.vhd*) describing a combinational circuit with three inputs, A, B, and C, and two outputs, F and G. Use K-map to optimize your design.

- Set WPD = 2 ns in the tb_comb_function.vhd. Simulate the *new_comb_function.vhd* design. Mark on your simulation waveform if there are any simulation errors. Explain why these errors are.
- Set WPD = 4 ns in the tb_comb_function.vhd. Simulate the *new_comb_function.vhd* design. Mark on your simulation waveform if there are any simulation errors. Explain why these errors are.
- Submit your VHDL design code and simulation waveforms.