1. Write VHDL code to implement the function expressed in the following truth table.

A	B	C	F
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

    a) Use *concurrent VHDL code* (Boolean expression)

```
entity function_F is
        port ( A,B,C : in std_logic;
                F : out std_logic);
end function_F;

architecture concurrent of function_F is
begin




end concurrent;
```

    b) Use *if* statement

```
entity function_F is
        port ( A,B,C : in std_logic;
                F : out std_logic);
end function_F;

architecture behavior_1 of function_F is
begin
proc1: process(A,B,C)
```

```
        end process proc1;
end behavior_1;
```