Component Instantiation using GENERATE (II)

Example: 16-to-1 Mux

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ARCHITECTURE Structure OF Example1 IS

    COMPONENT mux4to1
        PORT (   w0, w1, w2, w3     : IN     STD_LOGIC ;
                 s                  : IN     STD_LOGIC_VECTOR(1 DOWNTO 0) ;
                 f                  : OUT    STD_LOGIC ) ;
    END COMPONENT ;

    SIGNAL m : STD_LOGIC_VECTOR(0 TO 3) ;

BEGIN
    G1: FOR i IN 0 TO 3 GENERATE
        Muxes: mux4to1 PORT MAP (
                 w(4*i), w(4*i+1), w(4*i+2), w(4*i+3), s(1 DOWNTO 0), m(i) ) ;
    END GENERATE ;
    Mux5: mux4to1 PORT MAP ( m(0), m(1), m(2), m(3), s(3 DOWNTO 2), f ) ;
END Structure ;
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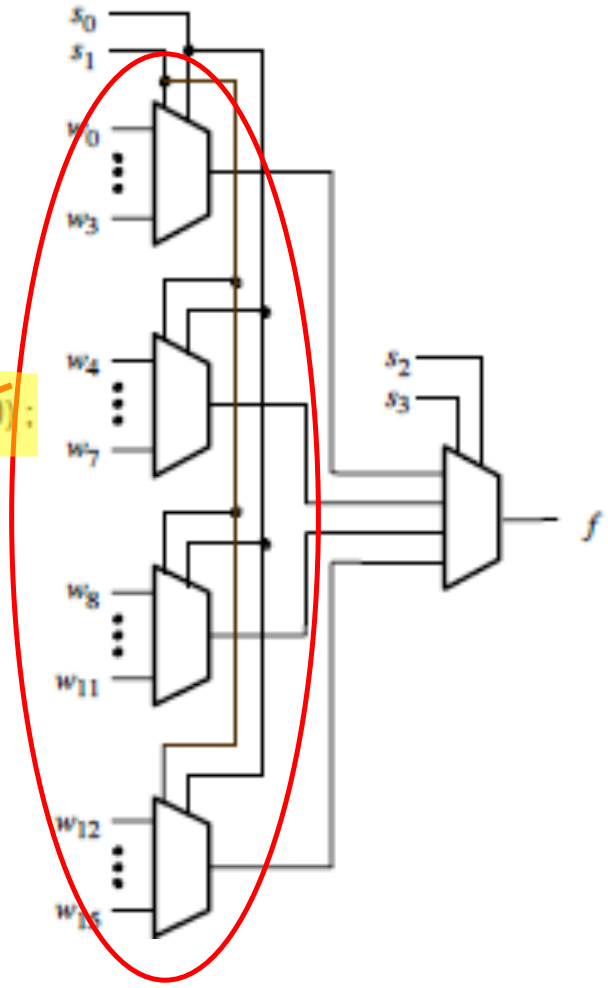
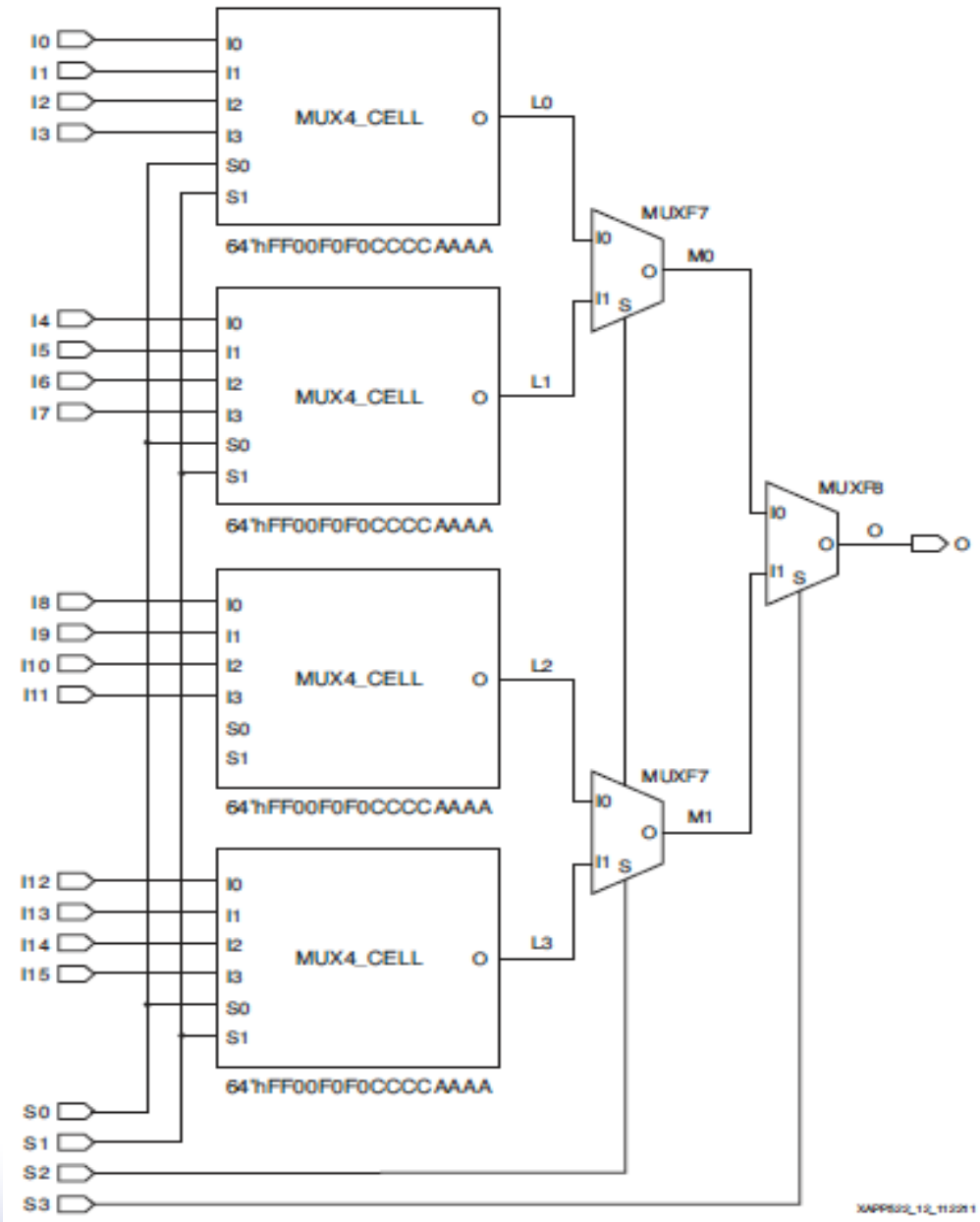


Example: 16-to-1 Mux

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ENTITY MUX16_CELL IS
        PORT (I : IN STD_LOGIC_VECTOR(0 TO 15) ;
              S : IN STD_LOGIC_VECTOR(0 TO 3) ;
              O : OUT STD_LOGIC ) ;
END MUX16_CELL;

ARCHITECTURE generate_structure OF MUX16_CELL IS

 -- Component declarations
 component MUX2_CELL

              port (I0, I1, S: in std_logic;
                    O: out std_logic);
 end component;

 component MUX4_CELL
              port (I0, I1, I3, I4, S0, S1: in std_logic;
                    O: out std_logic);
 end component;

 -- Declaration of signals used to interconnect gates

 SIGNAL L : STD_LOGIC_VECTOR(0 TO 3) ;
 SIGNAL M : STD_LOGIC_VECTOR(0 TO 1) ;

 BEGIN
        G1: FOR i IN 0 TO 3 GENERATE
              Muxes: MUX4_CELL PORT MAP (
                    I(4*i), I(4*i+1), I(4*i+2), I(4*i+3), S(0), S(1), L(i) ) ;
        END GENERATE ;

        Mux5: MUX2_CELL PORT MAP (L(0), L(1), S(2), M(0) ;
        Mux6: MUX2_CELL PORT MAP (L(2), L(3), S(2), M(1) ;
        Mux7: MUX2_CELL PORT MAP (M(0), M(1), S(3), O) ;

END generate_structure ;
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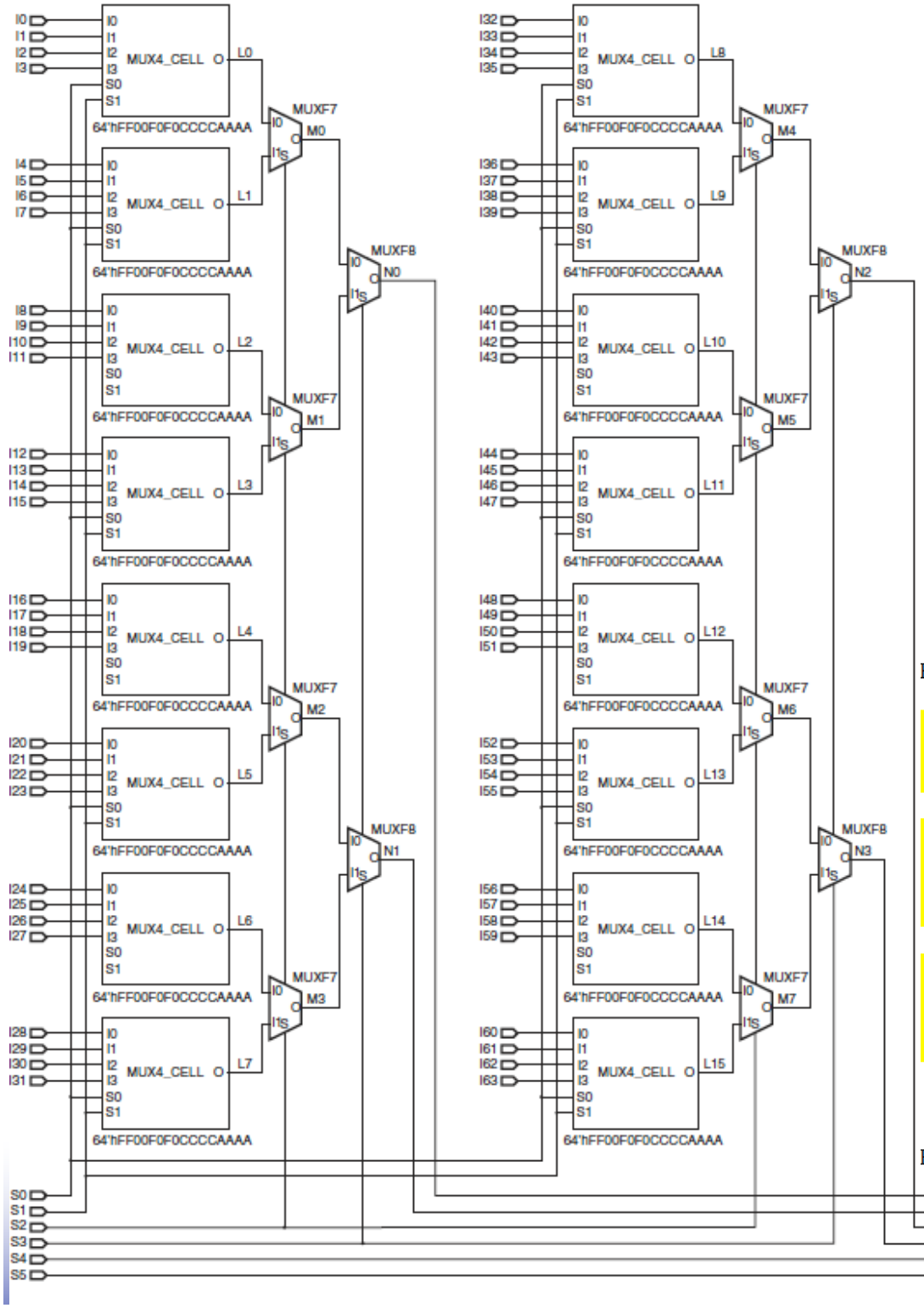


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ENTITY MUX64_CELL IS
        PORT (I : IN STD_LOGIC_VECTOR(0 TO 63) ;
                S : IN STD_LOGIC_VECTOR(0 TO 5) ;
                O : OUT STD_LOGIC ) ;
END MUX16_CELL;

ARCHITECTURE generate_structure OF MUX64_CELL IS

 -- Component declarations
 component MUX2_CELL
                port (I0, I1, S: in std_logic;
                        O: out std_logic);
 end component;

 component MUX4_CELL
                port (I0, I1, I3, I4, S0, S1: in std_logic;
                        O: out std_logic);
 end component;

 -- Declaration of signals used to interconnect gates

 SIGNAL L : STD_LOGIC_VECTOR(0 TO 15) ;
 SIGNAL M : STD_LOGIC_VECTOR(0 TO 7) ;

BEGIN
        G1: FOR i IN 0 TO 15 GENERATE
                Muxes: MUX4_CELL PORT MAP (
                        I(4*i), I(4*i+1), I(4*i+2), I(4*i+3), S(0), S(1), L(i) ) ;
        END GENERATE ;

        G2: FOR i IN 0 TO 7 GENERATE
                Muxes1: MUX2_CELL PORT MAP (
                        L(2*i), I(2*i+1), S(2), M(i) ) ;
        END GENERATE ;

        G3: FOR i IN 0 TO 3 GENERATE
                Muxes2: MUX2_CELL PORT MAP (
                        M(2*i), M(2*i+1), S(3), N(i) ) ;
        END GENERATE ;

        Mux29: MUX4_CELL PORT MAP (N(0), N(1), N(2), N(3), S(4), S(5), O) ;

END generate_structure ;
```