1. Write VHDL code to implement the function expressed in the following truth table.

A	B	C	F
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	x
1	1	0	x
1	1	1	0

Use ***case*** statement.

```
entity function_F is
        port ( A,B,C : in std_logic;
                F : out std_logic);
end function_F;

architecture behavior_2 of function_F is
        signal ABC: std_logic_vector(2 downto 0);
begin




end process my_proc;
```