1. Design of 4-bit binary comparator using IF-ELSE statements

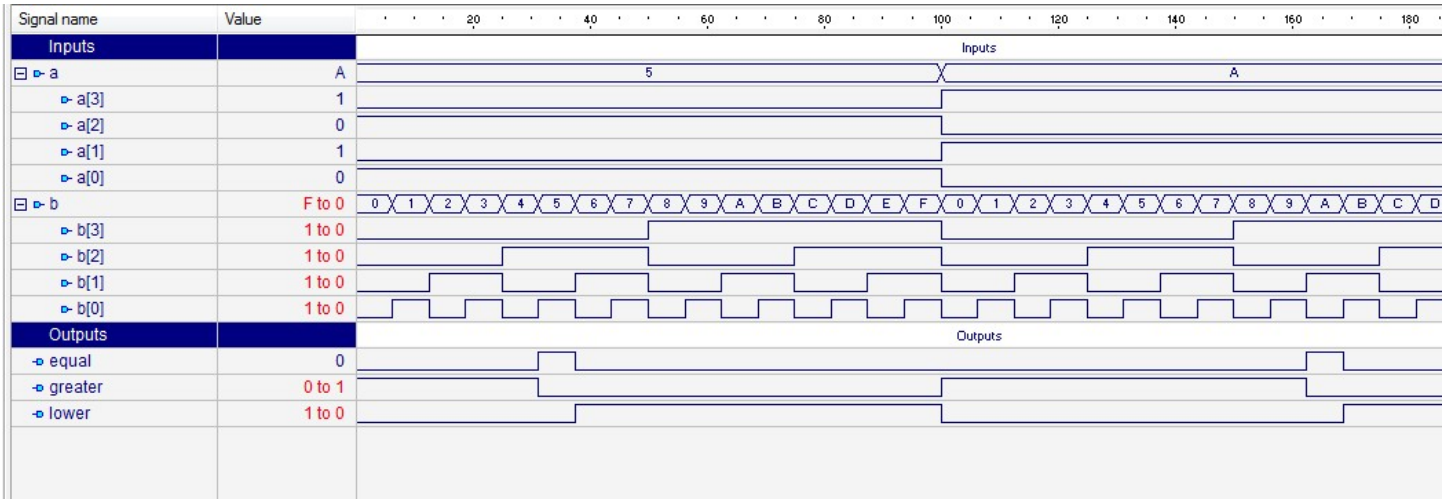
```
library IEEE;
use IEEE.STD_LOGIC_1164.all;

entity comparator_4bit is
    port(
       a : in STD_LOGIC_VECTOR(3 downto 0);
       b : in STD_LOGIC_VECTOR(3 downto 0);
       equal : out STD_LOGIC;
       greater : out STD_LOGIC;
       lower : out STD_LOGIC
       );
end comparator_4bit;


architecture comparator_4bit_arc of comparator_4bit is
begin

   comparator : process (a,b) is
   begin
      if (a=b) then
         equal <= '1';
         greater <= '0';
         lower <= '0';
      elsif (a<b) then
         equal <= '0';
         greater <= '0';
         lower <= '1';
      else
         equal <= '0';
         greater <= '1';
         lower <= '0';
      end if;
   end process comparator;

end comparator_4bit_arc;
```



2. Design of 4-bit binary parallel adder using FOR-LOOP statements

```
library IEEE;
use IEEE.STD_LOGIC_1164.all;

entity adder_4 is
    port(
       a : in STD_LOGIC_VECTOR(3 downto 0);
       b : in STD_LOGIC_VECTOR(3 downto 0);
       cin : in STD_LOGIC;
       sum : out STD_LOGIC_VECTOR(3 downto 0);
       cout : out STD_LOGIC);
end adder_4;


architecture adder4_arc of adder_4 is
begin

   adder4 : process (a,b, cin)
   variable temp_carry : std_logic;
   begin
      temp_carry := cin;
      for i in 0 to 3 loop
         sum(i) <= a(i) xor b(i) xor temp_carry ;
         temp_carry := (a(i) and b(i)) or (b(i) and temp_carry) or (temp_carry and a(i));
      end loop;
      cout <= temp_carry;
   end process;

end adder4_arc;
```