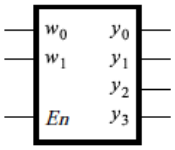
1.

a) The graphical symbol and truth table of a 2-to-4 decoder is shown below.

En	w_1	w_0	y_0	y_1	y_2	y_3
1	0	0	1	0	0	0
1	0	1	0	1	0	0
1	1	0	0	0	1	0
1	1	1	0	0	0	1
0	x	x	0	0	0	0

(a) Truth table



(b) Graphical symbol

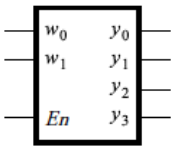
Complete the behavioral VHDL of 2-to-4 decoder (entity named **dec2to4**) using **IF-THEN-ELSE only.**

```
ENTITY dec2to4 IS
    PORT ( w : IN STD LOGIC VECTOR(1 DOWNTO 0) ;
           En : IN STD LOGIC ;
           y : OUT STD LOGIC VECTOR(0 TO 3) ) ;
END dec2to4 ;

ARCHITECTURE Behavior OF dec2to4 IS

BEGIN

    --- use IF-THEN-ELSE only ----




END Behavior ;
```

b) The graphical symbol and truth table of a 2-to-4 decoder is shown below.

En	w_1	w_0	y_0	y_1	y_2	y_3
1	0	0	1	0	0	0
1	0	1	0	1	0	0
1	1	0	0	0	1	0
1	1	1	0	0	0	1
0	x	x	0	0	0	0

(a) Truth table

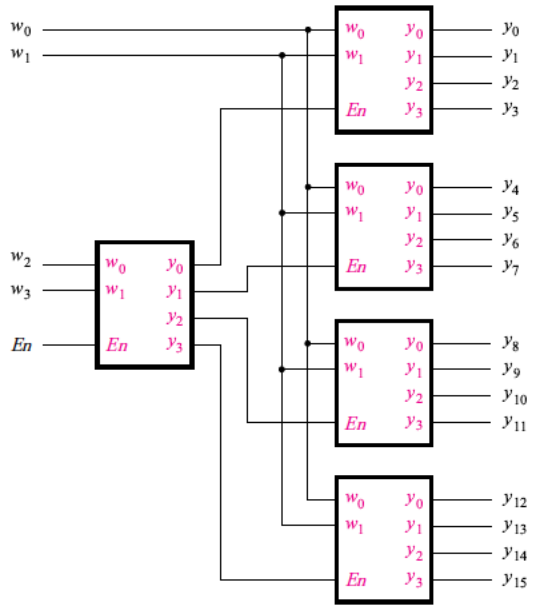


(b) Graphical symbol

Complete the behavioral VHDL of 2-to-4 decoder (entity named **dec2to4**) using IF and then **CASE.**

```
ENTITY dec2to4 IS
    PORT ( w : IN STD LOGIC VECTOR(1 DOWNTO 0) ;
           En : IN STD LOGIC ;
           y : OUT STD LOGIC VECTOR(0 TO 3) ) ;
END dec2to4 ;

ARCHITECTURE Behavior OF dec2to4 IS

BEGIN

    --- use IF and then CASE ----




END Behavior ;
```

c) Complete the behavioral VHDL of 4-to-16 decoder (entity named **dec4to16**).




```
ENTITY dec4to16 IS
      PORT ( w : IN STD LOGIC VECTOR(3 DOWNTO 0) ;
                  En : IN STD LOGIC ;
                  y : OUT STD LOGIC VECTOR(0 TO 15) ) ;
END dec4to16 ;

ARCHITECTURE Structure OF dec4to16 IS

---- component declaration ------

COMPONENT dec2to4
      PORT ( w : IN STD LOGIC VECTOR(1 DOWNTO 0) ;
                  En : IN STD LOGIC ;
                  y : OUT STD LOGIC VECTOR(0 TO 3) ) ;
END COMPONENT ;

---- signal declaration ------

SIGNAL m : STD LOGIC VECTOR(0 TO 3) ;

BEGIN




END Structure ;
```