EE4620/6620, CEG4324/6324

Digital Integrated Circuit Design with PLDs and FPGAs

Henry Chen / henry.chen@wright.edu
Office hours: 1:30-2:30 MTWR (325 Russ)

Summer 2024
11:40-1:20 pm MTWR (154 Russ)

Course Description

This course will provide students with the background needed to design, develop, and test digital circuits using IEEE standard VHSIC Hardware Description Language (VHDL). The course emphasis is placed on top-down design methodology beginning with purely structural VHDL and then behavioral VHDL description. We begin by developing VHDL skills and techniques for designing digital combinational, synchronous sequential, and pipeline circuits. Then, we cover introductory topics in Field Programmable Gate Array (FPGA) circuit design. We study the digital signal processor and FSM controller. We will discuss methods for mapping VHDL design circuits to the programmable logic devices for hardware implementation and verification. The course is lab and project-oriented, providing a good "hands-on" foundation for future digital work. Lab experience will allow the student to design and verify a variety of designs ranging from the simple to the complex. Prerequisite: EE2000 or equivalent.

Course Learning Objectives

Studeny will:

- Understand digital design with behavioral hardware description language (VHDL)
- Understand VHDL based digital design flow to include: design, simulation (test), and synthesis
- Understand FPGA programmable hardware to include: logic units (PLBs) and routing resources
- Understand FPGA configuration memory and types of configuration memory
- Understand how a FPGA is programmed
- Understand commercial CAD tools and design flow for mapping circuit to FPGAs
- Understand basic concepts and steps related to mapping circuits to FPGAs
- Design circuits and systems for FPGA implementation
- Simulate circuits during the design process to include: design, mapping, and post-PAR
- Download and demonstrate circuits on a FPGA

Course Outline

Week 1	Review EE2000, Introduction of Digital Design Using VHDL and PLDs
	Entity, Architecture, and Structural VHDL Modeling
	Prerequisite test : Thursday 05/11/2023 (no make-up)
Week 2	VHDL Signal, Variable, and Data Types
	Behavioral VHDL: Combinational Design
Week 3	Sequential Design/Finite State Machine
	Midterm: Thursday 05/23/2020 (No make-up)
Week 4	Booth Multipliers and Hardware Security in FPGA
Week 5	Synchronous Pipeline Architecture in FPGA
	Subprograms (Function vs. Procedure)
Week 6	Fixed-point number Adder & Multiplier
	Final: Thursday 06/13/2024 (No make-up)

Text (recommended, not required)

- My lecture presentation (drawn from a variety of sources).
- Digital System Design with FPGA: Implementation Using Verilog and VHDL, By Cem Unsalan and Bora Tar, 2017, ISBN: 9781259837906.

Note:

- We will adhere to this syllabus as closely as possible. However, I reserve the right to make changes (in the material covered) as necessary in order to meet timing constraints.

Exam Dates

Prerequisite Quiz	Thursday 05/11/2023
Midterm	Thursday 05/25/2023
Final	Thursday 06/15/2023

Grading

EE4620/CEG4324	
Attendance	50 pts
Prerequisite Quiz	50 pts
Midterm	150 pts
Final Exam	150 pts
TOTAL	400 pts

EE6620/CEG6324	
Attendance	50 pts
Prerequisite Quiz	50 pts
Midterm	150 pts
Additional assigned Lab final project*	50 pts
Final Exam	150 pts
TOTAL	450 pts

* **In the class, attendance is mandatory**. If you arrive after the sign-in sheet has gone around, it will count as absent; if you leave early, it will count as an absence. Missing **six classes** will result in the student **earning "0" out of "50" points** on the above "**Attendance**" for this class**. Signing someone else into class counts as a violation of the student code of conduct and will automatically fail the course.**

* EE6620/CEG6324 graduate student must read a new assigned research material in FPGA, identify problems, recommend promising solutions, and submit a final technical report.

Note: The final grade scale will be determined late in the semester. The tentative grading scale is shown below:

EE4620/CEG4324: **400 pts** = 100%
EE6620/CEG6324: **450 pts** = 100%

A for an overall score equal to or above 90%
B for an overall score between 80% and less than 90%
C for an overall score between 70% and less than 80%
D for an overall score between 60% and less than 70%
F for an overall score less than 60%

Student Learning Outcomes:

Students who successfully complete the course can:

1. Identify, formulate, and solve complex engineering problems by applying principles of engineering, science, and mathematics
2. Develop and conduct appropriate experimentation, analyze and interpret data, and use engineering judgment to draw conclusion