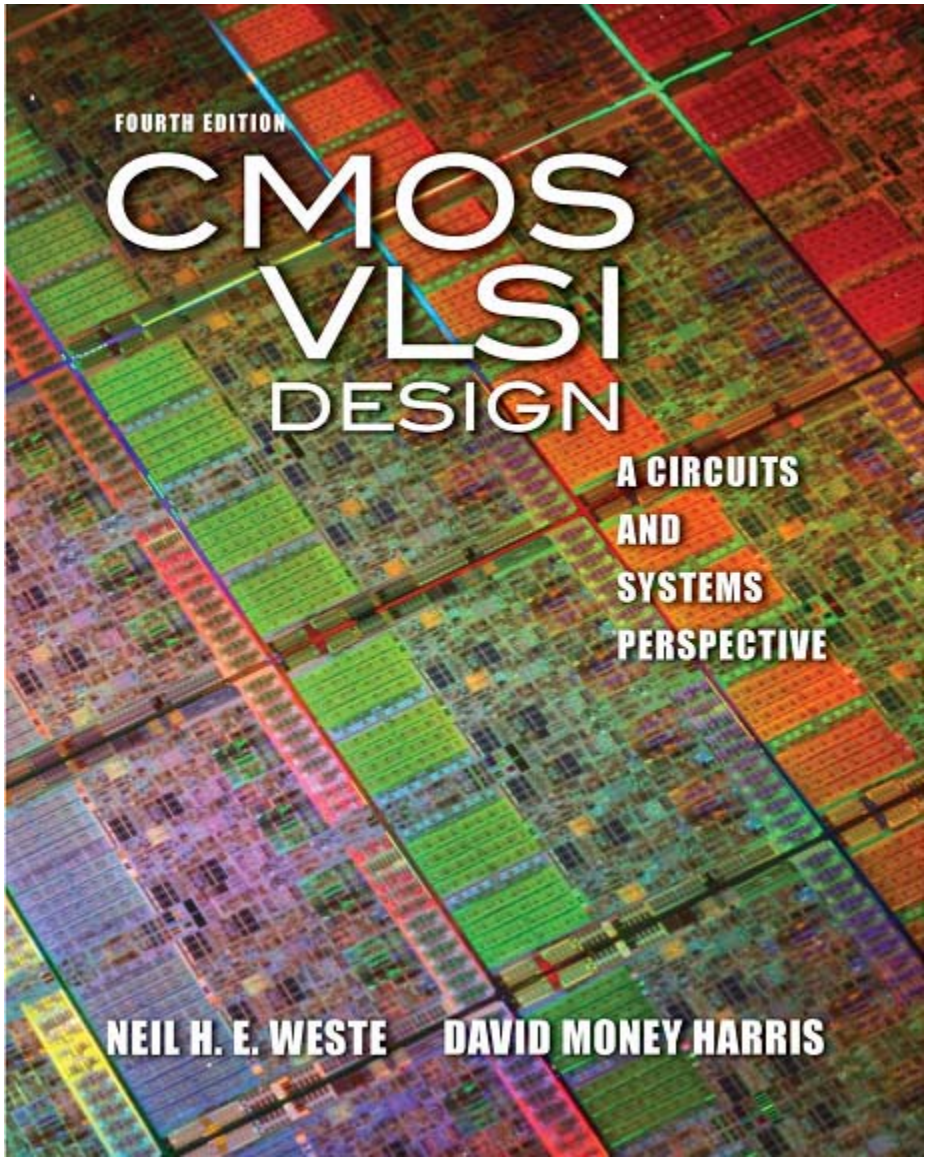


Introduction

Outline

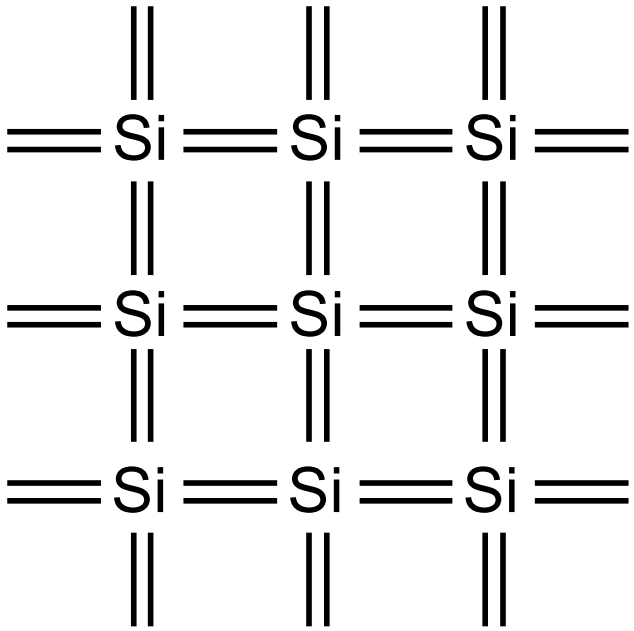
- p-n junction
- MOS transistor
- MOS transistor switch model
- CMOS Layout
  - Design rules
  - Stick diagram
- CMOS fabrication

Introduction

- Integrated circuit: many transistors are on one chip.
- *Very Large Scale Integration* (VLSI): million to billion
- *FET (**Field Effect Transistor**)*
- *CMOS-Complementary Metal Oxide Semiconductor*
  - cheap, low power, high density
- Today: How to build your own simple CMOS chip
  - CMOS transistors
  - Building logic gates from transistors
  - Transistor layout and fabrication
- Rest of the course: How to build a good CMOS chip

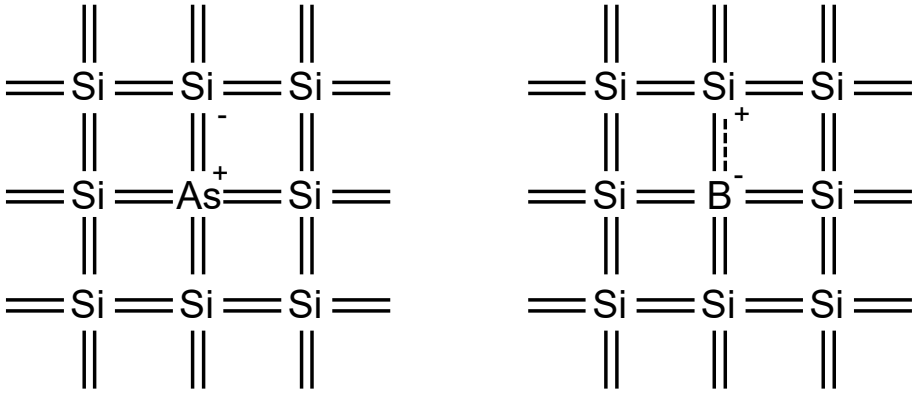
Silicon Lattice

- Transistors are built on a silicon substrate
- Silicon is a Group IV material
- Forms crystal lattice with bonds to four neighbors



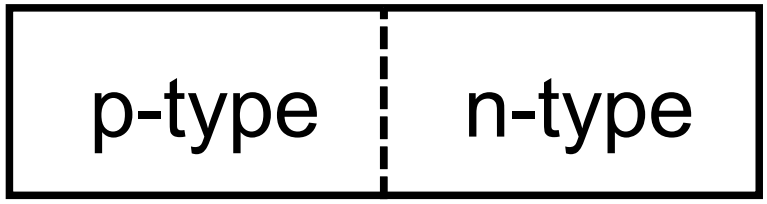
Dopants

- Silicon is a semiconductor
- Pure silicon has no free carriers and conducts poorly
- Adding dopants increases the conductivity
- Group V (Arsenic): extra electron (n-type)
- Group III (Boron): missing electron, called hole (p-type)

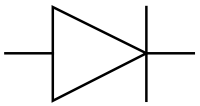


p-n Junctions

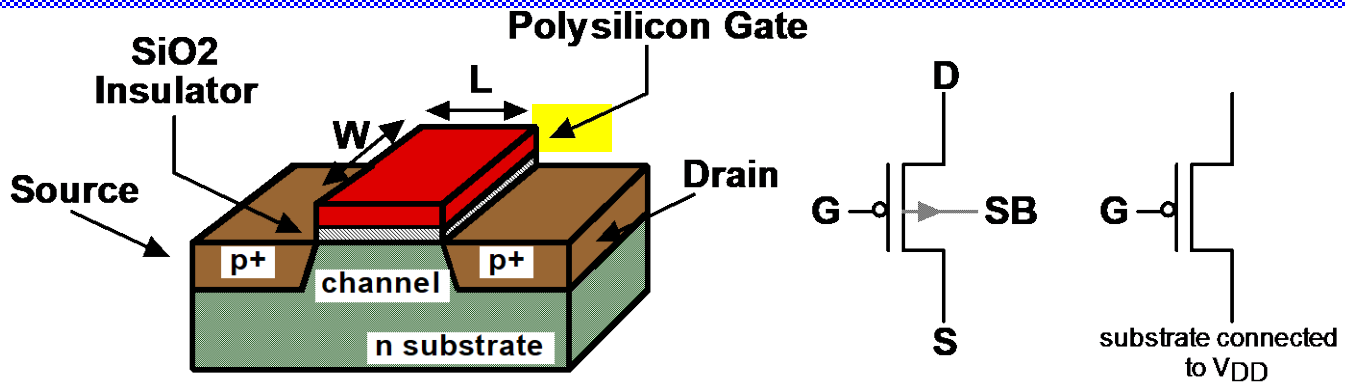
- A junction between p-type and n-type semiconductor forms a diode.
- Current flows only in one direction



anode cathode

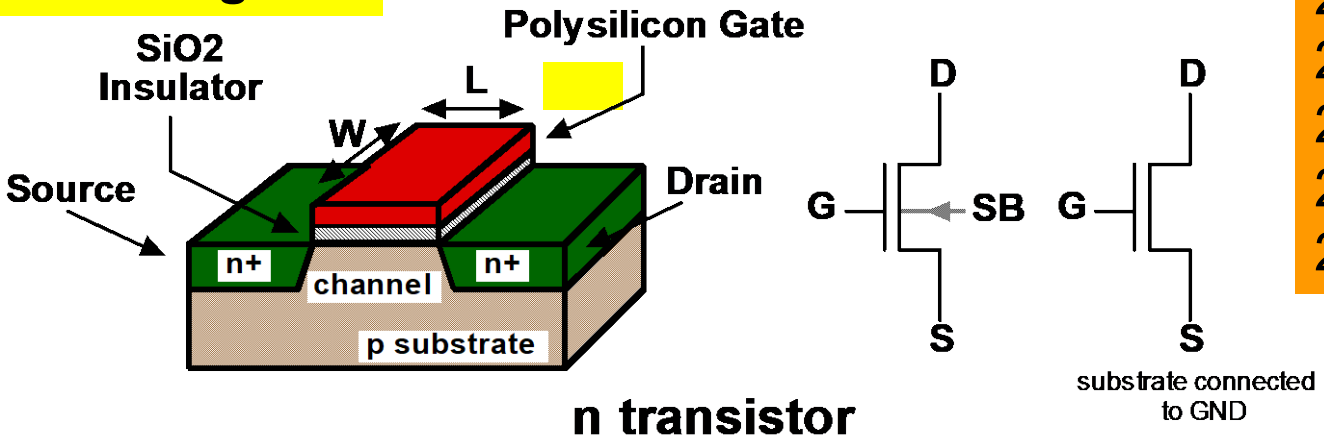


MOS Transistor (3D view)



p transistor

Key feature:
transistor **length L**

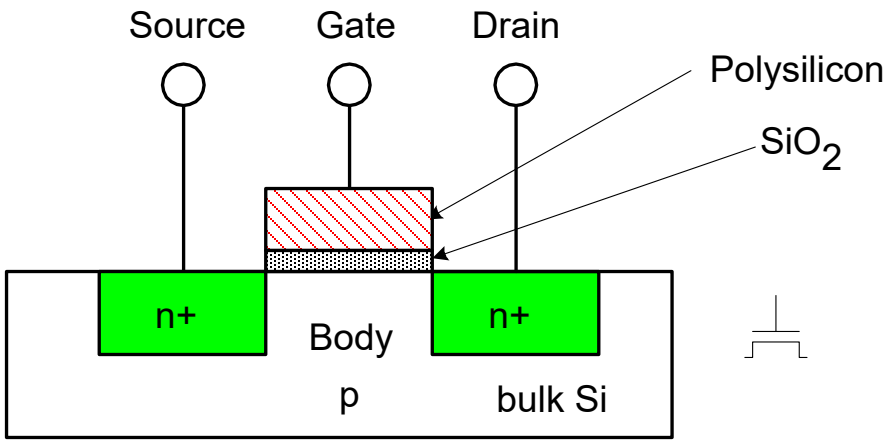


n transistor

2002: L=130nm
2003: L=90nm
2005: L=65nm
2008: L=45nm
2010: L=32nm
2016: L=10nm

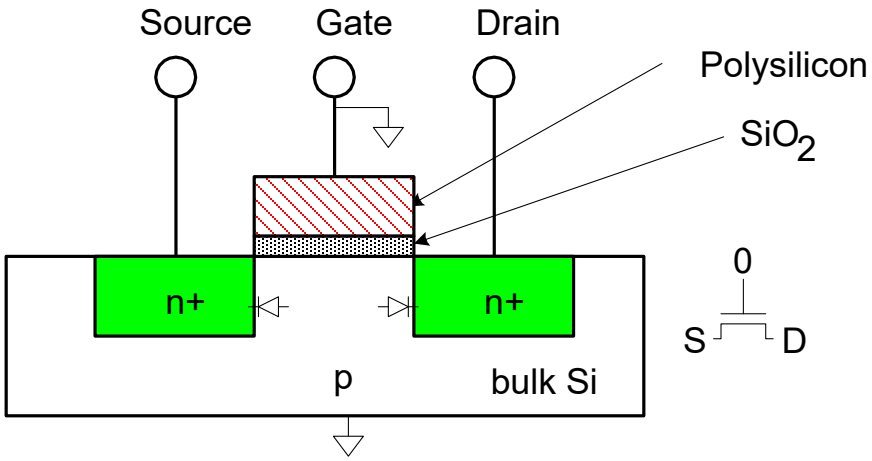
nMOS Transistor (cross-section view)

- Four terminals: gate, source, drain, body
- Gate – oxide – body stack looks like a capacitor
  - Gate and body are conductors
  - SiO_2 (oxide) is a very good insulator
  - Called Metal – Oxide – Semiconductor (MOS) capacitor



nMOS Operation

- Body is usually tied to ground (0 V) or the lowest voltage
- When the gate is at a low voltage (<V_T):
  - P-type body is at low voltage (0 V)
  - Source-body and drain-body diodes are OFF
  - No current flows, transistor is OFF

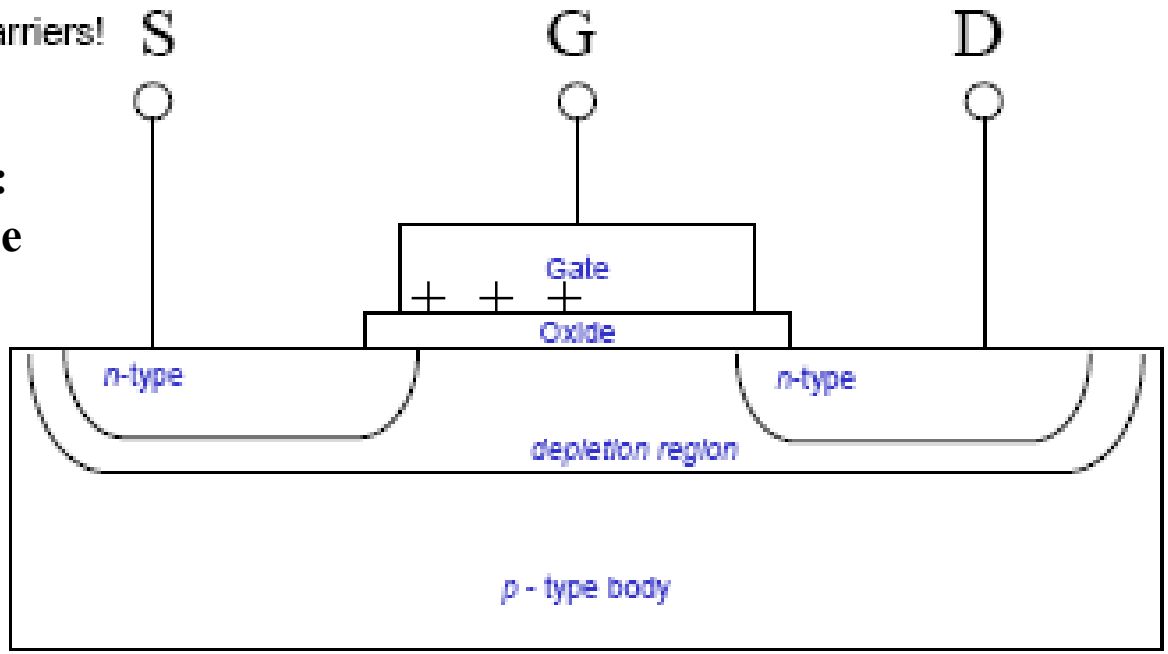


How do we make the current flow? $V_S = 0$ $V_{GS} < V_T$ $V_D > V_S$

We create a channel full of carriers!

V_T --Threshold voltage: minimum gate to source voltage (Vgs) to have channel inverted.

$V_{TN} > 0$



How do we make the current flow?

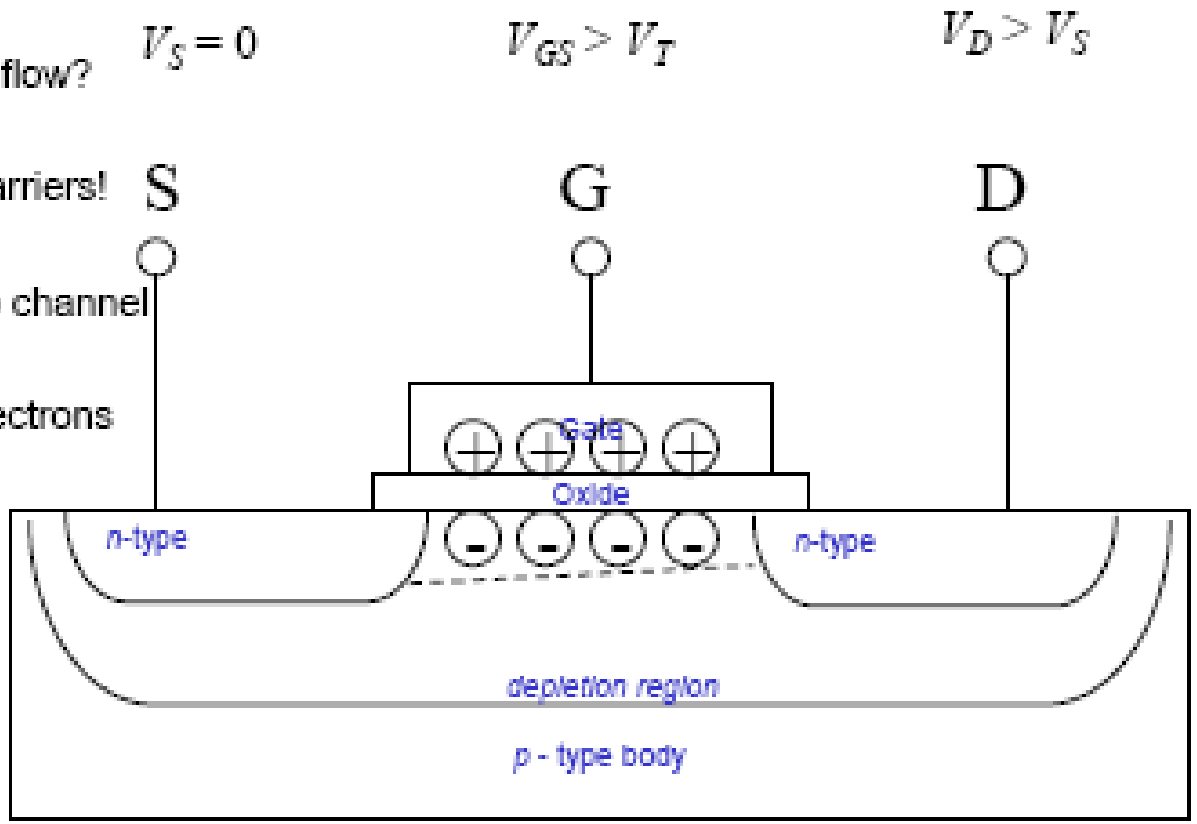
We create a channel full of carriers!

Pos charge on G attracts e to channel

Current flows from D to S (electrons flow from S to D)

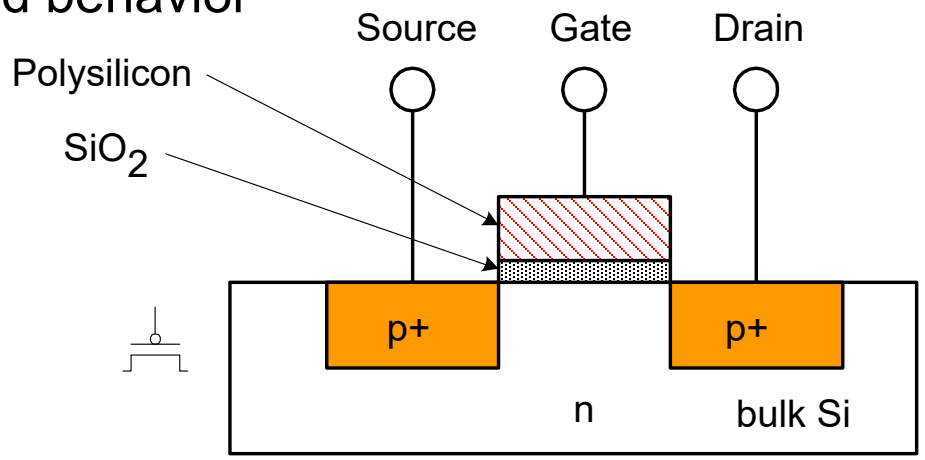
VCCD

$V_G > V_T$ => Device "On"
$V_G < V_T$ => Device "Off"



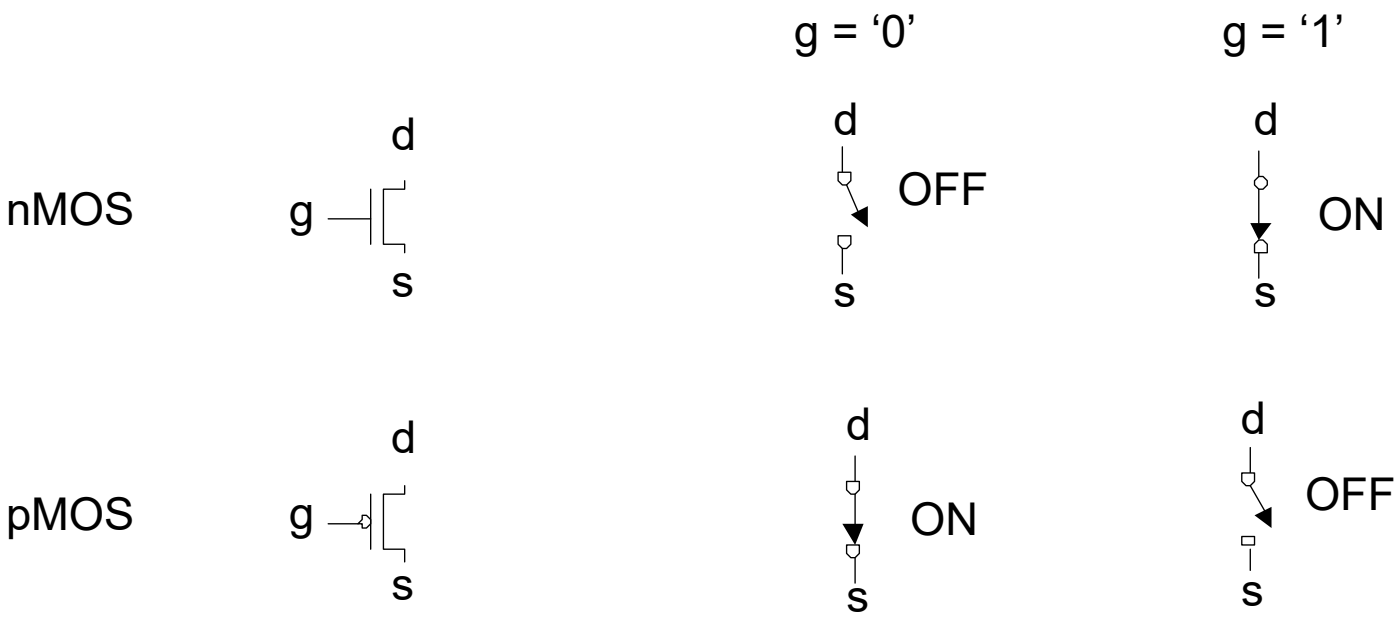
pMOS Transistor

- Similar to nMOS, but doping and voltages reversed
  - Body tied to highest voltage (VDD)
  - Gate low: transistor ON
  - Gate high: transistor OFF
  - $V_{TP}<0$; When $V_{GSP}<V_{TP}$, Inverts a channel under gate to p-type
  - When $V_S>V_D$, current can flow from source through channel to drain, transistor is ON
  - Bubble indicates inverted behavior



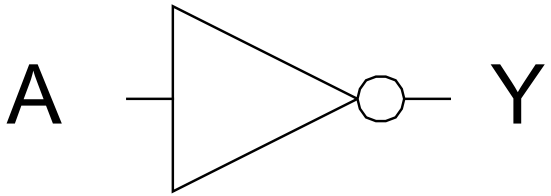
Transistors as Switches

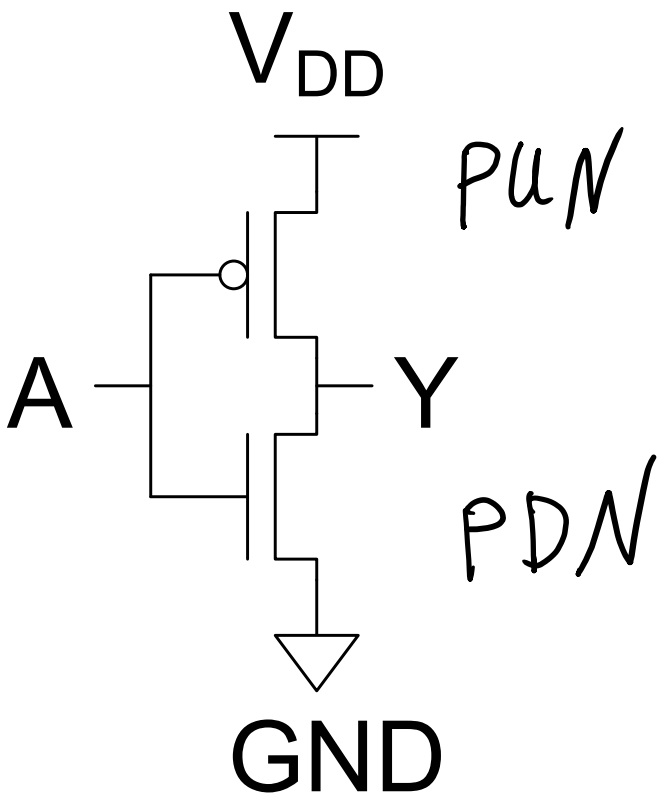
- We can view MOS transistors as **electrically controlled switches**
- Voltage at gate controls path from source to drain



CMOS Inverter

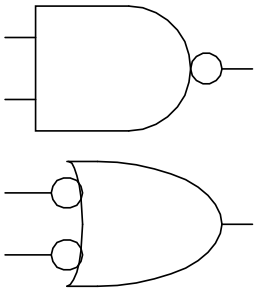
A	Y
0	
1	



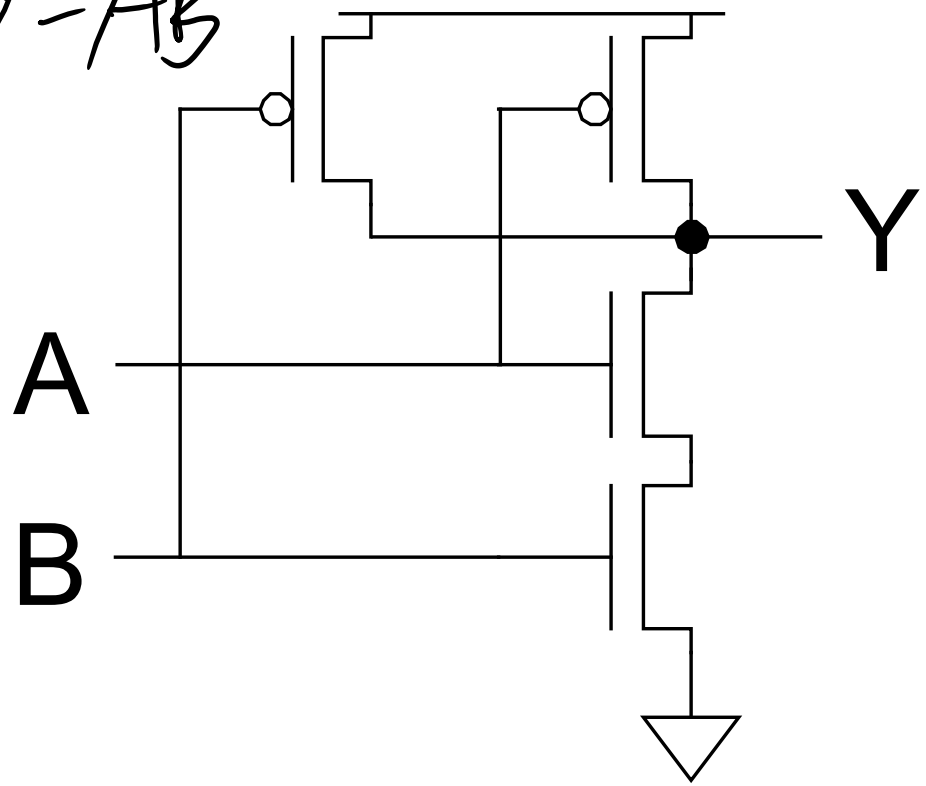


CMOS NAND2 Gate

A	B	Y
0	0	
0	1	
1	0	
1	1	

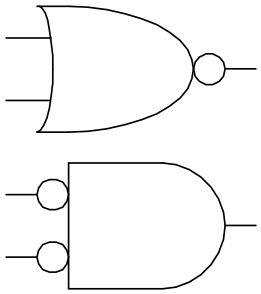


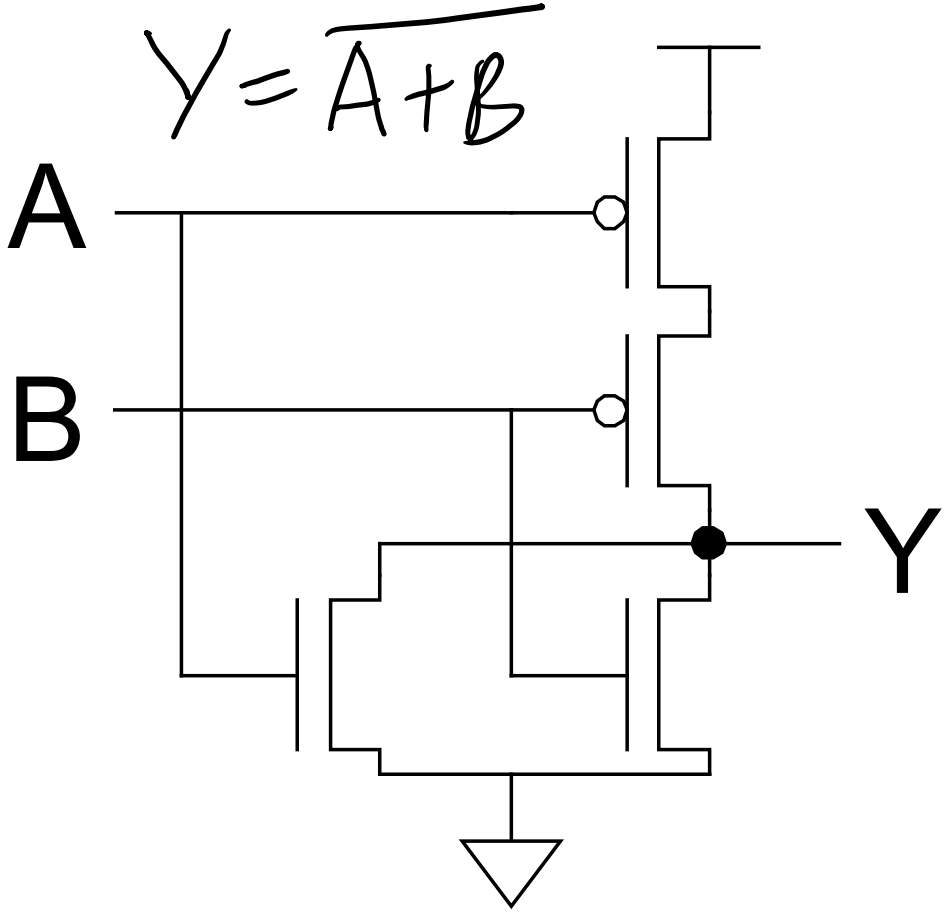
$Y = \overline{AB}$



CMOS NOR2 Gate

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0





3-input NAND Gate

- Y pulls low if ALL inputs are 1
- Y pulls high if ANY input is 0

$$Y = \overline{ABC}$$

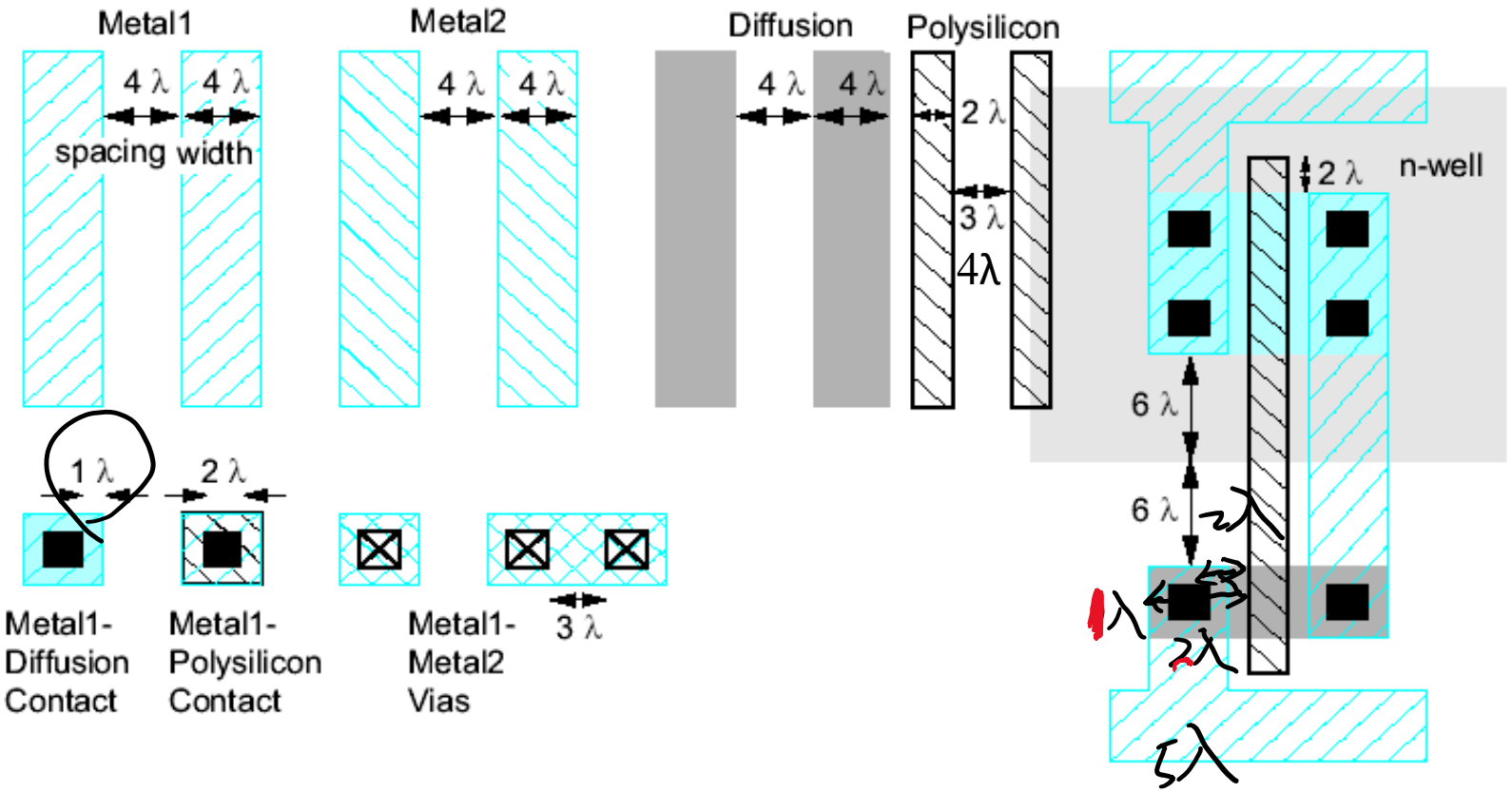
Layout

- Chips are specified with set of masks
- Minimum dimensions of masks determine transistor size (and hence speed, cost, and power)
- Feature size *f* = distance between source and drain
  - Set by minimum width of polysilicon
- Feature size reduces 30% every 3 years or so
- Normalize for feature size when describing design rules
- Express rules in terms of $\lambda = f/2$
  - E.g. λ = 0.3 μm in 0.6 μm process,

λ = ? in your lab

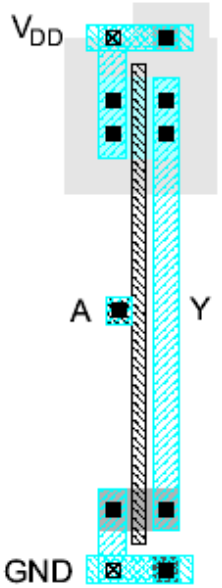
Simplified Design Rules

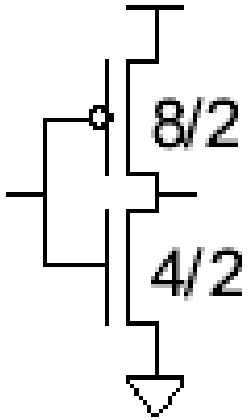
- Conservative rules to get you started

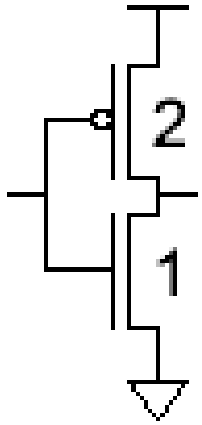


Inverter Layout

- Transistor dimensions specified as Width / Length
  - Minimum size is 4λ / 2λ, sometimes called 1 unit
  - In *f* = 0.6 μm process, this is 1.2 μm wide, 0.6 μm long for nMOS.



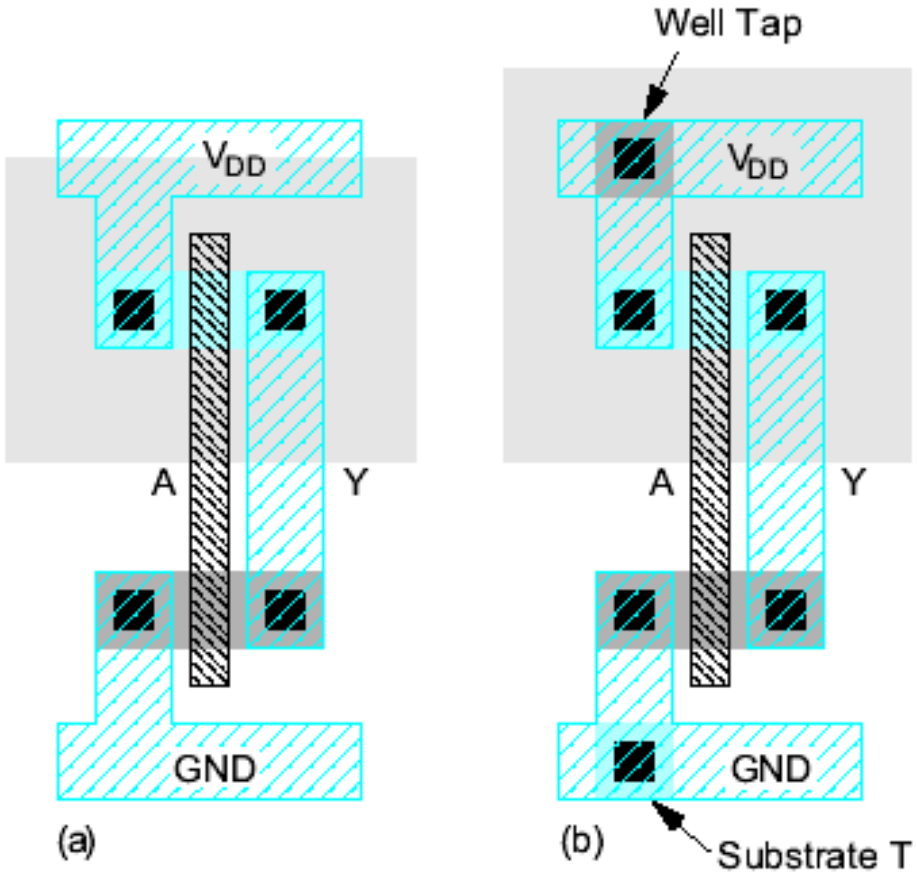




Logic Gates Layout

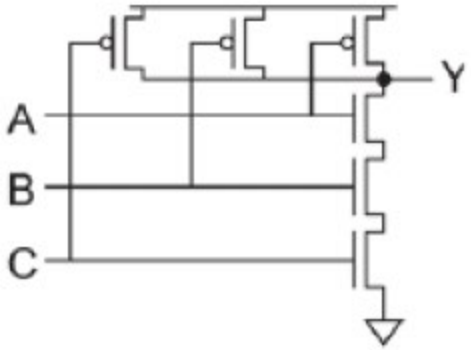
- Layout can be very time consuming
  - Design gates to fit together nicely
  - Build a library of standard cells
- Standard cell design methodology
  - V_{DD} and GND should abut (standard height)
  - Adjacent gates should satisfy design rules
  - nMOS at bottom and pMOS at top
  - All gates include well and substrate contacts

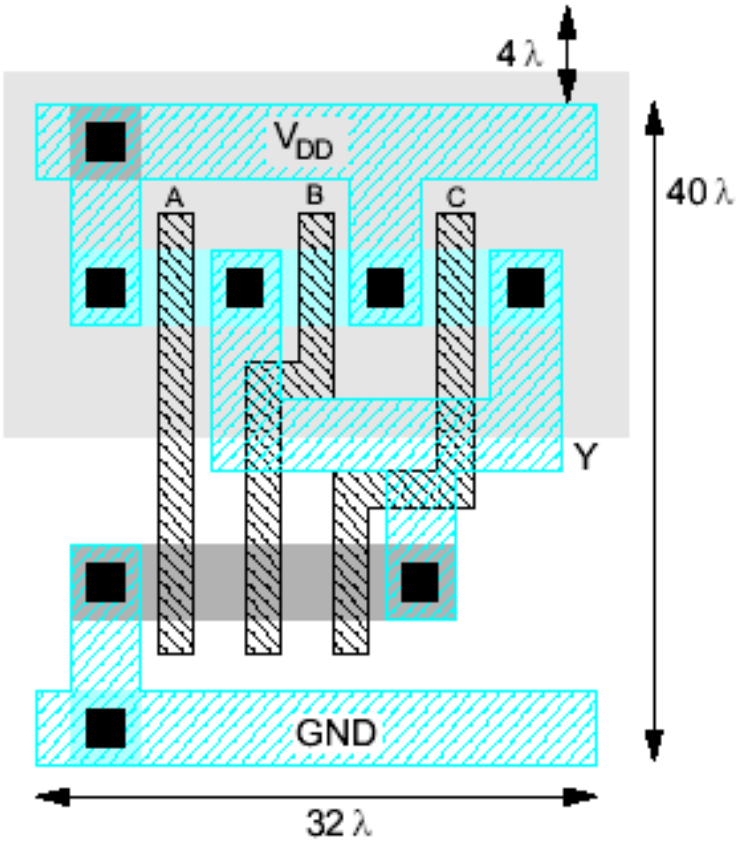
Example: Inverter



Example: NAND3

- Horizontal N-diffusion and p-diffusion strips
- Vertical polysilicon gates
- Metal1 V_{DD} rail at top
- Metal1 GND rail at bottom
- 32 λ by 40 λ

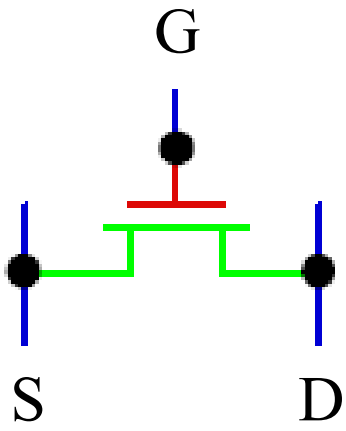




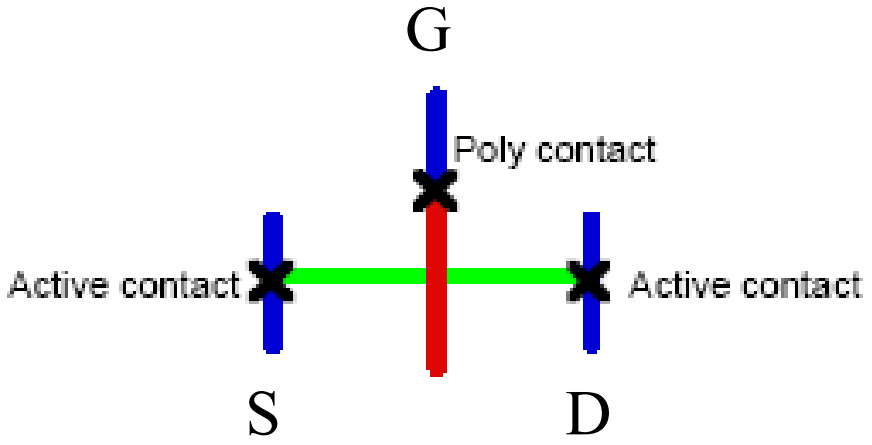
Stick Diagram Usage

- *Stick diagrams* help plan layout quickly
  - No need to scale
  - Draw with color pencils or dry-erase markers to aid in wiring of basic gates, or routing interconnect lines on chip
  - VLSI layout can become complicated due to the large number of wires that need to be included.
  - Stick diagram can be used to plan the wiring before you access a CAD tool. Many hours of frustration can be avoided by planning ahead.

Basic Stick Diagram Rule



Schematic

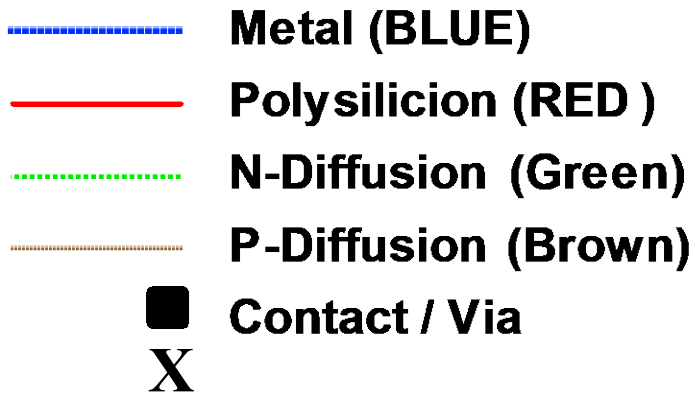


Stick diagram

Poly contact: Metal1-to-Poly
Active Contact: Metal1-to-Active

Basic Stick Diagram Rule (cont)

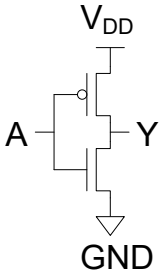
Layers

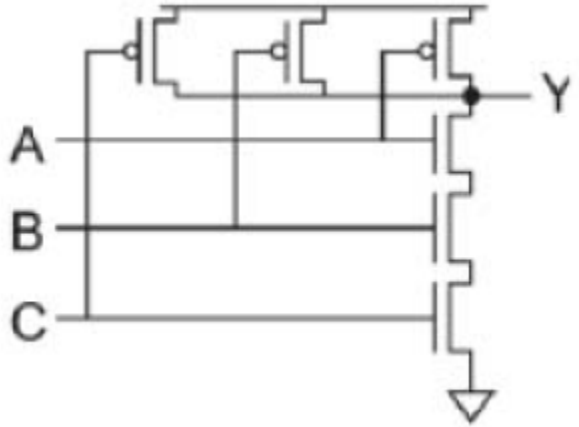


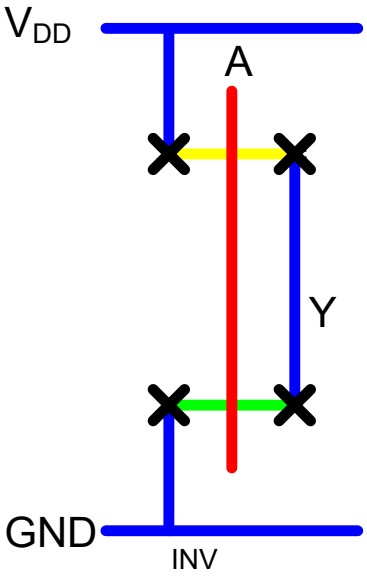
Connection Rules

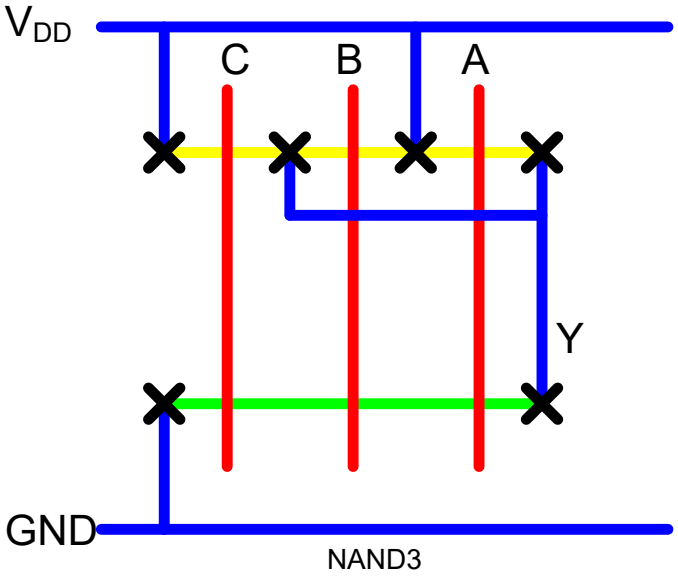
	poly	n-diff	p-diff	metal
poly	S	N	P	NC
n-diff		S	X	NC
p-diff			S	NC
metal				S

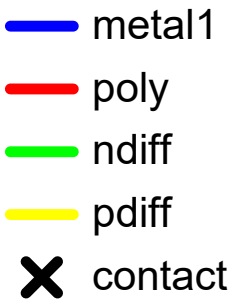
Example


V_{DD}
A
Y
GND

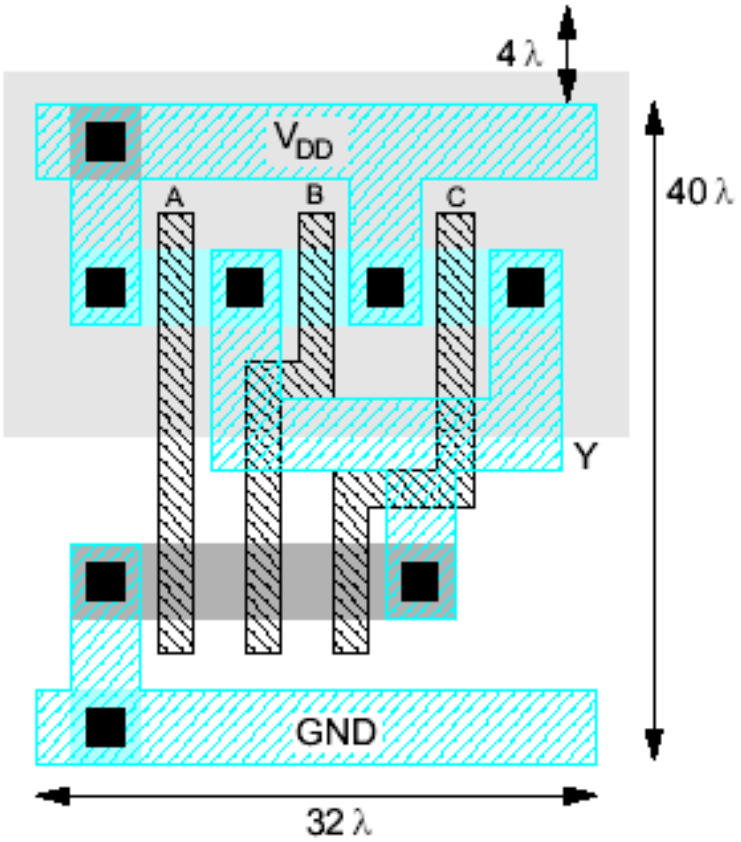

A
B
C
Y

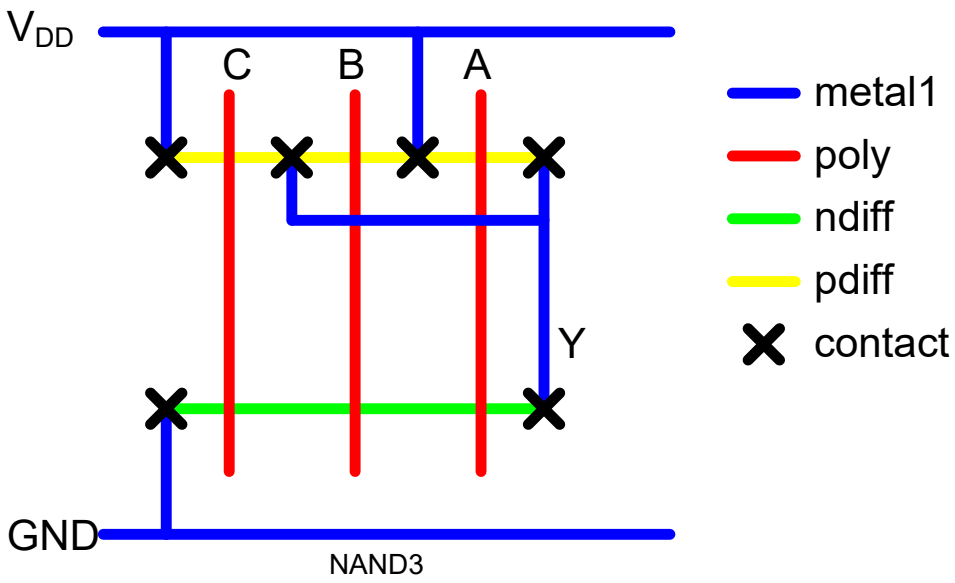

V_{DD}
A
Y
GND
INV


V_{DD}
C
B
A
Y
GND
NAND3

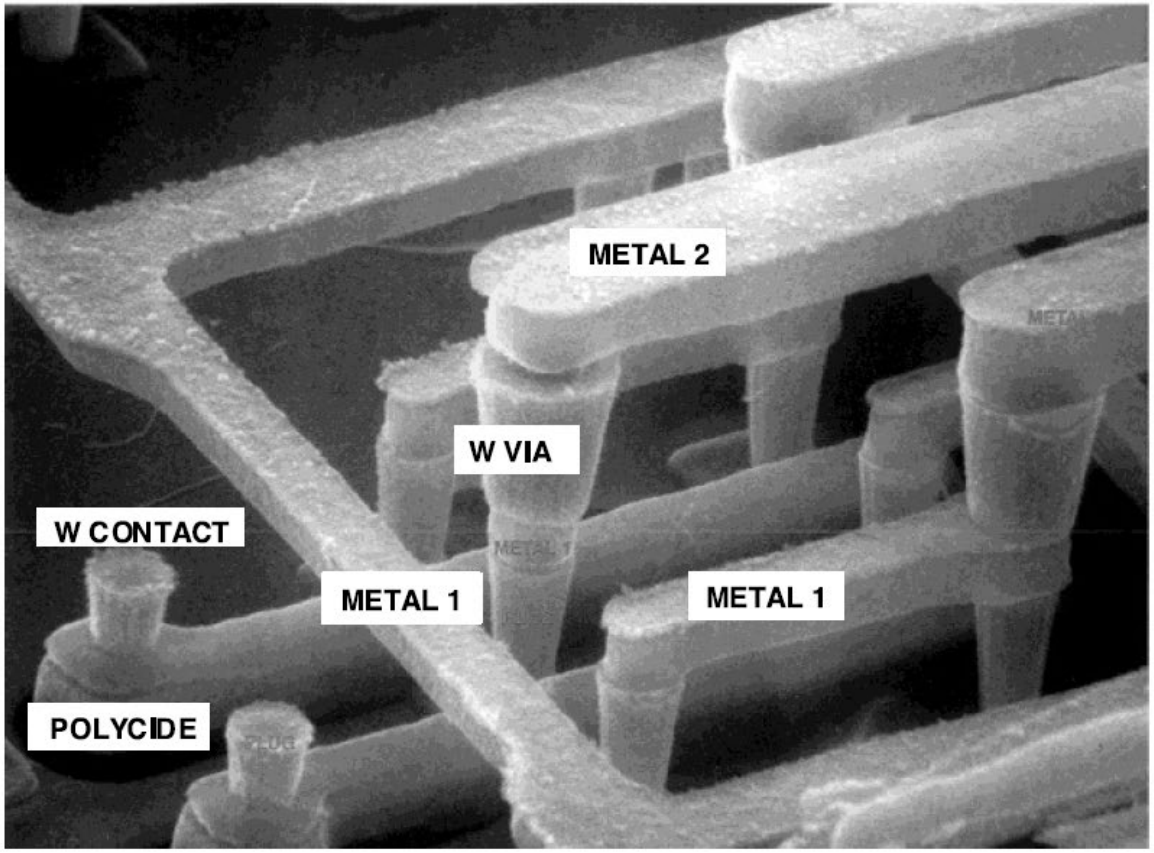

metal1
poly
ndiff
pdiff
contact

Example


4 λ
40 λ
VDD
A
B
C
Y
GND
32 λ

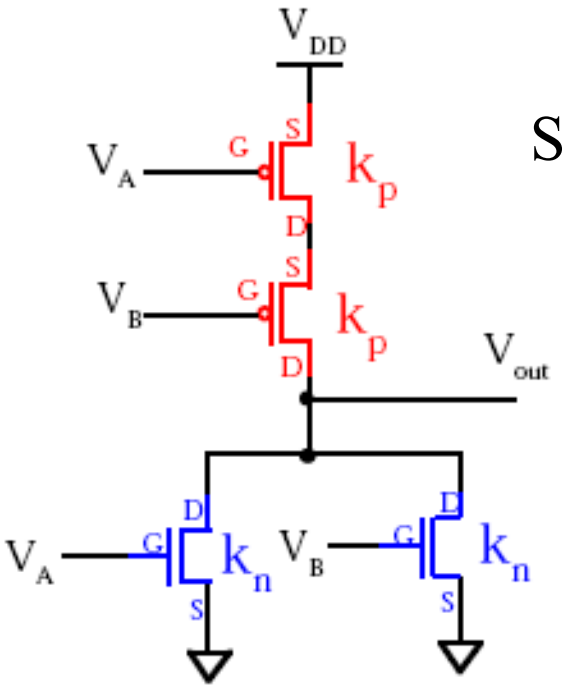

VDD
C
B
A
Y
GND
NAND3
metal1
poly
ndiff
pdiff
contact

SEM MICRO-GRAPH (ILM DIELECTRIC REMOVED)

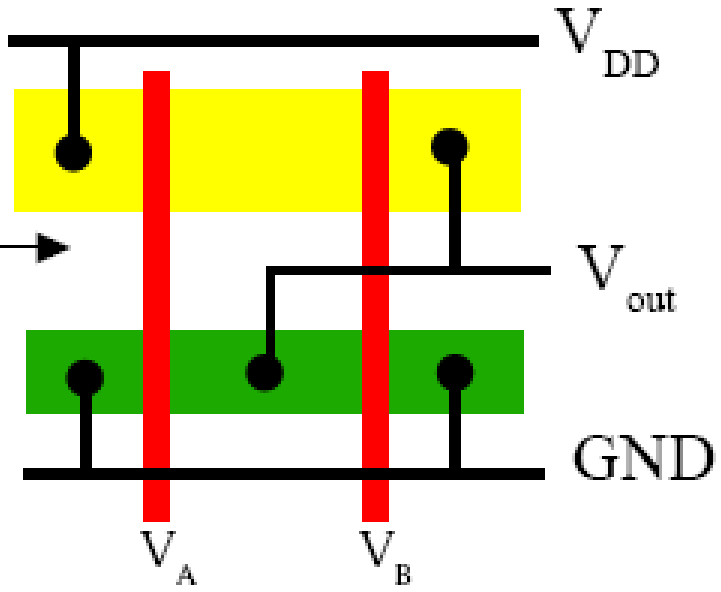


Courtesy: IBM

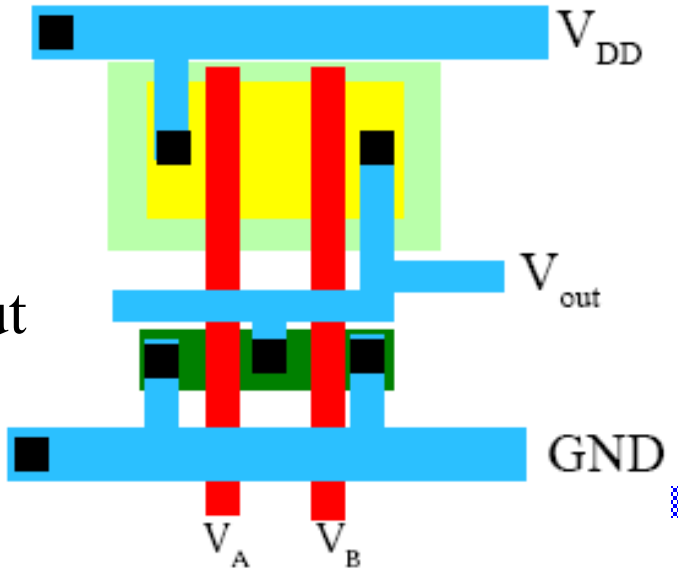
NOR2 layout



Stick diagram →

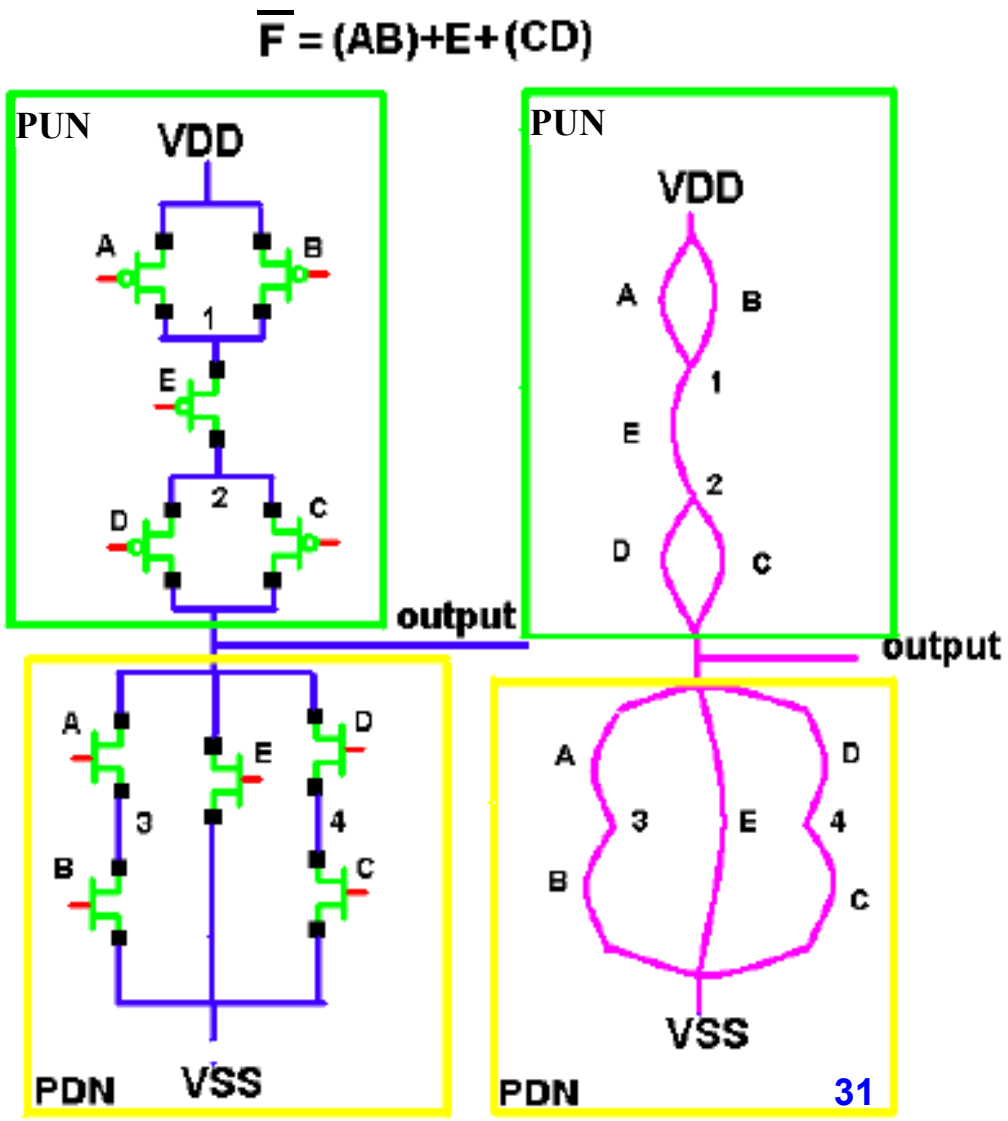


layout



Stick Diagram Method

- Stick diagram are often used to solve routing problems
- Three steps:
  1) The 1st step is to construct a logic diagram of the schematic
     a) Identify each transistor by a unique name of its gate signal
     b) Identify each connection to the transistor by a unique name



Stick Diagram Method (Cont)

2) The second step is to construct one Euler path for both pull up (pMOS) and pull down (nMOS) network.

a) Euler paths are defined by a path and traverses each node in the path, each edge (transistor) is visited only once.

b) The path is defined by the order of each transistor name. if the path traverses transistor A then B then C. The path name is {A,B,C}.

c) The Euler path of the PUN must be the same as the path of the PDN.

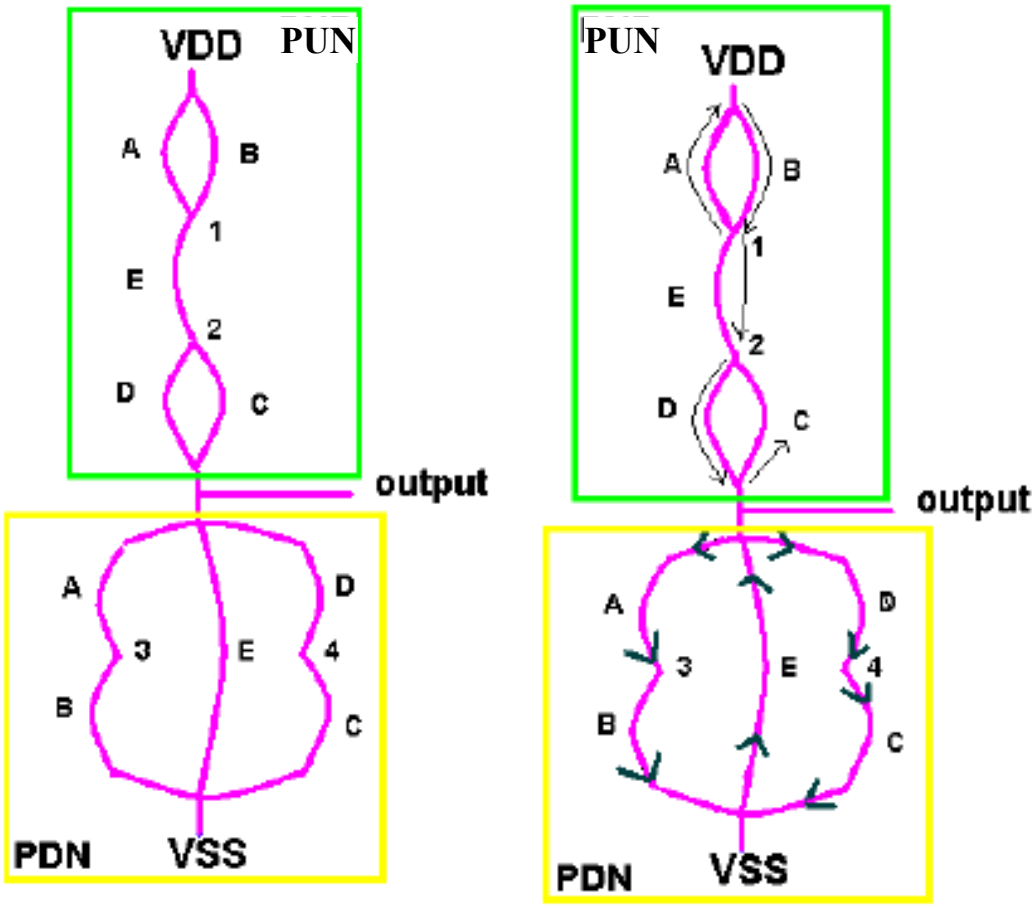
d) Euler paths are not necessarily unique.

e) It may be necessary to redefine the function to find a non-break Euler path.

F=E+(CD)+(AB)=(AB)+E+(CD)

Stick Diagram Method (Cont)

$\overline{F} = (AB)+E+(CD)$



EULER PATH = {A,B,E,D,C}

Stick Diagram Method (Cont)

3) Once the Euler path is found it is time to lay out the stick diagram

A) Trace two green lines horizontally to represent the NMOS and PMOS devices.

B) Trace the number of inputs (5 in this example) vertically across each green strip. These represent the gate contacts to the devices that are made of Poly.

C) Surround the NMOS device in a yellow box to represent the surrounding Pwell material.

D) Surround the PMOS device in a green box to represent the surrounding Nwell material.

E) Trace a blue line horizontally, above and below the PMOS and NMOS lines to represent the Metal 1 of VDD and VSS.

F) Label each Poly line with the Euler path label, in order from left to right.

G) Place the connection labels upon the NMOS and PMOS devices.

i) In the example of Figure 2 the connection labels are 1, 2, 3, 4. Connection 1 is the node that lies between the PMOS transistors A, B and E. The Euler path defines the transistor ordering of {A, B, E, D, C} therefore, transistor B is physically located beside transistor E. Place the connection label 1 between the transistors B and E. Later, we will route a Metal 1 connection from the drain of transistor A to the connection label of 1.

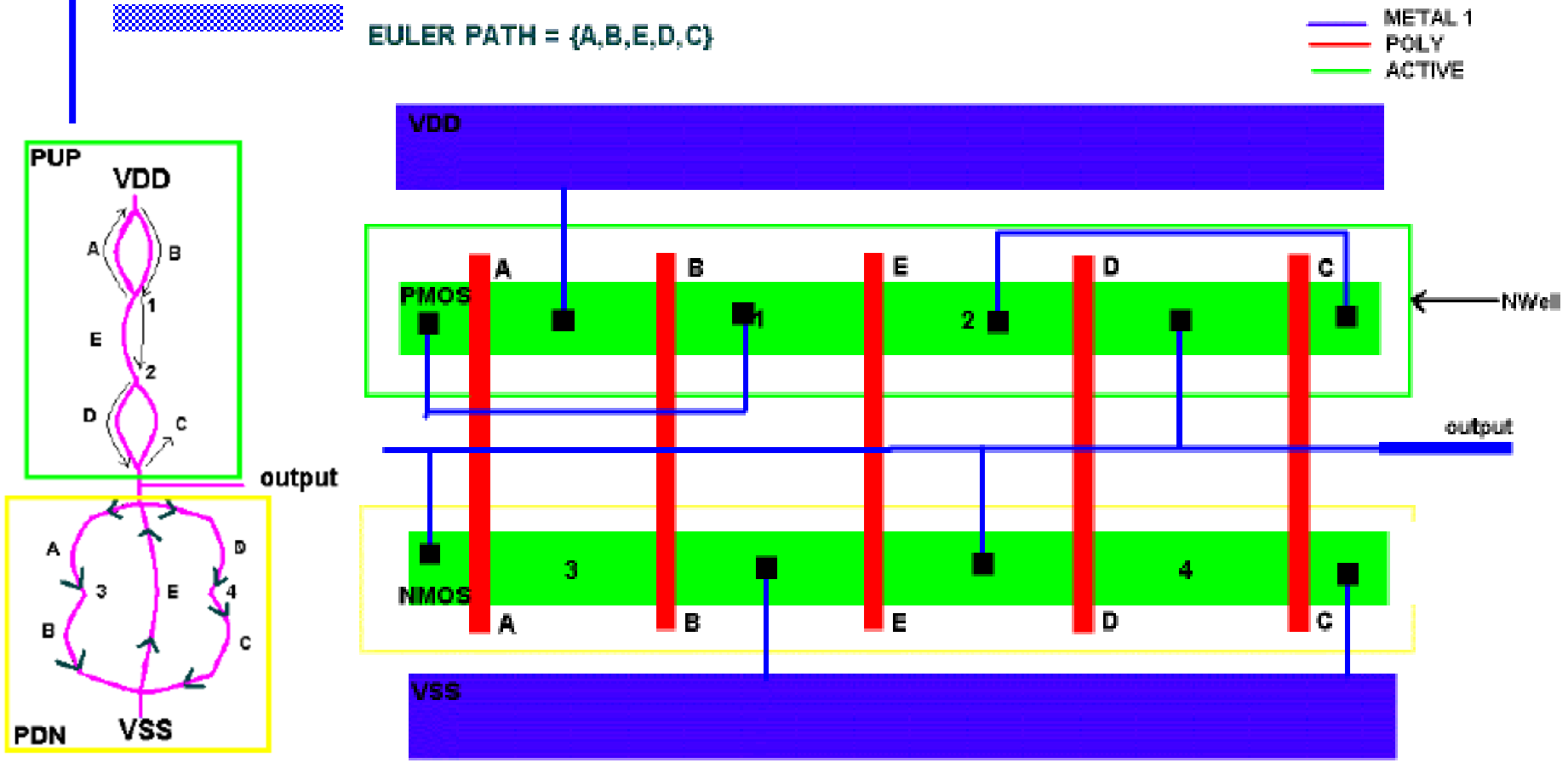
ii) Connection 2 is the node that connects the PMOS transistors of E, D, and C. Since the Euler path places transistors E and D next to each other, place the connection label between these two. Later, we will route a Metal 1 strip from the source of C to connection label 2.

iii) Connection label 3 lies between the NMOS transistors of A and B.

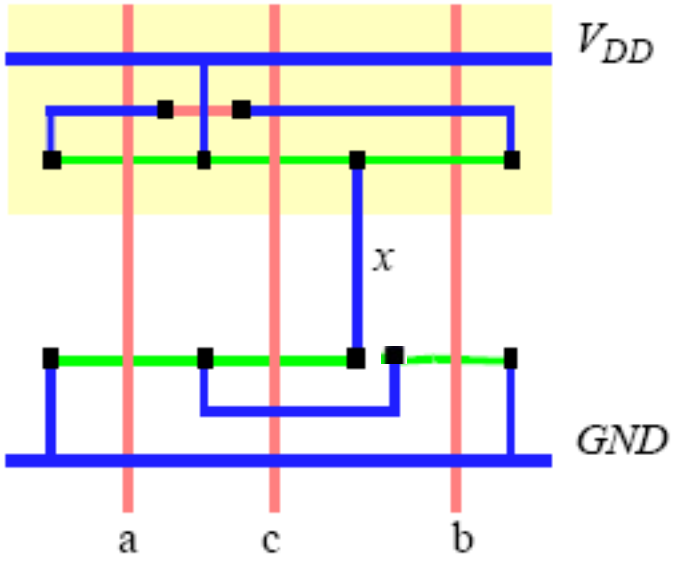
iiii) Connection label 4 lies between the NMOS transistors of D and C.

Stick Diagram, Interconnected

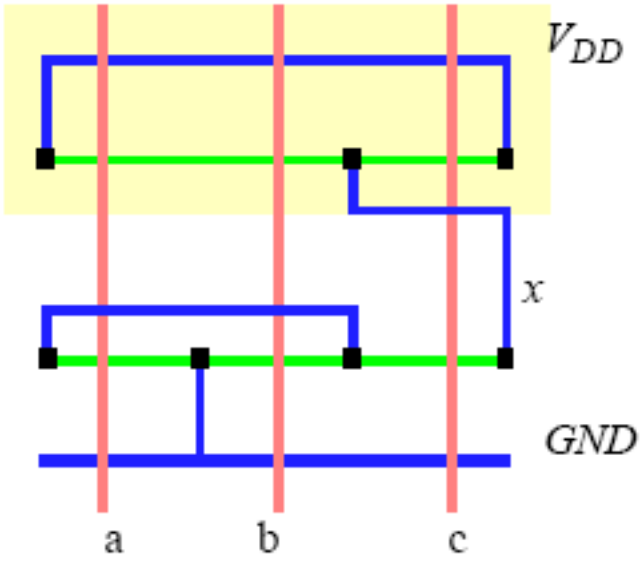
EULER PATH = {A,B,E,D,C}



Two Versions of (a+b).c



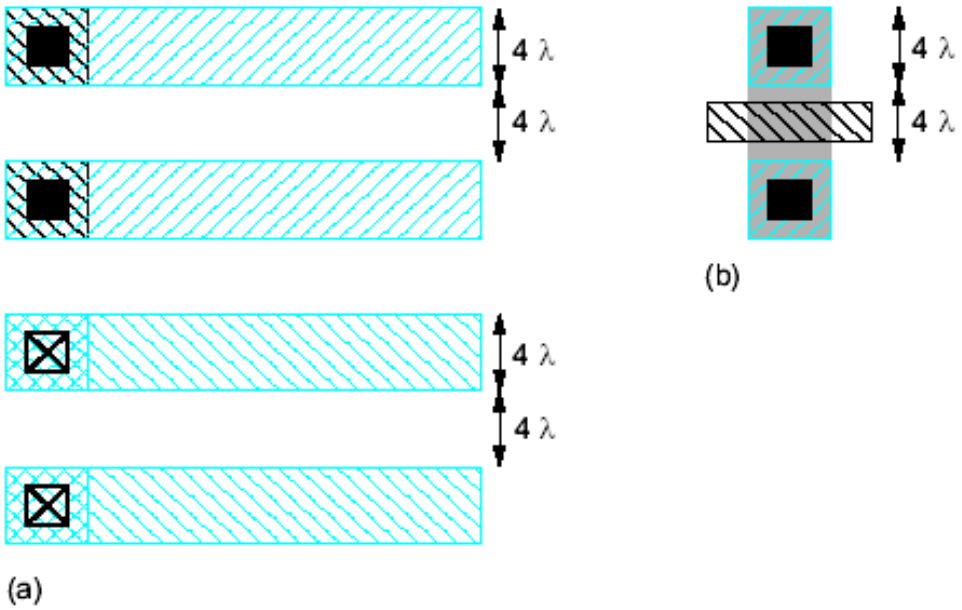
(a) Input order {*a c b*}



(b) Input order {*a b c*}

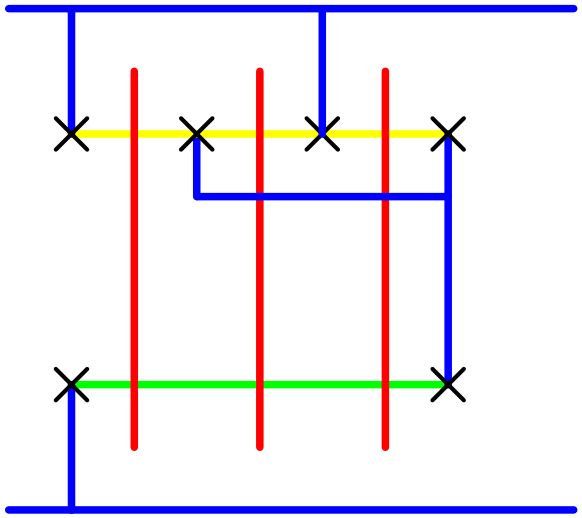
Wiring Tracks

- A *wiring track* is the space required for a wire
  - 4 λ width, 4 λ spacing from neighbor = 8 λ pitch
- Transistors also consume one wiring track



Area Estimation

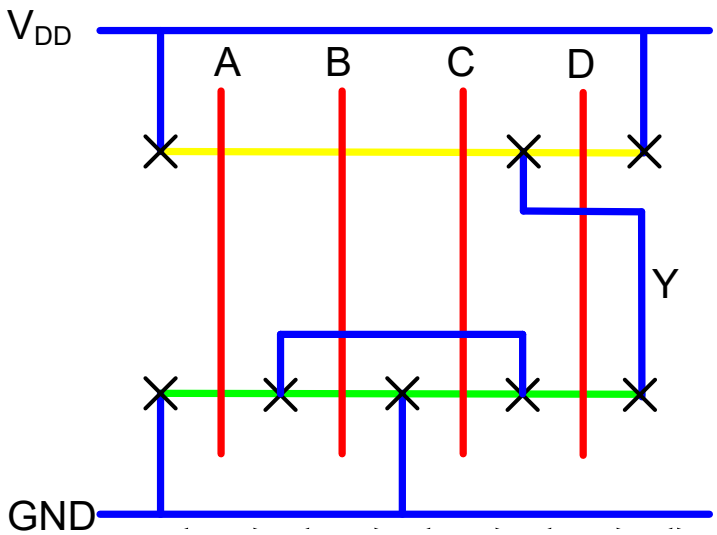
- Estimate area (x *y) by counting wiring tracks
  - Count maximum number of non-overlapped vertical metal wires and multiply it by 8λ for x size
  - Count maximum number of non-overlapped horizontal metal wires, plus one for pMOS transistor and one for nMOS transistor, then multiply it by 8λ for y size



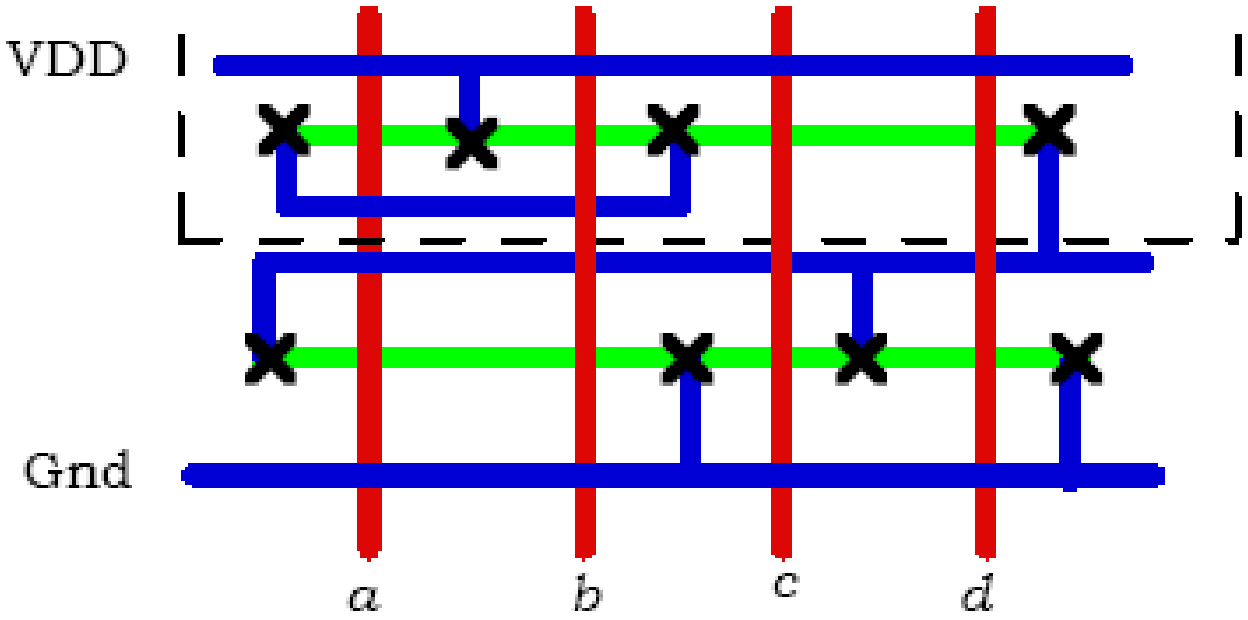
Example: O3AI

- Sketch a stick diagram for O3AI and estimate area

$$\overline{Y = (A + B + C) \cdot D}$$



Exercise1: please derive the Boolean function and schematic circuit of the following stick diagram



Exercise2: please draw the schematic circuit, Euler path and stick diagram of Boolean function f=(a+b)(c+d) with minimum size

Standard Cells

- The standard cells all share the same metals Vdd and Gnd locations with 60λ height so that power and ground can be connected by abutment. Inputs and outputs are provided in metal2.

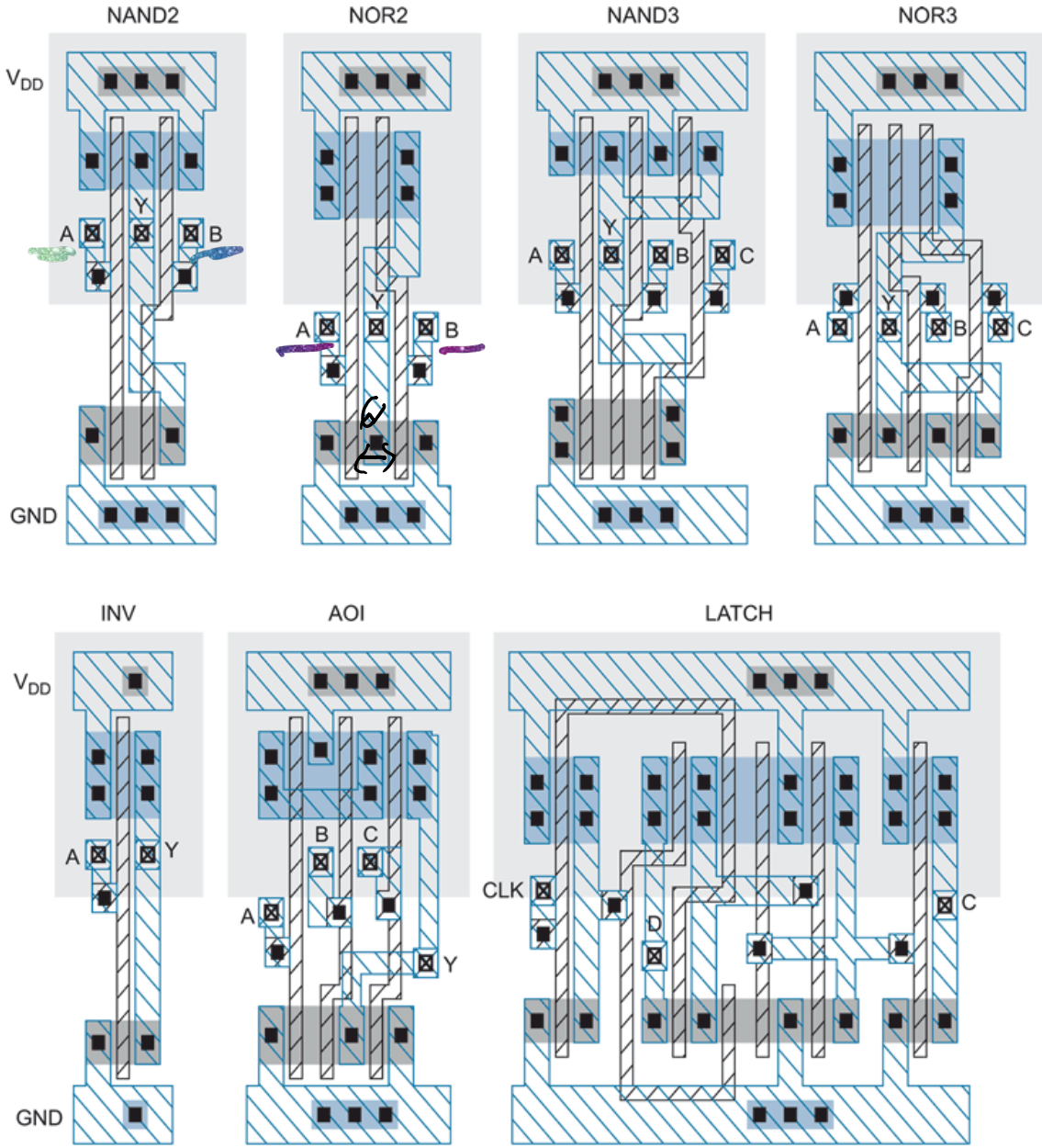


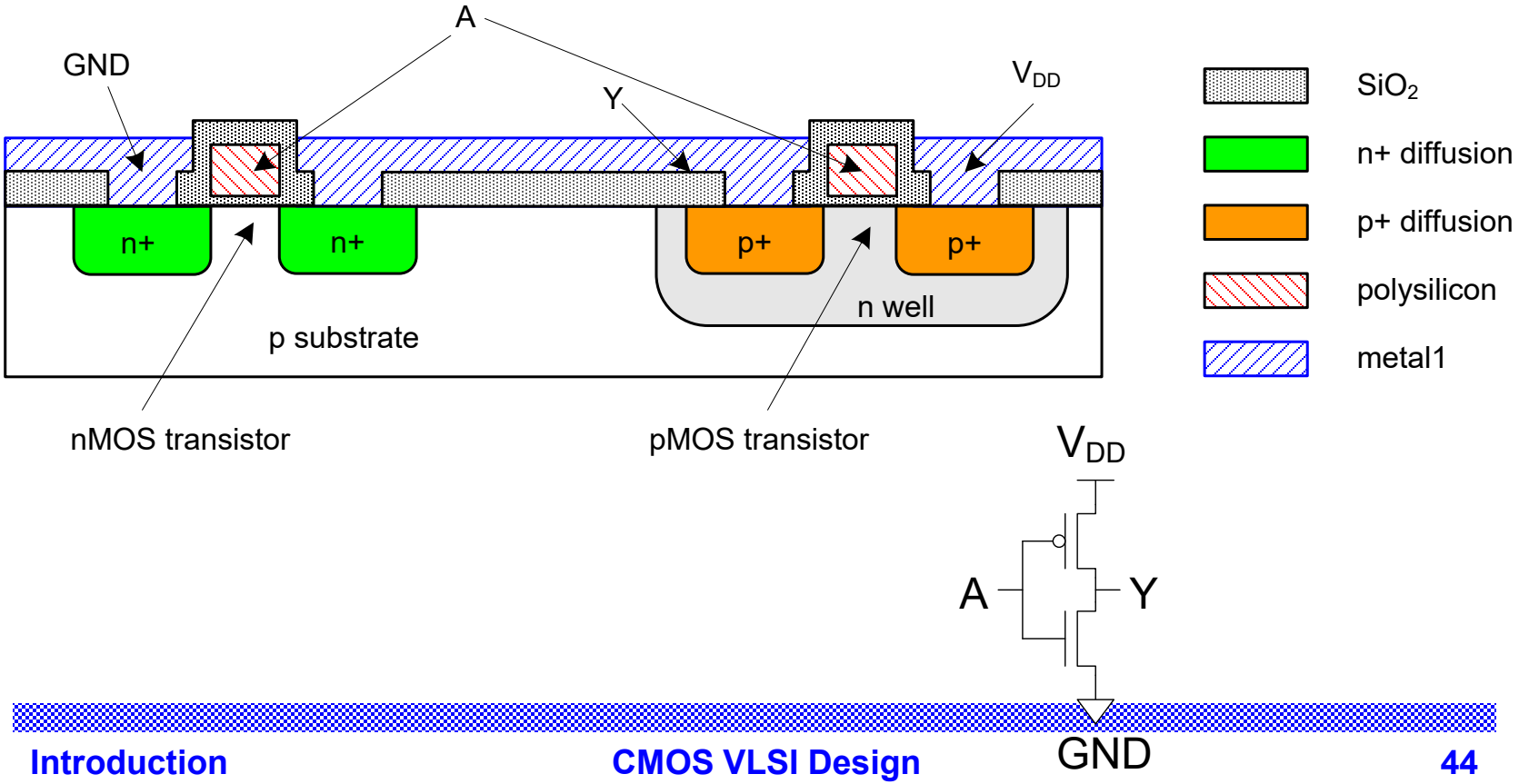
FIG 1.62 Simple standard cell library. Color version on inside front cover.

CMOS Fabrication

- CMOS transistors are fabricated on silicon wafer
- Lithography process similar to printing press
- On each step, different materials are deposited or etched
- Easiest to understand by viewing both top and cross-section of wafer in a simplified manufacturing process

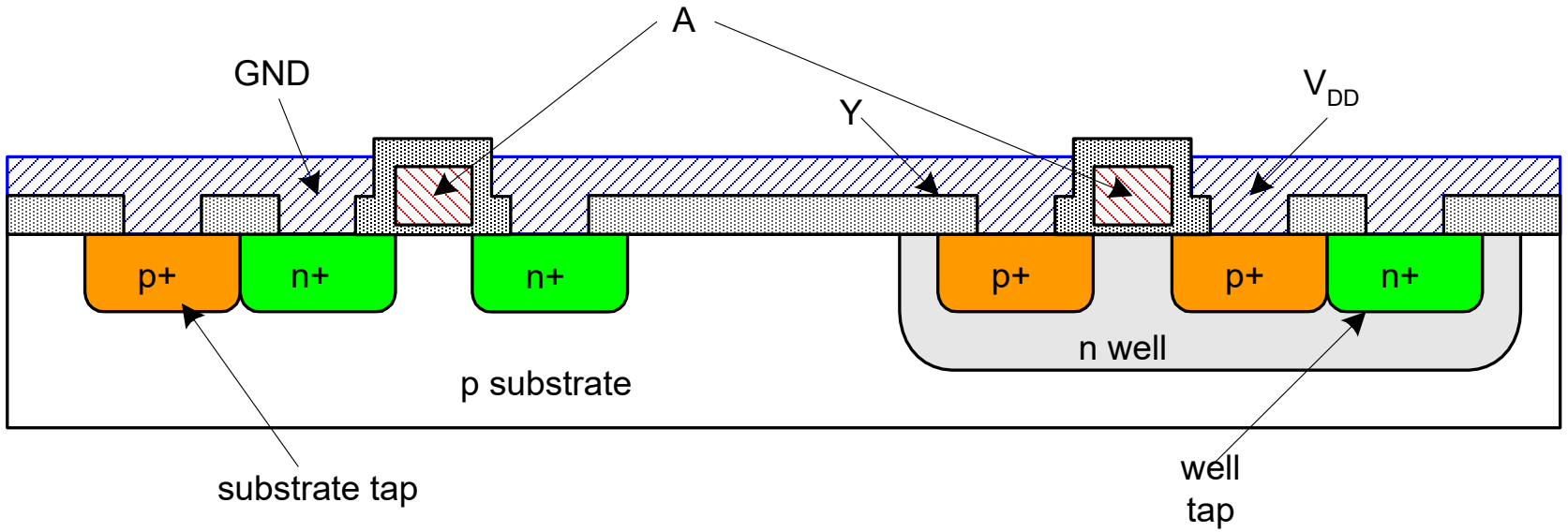
Inverter Cross-section

- Typically use p-type substrate for nMOS transistors
- Requires n-well for body of pMOS transistors



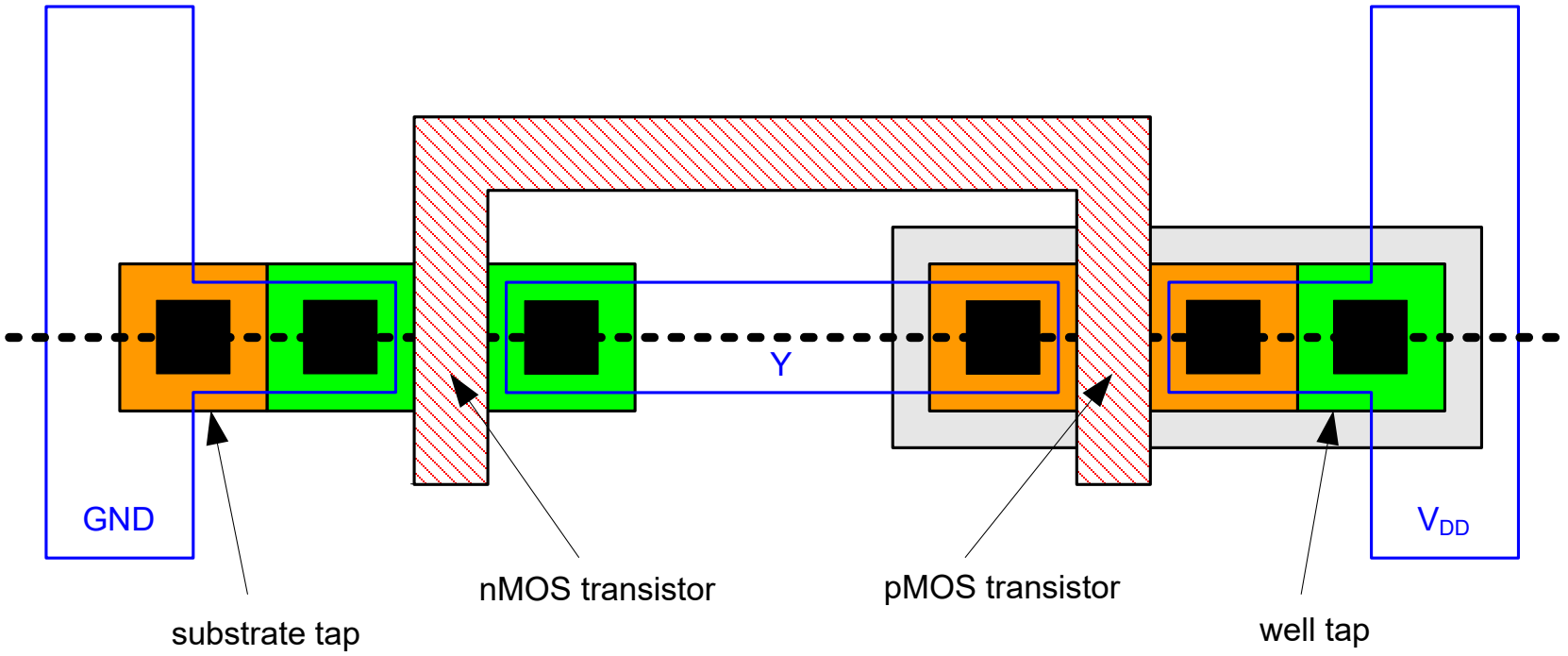
Well and Substrate Taps

- Substrate must be tied to GND and n-well to V_{DD}
- Metal to lightly-doped semiconductor forms poor connection called Schottky Diode
- Use heavily doped well and substrate contacts / taps



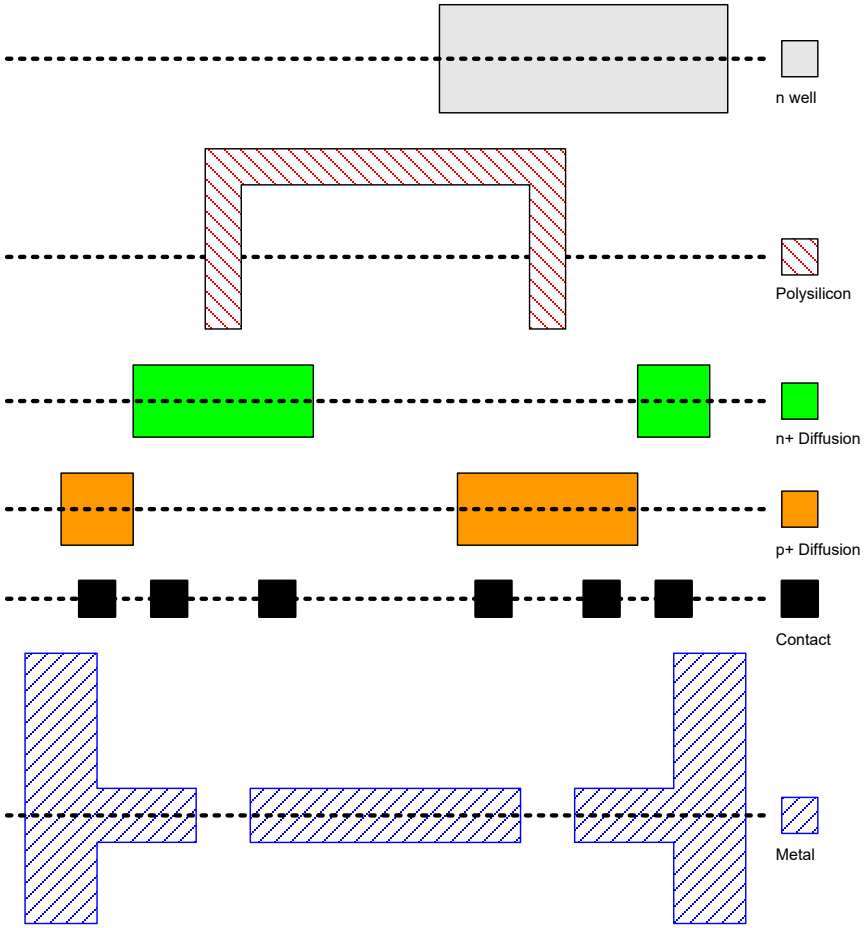
Inverter Mask Set (Top)

- Transistors and wires are defined by *masks*
- Cross-section taken along dashed line



Detailed Mask Views

- Six masks -- n-well
  - Polysilicon
  - n+ diffusion
  - p+ diffusion
  - Contact
  - Metal



Fabrication

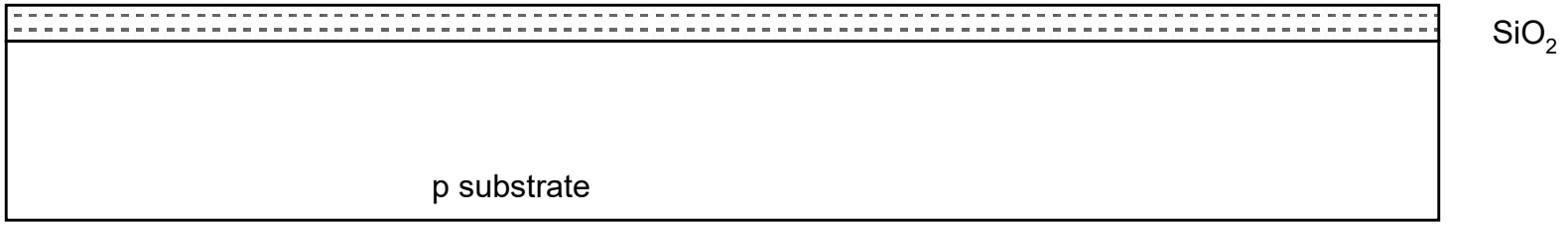
- Chips are built in huge factories called fabs
- Contain clean rooms as large as football fields

Fabrication Steps

- Start with blank wafer
- Build inverter from the bottom up
- First step will be to form the n-well
  - Cover wafer with protective layer of SiO_2 (oxide)
  - Remove layer where n-well should be built
  - Implant or diffuse n dopants into exposed wafer
  - Strip off SiO_2

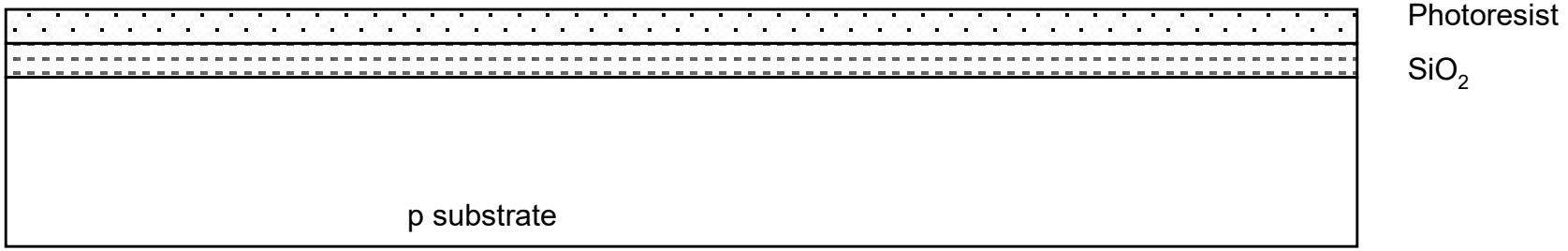
Oxidation

- Grow SiO_2 on top of Si wafer
  - 900 – 1200 ^oC with H_2O or O_2 in oxidation furnace



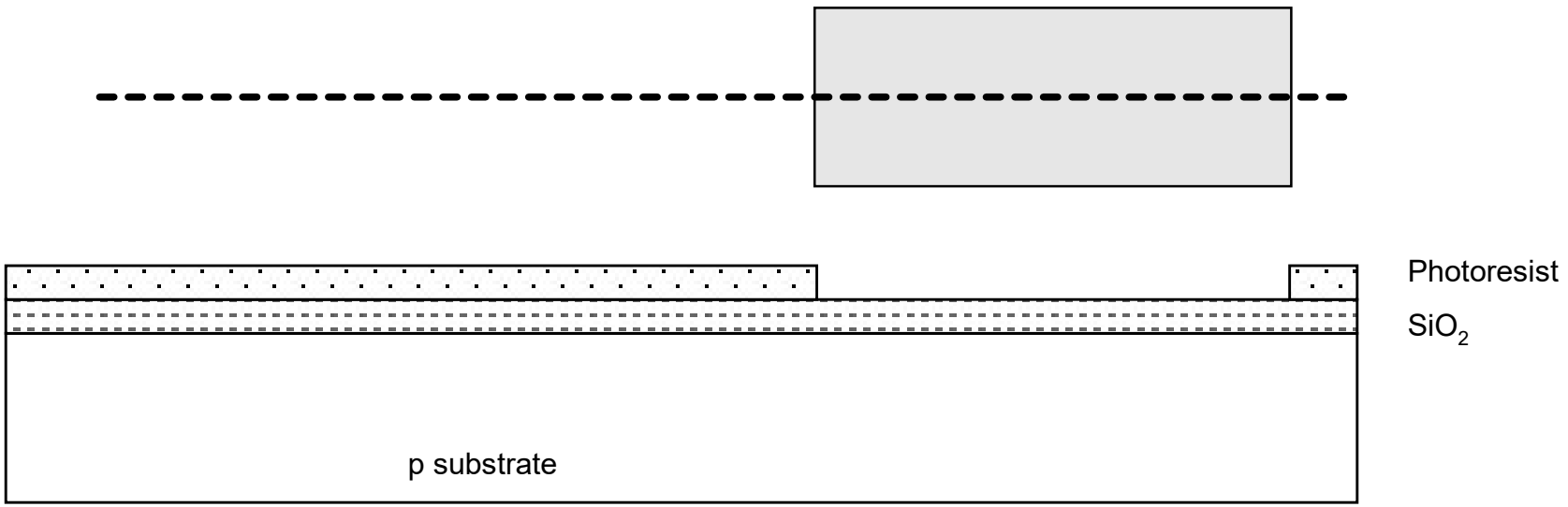
Photoresist

- Spin on photoresist
  - Photoresist is a light-sensitive organic polymer
  - Softens where exposed to light (ultraviolet)



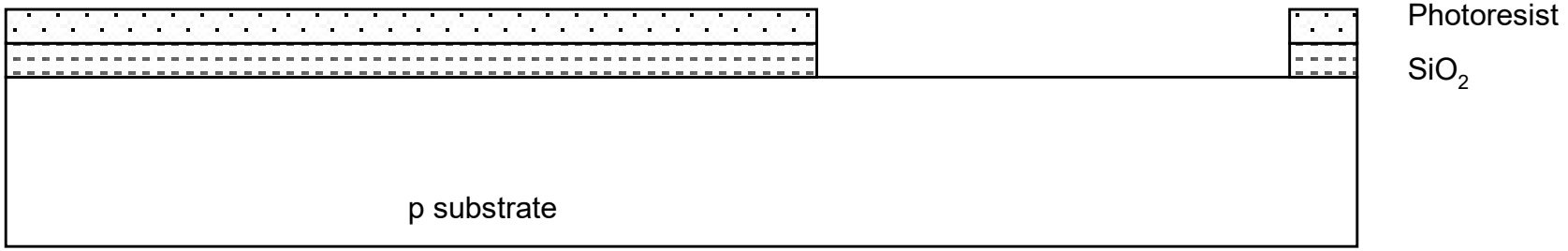
Lithography

- Expose photoresist through n-well mask
- Strip off exposed photoresist



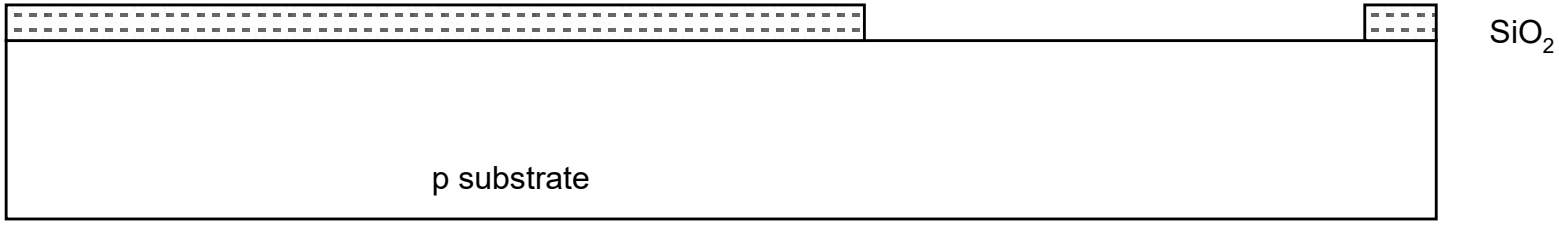
Etch

- Etch oxide with hydrofluoric acid (HF)
  - Seeps through skin and eats bone; nasty stuff!!!
- Only attacks oxide where resist has been exposed



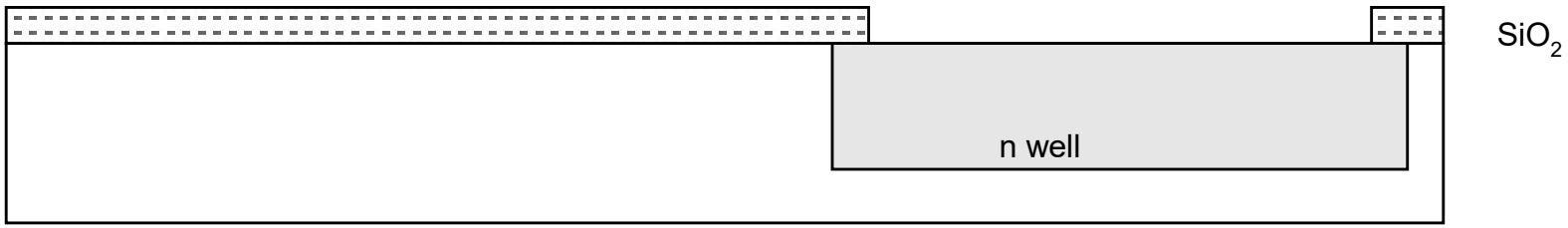
Strip Photoresist

- Strip off remaining photoresist
  - Use mixture of acids called piranah etch
- Necessary so photoresist doesn't melt in next step



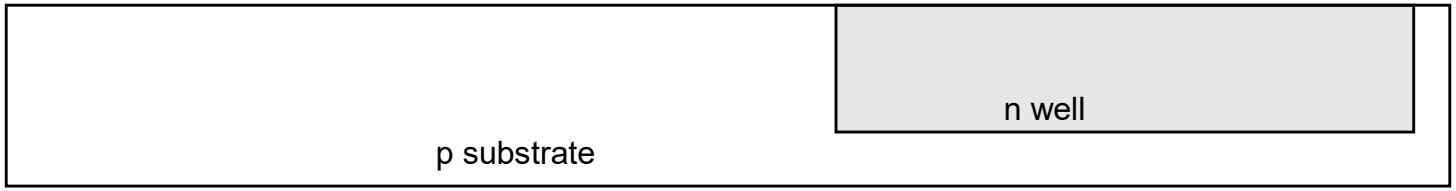
n-well

- n-well is formed with diffusion or ion implantation
- Diffusion
  - Place wafer in furnace with arsenic gas
  - Heat until As atoms diffuse into exposed Si
- Ion Implantation
  - Blast wafer with beam of As ions
  - Ions blocked by SiO_2, only enter exposed Si



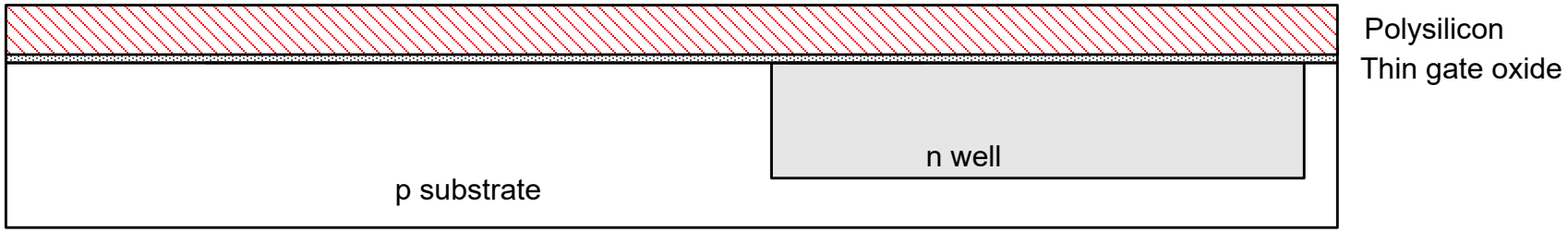
Strip Oxide

- Strip off the remaining oxide using HF
- Back to bare wafer with n-well
- Subsequent steps involve similar series of steps



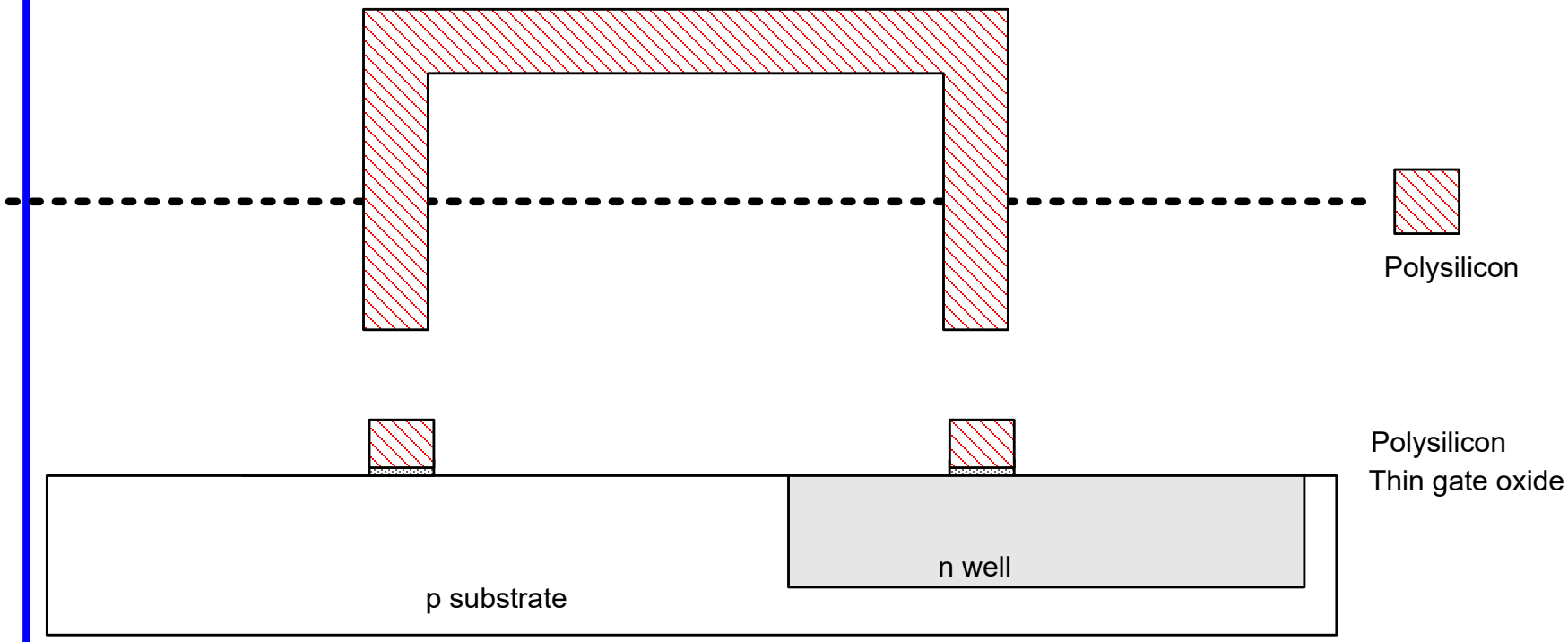
Polysilicon

- Deposit very thin layer of gate oxide
  - < 20 Å (6-7 atomic layers)
- Chemical Vapor Deposition (CVD) of silicon layer
  - Place wafer in furnace with Silane gas (SiH_4)
  - Forms many small crystals called polysilicon
  - Heavily doped to be good conductor



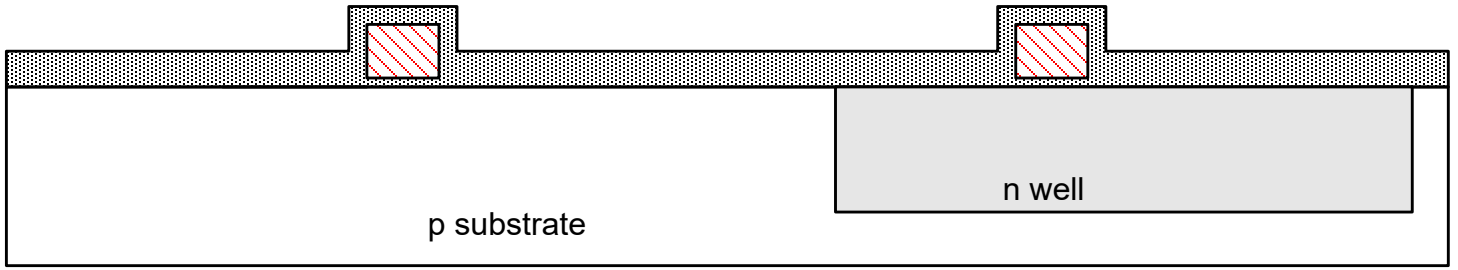
Polysilicon Patterning

- Use same lithography process to pattern polysilicon



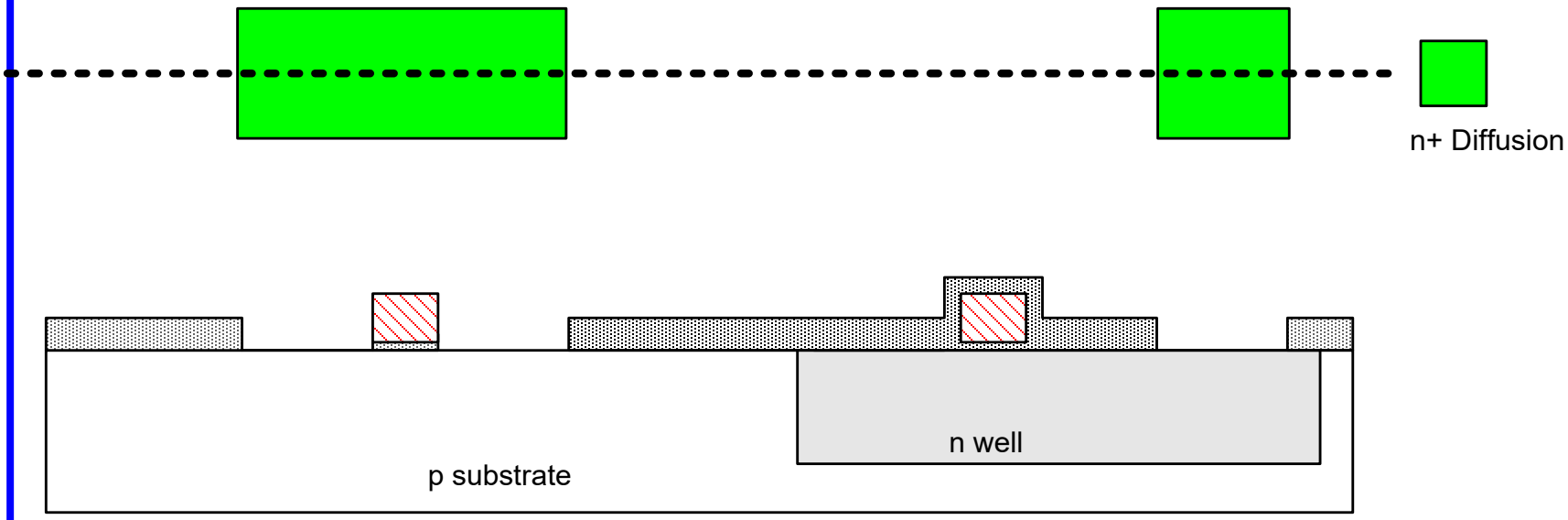
Self-Aligned Process

- Use oxide and masking to expose where n+ dopants should be diffused or implanted
- N-diffusion forms nMOS source, drain, and n-well contact



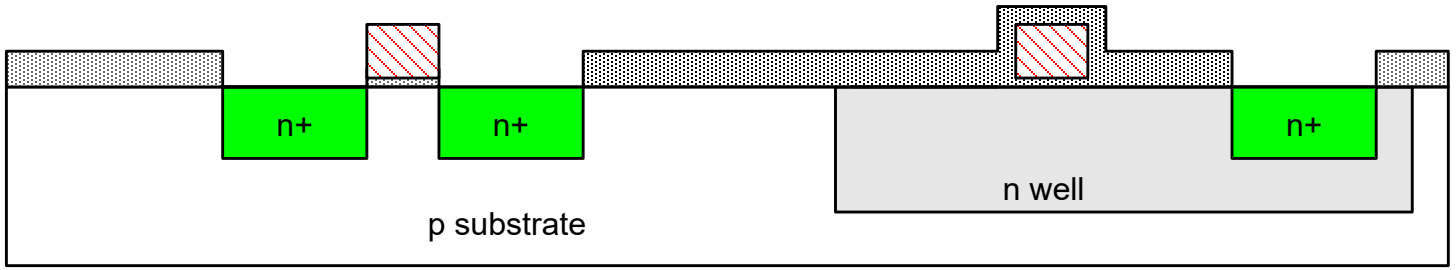
N-diffusion

- Pattern oxide and form n+ regions
- *Self-aligned process* where gate blocks diffusion
- Polysilicon is better than metal for self-aligned gates because it doesn't melt during later processing



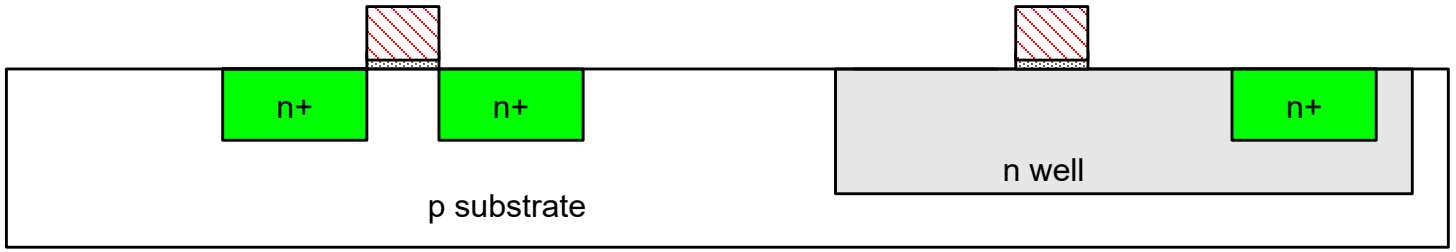
N-diffusion cont.

- Historically dopants were diffused
- Usually ion implantation today
- But regions are still called diffusion



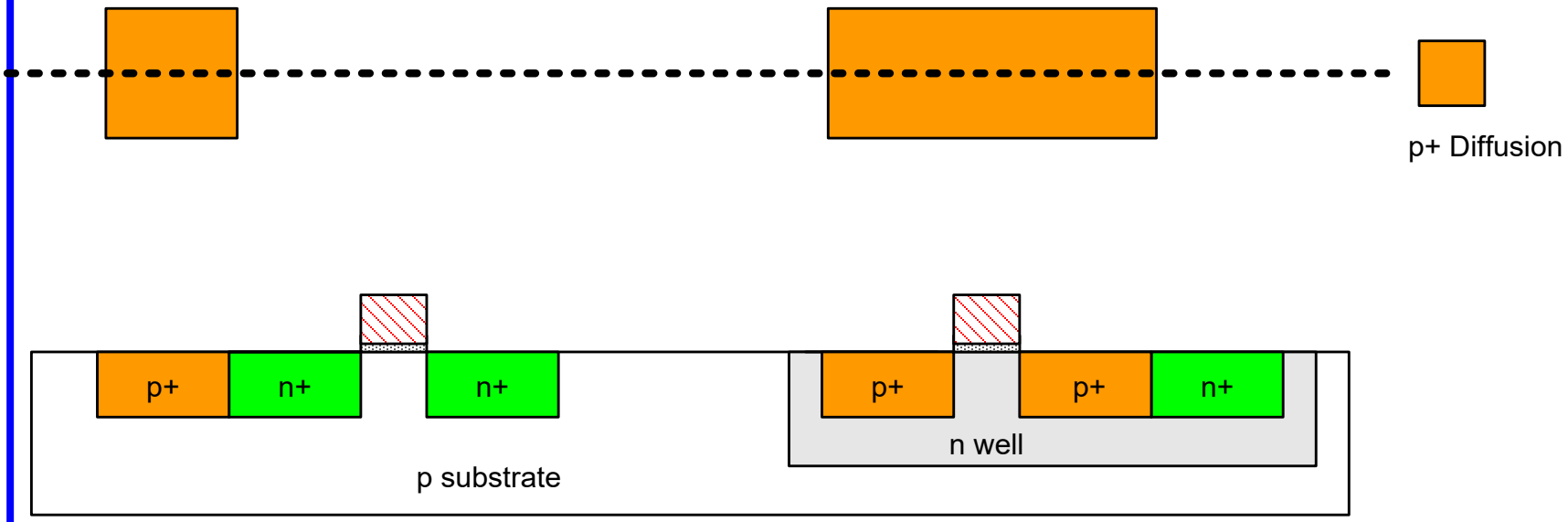
N-diffusion cont.

- Strip off oxide to complete patterning step



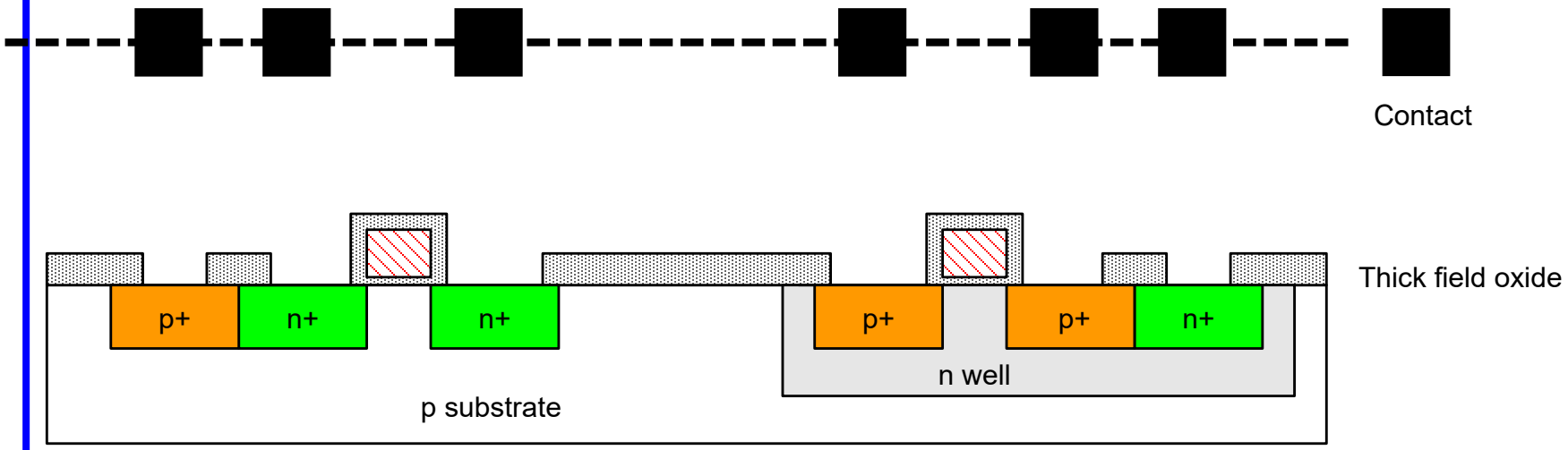
P-Diffusion

- Similar set of steps form p+ diffusion regions for pMOS source and drain and substrate contact



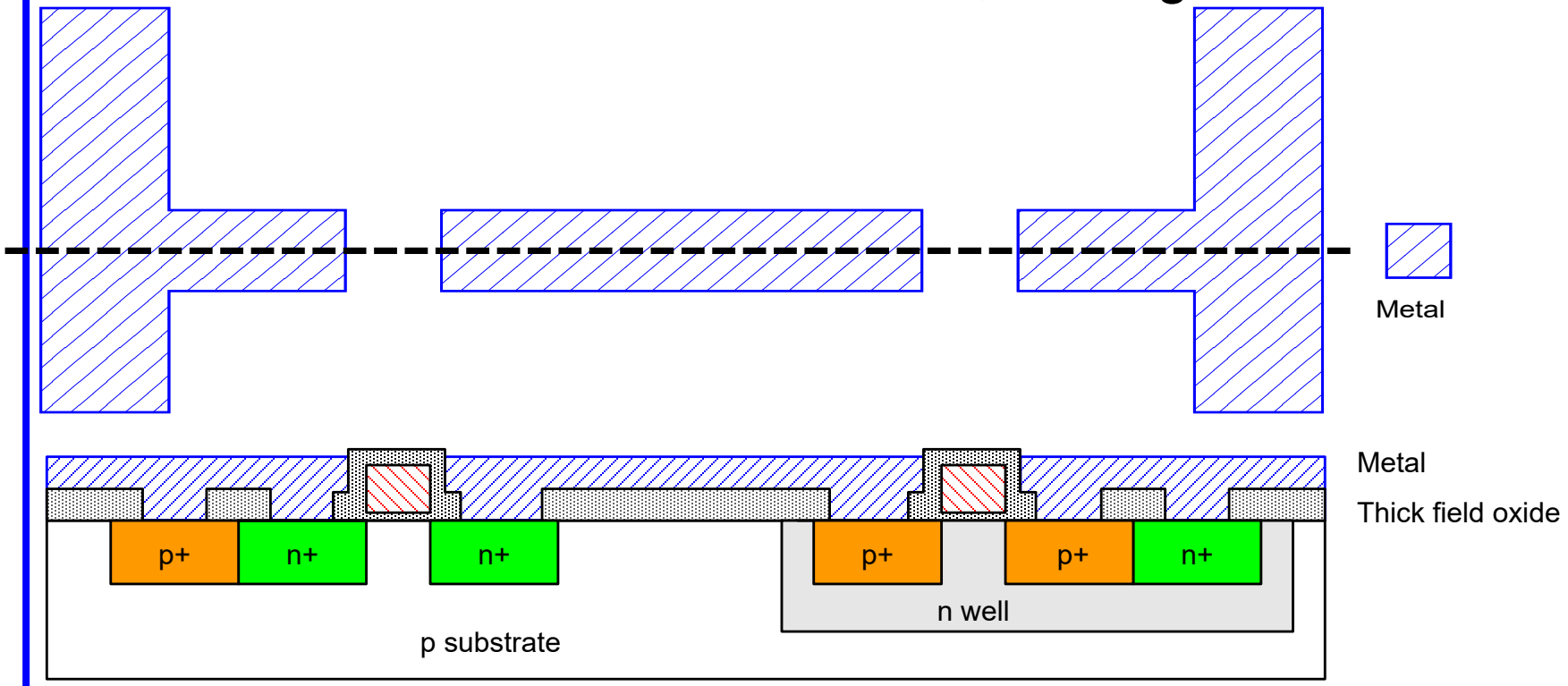
Contacts

- Now we need to wire together the devices
- Cover chip with thick field oxide
- Etch oxide where contact cuts are needed

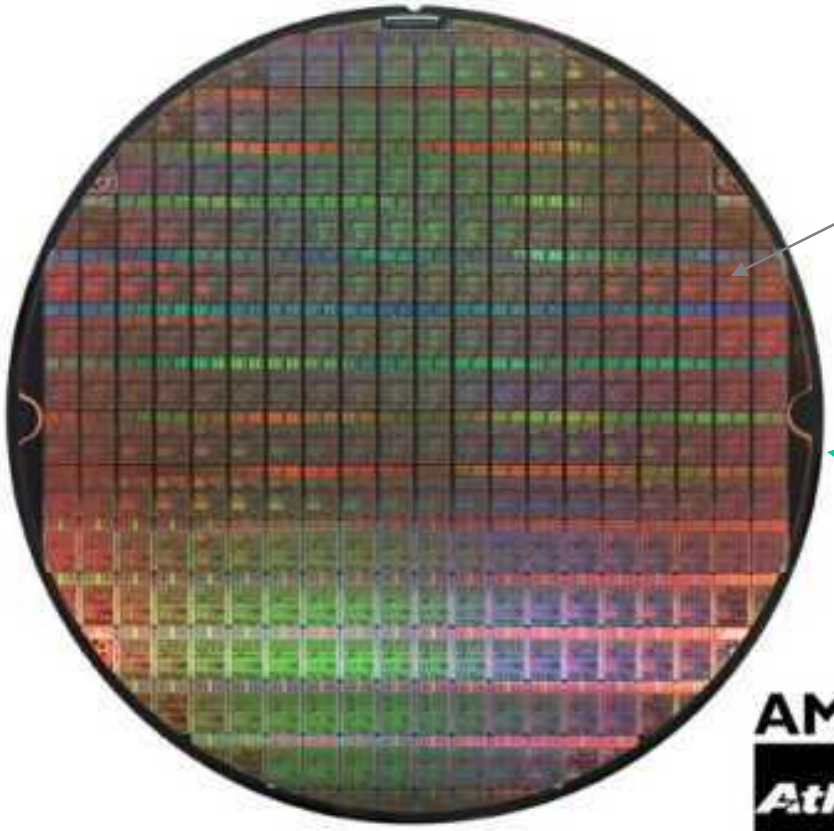


Metalization

- Sputter on aluminum/copper over whole wafer
- Pattern to remove excess metal, leaving wires



Die Cost



Single die

Wafer

AMD Athlon

Going up to 12" (30cm)

Summary

- MOS transistors are stacks of gate, oxide, silicon
- Threshold voltage (V_T) is the minimum voltage for V_{GS} to make the transistor on, which is process dependent.
- Act as electrically controlled switches
- Build logic gates out of switches
- Draw masks to specify layout of transistors
- Draw stick diagram
- Now you know everything necessary to start designing schematics and layout for a simple chip!