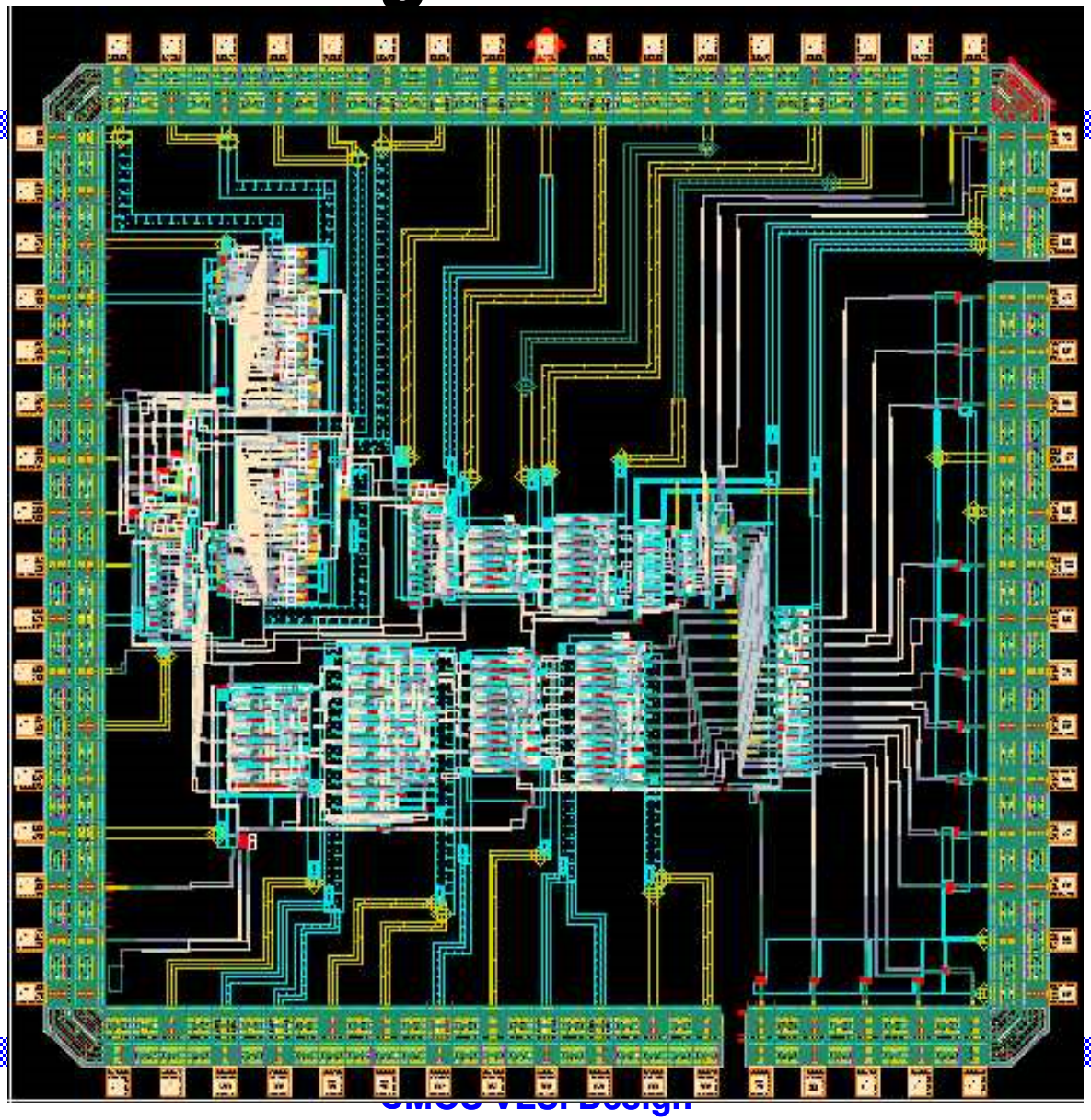
Wire Outline

- Introduction
- Interconnect Modeling
  - Wire Resistance
  - Wire Capacitance
- Wire RC Delay
- Crosstalk
- Wire Engineering
- Repeaters

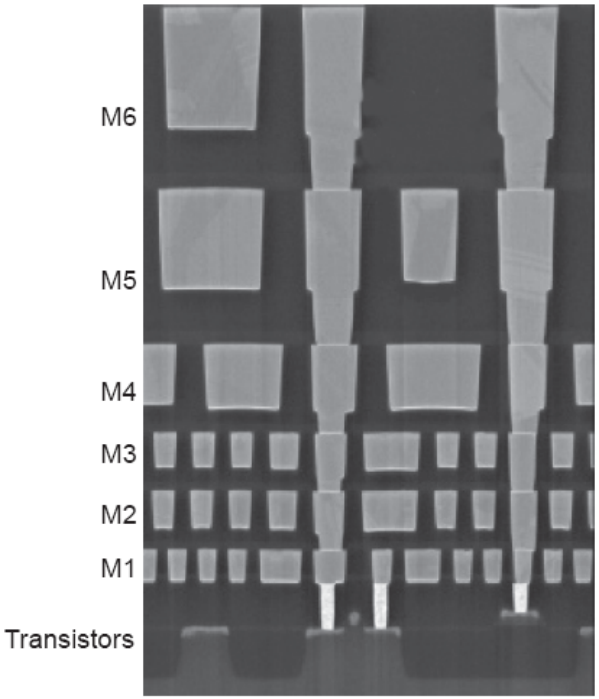
Introduction

- Chips are mostly made of wires called *interconnect*
  - In stick diagram, wires set size
  - Transistors are little things under the wires
  - Many layers of wires
- Wires are as important as transistors
  - Speed
  - Power
  - Noise
- Alternating layers run orthogonally

Layout of Two Stage Pipelined Delta Sigma ADC



Example



Intel 90 nm Stack

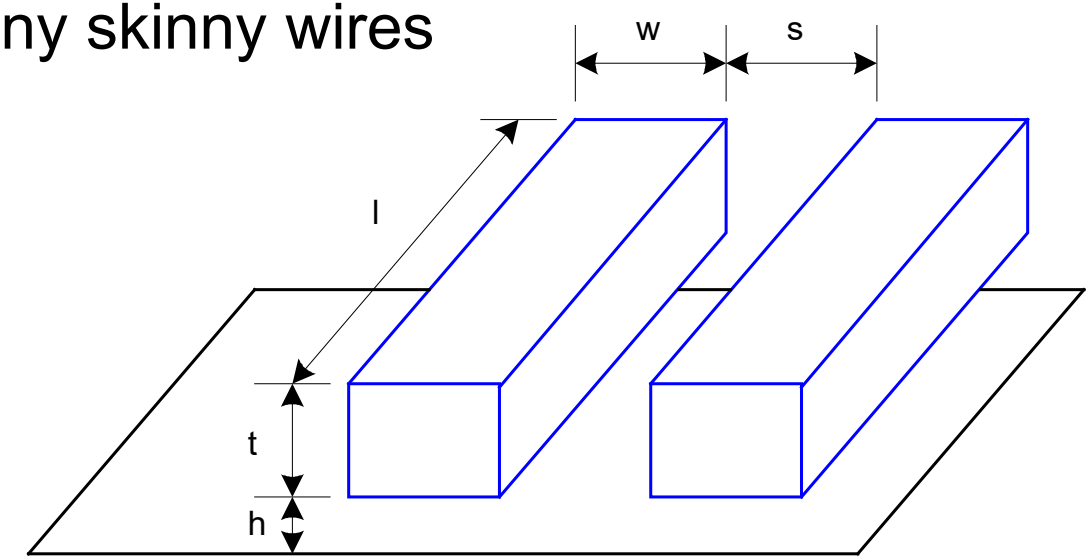
[Thompson02]

Intel 45 nm Stack

[Moon08]

Wire Geometry

- Pitch = w + s
- Aspect Ratio: AR = t/w
  - Old processes had AR << 1
  - Modern processes have AR ≈ 2
    - Pack in many skinny wires

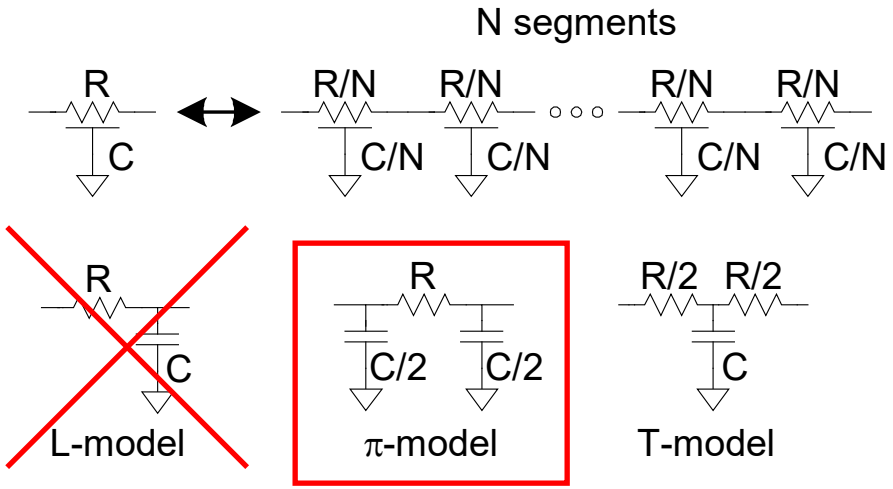


Layer Stack

- AMI (On) Semiconductor 0.6 μm process has 3 metal layers
  - M1 for within-cell routing
  - M2 for vertical routing between cells
  - M3 for horizontal routing between cells
- Modern processes use 6-10+ metal layers
  - M1: thin, narrow (< 3λ)
    - High density cells
  - Mid layers
    - Thicker and wider, (density vs. speed)
  - Top layers: thickest
    - For V_{DD}, GND, clk

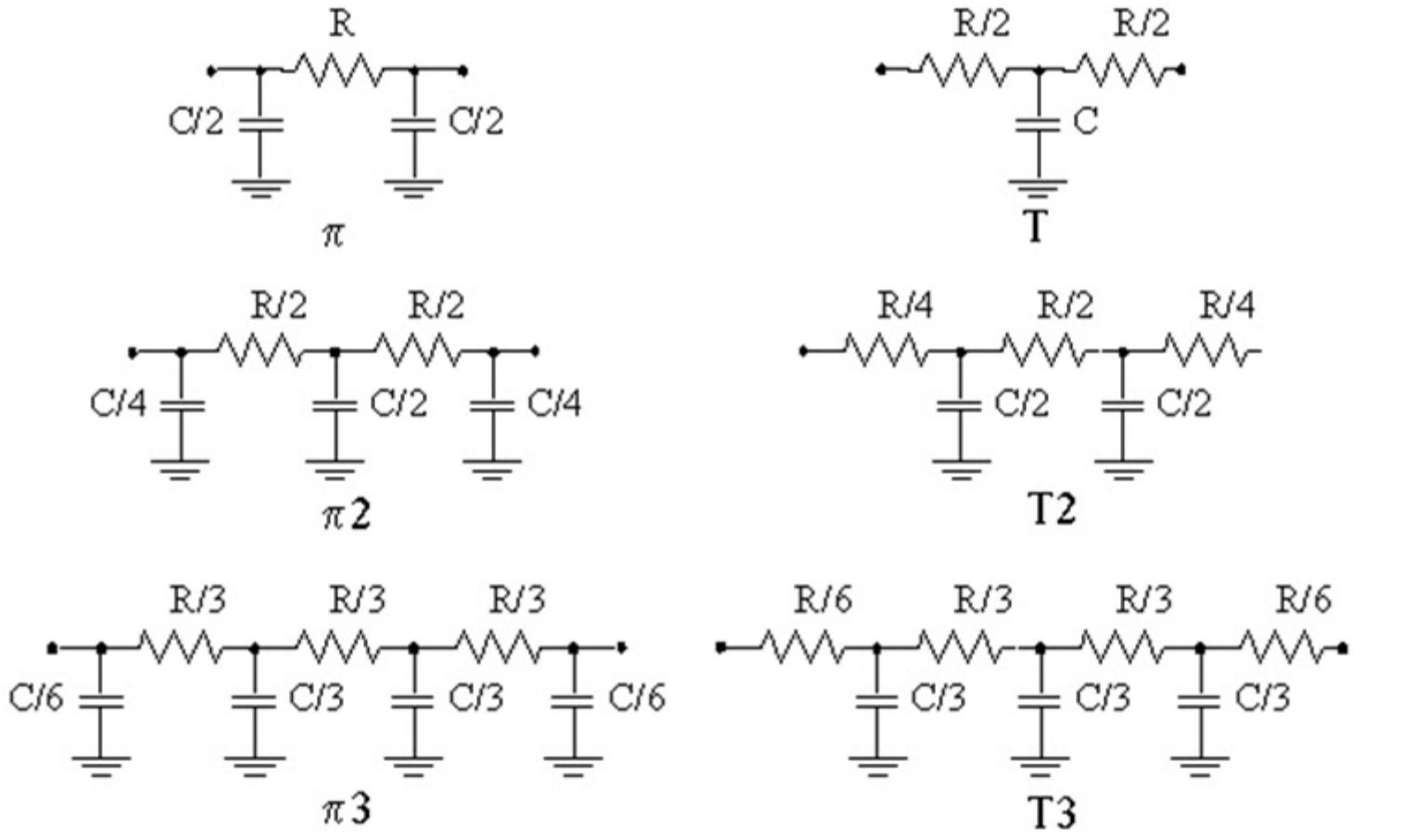
Lumped Element Models

- Wires are a distributed system
  - Approximate with lumped element models



- 3-segment π-model is accurate to 3% in simulation
- L-model needs 100 segments for same accuracy!
- T model is harder to be solved
- Use single segment π-model for Elmore delay

Multi-segment Models

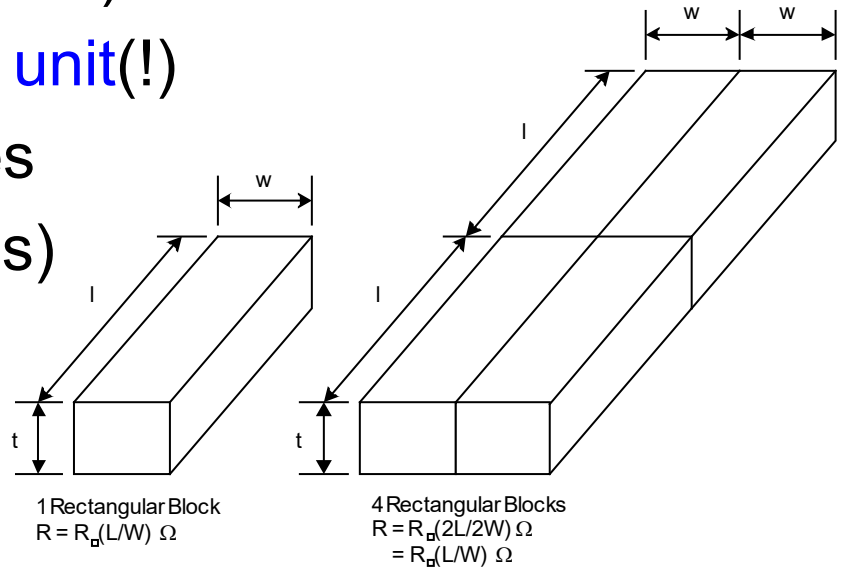


Wire Resistance

- ρ = *resistivity* (Ω*m)

$$R = \frac{\rho}{t}\frac{l}{w} = R_{\square}\frac{l}{w}$$

- $R_{\square}$ = *sheet resistance* ($\Omega/\square$)
  - $\square$ is a dimensionless unit(!)
- Count number of squares
  - $R = R_{\square}$ * (# of squares)



Choice of Metals

- Until 180 nm generation, most wires were aluminum
- Contemporary processes normally use copper
  - Cu atoms diffuse into silicon and damage FETs
  - Must be surrounded by a diffusion barrier

Metal	**Bulk resistivity ρ ($\mu\Omega \cdot$ cm)**
Silver (Ag)	1.6
Copper (Cu)	1.7
Gold (Au)	2.2
Aluminum (Al)	2.8
Tungsten (W)	5.3
Titanium (Ti)	43.0

Typical Sheet Resistance

- Sheet resistance for 180nm process with Aluminum interconnect

Table 4.7 Sheet resistances

Layer	Sheet Resistance (Ω /□)
Diffusion (silicided)	3-10
Diffusion (unsilicided)	50-200
Polysilicon (silicided)	3-10
Polysilicon (unsilicided)	50-400
Metal1	0.08
Metal2	0.05
Metal3	0.05
Metal4	0.03
Metal5	0.02
Metal6	0.02

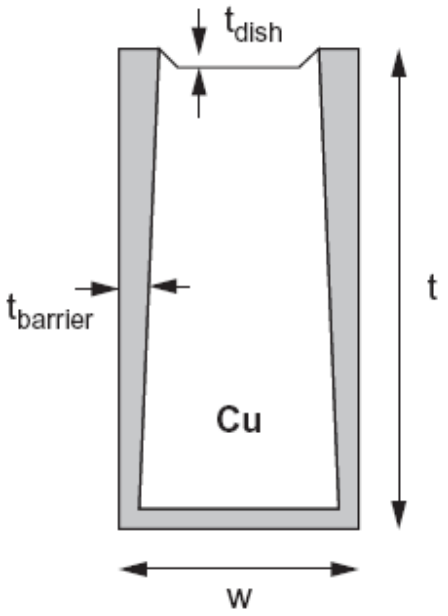
Contacts Resistance

- Contacts and vias also have 2-20 Ω
- Use many contacts for lower R
  - Many small contacts for current crowding around periphery

Copper Issues

- Copper wires diffusion barrier has high resistance
- Copper is also prone to *dishing* during polishing
- Effective resistance is higher

$$R = \frac{\rho}{(t - t_{\text{dish}} - t_{\text{barrier}})} \frac{l}{(w - 2t_{\text{barrier}})}$$



Example

- Compute the sheet resistance of a 0.17 μm thick Cu wire in a 65 nm process. Ignore dishing.

$$R_{\square} =$$

- Find the total resistance if the wire is 0.125 μm wide and 1 mm long. Ignore the barrier layer.

$$R =$$

Example

- Compute the sheet resistance of a 0.17 μm thick Cu wire in a 65 nm process. Ignore dishing.

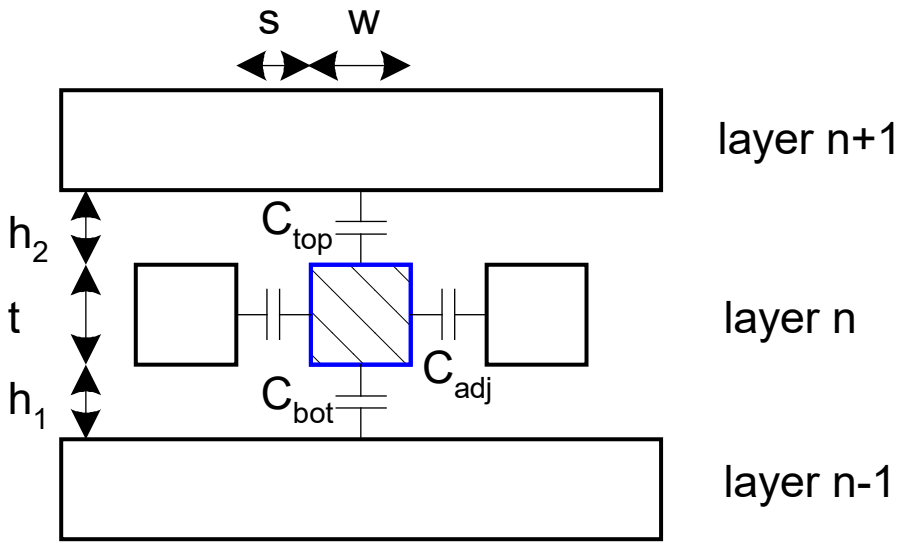
$$R_{\square} = \frac{1.7 \times 10^{-8}\ \Omega\,\square\,\text{m}}{.17\ \times 10^{-6}\ \text{m}} = 0.10\ \Omega/\square$$

- Find the total resistance if the wire is 0.125 μm wide and 1 mm long. Ignore the barrier layer.

$$R = \left(0.10\ \Omega/\square\right)\frac{1000\ \mu\text{m}}{0.125\ \mu\text{m}} = 800\ \Omega$$

Wire Capacitance

- Wire has capacitance per unit length
  - To neighbors
  - To layers above and below
- $C_{total} = C_{top} + C_{bot} + 2C_{adj}$



Capacitance Trends

- Parallel plate equation: $C = \varepsilon_{ox} A/d$
  - Wires are not parallel plates, but obey trends
  - Increasing area (W, t, L) increases capacitance
  - Increasing distance (s, h) decreases capacitance
- Dielectric constant (permittivity)
  - $\varepsilon_{ox} = k\varepsilon_0$
    - $\varepsilon_0 = 8.85 \times 10^{-14}$ F/cm
    - k = 3.9 for SiO_2
- Processes are starting to use low-k dielectrics
  - $k \approx 3$ (or less) as dielectrics use air pockets

Capacitance Formula

- Capacitance of a line without neighbors can be approximated as

$$C_{tot} = \varepsilon_{ox} l \left[\frac{w}{h} + 0.77 + 1.06 \left(\frac{w}{h} \right)^{0.25} + 1.06 \left(\frac{t}{h} \right)^{0.5} \right] \approx l * C/\mu m$$

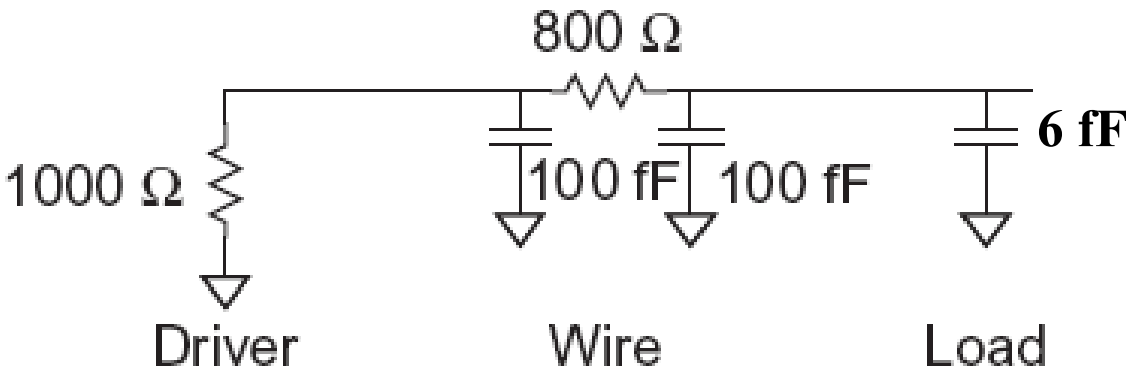
- This empirical formula is accurate to 6% for AR < 3.3

Diffusion & Polysilicon

- Diffusion capacitance is very high (1-2 fF/μm)
  - Comparable to gate capacitance
  - Diffusion also has high resistance
  - Avoid using diffusion *runners* for wires!
- Polysilicon has lower C but high R
  - Use for transistor gates
  - Occasionally for very short wires between gates

Wire RC Delay

- Estimate the delay of a 30 units inverter driving a 6 units inverter at the end of the 1 mm copper wire (0.17um thickness and 0.125um width). Assume wire capacitance is 0.2 fF/μm and that a unit-sized inverter has R = 10 KΩ for nMOS and C = 1.0 fF.
  - t_{pd} =



Wire RC Delay

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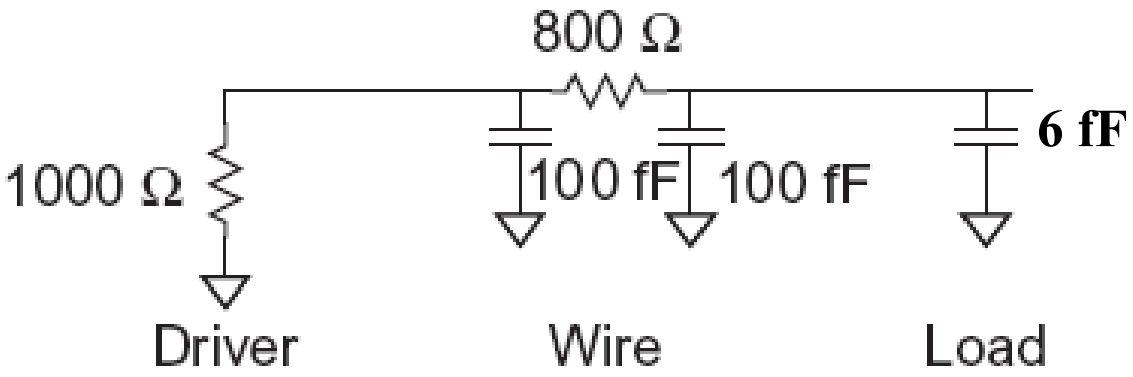
  - t_{pd} = (1000 Ω)(130 fF) + (1000 + 800) Ω (100 + 6) fF = 320.8 ps



Wire Energy

- Estimate the energy per unit length (mm) to send a bit of information (one rising and one falling transition) in a CMOS process (65 nm, Vdd=1.0v).

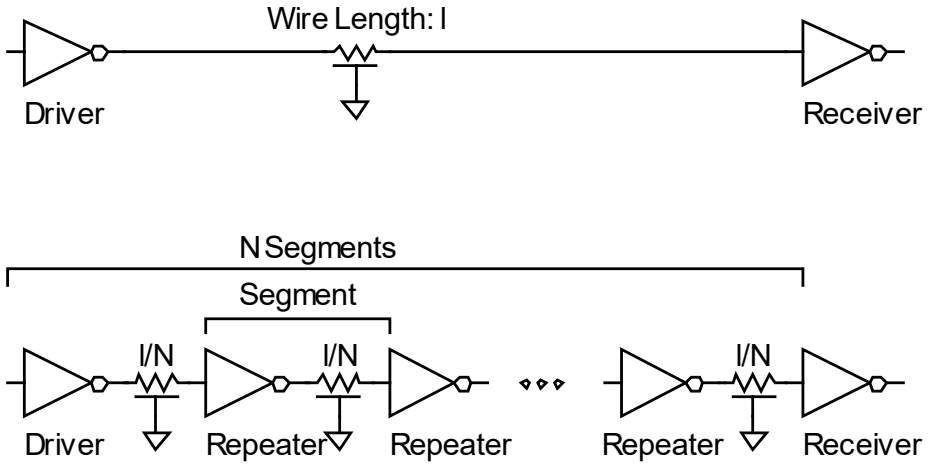
- $E = CV^2$

  $= (0.2\ pF/mm)(1.0\ V)^2$ $= 0.2\ pJ/bit/mm$

  $= 0.2\ mW/(Gb/s)/mm$

Repeaters

- R and C are proportional to L
- RC delay is proportional to L^2
  - Unacceptably great for long wires
- Break long wires into N shorter segments
  - Drive each one with an inverter or buffer



Repeater Design

- How many repeaters should we use?
- How large should each one be?
- Equivalent Circuit-- Wire has resistance R_w and C_w per unit length
  - Single wire segment--wire length = *L/N*
    - Wire Capacitance C_w*L/N, Resistance R_w*L/N
  - Inverter width 3W (nMOS = W, pMOS = 2W)
    - Gate Capacitance C'*W, Resistance R/W, C'=3C_{unit}

Repeater Results

- Write equation for Elmore Delay

The Elmore delay of each segment is

$$t_{pd-seg} = \frac{R}{W}\left(\frac{C_w l}{N} + C'W\right) + \left(\frac{R_w l}{N}\right)\left(\frac{C_w l}{2N} + C'W\right)$$

The total delay is N times greater:

$$t_{pd} = NRC' + L\left(R_w C'W + \frac{RC_w}{W}\right) + L^2\frac{R_w C_w}{2N}$$

Take the partial derivatives with respect to N and W and set them to 0 to minimize delay:

$$\frac{\partial t_{pd}}{\partial N} = RC' - l^2\frac{R_w C_w}{2N^2} = 0 \Rightarrow N = l\sqrt{\frac{R_w C_w}{2RC'}}$$

$$\frac{\partial t_{pd}}{\partial W} = l\left(R_w C' - \frac{RC_w}{W^2}\right) = 0 \Rightarrow W = \sqrt{\frac{RC_w}{R_w C'}}$$

Repeater Results

- Summary

The best length of wire between repeaters is $\frac{l}{N} = \sqrt{\frac{2RC'}{R_w C_w}}$

The best number of segment, **N=?**

The delay per unit length is

$$\frac{t_{pd}}{l} = \left(2+\sqrt{2}\right)\sqrt{RC'R_w C_w}$$

~40 ps/mm

in 65 nm process

The total delay of the entire length is ?

The inverter nMOS transistor width is $W = \sqrt{\frac{RC_w}{R_w C'}}$

Repeater Example(1)

- Determine the best distance between repeaters for a minimum pitch metal2 line in a 180 nm process for least delay. Assume the unit transistor resistance is 3 kΩ.μm, the gate unit capacitance is C=1.7 fF/μm, and the metal2 per unit length capacitance is C_w=0.21 fF/μm, resistance is R_w=0.16 Ω /μm.

  1) How far should the repeater be spaced?

$$\text{repeaters spaced} = \frac{l}{N} = \sqrt{\frac{2RC'}{R_w C_w}} = \sqrt{\frac{2(3000\Omega \cdot \mu m)\left(5.1\frac{fF}{\mu m}\right)}{\left(0.16\frac{\Omega}{\mu m}\right)\left(0.21\frac{fF}{\mu m}\right)}} = 950\mu m$$

C'=3C= 5.1 fF/μm

Repeater Example(2)

- Determine the best distance between repeaters for a minimum pitch metal2 line in a 180 nm process. Assume the unit transistor resistance is 3 kΩ.μm, the gate unit capacitance is C=1.7 fF/μm, and the metal2 per unit length capacitance is C_w=0.21 fF/μm, resistance is R_w=0.16 Ω /μm.
  1) How far should the repeater be spaced?
  2) How wide should the repeater transistor be?

$$W = \sqrt{\frac{RC_w}{R_w C'}} = \sqrt{\frac{(3000\Omega \cdot \mu m)\left(0.21\frac{fF}{\mu m}\right)}{\left(0.16\frac{\Omega}{\mu m}\right)\left(5.1\frac{fF}{\mu m}\right)}} = 28\mu m = Wn,\ Wp \approx 2Wn$$

Repeater Example(3)

- Determine the best distance between repeaters for a minimum pitch metal2 line in a 180 nm process. Assume the unit transistor resistance is 3 kΩ.μm, the gate unit capacitance is C=1.7 fF/μm, and the metal2 per unit length capacitance is C_w=0.21 fF/μm, resistance is R_w=0.16 Ω /μm.

3) What is the delay per unit length (mm) of the wire

delay per unit length

$$= \left(2+\sqrt{2}\right)\sqrt{RC \cdot R_w C_w}$$

$$= \left(2+\sqrt{2}\right)\sqrt{(3000\Omega \cdot \mu m)\left(5.1\frac{fF}{\mu m}\right)\left(0.16\frac{\Omega}{\mu m}\right)\left(0.21\frac{fF}{\mu m}\right)}$$

$$= 77\frac{\text{ps}}{\text{mm}}$$

Repeater Example(4)

- Determine the best distance between repeaters for a minimum pitch metal5 line in a 180 nm process. Assume the transistor resistance is 3 kΩ.μm, the gate capacitance is C=1.7 fF/μm, and the metal5 capacitance is C_w=0.24 fF/μm, resistance is R_w=0.025 Ω /μm.
  1) How far should the repeater be spaced? (2260 um)
  2) How wide should the repeater transistor be? (W = 75um)
  3) What is the signal delay per unit length of the wire? (30 ps/mm)

Summary: wide upper level metal lines are faster, but take more space. Therefore, they are precious routing resource

Repeater Energy

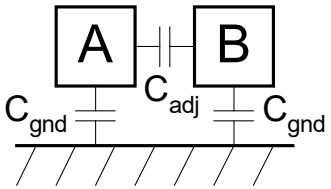
- Energy / length ≈ $1.87C_wV_{DD}^2$
  - 87% premium over unrepeated wires
  - The extra power is consumed in the large repeaters
- If the repeaters are downsized for minimum EDP:
  - Energy premium is only 30%
  - Delay increases by 14% from min delay

Crosstalk

- A capacitor does not like to change its voltage instantaneously.
- A wire has high capacitance to its neighbor.
  - When the neighbor switches from 1-> 0 or 0->1, the wire tends to switch too.
  - Called capacitive *coupling* or *crosstalk*.
- Crosstalk effects
  - Noise on nonswitching wires
  - Increased delay on switching wires

Crosstalk Delay

- Assume layers above and below on average are quiet
  - Second terminal of capacitor can be ignored
  - Model as $C_{gnd} = C_{top} + C_{bot}$
- Effective C_{adj} depends on behavior of neighbors
  - *Miller effect*
  - *MCF—Miller Coupling Factor*

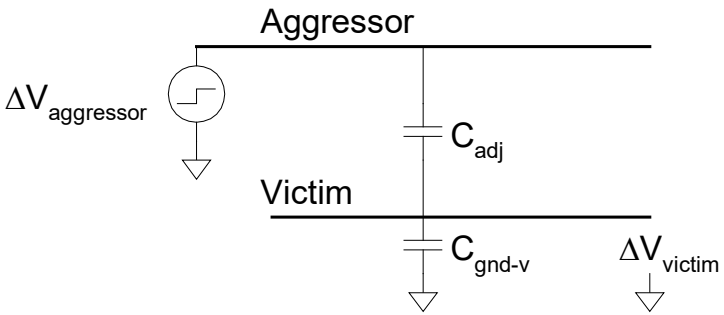


B	**ΔV**	**$C_{eff(A)}$**	**MCF**
Constant	V_{DD}	$C_{gnd} + C_{adj}$	1
Switching with A	0	C_{gnd}	0
Switching opposite A	$2V_{DD}$	$C_{gnd} + 2\,C_{adj}$	2

Crosstalk Noise

- Crosstalk causes noise on nonswitching wires
- If victim is floating:
  - model as capacitive voltage divider

$$\Delta V_{victim} = \frac{C_{adj}}{C_{gnd-v} + C_{adj}} \Delta V_{aggressor}$$

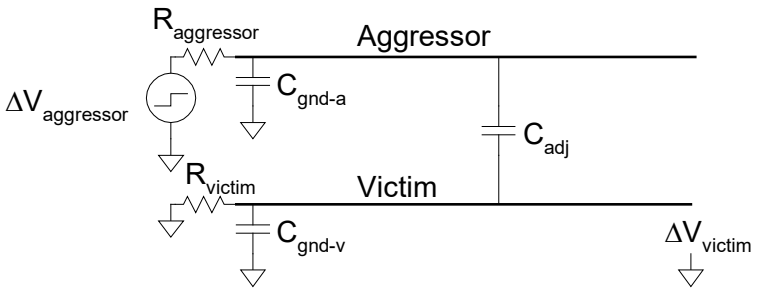


Driven Victims

- Usually victim is driven by a gate that fights noise
  - Noise depends on relative resistances
  - Victim driver is in linear region, aggressor in saturation
  - If sizes are same, $R_{aggressor}$ = 2-4 x R_{victim}

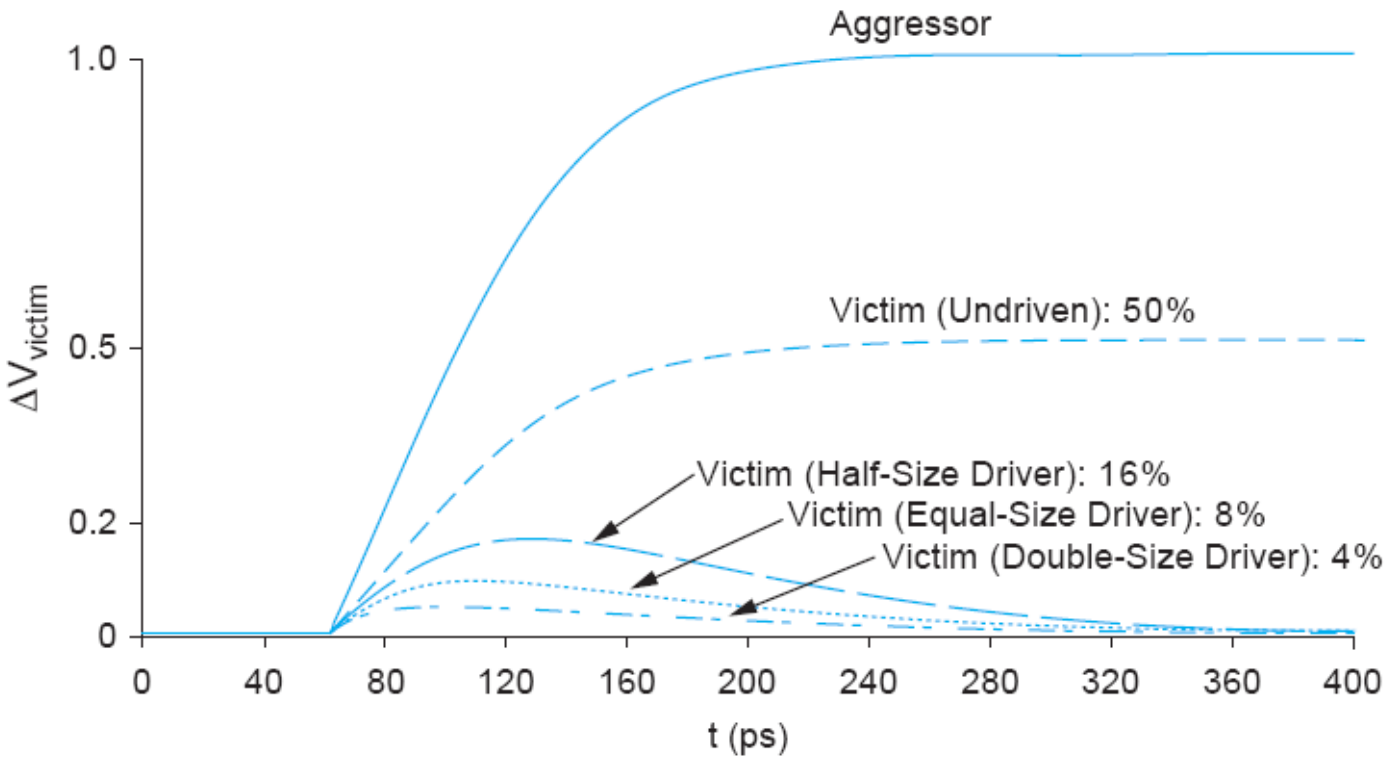
$$\Delta V_{victim} = \frac{C_{adj}}{C_{gnd-v} + C_{adj}} \frac{1}{1+k} \Delta V_{aggressor}$$

$$k = \frac{\tau_{aggressor}}{\tau_{victim}} = \frac{R_{aggressor}\left(C_{gnd-a} + C_{adj}\right)}{R_{victim}\left(C_{gnd-v} + C_{adj}\right)}$$



Coupling Waveforms

- Simulated coupling for $C_{adj} = C_{victim}$



Noise Implications

- *So what* if we have noise?
- If the noise is less than the noise margin, nothing happens to digital circuits
- Static CMOS logic will eventually settle to correct output even if disturbed by large noise spikes
  - But glitches cause extra delay
  - Also cause extra power from false transitions
- Dynamic logic never recovers from glitches
- Memories and other sensitive circuits also can produce the wrong answer

Wire Engineering

- Goal: achieve delay, area, power goals with acceptable noise
- Degrees of freedom:
  - Width
  - Spacing
  - Layer
  - Shielding