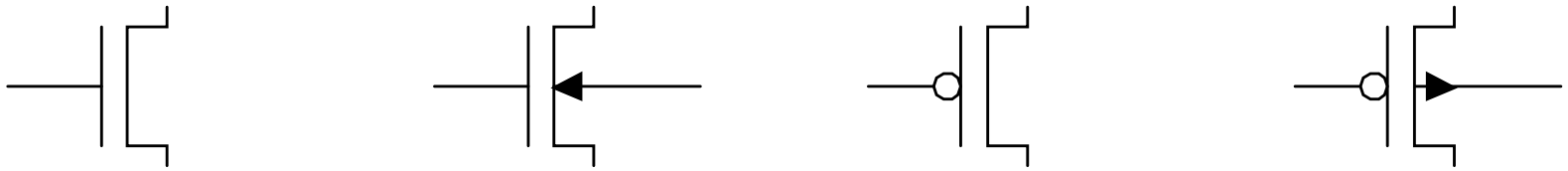
CMOS Transistor Theory Outline

- Introduction
- MOS Capacitor
- nMOS I-V Characteristics
- pMOS I-V Characteristics
- Gate and Diffusion Capacitance

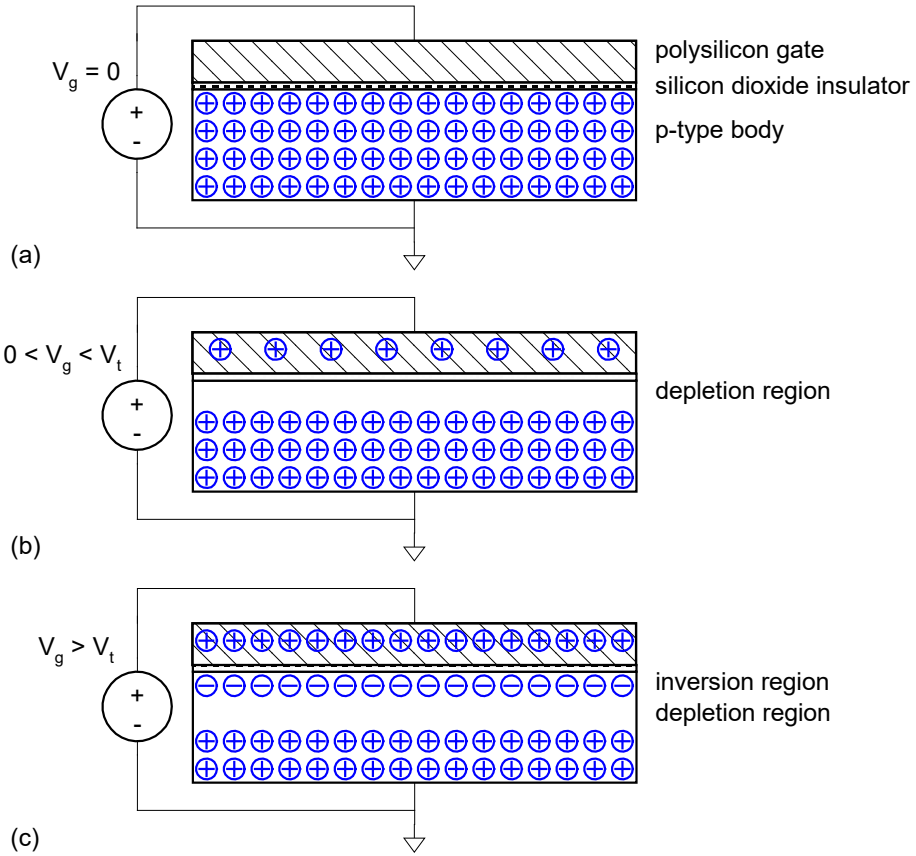
Introduction

- So far, we have treated transistors as ideal switches
- An ON transistor passes a finite amount of current
  - Depends on terminal voltages
  - Derive current-voltage (I-V) relationships
- Transistor gate, source, drain all have capacitance
  - $I = C (\Delta V/\Delta t) = \Delta Q/\Delta t \rightarrow \Delta t = (C/I)\, \Delta V$
  - Capacitance and current determine speed



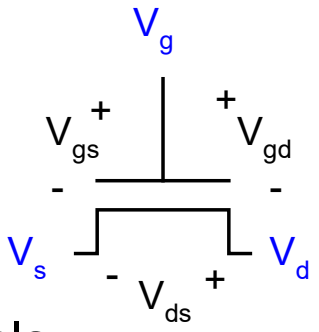
MOS Capacitor

- Gate and body form MOS capacitor
- Operating modes
  - Accumulation
  - Depletion
  - Inversion



NMOS Terminal Voltages

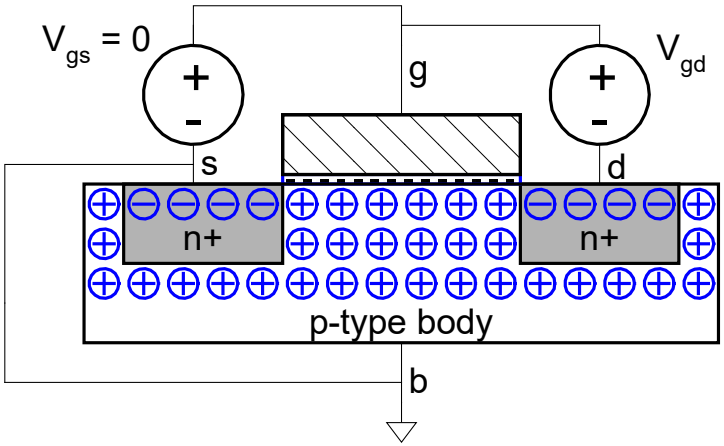
- Mode of operation depends on V_g, V_d, V_s
  - $V_{gs} = V_g - V_s$
  - $V_{gd} = V_g - V_d$
  - $V_{ds} = V_d - V_s = V_{gs} - V_{gd}$

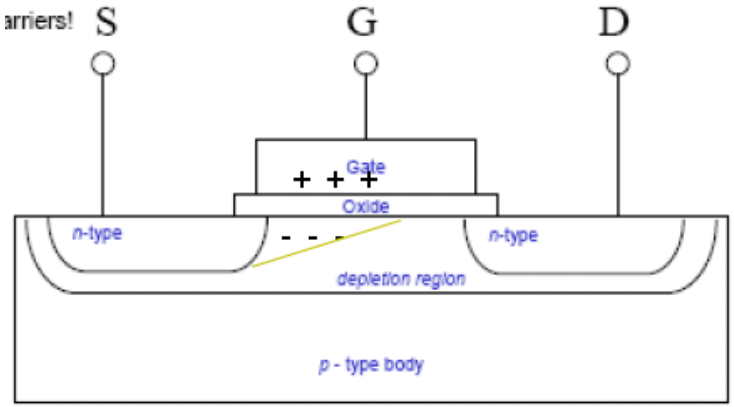


- Source and drain are symmetric diffusion terminals
  - By convention, source is terminal at lower voltage for nMOS
  - Hence $V_{ds} \geq 0$
- nMOS body is grounded. First assume source is 0 too.
- Three regions of operation
  - *Cutoff*
  - *Linear*
  - *Saturation*

nMOS Cutoff Region

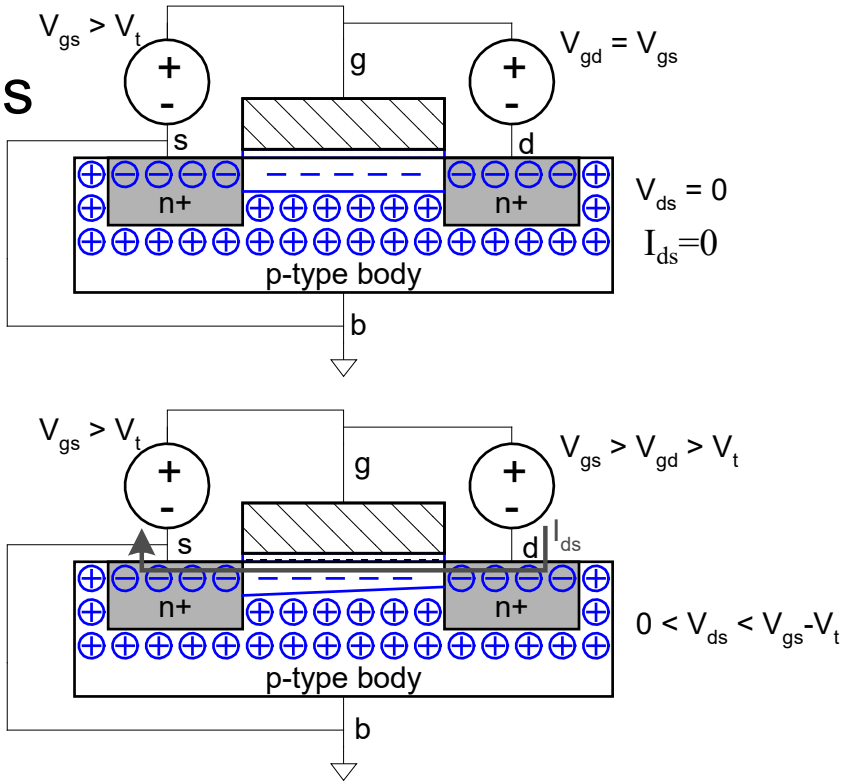
- Vgs<Vt
- No channel
- $I_{ds} = 0$





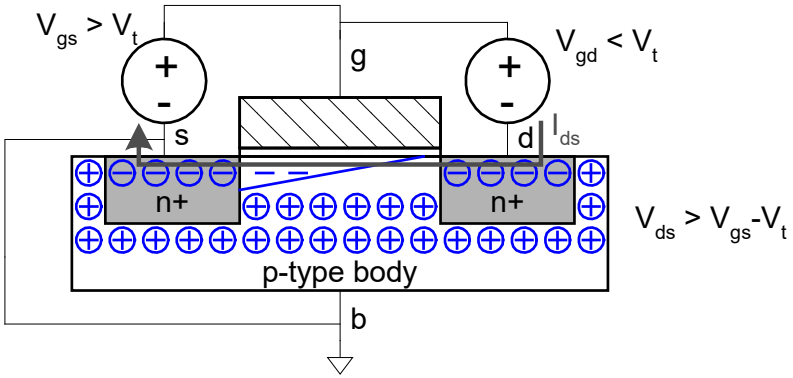
nMOS Linear (Resistive) Region

- Vgs>Vth, channel forms, but no current if Vds=0
- Until Vds>0
  - Current flows from d to s
  - e^- from s to d
- I_{ds} increases with V_{ds}
- Similar to linear resistor



nMOS Saturation

- As Vds increased, Vgd is getting smaller, the channel of drain side is getting narrower
- When $V_{gd} <= V_t$, channel pinches off, the channel is no longer inverted near the drain. Conduction is brought about by the drift of electrons under the influence of the positive drain voltage.
- I_{ds} is independent of V_{ds}, only controlled by V_{gs} for long channel
- We say current saturates
- Similar to current source

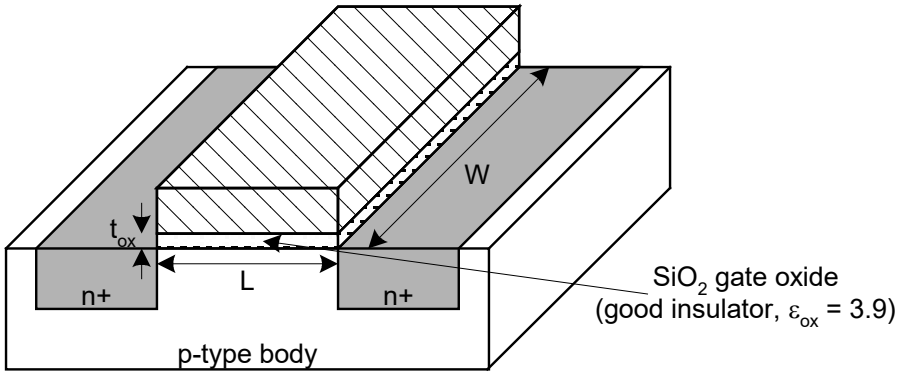


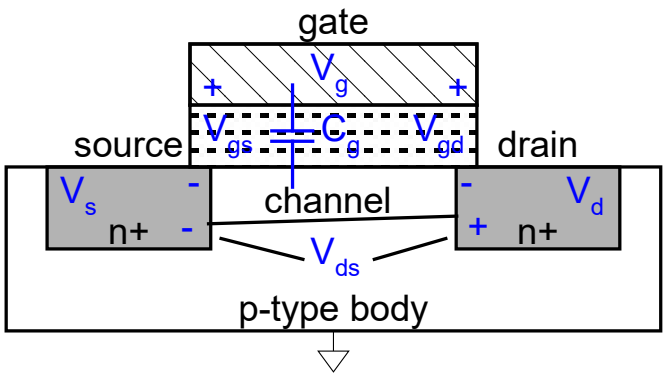
nMOS I-V Characteristics

- In Linear region, I_{ds} depends on
  - How much charge is in the channel?
  - How fast is the charge moving?

N Channel Charge

- MOS structure looks like parallel plate capacitor while operating in inversion
  - Gate – oxide – channel
- Charge on each plate of the capacitor is $Q_{channel} = CV$
- $C = C_g = \varepsilon_{ox}WL/t_{ox} = C_{ox}WL$





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  Permittivity $\varepsilon_{ox}=3.9\varepsilon_{o,}$ ε_o is the permittivity of free space, equals $8.85*10^{-14}$F/cm

  $C_{ox} = \varepsilon_{ox} / t_{ox,}$ the capacitance per unit area of the gate oxide.

  t_{ox} is the thickness of the gate oxide

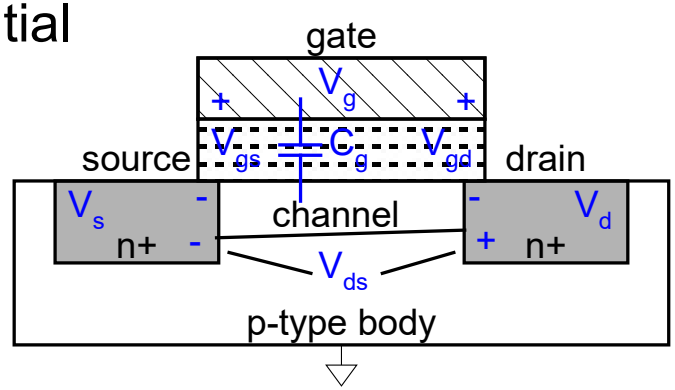
N Channel Charge

- MOS structure looks like parallel plate capacitor while operating in inversion
  - Gate – oxide – channel
- Charge on each plate of the plate is $Q_{channel} = CV$
- $C = C_g = \varepsilon_{ox} WL/t_{ox} = C_{ox} WL$
- $V = V_{gc} - V_t = (V_{gs} - V_{ds}/2) - V_t = V_{gs} - V_t - V_{ds}/2$
  - Average gate to channel potential

    Vgc=(Vgs+Vgd)/2

    =(Vgs+Vgs-Vds)/2

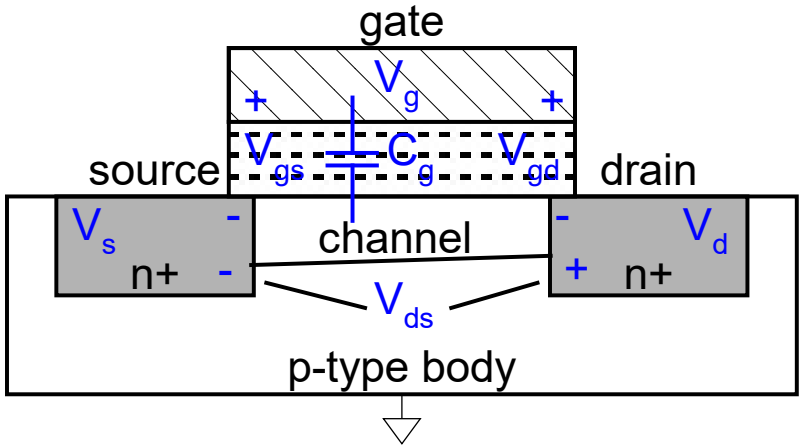
    =Vgs-Vds/2



Carrier velocity

- Charge is carried by e- for nMOS and hole for pMOS
- Carrier velocity *v* proportional to lateral E-field between source and drain
- $v = \mu E$ μ called mobility
- $E = V_{ds}/L$
- Time for carrier to cross channel:

$$t = \frac{L}{v} = \frac{L}{\mu E} = \frac{L}{\mu V_{ds}/L} = \frac{L^2}{\mu V_{ds}}$$



nMOS Linear I-V

- Now we know
  - How much charge $Q_{channel}$ is in the channel
  - How much time (*t*) each carrier takes to cross

$$I_{ds} = \frac{Q_{\text{channel}}}{t} \longrightarrow = Cox(WL)\frac{Vgs - Vt - Vds/2}{L^2/\mu Vds}$$

$$= \mu C_{\text{ox}} \frac{W}{L}\left(V_{gs} - V_t - V_{ds}/2\right)V_{ds}$$

$$= \beta\left(V_{gs} - V_t - V_{ds}/2\right)V_{ds}$$

$$\beta = \mu C_{\text{ox}} \frac{W}{L}$$

nMOS Saturation I-V

- When $V_{gd} = V_t$, channel pinches off near drain that V_{ds} is called drain saturation voltage, V_{dsat}
  - Calculate V_{dsat}

$$V_{dsat}=V_d-V_s=V_d-V_g+V_g-V_s=(V_g-V_s)-(V_g-V_d)$$
$$=V_{gs}-V_{gd}=V_{gs}-V_t$$

- Now drain voltage no longer increases current

$$I_{ds} = \beta\left(V_{gs} - V_t - V_{dsat}/2\right)V_{dsat}$$

$$= \frac{\beta}{2}\left(V_{gs} - V_t\right)^2$$

nMOS I-V Summary

- *Shockley* 1st order transistor models

$$I_{ds} = \begin{cases} 0 & V_{gs} < V_t \quad \text{cutoff} \\ \beta\left(V_{gs} - V_t - V_{ds}/2\right)V_{ds} & V_{gs} > V_t,\ V_{ds} < V_{dsat} \quad \text{linear} \\ \frac{\beta}{2}\left(V_{gs} - V_t\right)^2 & V_{gs} > V_t,\ V_{ds} > V_{dsat} \quad \text{saturation} \end{cases}$$

$$\beta = \mu C_{ox} \frac{W}{L} \qquad V_{dsat} = V_{gs} - V_t$$

Example

- Example: nMOS transistor in a 180 nm process
  - t_{ox} = 40 Å
  - μ_n = 180 $cm^2/V*s$
  - V_{tn0} = 0.4 V
- Plot I_{ds} vs. V_{ds}
  - V_{gs} = 0, 0.3, 0.6, 0.9, 1.2, 1.5 1.8V
  - Use W/L = (4 λ) /(2 λ)

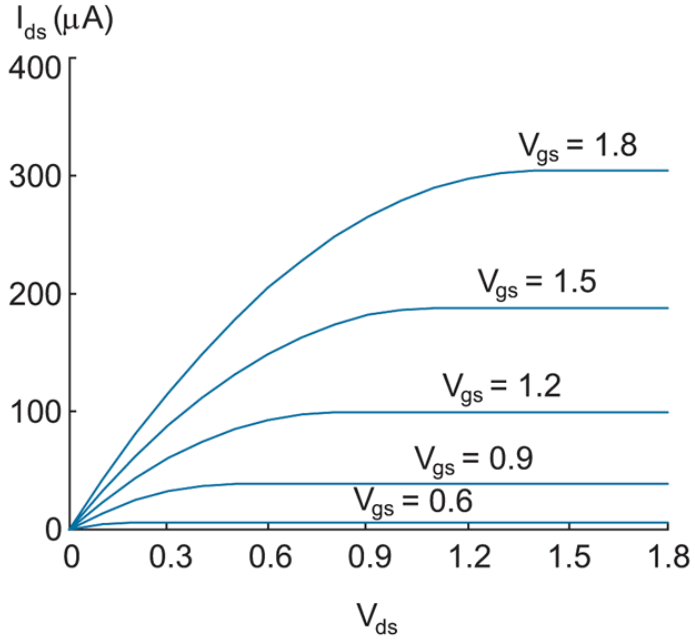


FIG 2.7 I-V characteristics of ideal nMOS transistor

$$\beta = \mu C_{ox}\frac{W}{L} = (180\frac{cm^2}{V.s})\left(\frac{3.9\times 8.85\bullet 10^{-14}\frac{F}{cm}}{40\bullet 10^{-8}cm}\right)\left(\frac{W}{L}\right) = 155\frac{W}{L}\frac{\mu A}{V^2}$$

pMOS I-V

- All dopings and voltages are inverted for pMOS
- Mobility μ_p is determined by holes
  - Typically 2-3x lower than that of electrons μ_n
  - 90 $cm^2/V*s$ in 180 μm process
  - V_{tp} = - 0.4 V
- Thus pMOS must be wider to provide same current
  - In this class, assume $\mu_n / \mu_p = 2$

pMOS I-V Summary (1)

- *Shockley* 1st order transistor models

$$I_{ds} = \begin{cases} 0 & V_{gs} > V_{thp} \quad \text{cutoff} \\ \beta\left(V_{gs} - V_{thp} - V_{ds}/2\right)V_{ds} & V_{gs} < V_{thp} \text{ and } V_{ds} > V_{dsat} \quad \text{linear} \\ -\frac{\beta}{2}\left(V_{gs} - V_{thp}\right)^2 & V_{gs} < V_{thp} \text{ and } V_{ds} < V_{dsat} \quad \text{saturation} \end{cases}$$

$$V_{dsat} = V_{gs} - V_{thp}$$

pMOS I-V Summary (2)

- *Shockley* 1st order transistor models

$$I_{sd} = \begin{cases} 0 & V_{sg} < |V_{tp}| \quad \text{cutoff} \\ \beta_p \left(V_{sg} - |V_{tp}| - V_{sd}/2 \right) V_{sd} & V_{sd} < V_{ssat} \quad \text{linear} \\ \frac{\beta_p}{2} \left(V_{sg} - |V_{tp}| \right)^2 & V_{sd} > V_{ssat} \quad \text{saturation} \end{cases}$$

$$V_{ssat} = V_{sg} - |V_{tp}|$$

pMOS I-V Characteristic

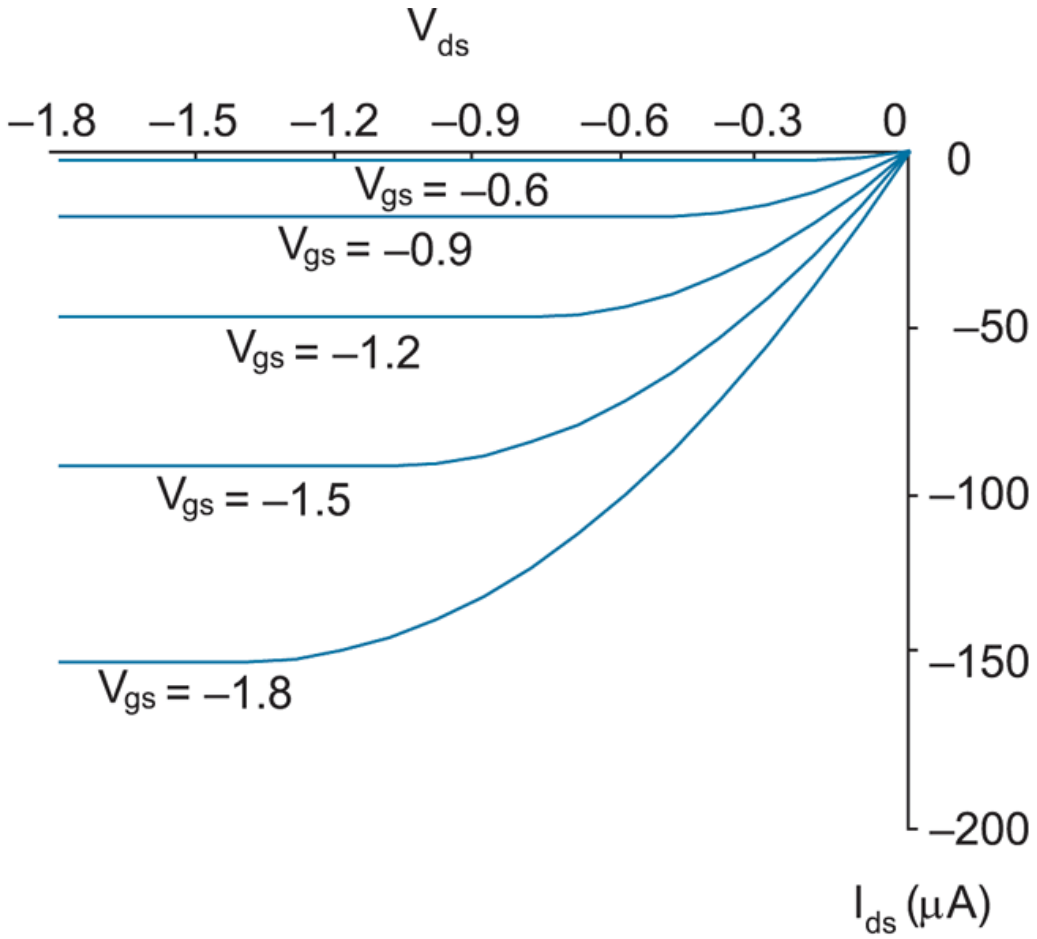


FIG 2.8 I-V characteristics of ideal pMOS transistor

MOS I-V Characteristic

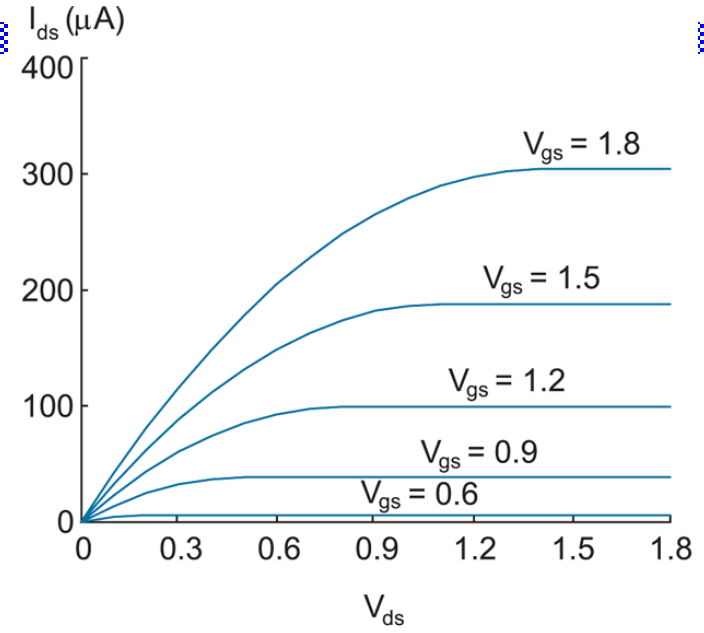


FIG 2.7 I-V characteristics of ideal nMOS transistor

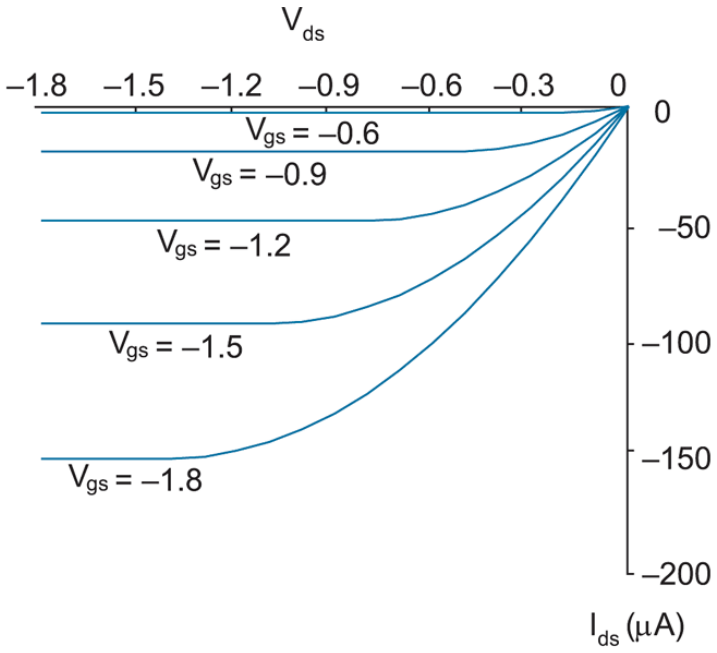
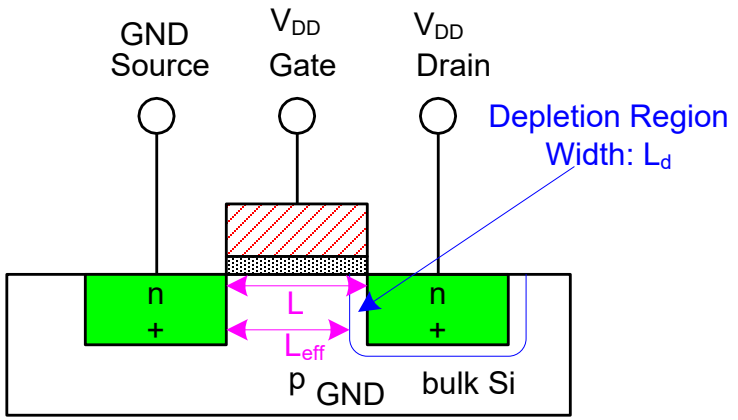


FIG 2.8 I-V characteristics of ideal pMOS transistor

Channel Length Modulation

- Ideally I_{ds} is independent of V_{ds} under saturation—long channel
- $L_{eff}=L-L_d$, where L_{eff} is the effective channel length, L is the drawn channel length, L_d is the depletion region formed by the reverse-biased p-n junction between the drain and body. L_d is proportional to V_{db}
- In the saturation $$I_{ds} = \frac{\beta}{2}\left(V_{gs} - V_{th}\right)^2\left(1+\lambda V_{ds}\right)$$

  λ is called channel modulation factor, which is inversely dependent on channel length.



Body Effect

- The threshold voltage is modeled as

$$V_t = V_{t0} + \gamma\left(\sqrt{\phi_s + V_{sb}} - \sqrt{\phi_s}\right)$$

where V_{t0} is the threshold voltage when $V_{sb} = 0$, ϕ_s is the surface potential at threshold, γ is the body effect coefficient

$$\phi_s = 2v_T \ln\frac{N_A}{n_i}; \qquad \gamma = \frac{t_{ox}}{\varepsilon_{ox}}\sqrt{\frac{2q\varepsilon_{si}N_A}{C_{ox}}}$$

where v_T is the thermal voltage, N_A is the doping level, N_i is the silicon intrinsic level

Example

- 180nm process with v_{tn0}=0.4v, N_A=8.10^{17} cm^{-3}. The body is tied to ground and V_{sb}=1.1V.

At room temperature, $v_T = kT/q = 26\text{mV}$ and $n_i = 1.45 \bullet 10^{10}\ \text{cm}^{-3}$

$$\phi_s = 2(.026V)\ln\frac{8\bullet 10^{17}\,cm^{-3}}{1.45\bullet 10^{10}\ \text{cm}^{-3}} = 0.93V$$

$$\gamma = \frac{40\bullet 10^{-8}\,cm^{-3}}{3.9\bullet 10^{-14}\,\frac{F}{cm}}\sqrt{2\left(1.6\bullet 10^{-19}C\right)\left(11.7\bullet 8.85\bullet 10^{-14}\,\frac{F}{cm}\right)\left(8\bullet 10^{17}\,cm^{-3}\right)}$$

$$= 0.60V^{\frac{1}{2}}$$

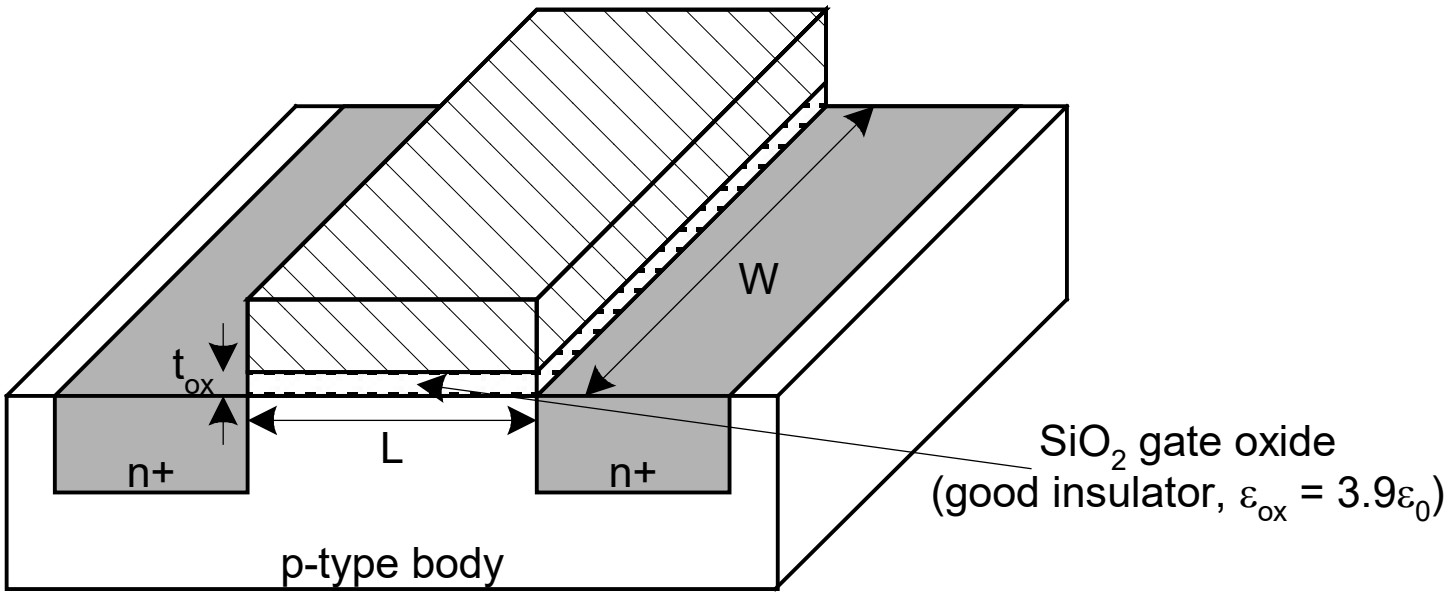
$$Vt = 0.4V + \gamma\left(\sqrt{\phi_s + 1.1V} - \sqrt{\phi_s}\right) = 0.68V$$

Capacitance

- Any two conductors separated by an insulator have capacitance
- Gate to channel capacitor (C_g) is very important
  - Creates channel charge necessary for operation
- Source and drain have capacitance to body
  - Across reverse-biased diodes
  - Called diffusion capacitance because it is associated with source/drain diffusion

Gate Capacitance

- Approximate channel as connected to source
- $C_g = \varepsilon_{ox}WL/t_{ox} = C_{ox}WL = C_{permicron}W = C_0$
- $C_{permicron}$ is typically about 2 fF/μm



$$C_0 = WLC_{ox} = C_{permicron}(W)$$

Table 2.1 Approximation of intrinsic MOS gate capacitance

Parameter	Cutoff	Linear	Saturation
C_{gb}	C_0	0	0
C_{gs}	0	$C_0/2$	$2/3\ C_0$
C_{gd}	0	$C_0/2$	0
$C_g = C_{gs} + C_{gd} + C_{gb}$	C_0	C_0	$2/3\ C_0$

Diffusion Capacitance

- C_{sb}, C_{db}
- Undesirable, also called *parasitic* capacitance
- Capacitance depends on area and perimeter
  - Use small diffusion nodes
  - Comparable to C_g for contacted diffusion cap
  - ½ C_g for uncontacted
  - Varies with process