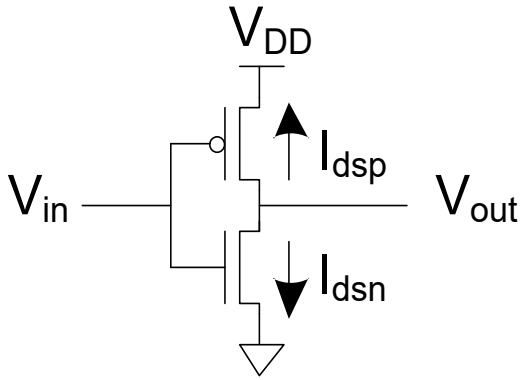
DC & Transient Response Outline

- DC Response
- Logic Levels and Noise Margins
- Transient Response
- Delay Estimation

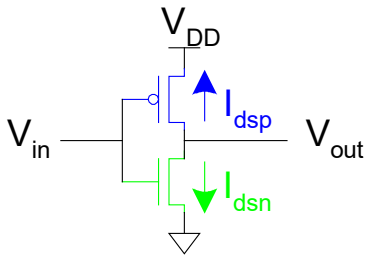
DC Response

- DC Response: V_{out} vs. V_{in} for a gate (input)
- Ex: Inverter
  - When $V_{in} = 0$ -> $V_{out} = V_{DD}$
  - When $V_{in} = V_{DD}$ -> $V_{out} = 0$
  - In between, V_{out} depends on transistor size and current
  - By KCL, must settle such that $I_{dsn} = - I_{dsp} = I_{sdp}$

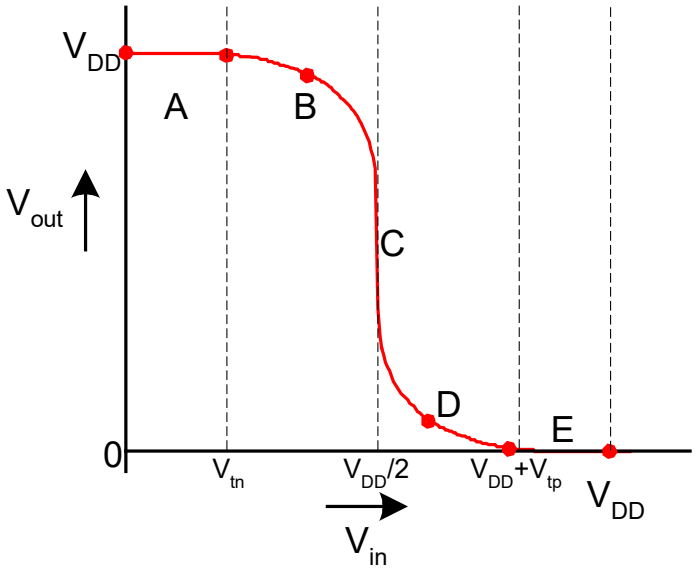


Operating Regions

- Transistor operating regions



Region	nMOS	pMOS
A	Cutoff	Linear
B	Saturation	Linear
C	Saturation	Saturation
D	Linear	Saturation
E	Linear	Cutoff



Operating Regions

- Revisit transistor operating regions

Region	nMOS	pMOS
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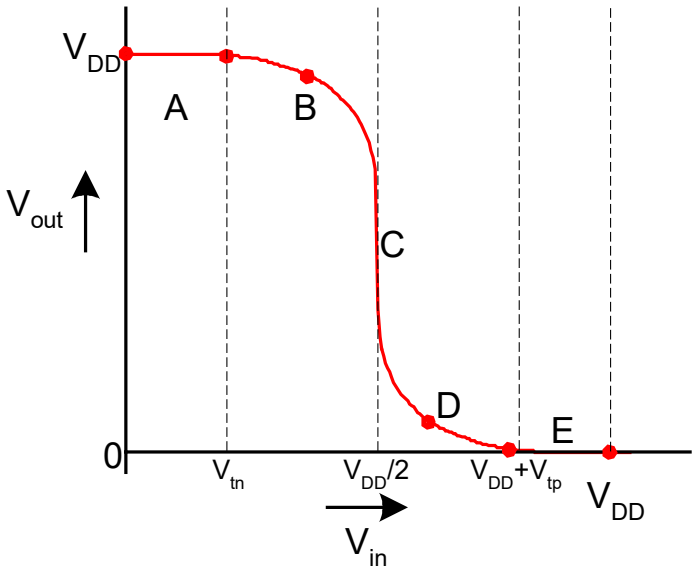
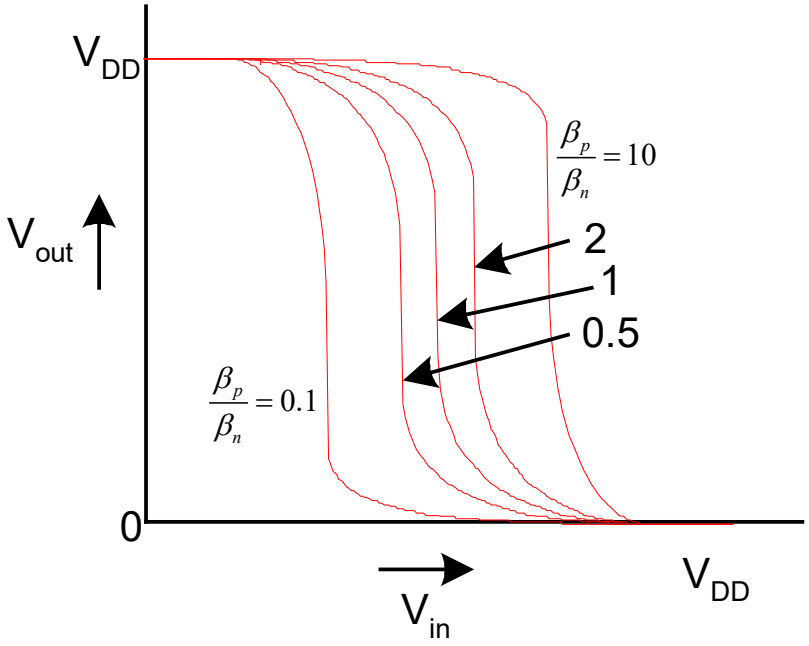
C	Saturation	Saturation
D	Linear	Saturation
E	Linear	Cutoff



C point is called switching point, is about $V_{DD}/2$ if $\beta_n=\beta_p$

Beta Ratio

- If $\beta_p / \beta_n \neq 1$, switching point will move from $V_{DD}/2$
- Called *skewed* gate
- Other gates: collapse into equivalent inverter



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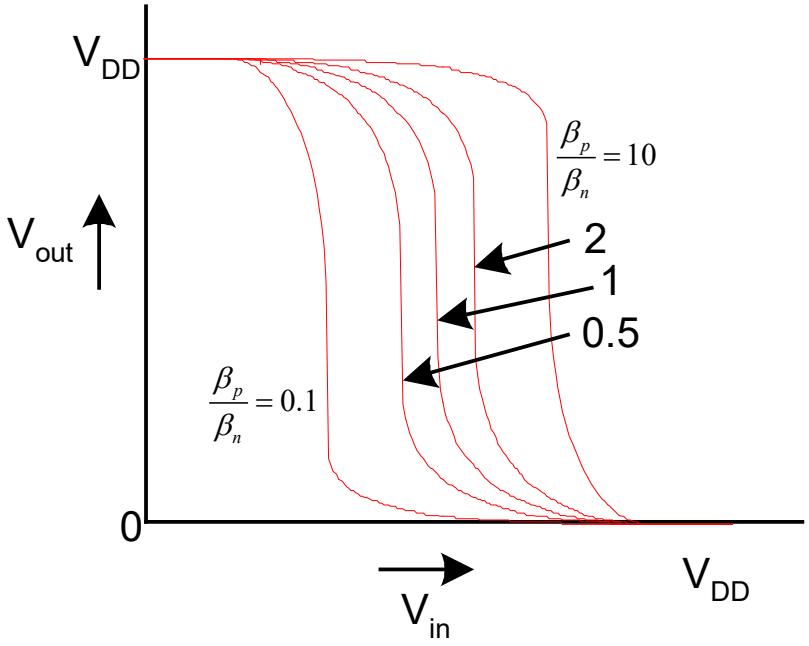
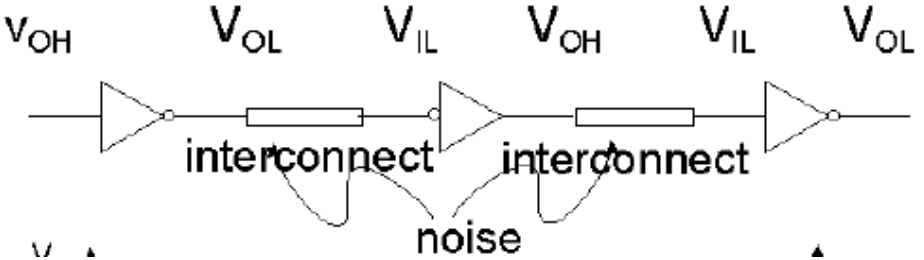
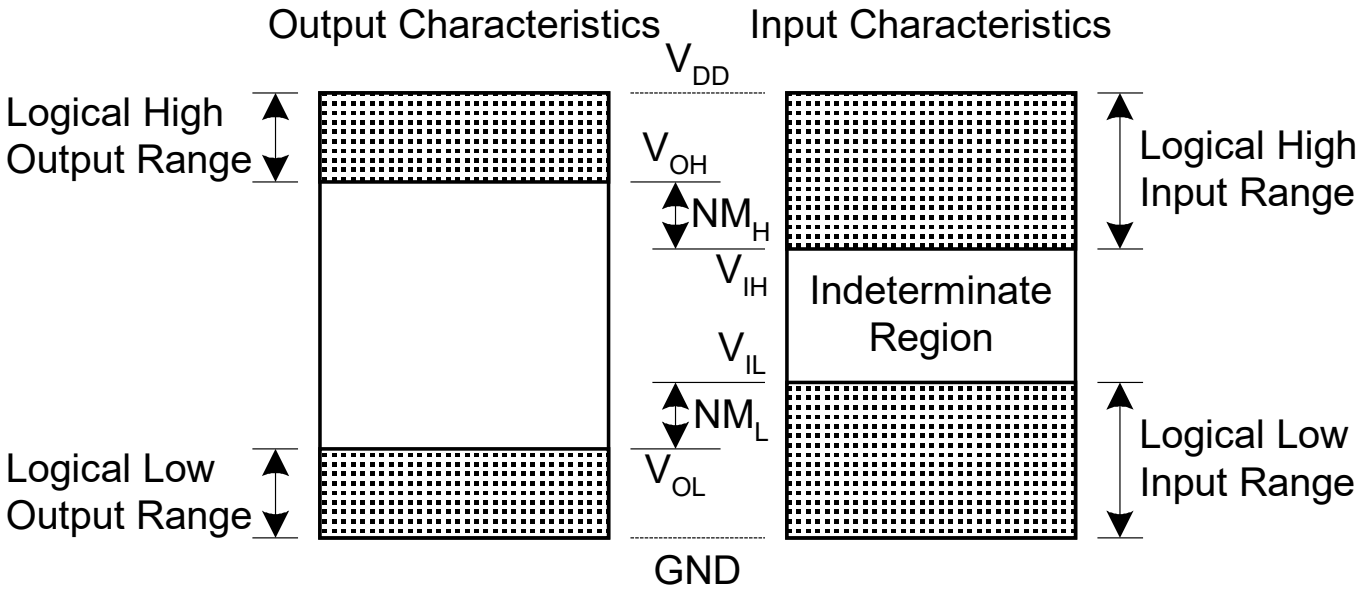


Noise Margins



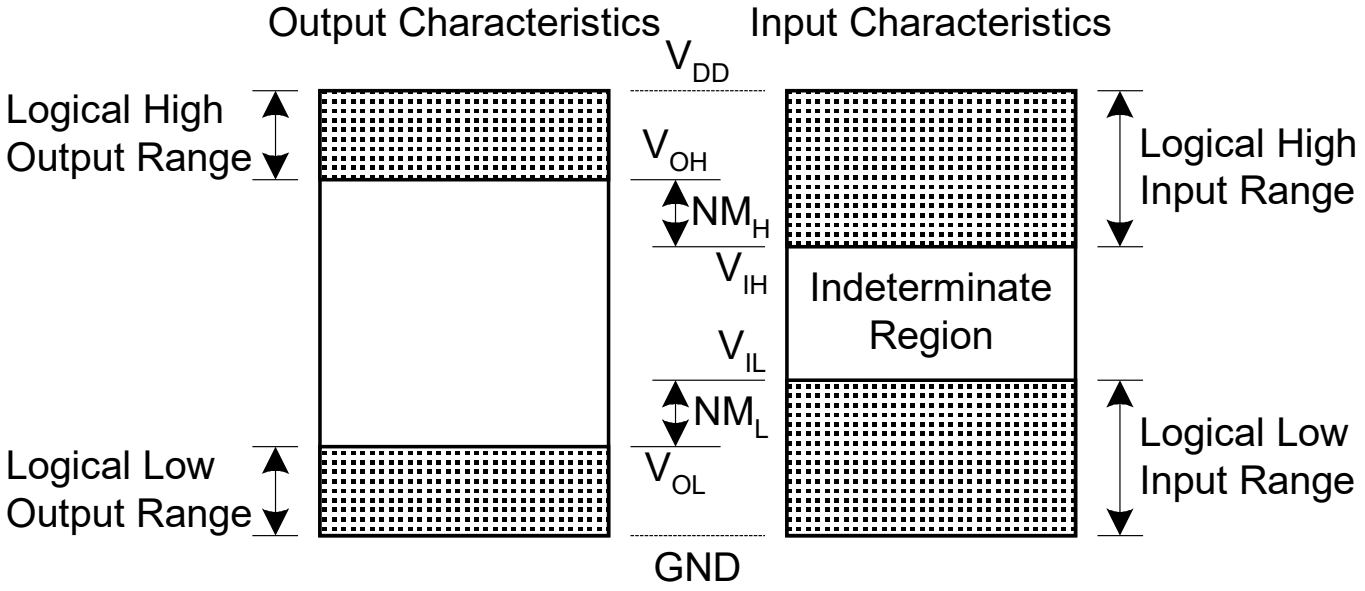
- How much noise can a gate input see before it does not recognize the input?

Inverter buffer



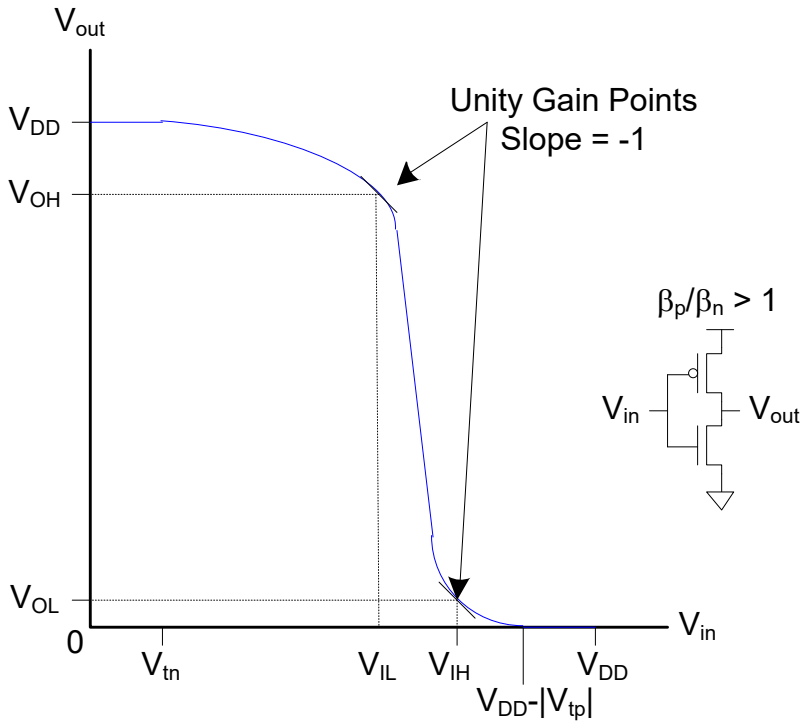
Noise Margins

- Low Noise Margin $NM_L = V_{IL} - V_{OL}$; High $NM_H = V_{OH} - V_{IH}$;
  - V_{IH}=minimum high input voltage; V_{IL}=maximum low input voltage
  - V_{OH}=minimum high output voltage; V_{OL}=maximum low output voltage



Logic Levels

- To maximize noise margins, select logic levels at negative unity gain point of DC transfer characteristic



Exercise

- 2.2, 2.4, 2.7, 2.14, 2.15, 2.16, 2.21, 2.22, 3.7

Transient Response

- *DC analysis* tells us V_{out} if V_{in} is constant regarding of time
- *Transient analysis* tells us $V_{out}(t)$ if $V_{in}(t)$ changes following time
  - Requires solving differential equations
- Input is usually considered to be a step or ramp signal
  - From 0 to V_{DD} or vice versa

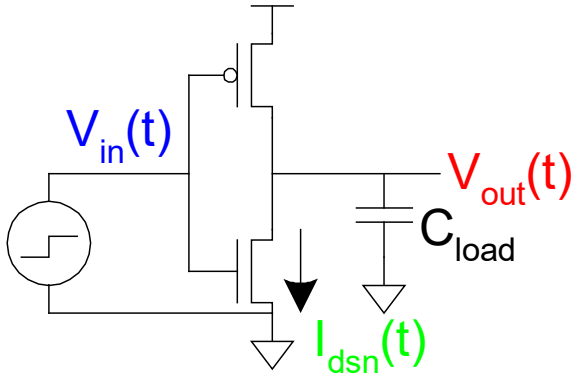
Inverter Step Response

- Ex: find step response of inverter driving load cap

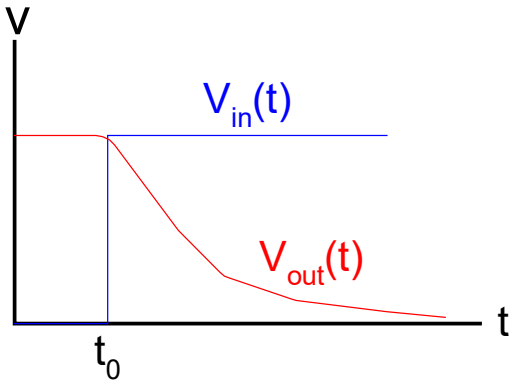
$$V_{in}(t) = u(t - t_0)V_{DD}$$

$$V_{out}(t < t_0) = V_{DD}$$

$$\frac{dV_{out}(t)}{dt} = -\frac{I_{dsn}(t)}{C_{load}}$$



$$I_{dsn}(t) = \begin{cases} 0 & t \le t_0 \\ \frac{\beta}{2}(V_{DD} - V_t)^2 & V_{out} > V_{DD} - V_t \\ \beta\left(V_{DD} - V_t - V_{out}(t)/2\right)V_{out}(t) & V_{out} < V_{DD} - V_t \end{cases}$$



Delay Types

- Delay determines how quickly the circuit is able to process data.
- In **combinationa**l circuit, two types of delay are important: **contaminatio**n delay and **propagation** delay.

Propagation Delay Definition

- **Propagation** delay is the time it takes from a change in the input to the *completion (switching point)* of the change in the output (worst delay)
- $\mathbf{t_{pdr}}$: *rising propagation delay*
  - From input change crossing $V_{DD}/2$ to rising output crossing $V_{DD}/2$ (upper bound)
- $\mathbf{t_{pdf}}$: *falling propagation delay*
  - From input change crossing $V_{DD}/2$ to falling output crossing $V_{DD}/2$ (upper bound)
- $\mathbf{t_{pd}}$: *average propagation delay*
  - $t_{pd} = (t_{pdr} + t_{pdf})/2$
- $\mathbf{t_r}$: *rise time*
  - From output crossing 0.2 (0.1) V_{DD} to 0.8 (0.9) V_{DD}
- $\mathbf{t_f}$: *fall time*
  - From output crossing 0.8 (0.9) V_{DD} to 0.2 (0.1) V_{DD}

Propagation Delay

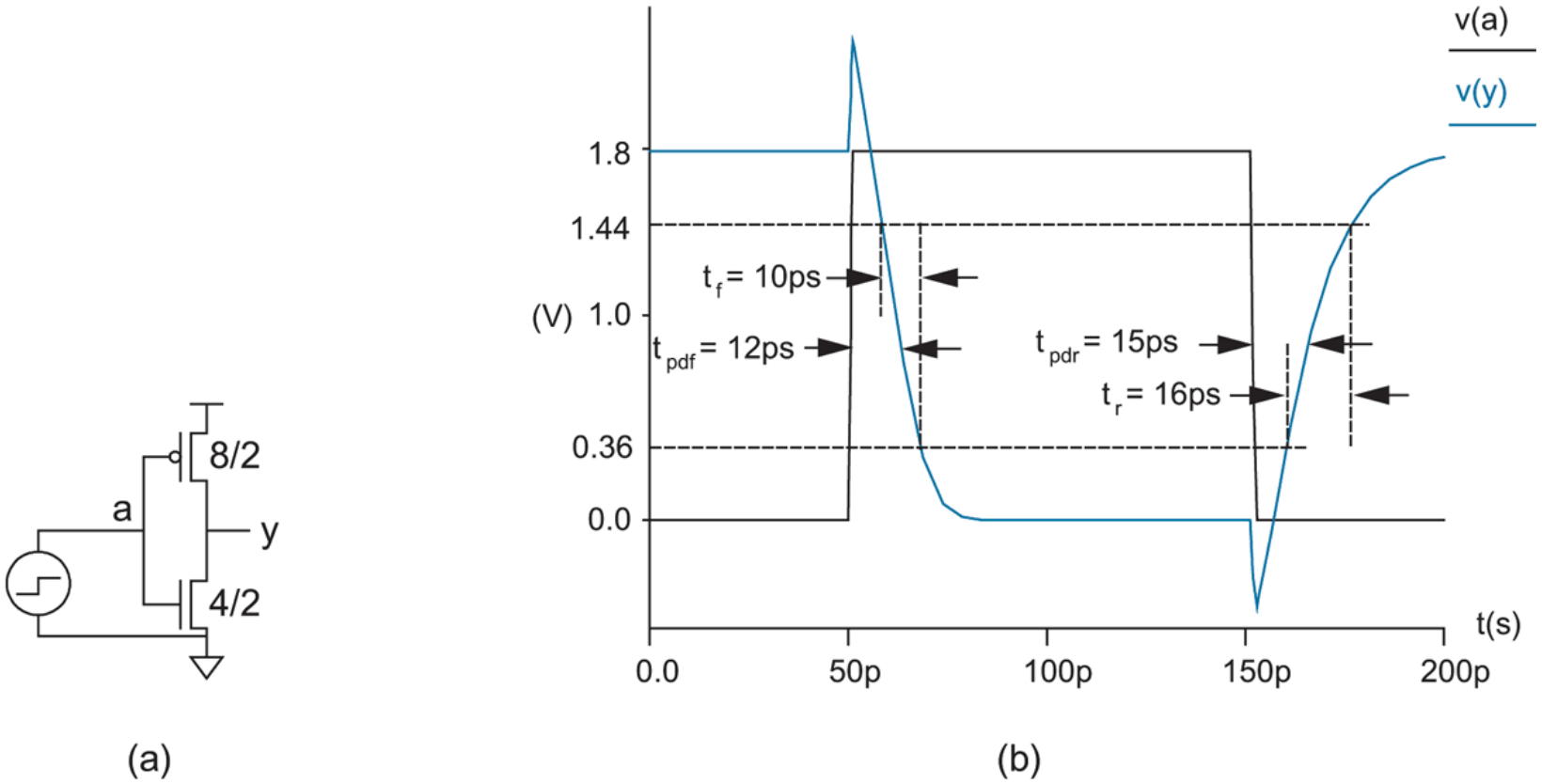
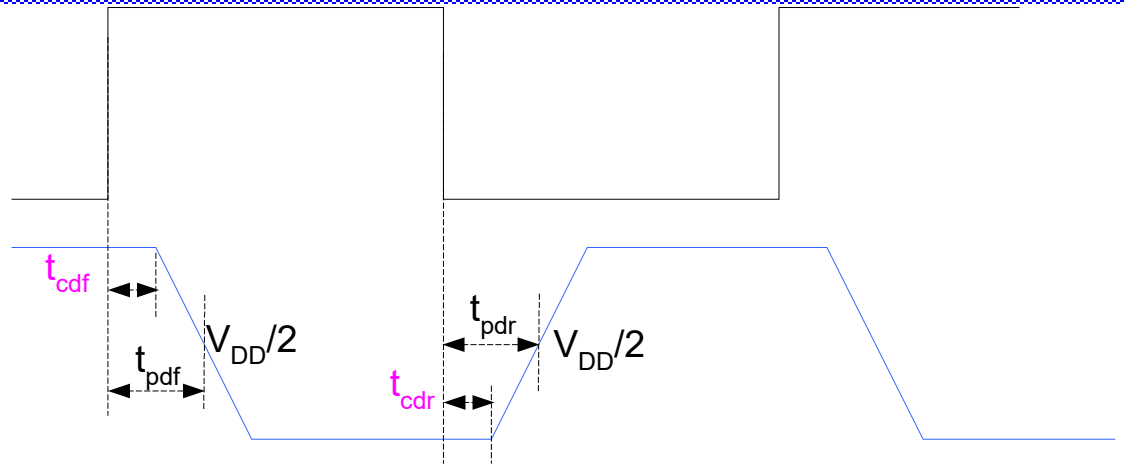


FIG 5.7 Unloaded inverter

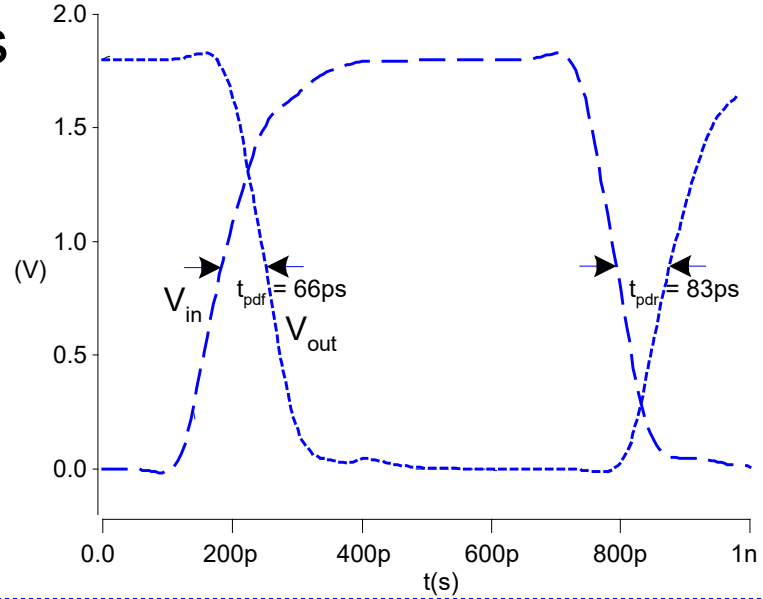
Delay



- When different logic gates are connected to form a circuit, the contamination and propagation delays of the individual gates sum to form the overtall circuit delays.
- Because contamination delay refers to the ***start*** of the output change: Overall contamination delay for a circuit is the **smallest** sum of contamination delays through gates from input to output.
- Conversely, since propagation delay refers to the **completion** of the output change: Overall propagation delay for a circuit is the **largest** sum of propagation delays through gates from input to output.

Simulated Inverter Delay

- Solving differential equations by hand is too hard
- SPICE simulator solves the equations numerically
  - Uses more accurate I-V models too!
- But simulations do take time to complete for large circuits



Delay Estimation

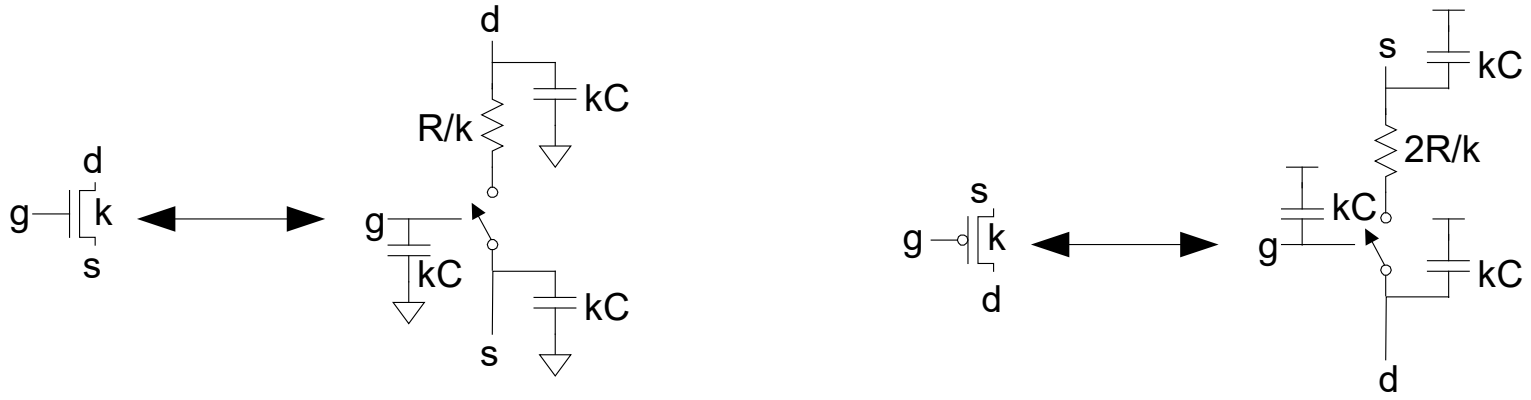
- We would like to be able to easily estimate delay
  - Not as accurate as simulation
  - But easier to ask "What if?"
- The step response usually looks like a 1st order RC response with a decaying exponential.
- Use RC delay models to estimate delay
  - C = total capacitance on output node
  - Use *effective resistance* R
  - So that t_{pd} = RC
- Characterize transistors by finding their effective R
  - Depends on average current as gate switches

RC Values

- Capacitance
  - $C = C_g = C_{sb} = C_{db} = 2$ fF/μm of gate width
  - Values similar across many processes
- Resistance
  - $R \approx 2$ KΩ*μm in 180 nm process
  - Improves with shorter channel lengths
- Unit transistors
  - May refer to minimum contacted device (4λ/2λ)
  - Or maybe 1 μm wide device
  - Doesn't matter as long as you are consistent

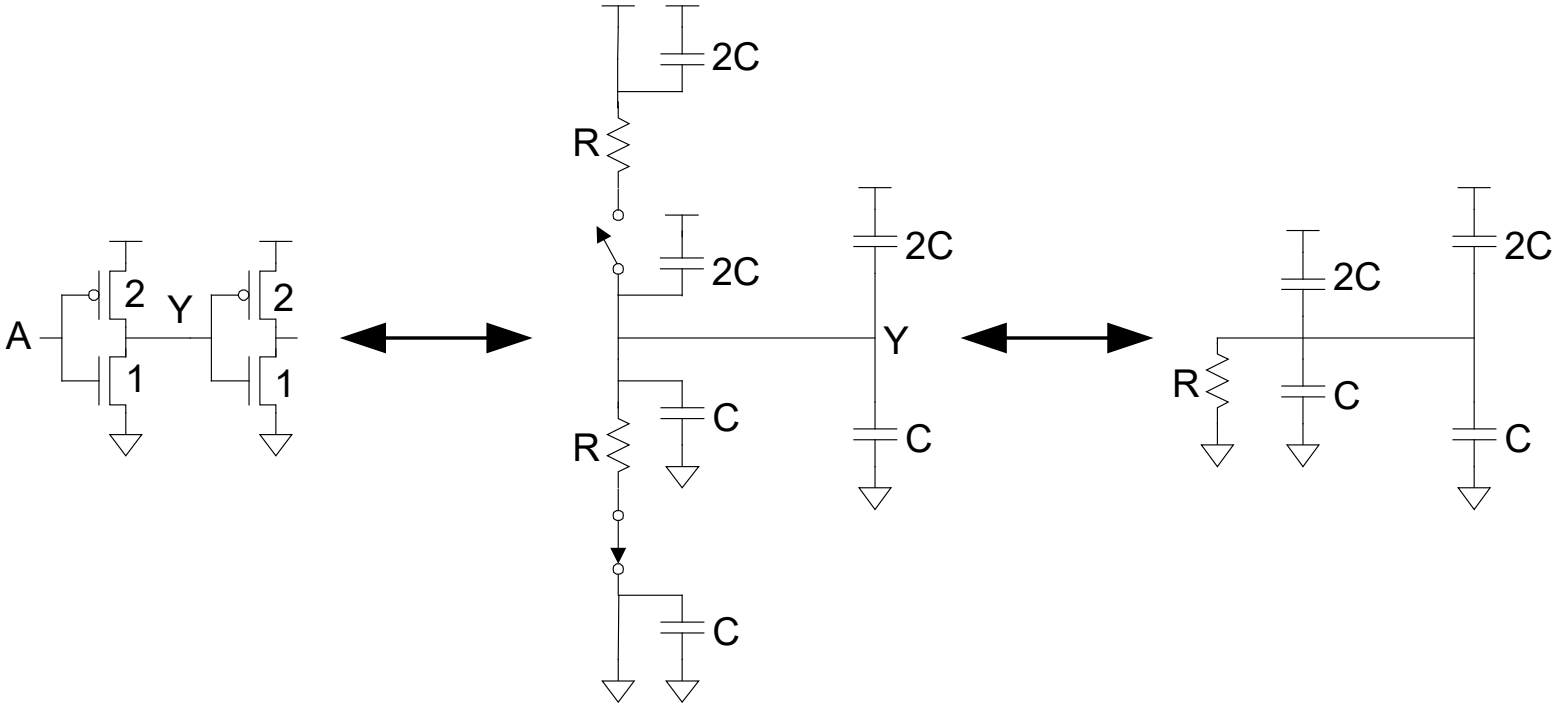
RC Delay Model

- Use equivalent circuits for MOS transistors
  - Ideal switch + capacitance and ON resistance
  - Unit nMOS has resistance R, capacitance C
  - Unit pMOS has resistance 2R, capacitance C
- Capacitance proportional to width
- Resistance inversely proportional to width



Inverter Delay Estimate

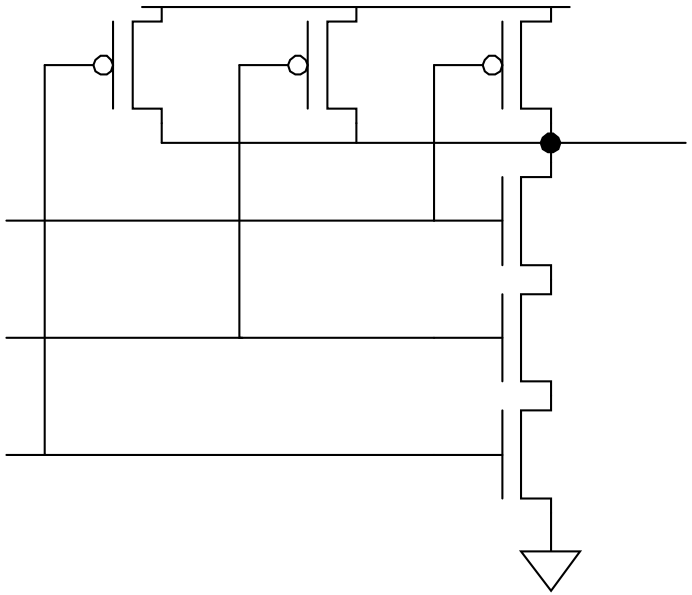
- Estimate the delay of a fanout-of-1 inverter at node Y



d = 6RC

Example: 3-input NAND sizes

- Sketch a 3-input NAND with transistor widths chosen to achieve effective rise and fall resistances equal to a unit inverter (R).



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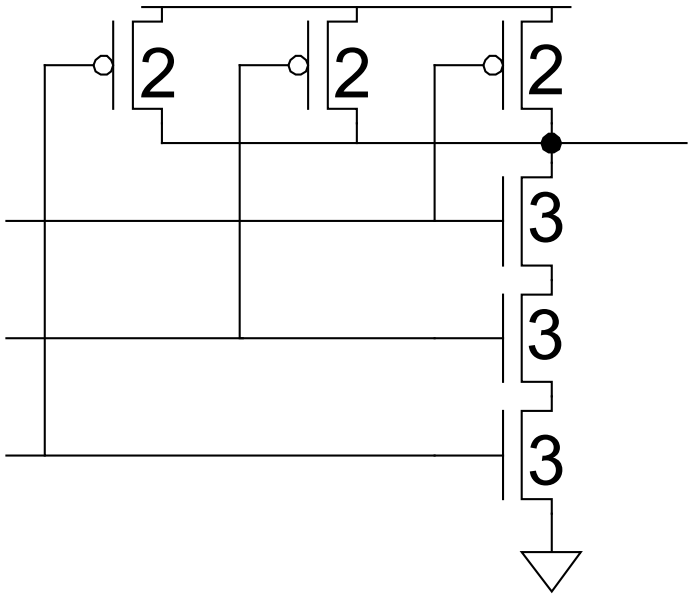
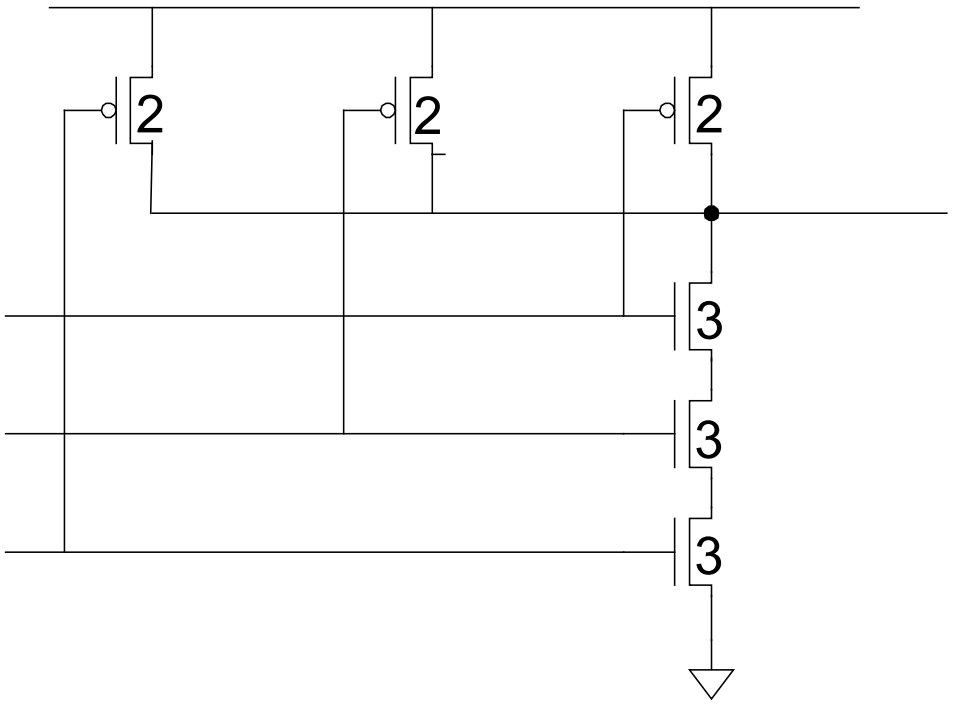


3-input NAND Caps

- Annotate the 3-input NAND gate with gate and diffusion capacitance.



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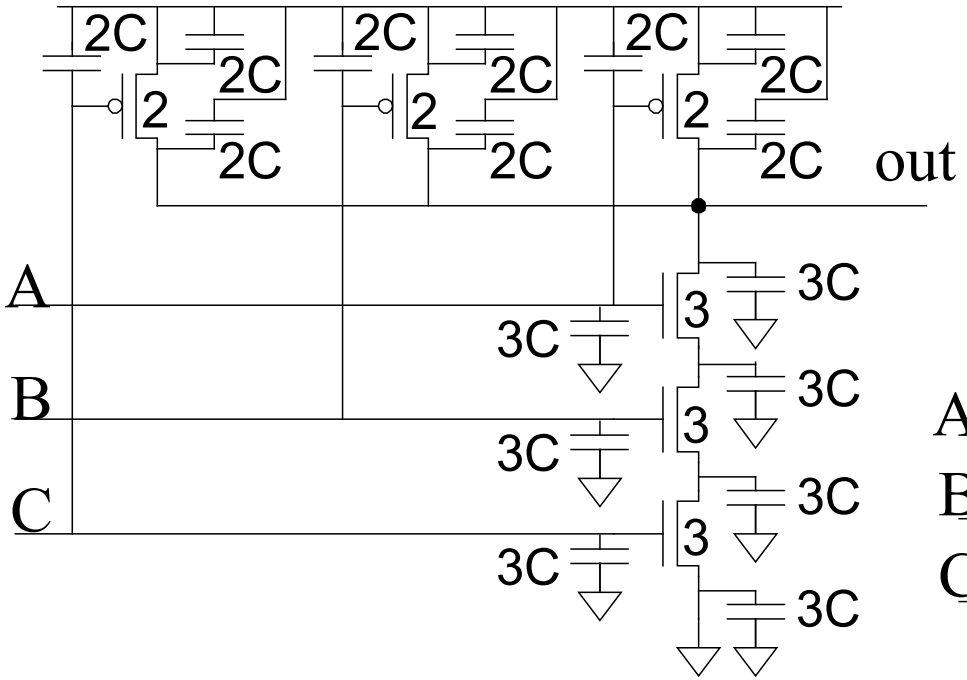
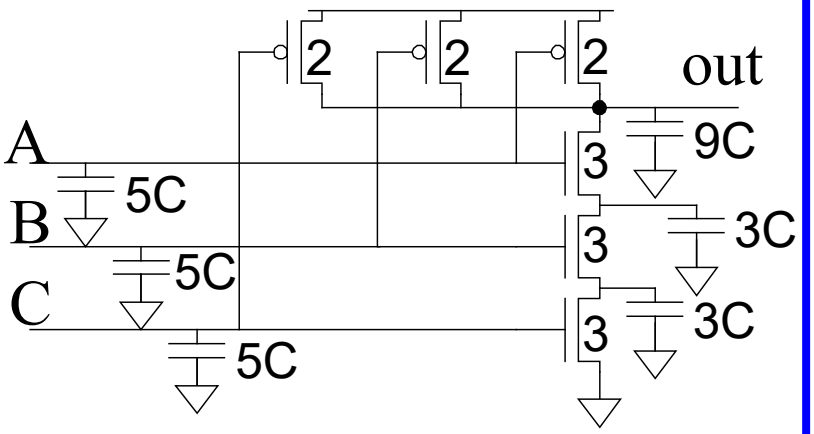


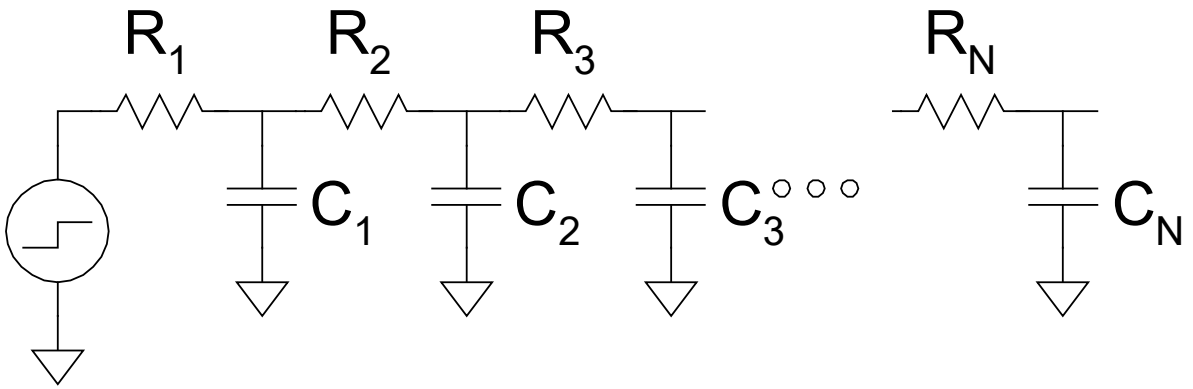


Elmore Delay

- ON transistors look like resistors
- Pullup or pulldown network modeled as *RC ladder*
- Elmore delay of RC ladder

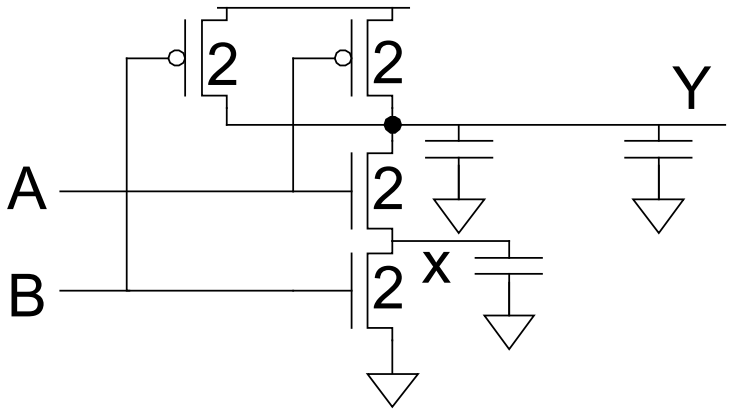
$$t_{pd} \approx \sum_{\text{nodes } i} R_{i-to-source} C_i$$

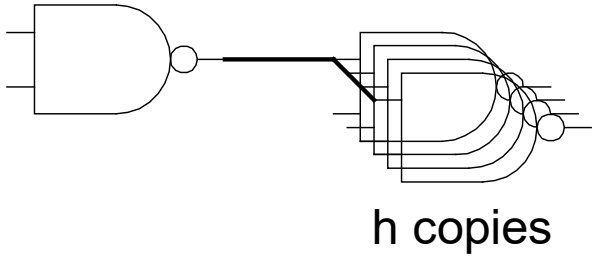
$$= R_1 C_1 + (R_1 + R_2) C_2 + \ldots + (R_1 + R_2 + \ldots + R_N) C_N$$



Example: 2-input NAND

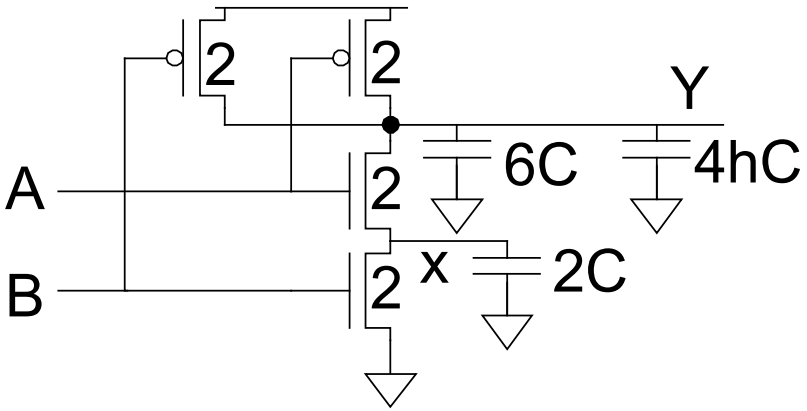
- Estimate worst-case rising and falling delay of 2-input NAND driving *h* identical gates.

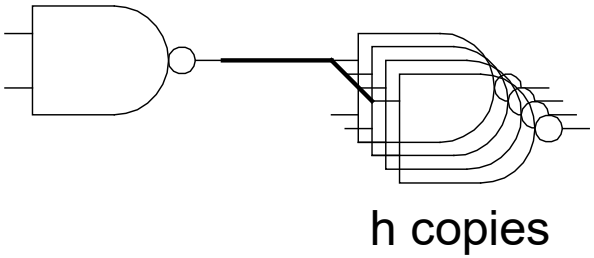


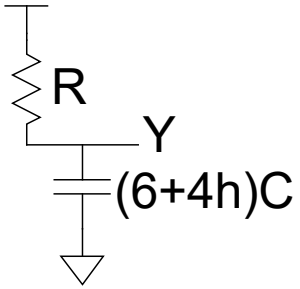


Example: 2-input NAND

- Estimate worst case rising propagation delays of a 2-input NAND driving *h* identical gates.



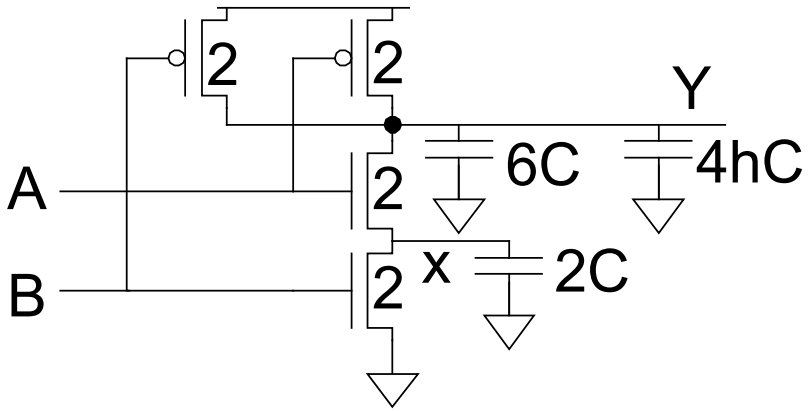


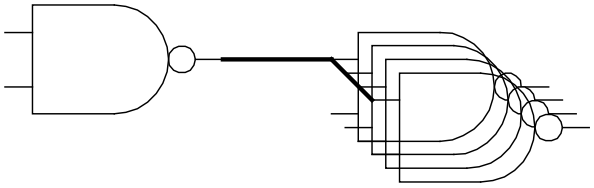


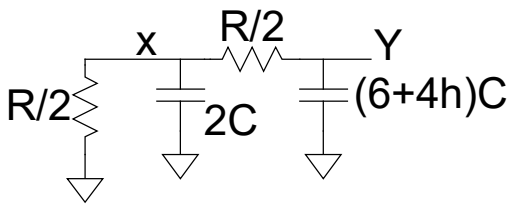
$$t_{pdr} = (6 + 4h)RC$$

Example: 2-input NAND

- Estimate falling propagation delays of a 2-input NAND driving *h* identical gates.







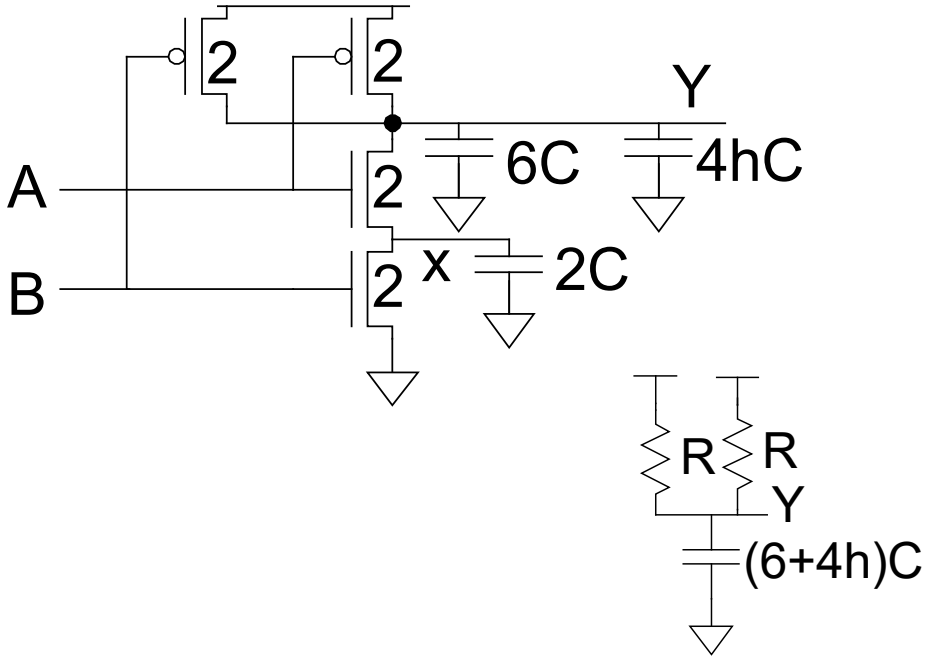
$$t_{pdf} = (2C)\left(\frac{R}{2}\right) + \left[(6+4h)C\right]\left(\frac{R}{2}+\frac{R}{2}\right)$$
$$= (7+4h)RC$$

Delay Components

- Delay has two parts (components)
  - *Parasitic delay*—*determined by the gate driving its own* internal diffusion capacitance
    - 6 RC or 7 RC for the previous NAND2
    - Independent of load
  - *Effort delay*—*depends on the ratio of external load capacitance to input capacitance. The capacitance ratio is called the* ***electrical effort*** *or* ***fanout****, will be discussed later.*
    - 4h RC for the previous NAND2
    - Proportional to load capacitance

Contamination Delay

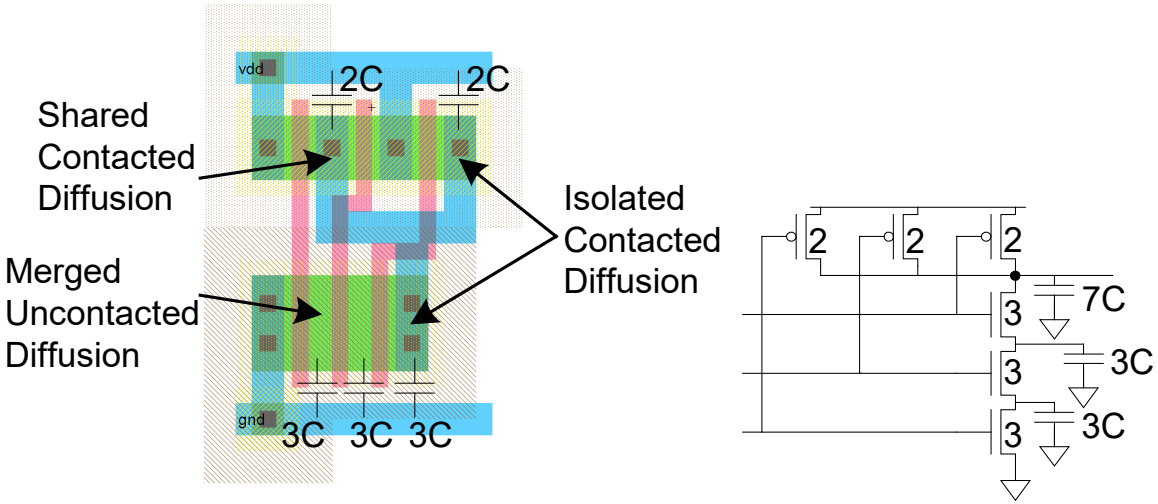
- Best-case (contamination) delay can be substantially less than propagation delay.
- Ex: If both inputs fall (from ‘1’ go to ‘0’) simultaneously



$$t_{cdr} = (3 + 2h)RC$$

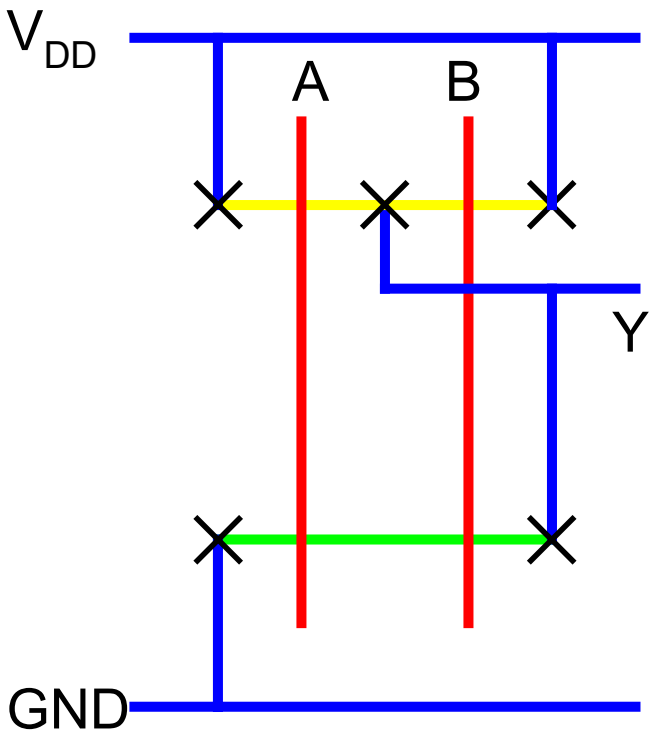
Diffusion Capacitance

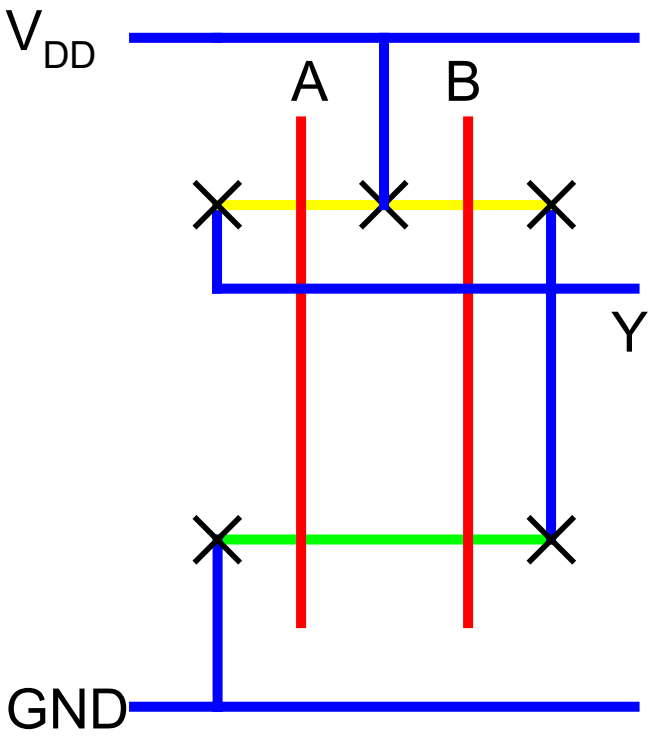
- we assumed contacted diffusion on every s and d.
- *Good layout minimizes* diffusion area
- Ex: NAND3 layout shares one diffusion contact
  - Reduces output capacitance by 2C
  - Merged uncontacted diffusion help too



Layout Comparison

- Which layout is better?





Exercise

- 4.2, 4.3, 4.4
- Develop an one bit full adder function and schematic circuit
- Develop a half adder function and schematic circuit
- Draw the schematic circuits of a latch and a rising edge trigger DFF (refer to the previous class note by using transmission gate and other logic)